

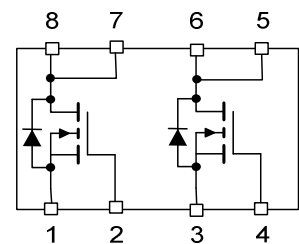
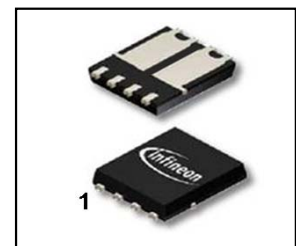
OptiMOS[®] Power-Transistor

Product Summary

V_{DS}	55	V
$R_{DS(on),max}^{4)}$	35	m Ω
I_D	20	A

Features

- Dual N-channel Logic Level - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested
- Feasible for automatic optical inspection (AOI)

PG-TDSON-8-10


Type	Package	Marking
IPG20N06S2L-35A	PG-TDSON-8-10	2N06L35

Maximum ratings, at $T_j=25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current one channel active ²⁾	I_D	$T_C=25\text{ }^\circ\text{C}$, $V_{GS}=10\text{ V}^{1)}$	20	A
		$T_C=100\text{ }^\circ\text{C}$, $V_{GS}=10\text{ V}$	20	
Pulsed drain current ²⁾ one channel active	$I_{D,pulse}$	-	80	
Avalanche energy, single pulse ^{2, 4)}	E_{AS}	$I_D=10\text{ A}$	100	mJ
Avalanche current, single pulse ⁴⁾	I_{AS}	-	15	A
Gate source voltage	V_{GS}	-	± 20	V
Power dissipation one channel active	P_{tot}	$T_C=25\text{ }^\circ\text{C}$	65	W
Operating and storage temperature	T_j , T_{stg}	-	-55 ... +175	$^\circ\text{C}$
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics²⁾						
Thermal resistance, junction - case	R_{thJC}	-	-	-	2.3	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	100	-	
		6 cm ² cooling area ³⁾	-	60	-	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	55	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=27\text{ }\mu\text{A}$	1.2	1.6	2.0	
Zero gate voltage drain current ⁴⁾	I_{DSS}	$V_{DS}=55\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.01	1	μA
		$V_{DS}=55\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}^{2)}$	-	1	100	
Gate-source leakage current ⁴⁾	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	1	100	nA
Drain-source on-state resistance ⁴⁾	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=10\text{ A}$	-	35	44	$\text{m}\Omega$
		$V_{GS}=10\text{ V}, I_D=15\text{ A}$	-	28	35	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance ⁴⁾	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	610	790	pF
Output capacitance ⁴⁾	C_{oss}		-	180	230	
Reverse transfer capacitance ⁴⁾	C_{rss}		-	65	100	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=27.5\text{ V},$ $V_{GS}=10\text{ V}, I_D=20\text{ A},$ $R_G=11\ \Omega$	-	3	-	ns
Rise time	t_r		-	5	-	
Turn-off delay time	$t_{d(off)}$		-	25	-	
Fall time	t_f		-	15	-	

Gate Charge Characteristics^{2, 4)}

Gate to source charge	Q_{gs}	$V_{DD}=44\text{ V}, I_D=20\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	2	2.6	nC
Gate to drain charge	Q_{gd}		-	6.5	10	
Gate charge total	Q_g		-	18	23	
Gate plateau voltage	$V_{plateau}$		-	3.5	-	V

Reverse Diode

Diode continuous forward current ²⁾ one channel active	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	20	A
Diode pulse current ²⁾ one channel active	$I_{S,pulse}$		-	-	80	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=15\text{ A},$ $T_J=25\text{ }^\circ\text{C}$	-	1.0	1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=27.5\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	40	-	ns
Reverse recovery charge ^{2, 4)}	Q_{rr}		-	40	-	nC

¹⁾ Current is limited by bondwire; with an $R_{thJC}=2.3\text{ K/W}$ the chip is able to carry 30.4A at 25°C.

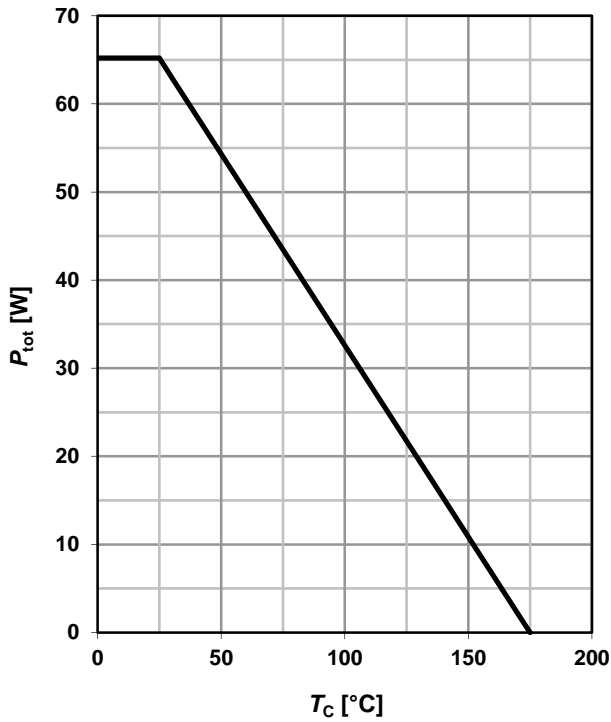
²⁾ Specified by design. Not subject to production test.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

⁴⁾ Per channel

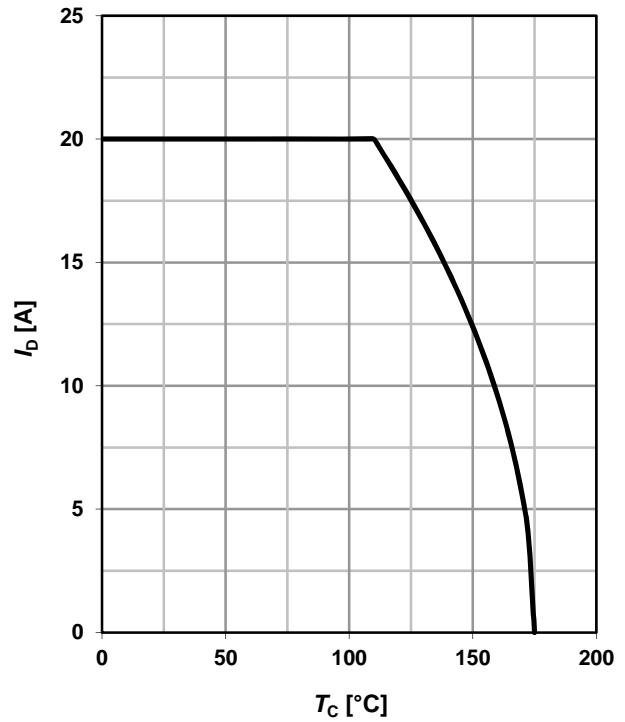
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} \geq 6 \text{ V}; \text{ one channel active}$



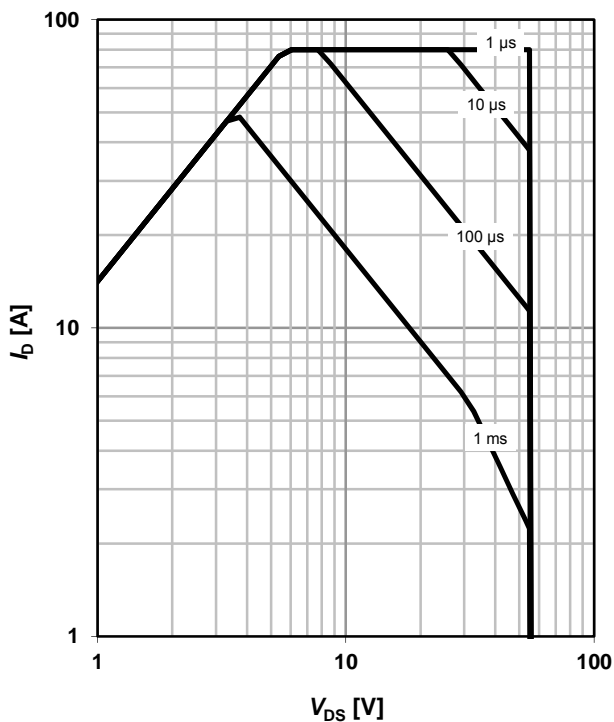
2 Drain current

$I_D = f(T_C); V_{GS} \geq 6 \text{ V}; \text{ one channel active}$



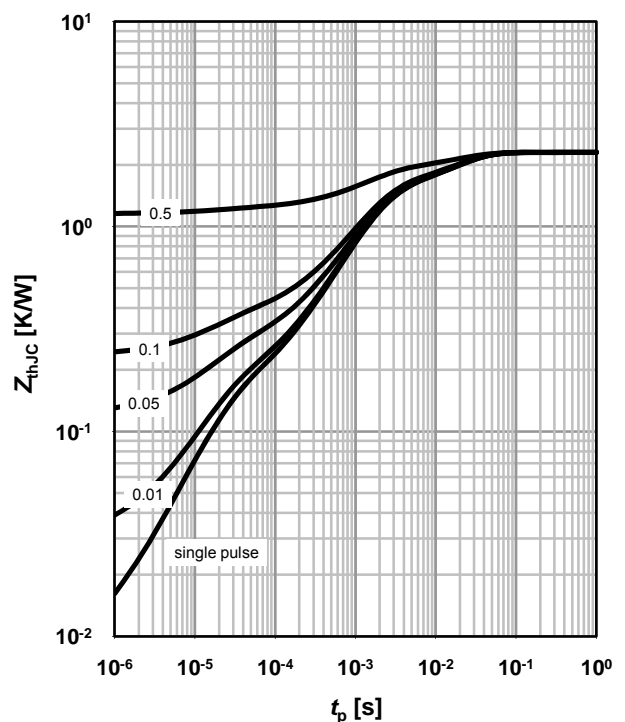
3 Safe operating area

$I_D = f(V_{DS}); T_C = 25^\circ\text{C}; D = 0; \text{ one channel active}$
parameter: t_p



4 Max. transient thermal impedance

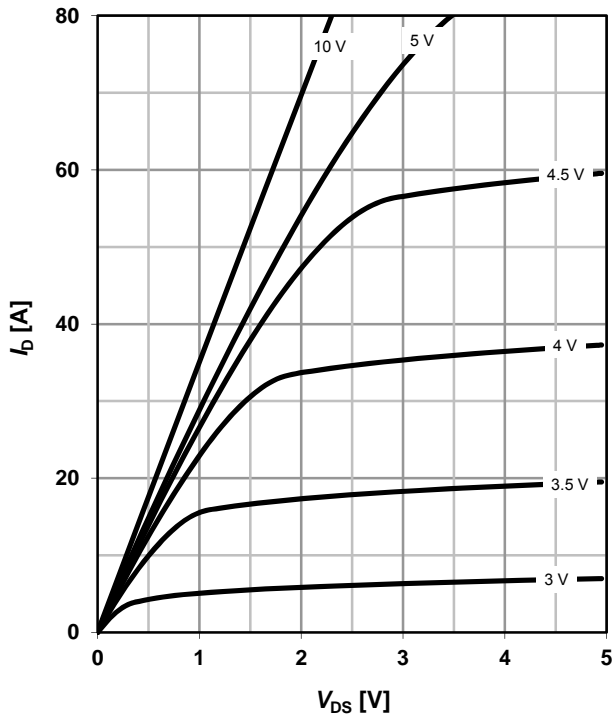
$Z_{thJC} = f(t_p)$
parameter: $D = t_p/T$



5 Typ. output characteristics⁴⁾

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

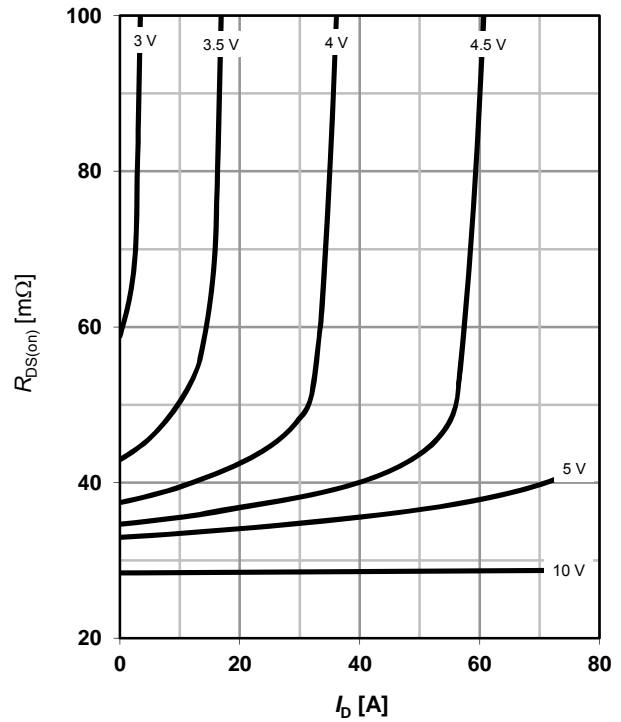
parameter: V_{GS}



6 Typ. drain-source on-state resistance⁴⁾

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

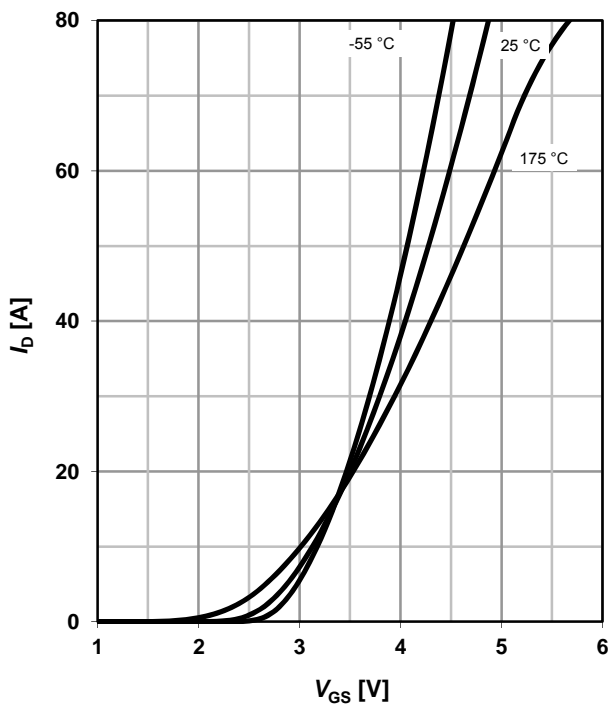
parameter: V_{GS}



7 Typ. transfer characteristics⁴⁾

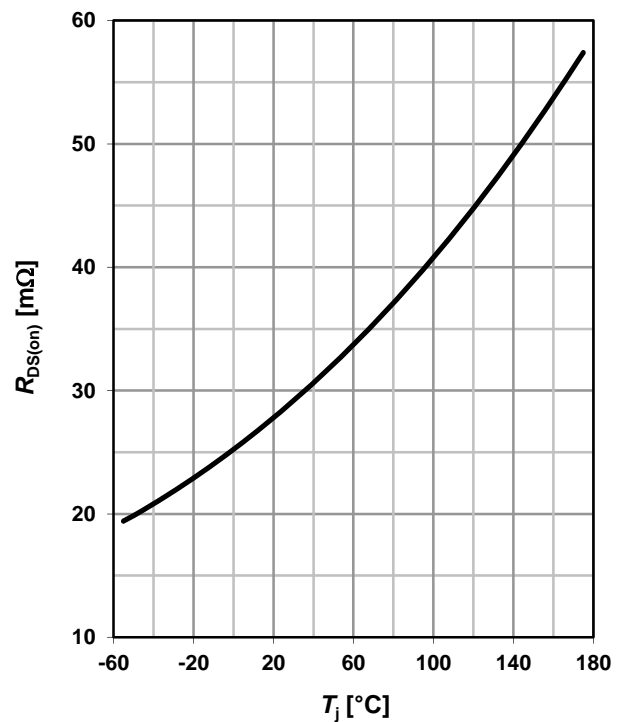
$I_D = f(V_{GS}); V_{DS} = 6V$

parameter: T_j



8 Typ. drain-source on-state resistance⁴⁾

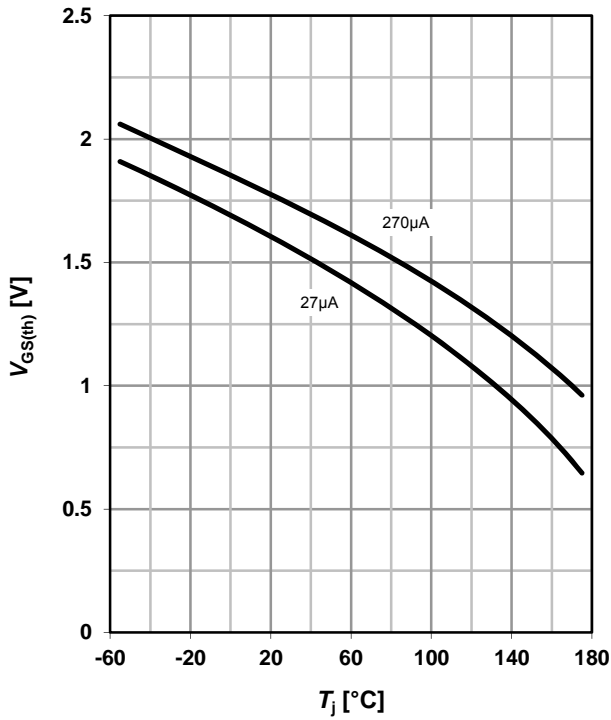
$R_{DS(on)} = f(T_j); I_D = 15\text{ A}; V_{GS} = 10\text{ V}$



9 Typ. gate threshold voltage

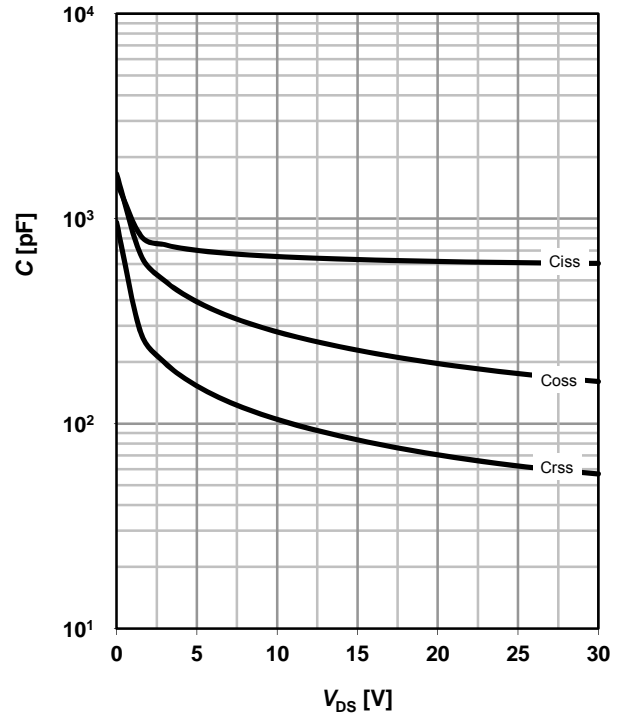
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. Capacitances⁴⁾

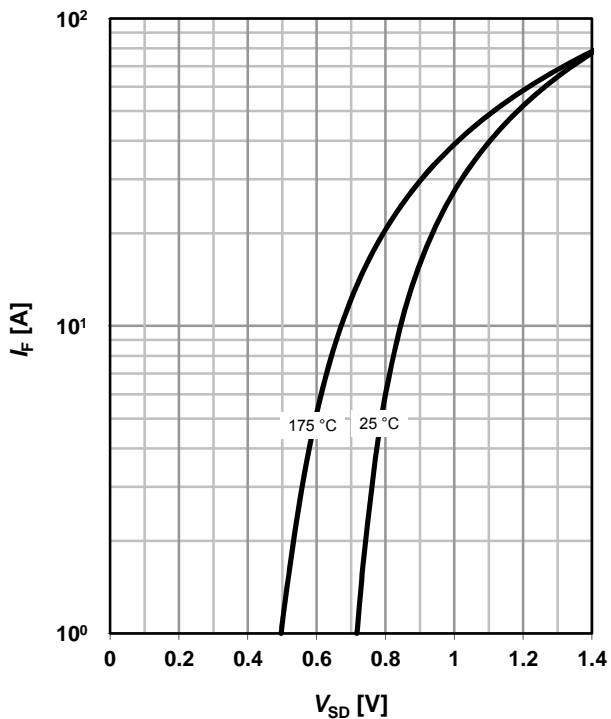
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



11 Typical forward diode characteristics⁴⁾

$I_F = f(V_{SD})$

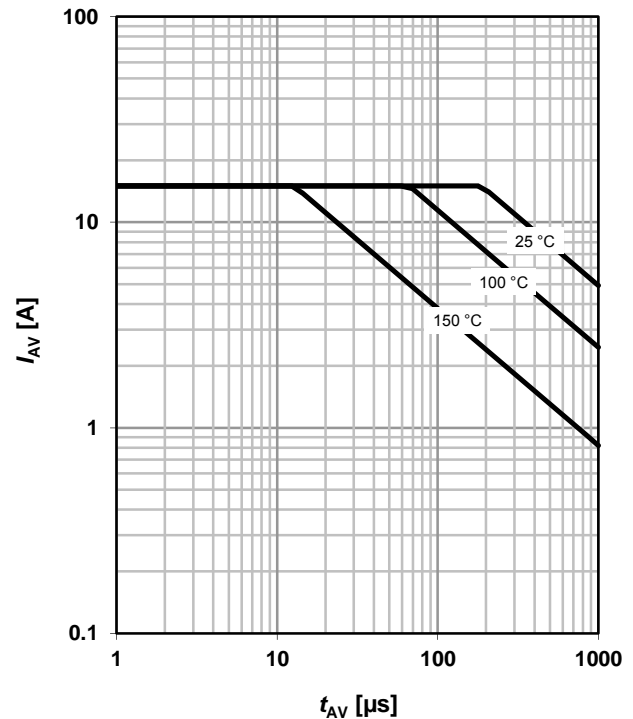
parameter: T_j



12 Avalanche characteristics⁴⁾

$I_{AS} = f(t_{AV})$

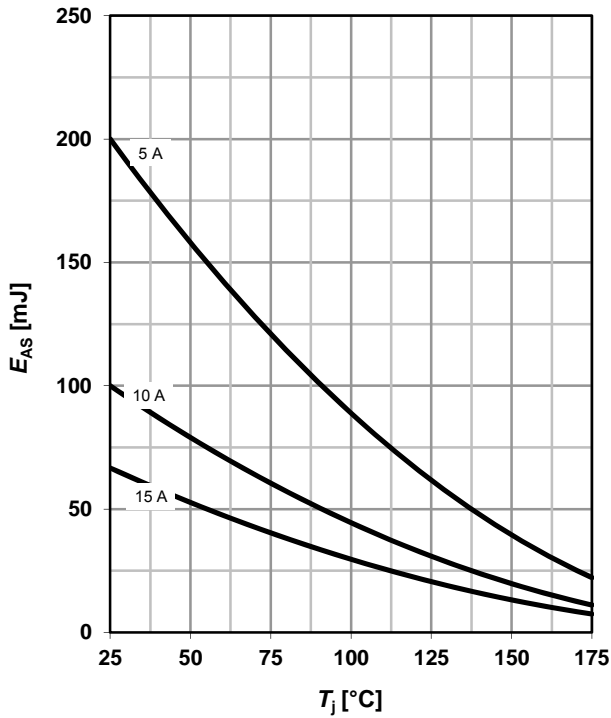
parameter: $T_{j(start)}$



13 Avalanche energy⁴⁾

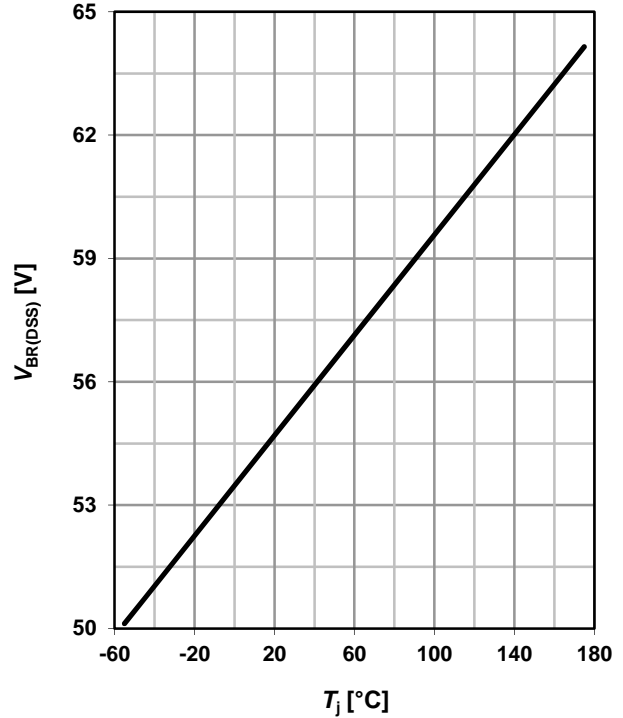
$E_{AS} = f(T_j)$

parameter: I_D



14 Drain-source breakdown voltage

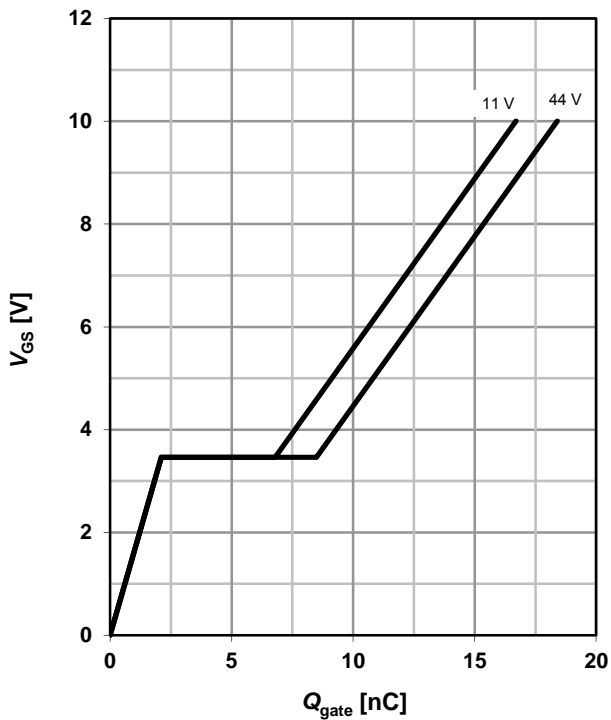
$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$



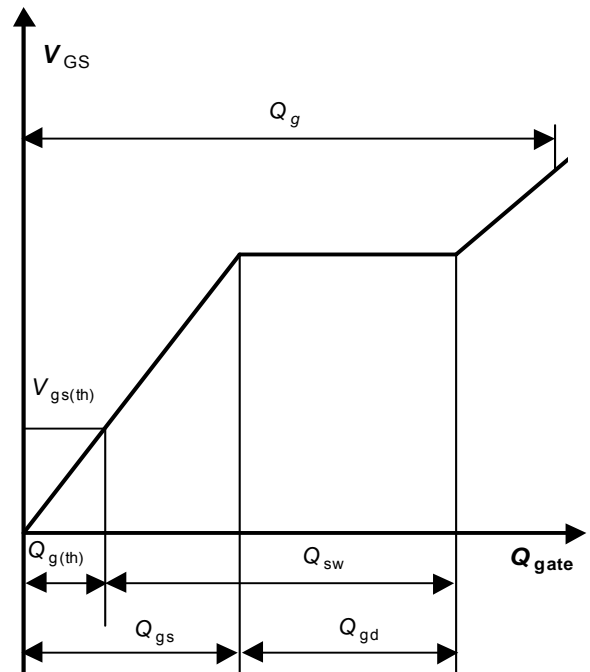
15 Typ. gate charge⁴⁾

$V_{GS} = f(Q_{gate}); I_D = 20 \text{ A pulsed}$

parameter: V_{DD}



16 Gate charge waveforms



Published by
Infineon Technologies AG
81726 Munich, Germany

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If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Version	Date	Changes
Revision 1.0	20.09.2012	Final Data Sheet

单击下面可查看定价，库存，交付和生命周期等信息

[>>Infineon\(英飞凌\)](#)