CoolMOS® Power Transistor

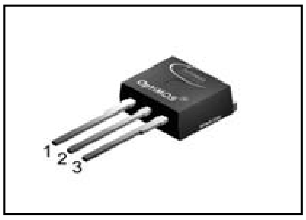
Features

- Lowest figure-of-merit $R_{ON}xQ_g$
- Ultra low gate charge
- Extreme dv/dt rated
- High peak current capability
- Qualified according to JEDEC[1)]for target applications
- Pb-free lead plating; RoHS compliant

Product Summary

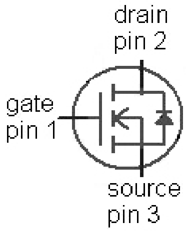
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	0.199	Ω
$Q_{g,typ}$	32	nC

PG-TO262



CoolMOS CP is specially designed for:

- Hard switching topologies, for Server and Telecom



Type	Package	Ordering Code	Marking
IPI60R199CP	PG-TO262	SP000103248	6R199P

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	16	A
		T_C=100 °C	10	
Pulsed drain current[2)]	$I_{D,pulse}$	T_C=25 °C	51	
Avalanche energy, single pulse	E_{AS}	I_D=6.6 A, V_{DD}=50 V	436	mJ
Avalanche energy, repetitive t_{AR}[2),3)]	E_{AR}	I_D=6.6 A, V_{DD}=50 V	0.66	
Avalanche current, repetitive t_{AR}[2),3)]	I_{AR}		6.6	A
MOSFET dv/dt ruggedness	dv/dt	V_{DS}=0...480 V	50	V/ns
Gate source voltage	V_{GS}	static	±20	V
		AC (f>1 Hz)	±30	
Power dissipation	P_{tot}	T_C=25 °C	139	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous diode forward current	I_S	T_C=25 °C	9.9	A
Diode pulse current[2)]	$I_{S,pulse}$		51	
Reverse diode dv/dt[4)]	dv/dt		15	V/ns

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	0.9	K/W
Thermal resistance, junction - ambient	R_{thJA}	leaded	-	-	62	
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	1.6 mm (0.063 in.) from case for 10 s	-	-	260	°C
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=250 µA	600	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=0.66 mA	2.5	3	3.5	
Zero gate voltage drain current	I_{DSS}	V_{DS}=600 V, V_{GS}=0 V, T_j=25 °C	-	-	1	µA
		V_{DS}=600 V, V_{GS}=0 V, T_j=150 °C	-	10	-	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=9.9 A, T_j=25 °C	-	0.18	0.199	Ω
		V_{GS}=10 V, I_D=9.9 A, T_j=150 °C	-	0.49	-	
Gate resistance	R_G	f=1 MHz, open drain	-	2	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz	-	1520	-	pF
Output capacitance	C_{oss}		-	72	-	
Effective output capacitance, energy related[5]	$C_{o(er)}$	V_{GS}=0 V, V_{DS}=0 V to 480 V	-	69	-	
Effective output capacitance, time related[6]	$C_{o(tr)}$		-	180	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=400 V, V_{GS}=10 V, I_D=9.9 A, R_G=3.3 Ω	-	10	-	ns
Rise time	t_r		-	5	-	
Turn-off delay time	$t_{d(off)}$		-	50	-	
Fall time	t_f		-	5	-	
Gate Charge Characteristics						
Gate to source charge	Q_{gs}	V_{DD}=400 V, I_D=9.9 A, V_{GS}=0 to 10 V	-	8	-	nC
Gate to drain charge	Q_{gd}		-	11	-	
Gate charge total	Q_g		-	32	43	
Gate plateau voltage	$V_{plateau}$		-	5.0	-	V
Reverse Diode						
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=9.9 A, T_j=25 °C	-	0.9	1.2	V
Reverse recovery time	t_{rr}	V_R=400 V, I_F=I_S, di_F/dt=100 A/µs	-	340	-	ns
Reverse recovery charge	Q_{rr}		-	5.5	-	µC
Peak reverse recovery current	I_{rrm}		-	33	-	A

[1] J-STD20 and JESD22

[2] Pulse width t_p limited by $T_{j,max}$

[3] Repetitive avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR}*f$.

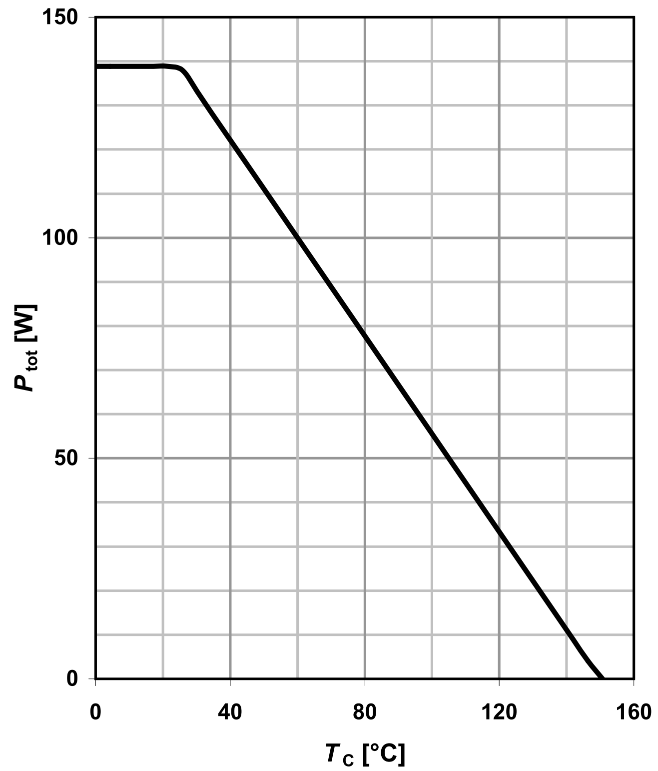
[4] $I_{SD} \leq I_D$, di/dt≤200A/µs, V_{DClink}=400V, $V_{peak} < V_{(BR)DSS}$, $T_j < T_{jmax}$, identical low side and high side switch.

[5] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

[6] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

1 Power dissipation

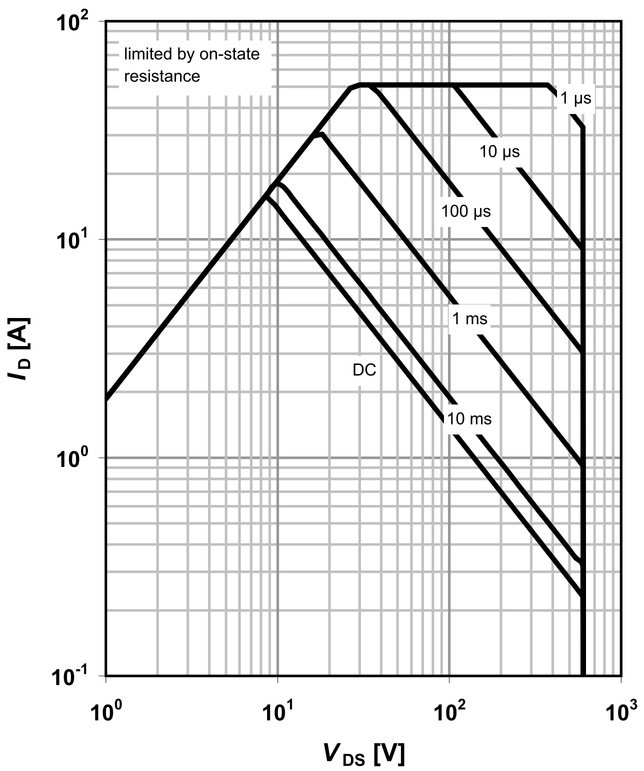
$P_{tot}=f(T_C)$



2 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

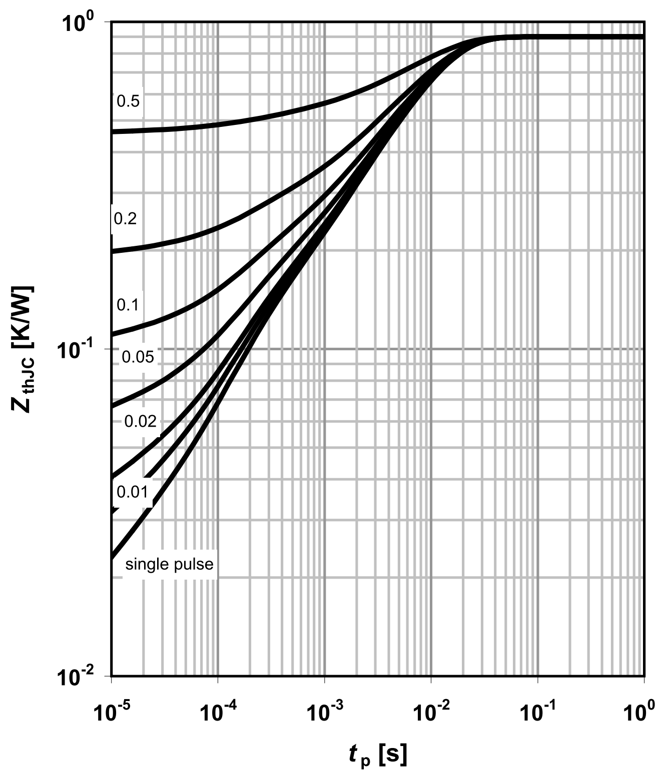
parameter: t_p



3 Max. transient thermal impedance

$Z_{thJC}=f(t_P)$

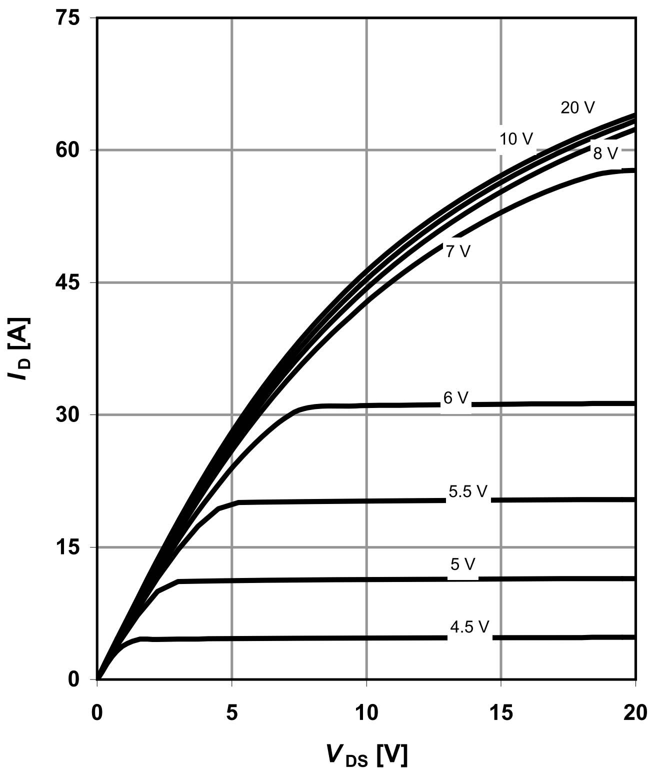
parameter: $D=t_p/T$



4 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

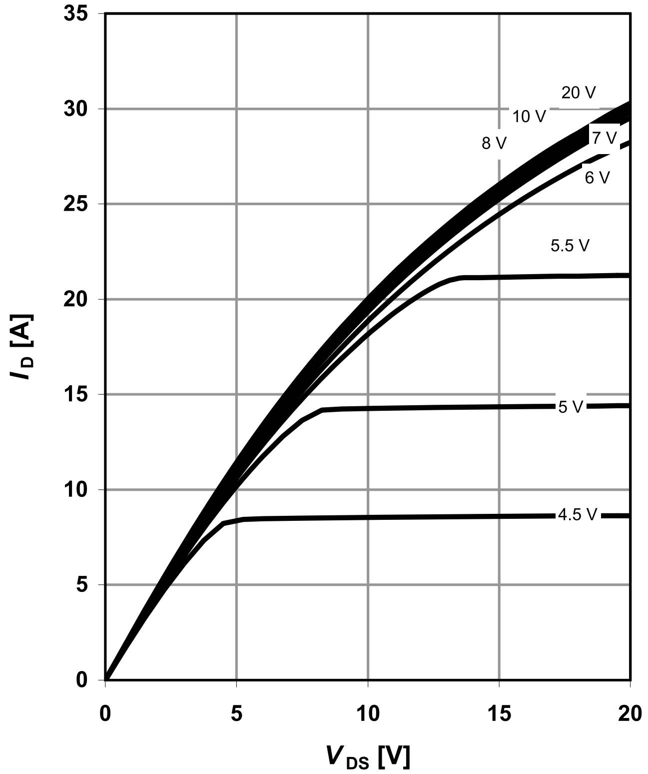
parameter: V_{GS}



5 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=150$ °C

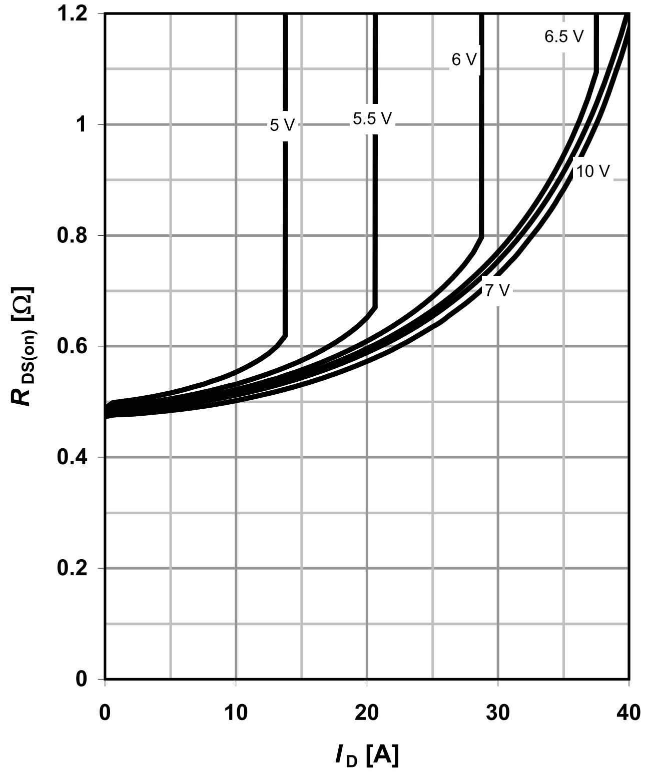
parameter: V_{GS}



6 Typ. drain-source on-state resistance

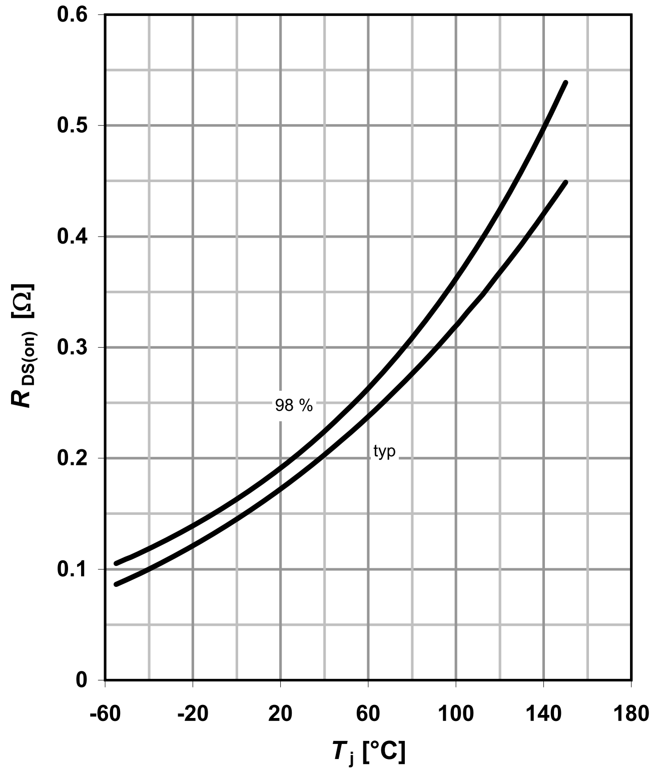
$R_{DS(on)}=f(I_D)$; $T_j=150$ °C

parameter: V_{GS}



7 Drain-source on-state resistance

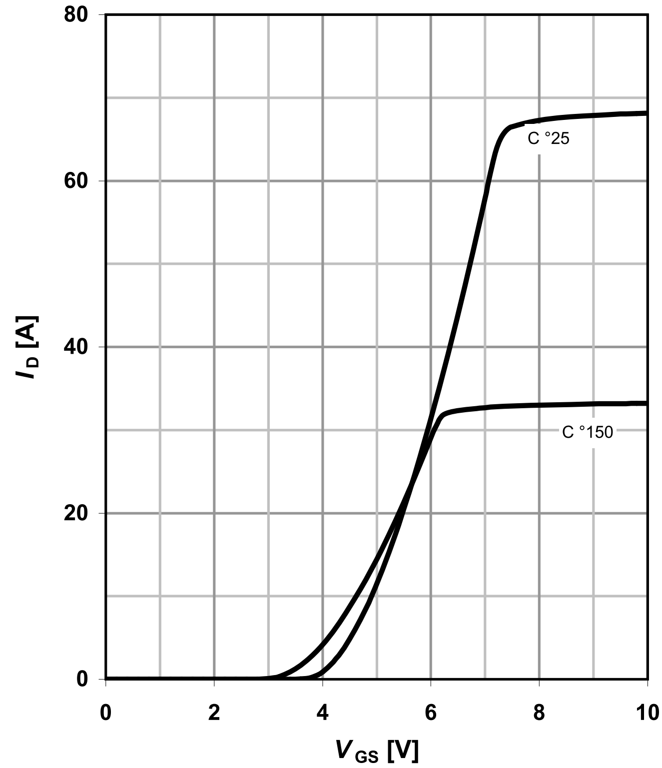
$R_{DS(on)}=f(T_j)$; $I_D=9.9$ A; $V_{GS}=10$ V



8 Typ. transfer characteristics

$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$

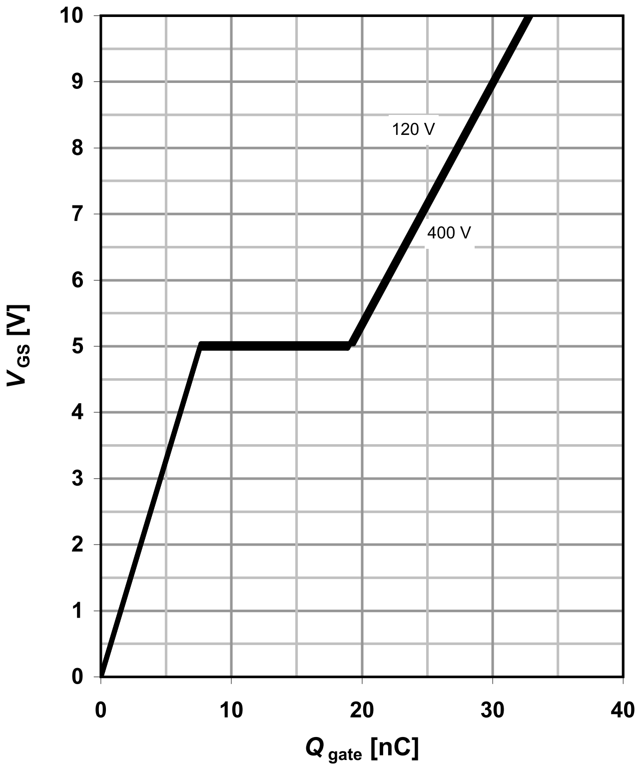
parameter: T_j



9 Typ. gate charge

V_{GS}=f(Q_{gate}); I_D=9.9 A pulsed

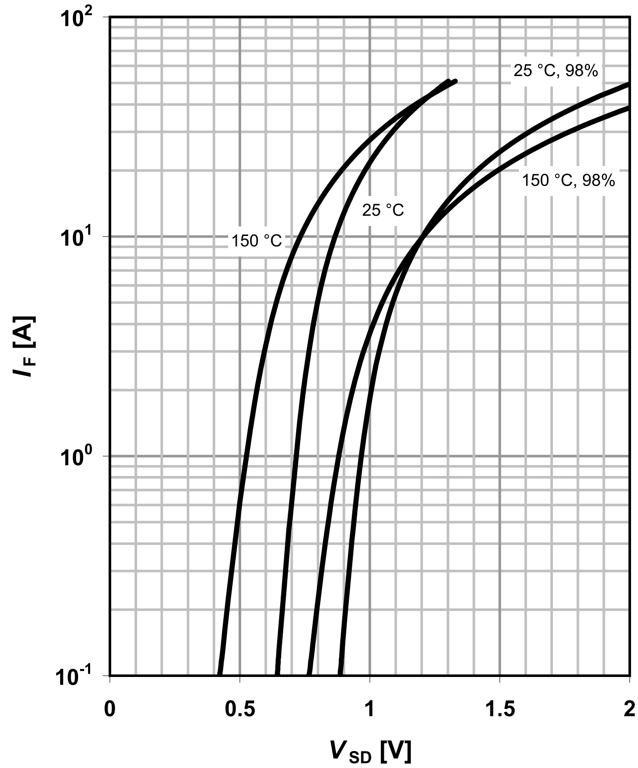
parameter: V_{DD}



10 Forward characteristics of reverse diode

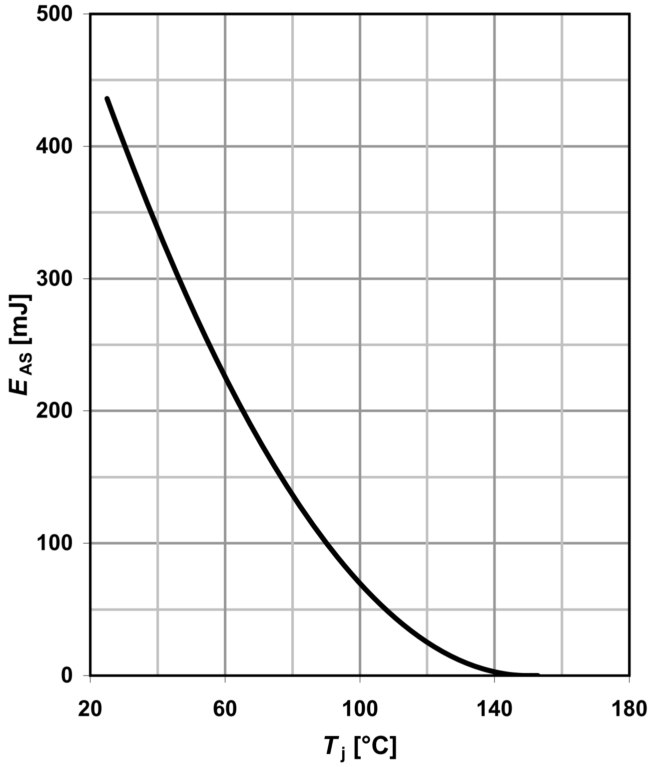
I_F=f(V_{SD})

parameter: T_j



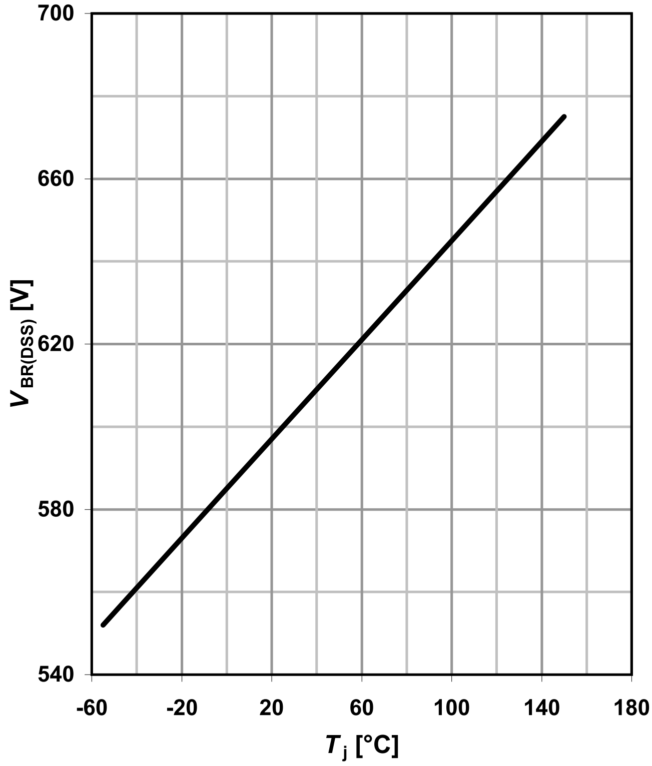
11 Avalanche energy

E_{AS}=f(T_j); I_D=6.6 A; V_{DD}=50 V

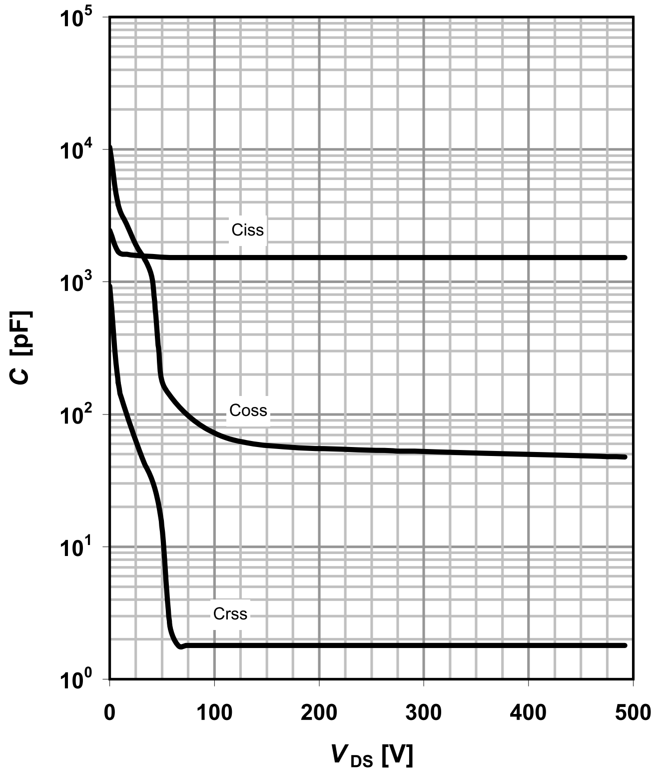


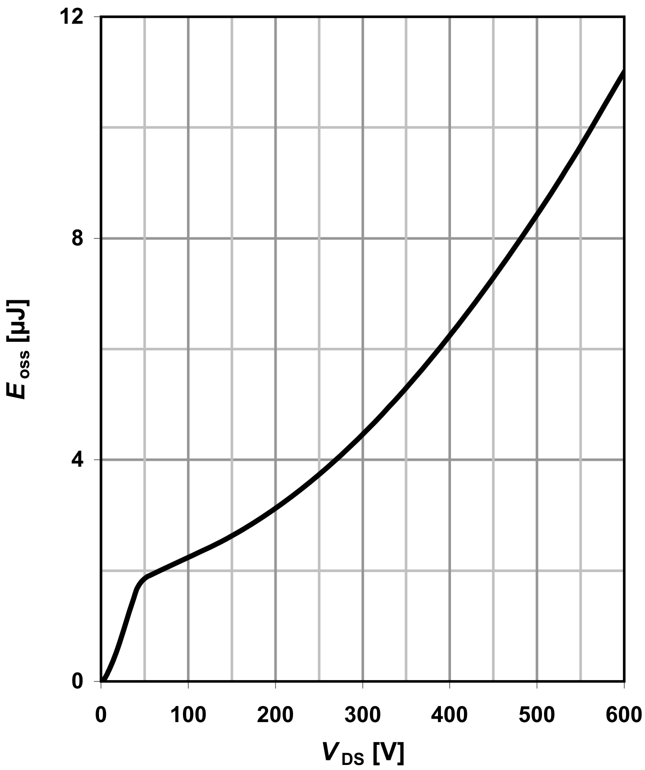
12 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=0.25 mA

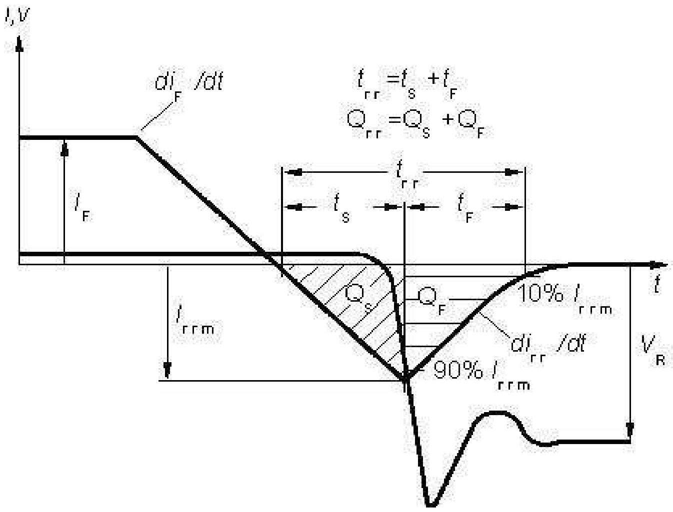


13 Typ. capacitances	**14 Typ. Coss stored energy**
$C=f(V_{DS})$; V_{GS}=0 V; f=1 MHz	$E_{oss}=f(V_{DS})$

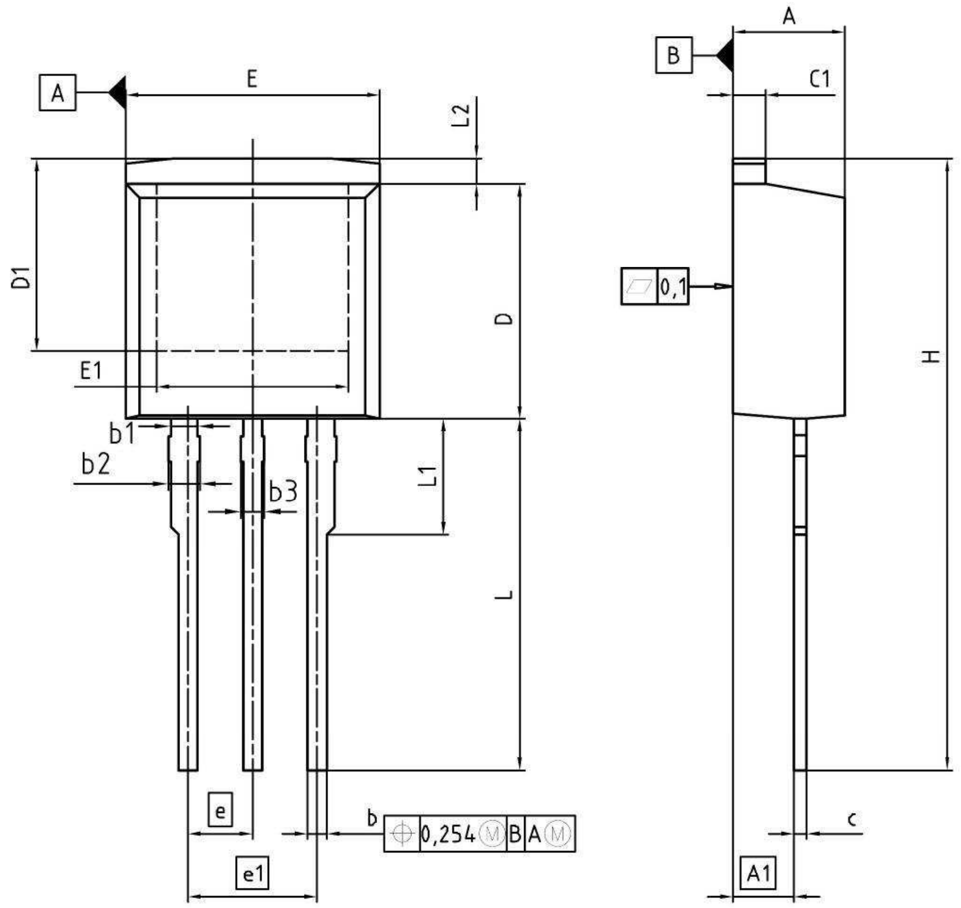




Definition of diode switching characteristics



6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.300	4.572	0.169	0.180
A1	2.150	2.718	0.085	0.107
b	0.650	0.864	0.026	0.034
b1	0.950	1.093	0.037	0.043
b2	0.950	1.400	0.037	0.055
b3	0.650	1.118	0.026	0.044
c	0.330	0.600	0.013	0.024
c1	1.170	1.400	0.046	0.055
D	8.509	9.450	0.335	0.372
D1	6.900	-	0.272	-
E	9.700	10.363	0.382	0.408
E1	6.500	8.600	0.256	0.339
e	2.540		0.100	
e1	5.080		0.200	
N	3		3	
L	13.000	14.000	0.512	0.551
L1	-	4.800	-	0.189
L2	-	1.727	-	0.068

REFERENCE
Z8B00003325

SCALE 0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
05-05-2006

REVISION
03

Figure 1 Outline PG-TO 262, dimensions in mm/inches

Revision History

IPI60R199CP		
Revision: 2017-08-11, Rev. 2.3		
Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.3	2017-08-11	Revised package drawing on Page 9

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