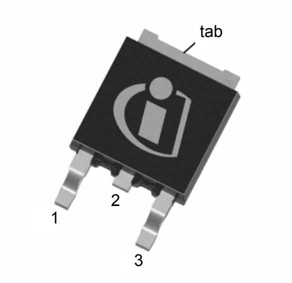
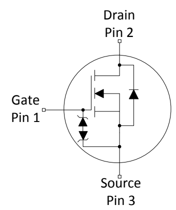
MOSFET

600V CoolMOS™ P7 Power Transistor

The CoolMOS™ 7th generation platform is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. The 600V CoolMOS™ P7 series is the successor to the CoolMOS™ P6 series. It combines the benefits of a fast switching SJ MOSFET with excellent ease of use, e.g. very low ringing tendency, outstanding robustness of body diode against hard commutation and excellent ESD capability. Furthermore, extremely low switching and conduction losses make switching applications even more efficient, more compact and much cooler.

DPAK





Features

- Suitable for hard and soft switching (PFC and LLC) due to an outstanding commutation ruggedness
- Significant reduction of switching and conduction losses
- Excellent ESD robustness >2kV (HBM) for all products
- Better $R_{DS(on)}$/package products compared to competition enabled by a low $R_{DS(on)}$*A (below 1Ohm*mm²)
- Product validation acc. JEDEC Standard

Benefits

- Ease of use and fast design-in through low ringing tendency and usage across PFC and PWM stages
- Simplified thermal management due to low switching and conduction losses
- Increased power density solutions enabled by using products with smaller footprint and higher manufacturing quality due to >2 kV ESD protection
- Suitable for a wide variety of applications and power ranges

Potential applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	360	mΩ
$Q_{g,typ}$	13	nC
$I_{D,pulse}$	26	A
E_{oss} @ 400V	1.6	µJ
Body diode di_F/dt	900	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPD60R360P7S	PG-TO 252-3	60S360P7	see Appendix A

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Table of Contents

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1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	9 6	A	T_C=25°C T_C=100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	26	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	27	mJ	I_D=2.5A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.14	mJ	I_D=2.5A; V_{DD}=50V; see table 10
Avalanche current, single pulse	I_{AS}	-	-	2.5	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	80	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	41	W	T_C=25°C
Storage temperature	T_{stg}	-40	-	150	°C	-
Operating junction temperature	T_j	-40	-	150	°C	-
Mounting torque	-	-	-	-	Ncm	-
Continuous diode forward current	I_S	-	-	9	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	26	A	T_C=25°C
Reverse diode dv/dt[3]	dv/dt	-	-	50	V/ns	V_{DS}=0...400V, I_{SD}<=9A, T_j=25°C see table 8
Maximum diode commutation speed	di_F/dt	-	-	900	A/µs	V_{DS}=0...400V, I_{SD}<=9A, T_j=25°C see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

[1] Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.50
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch with identical R_G

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2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.04	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	reflow MSL3

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3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	V_{DS}=V_{GS}, I_D=0.14mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=600V, V_{GS}=0V, T_j=25°C V_{DS}=600V, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	1000	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.300 0.702	0.360 -	Ω	V_{GS}=10V, I_D=2.7A, T_j=25°C V_{GS}=10V, I_D=2.7A, T_j=150°C
Gate resistance	R_G	-	6.2	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	555	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	10	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Effective output capacitance, energy related[1]	$C_{o(er)}$	-	20	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	214	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	8	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=2.7A, R_G=10.0Ω; see table 9
Rise time	t_r	-	7	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=2.7A, R_G=10.0Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	42	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=2.7A, R_G=10.0Ω; see table 9
Fall time	t_f	-	10	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=2.7A, R_G=10.0Ω; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	3	-	nC	V_{DD}=400V, I_D=2.7A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	4	-	nC	V_{DD}=400V, I_D=2.7A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	13	-	nC	V_{DD}=400V, I_D=2.7A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.2	-	V	V_{DD}=400V, I_D=2.7A, V_{GS}=0 to 10V

[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

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Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=2.7A, T_j=25°C
Reverse recovery time	t_{rr}	-	145	-	ns	V_R=400V, I_F=1A, di_F/dt=100A/µs; see table 8
Reverse recovery charge	Q_{rr}	-	0.74	-	µC	V_R=400V, I_F=1A, di_F/dt=100A/µs; see table 8
Peak reverse recovery current	I_{rrm}	-	11	-	A	V_R=400V, I_F=1A, di_F/dt=100A/µs; see table 8

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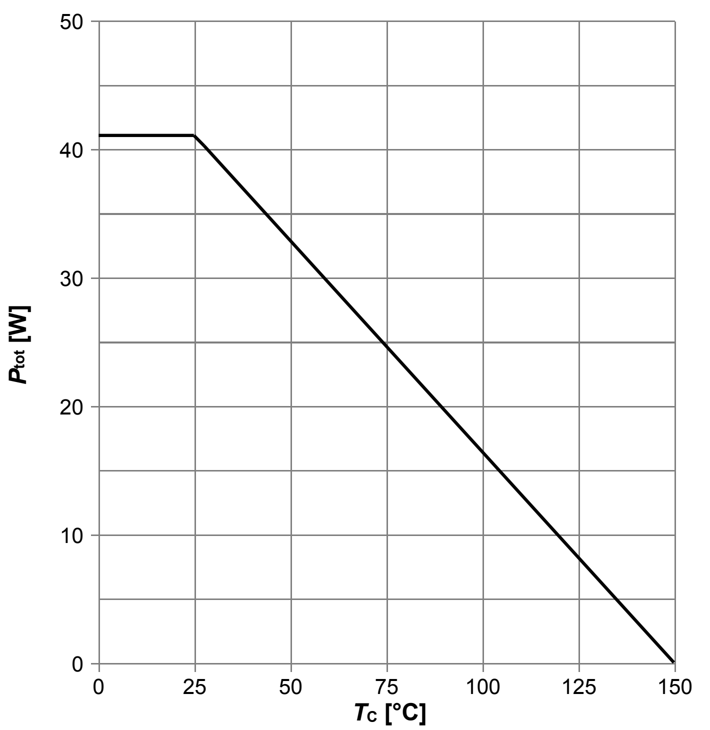
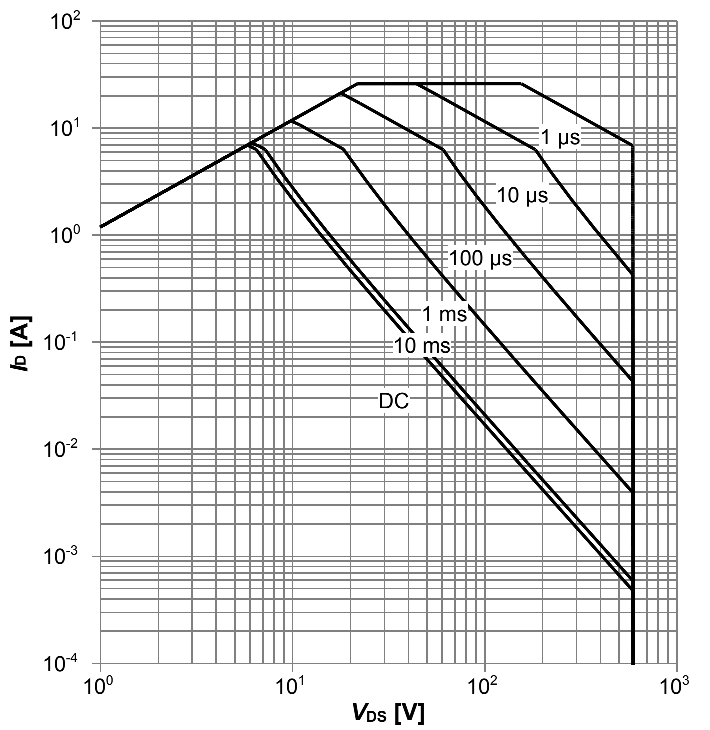
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



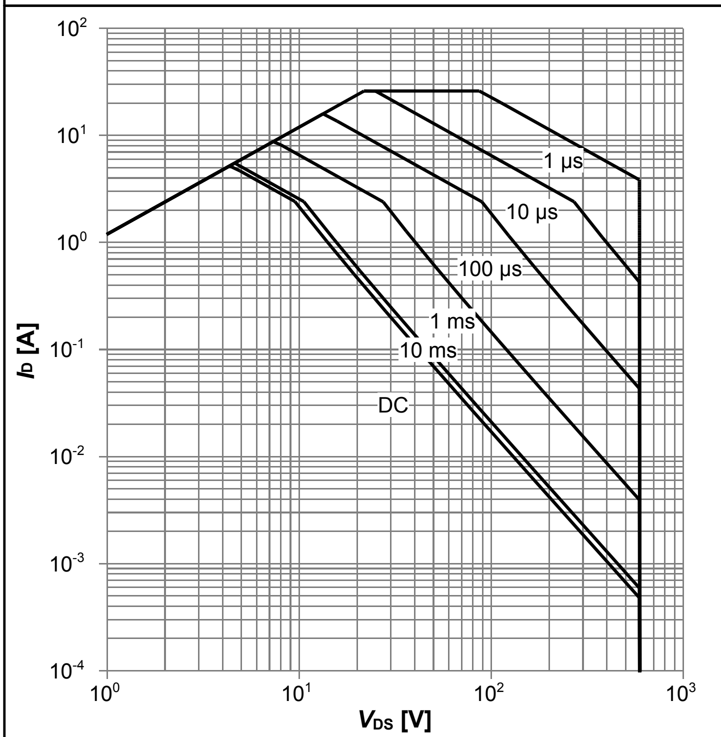
P_{tot}=f(T_C)

Diagram 2: Safe operating area



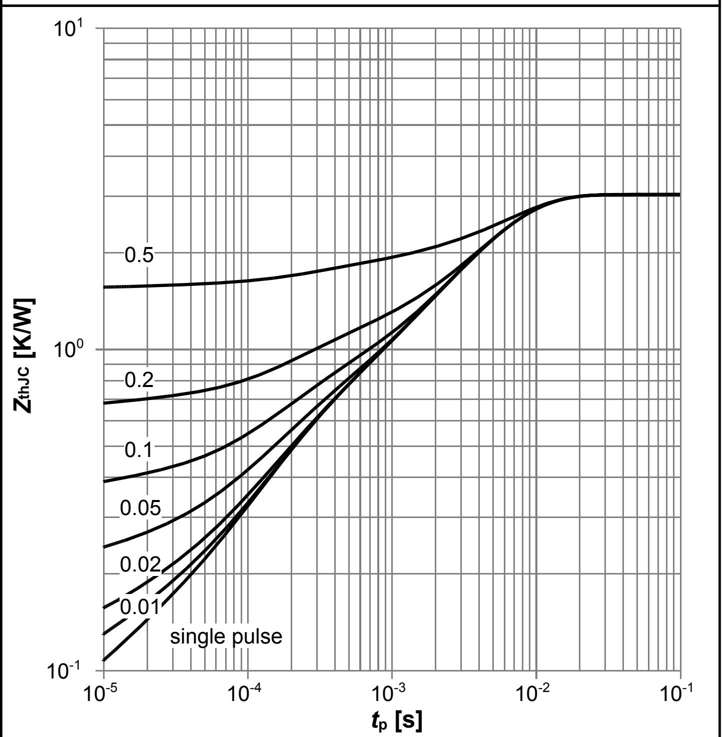
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



Z_{thJC} =f(t_P); parameter: D=t_p/T

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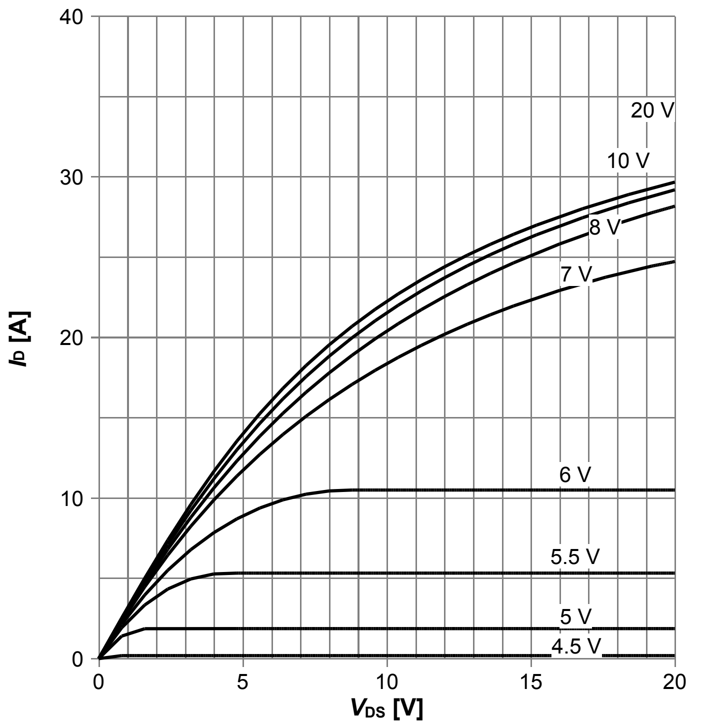
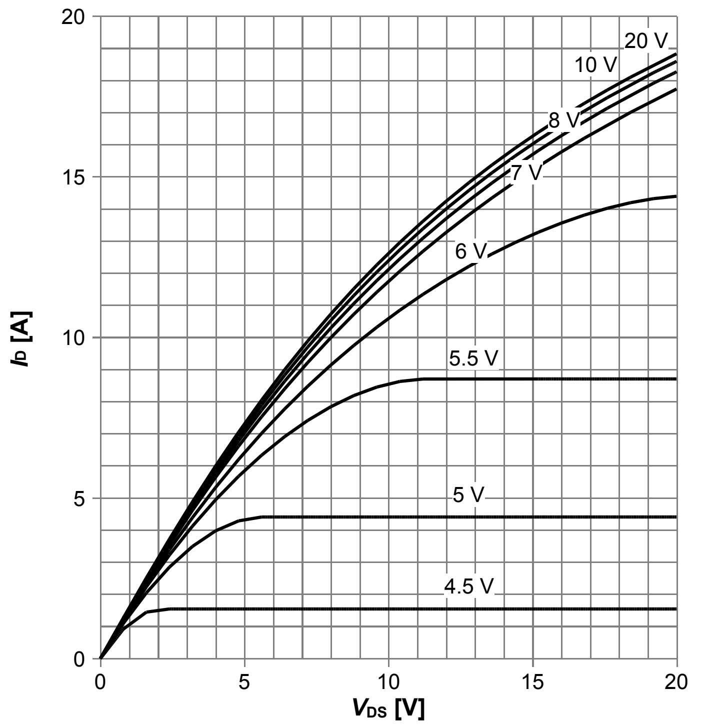
Diagram 5: Typ. output characteristics



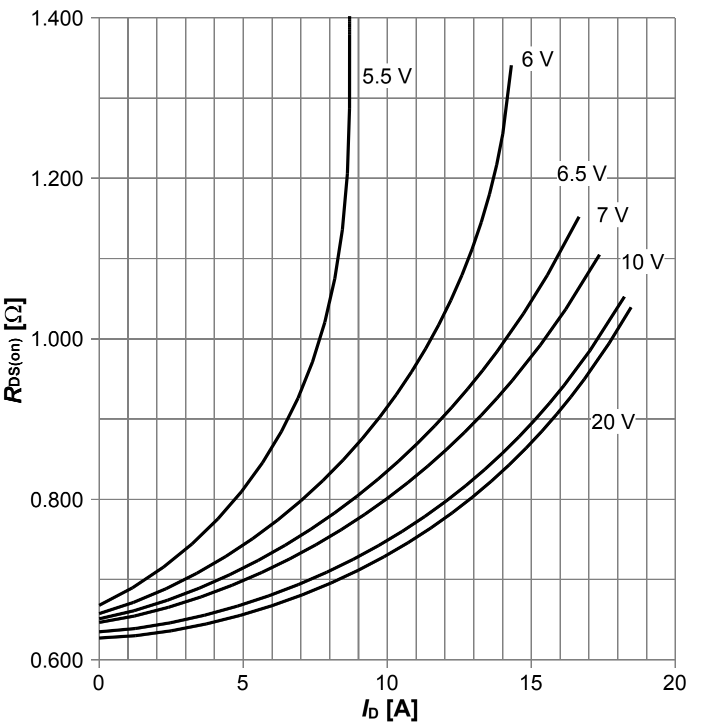
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



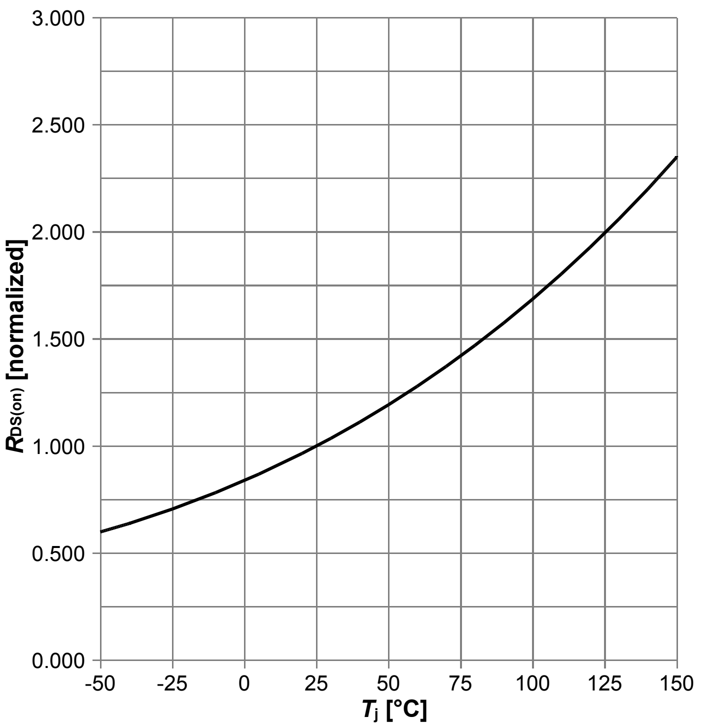
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



$R_{DS(on)}$=f(T_j); I_D=2.7 A; V_{GS}=10 V

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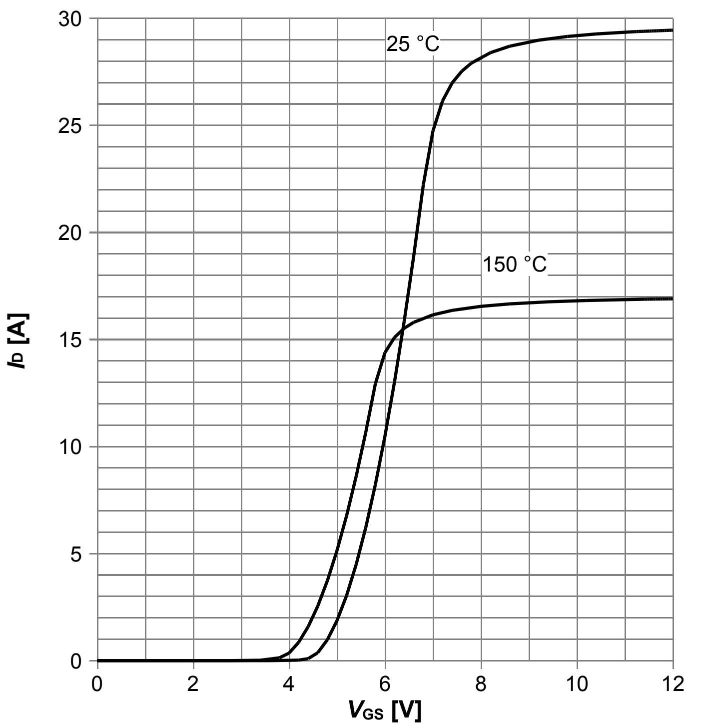
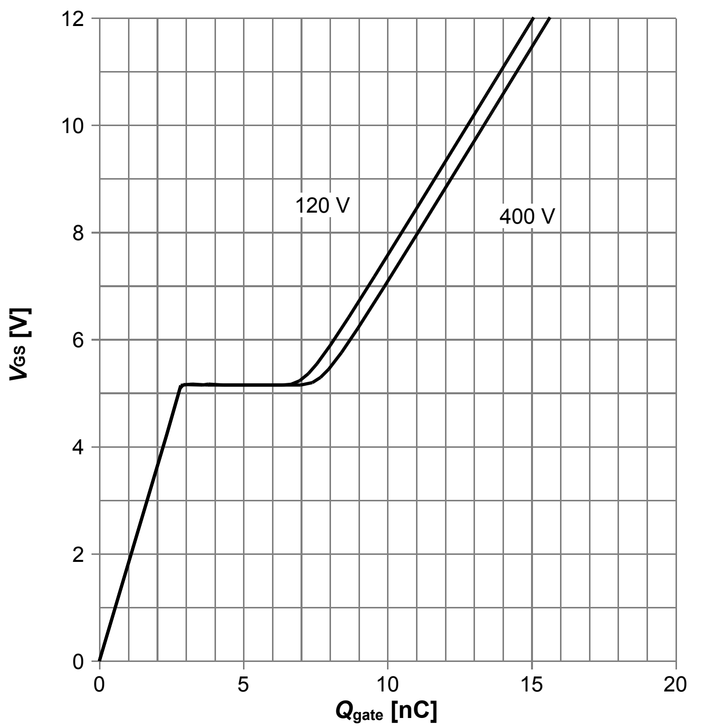
Diagram 9: Typ. transfer characteristics	Diagram 10: Typ. gate charge
	
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j	V_{GS}=f(Q_{gate}); I_D=2.7 A pulsed; parameter: V_{DD}

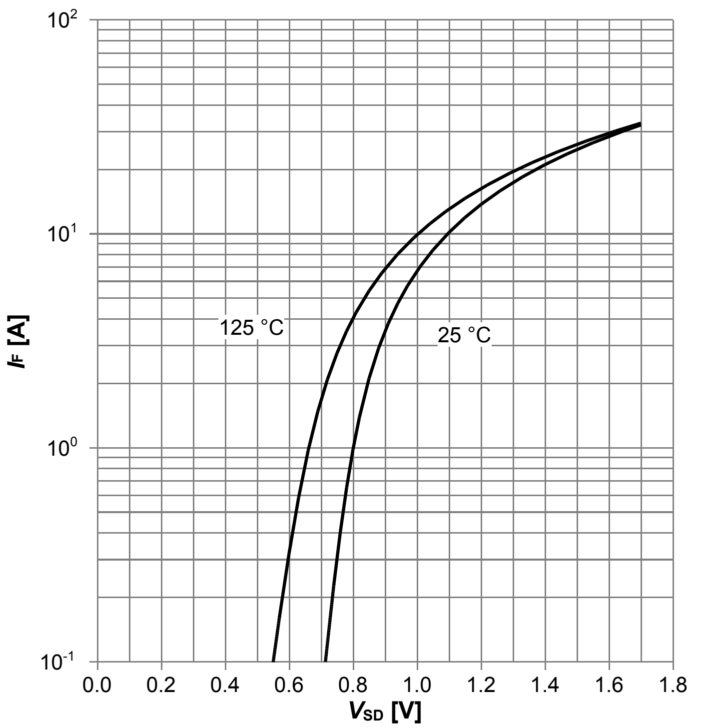
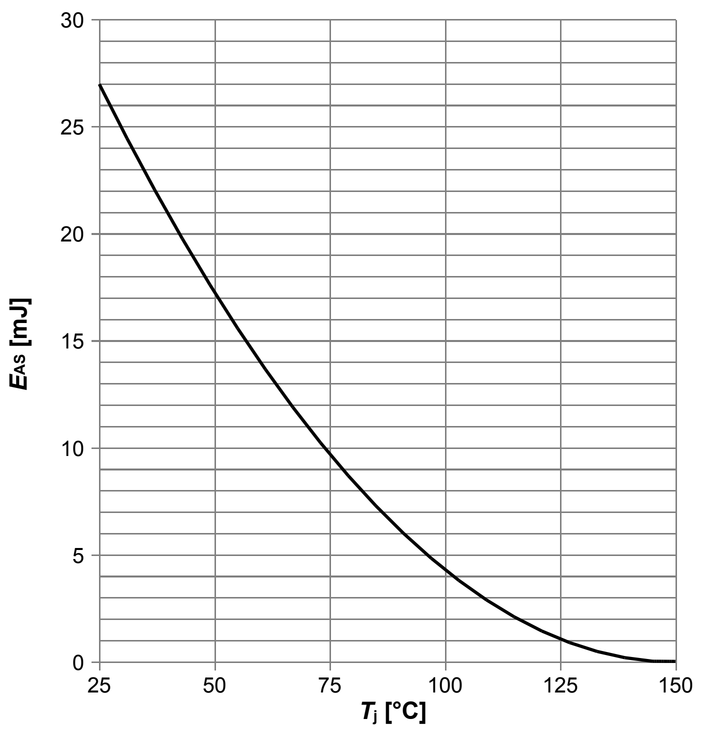
Diagram 11: Forward characteristics of reverse diode	Diagram 12: Avalanche energy
	
I_F=f(V_{SD}); parameter: T_j	E_{AS}=f(T_j); I_D=2.5 A; V_{DD}=50 V

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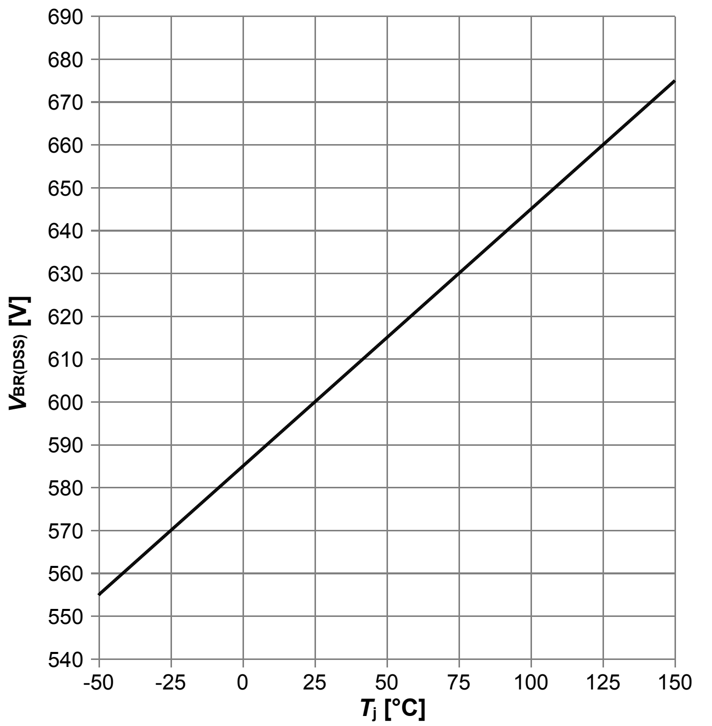
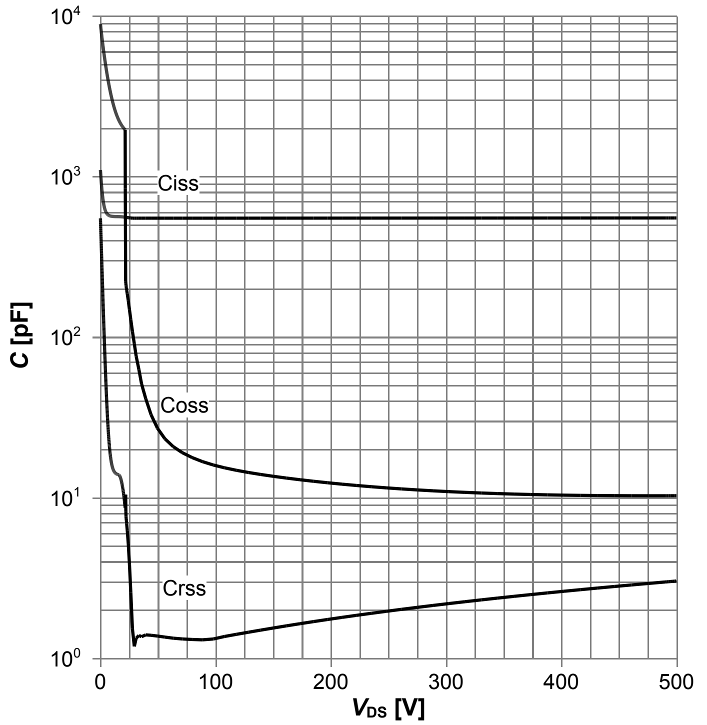
Diagram 13: Drain-source breakdown voltage



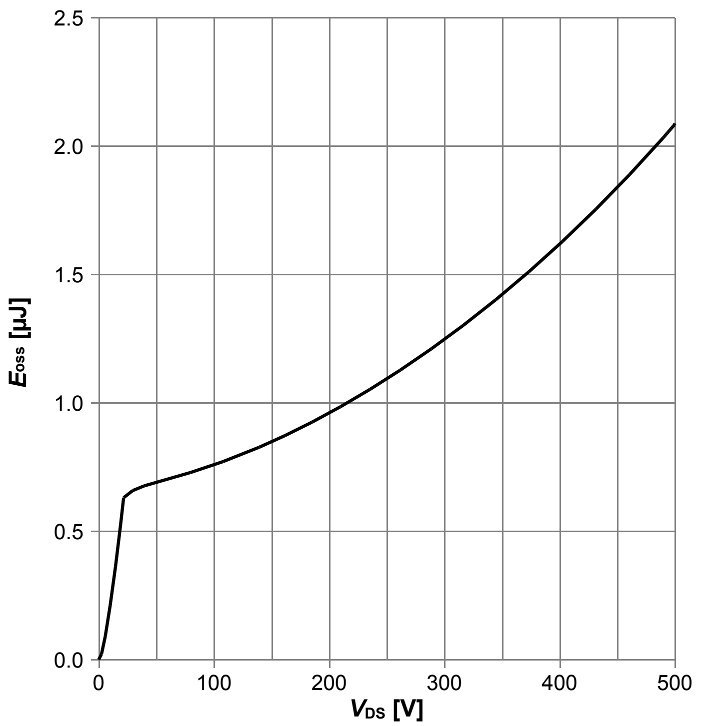
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy



E_{oss}=f(V_{DS})

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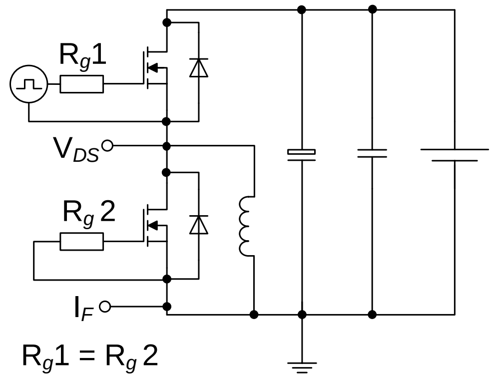
5 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics	Diode recovery waveform



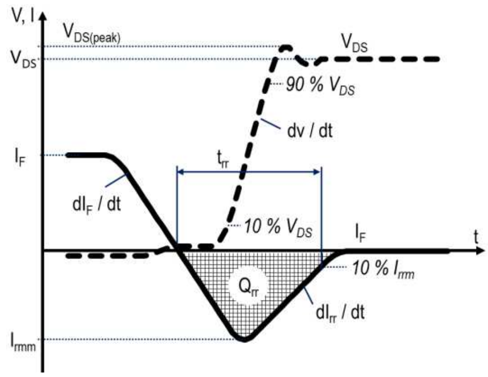
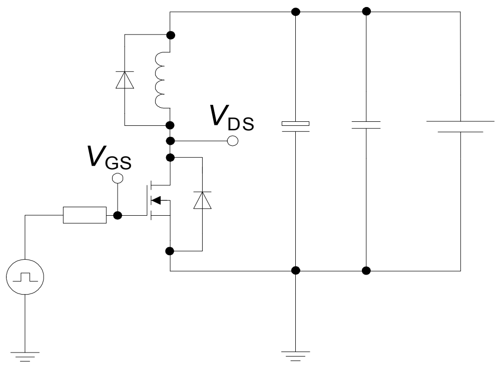


Table 9 Switching times

Switching times test circuit for inductive load	Switching times waveform



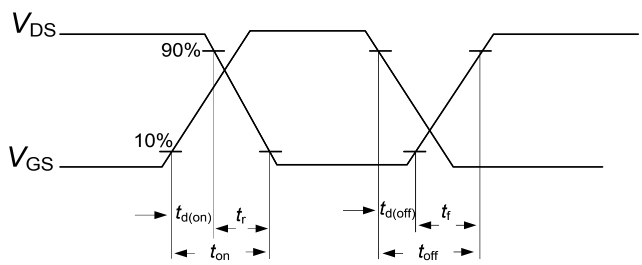
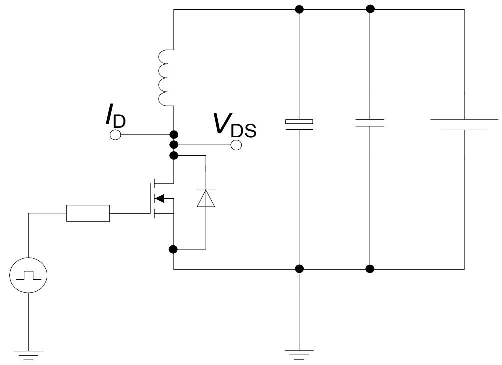
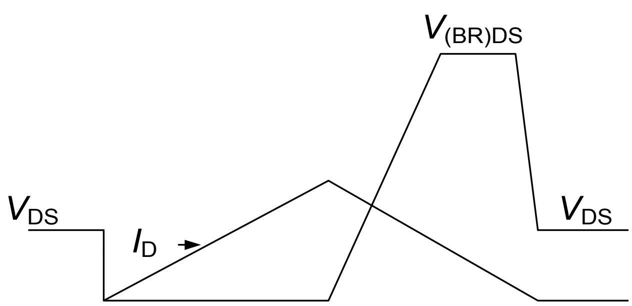


Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform





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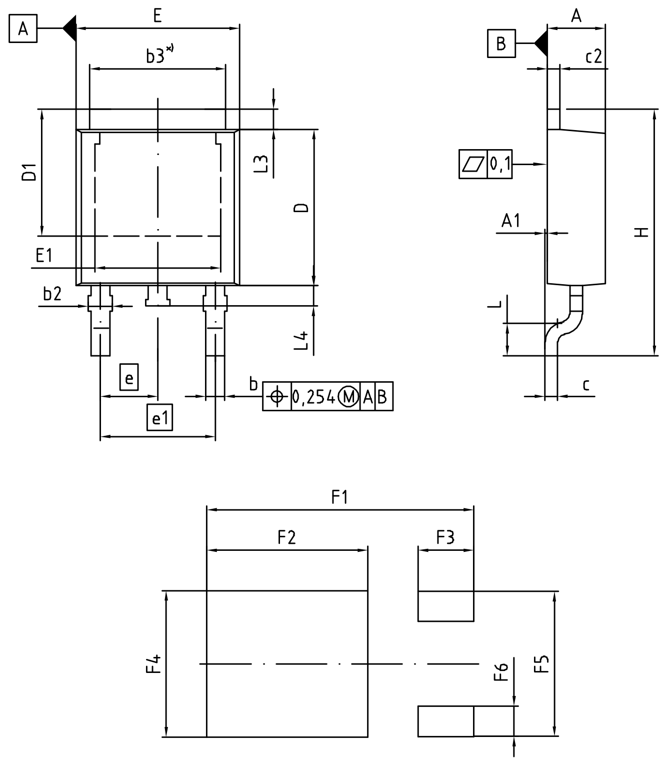
6 Package Outlines

TO252-3 (DPAK)



*) mold flash not included

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.21	0.185	0.205
e	2.29 (BSC)		0.090 (BSC)	
e1	4.57		0.180	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.60		0.417	
F2	6.40		0.252	
F3	2.20		0.087	
F4	5.80		0.228	
F5	5.76		0.227	
F6	1.20		0.047	

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Z8B00003328

SCALE 0 2.0 4mm

EUROPEAN PROJECTION

ISSUE DATE
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REVISION
04

Figure 1 Outline PG-TO 252-3, dimensions in mm/inches

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7 Appendix A

Table 11 Related Links

- **IFX CoolMOS P7 Webpage:** www.infineon.com
- **IFX CoolMOS P7 application note:** www.infineon.com
- **IFX CoolMOS P7 simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

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Revision History

IPD60R360P7S

Revision: 2018-04-25, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2017-06-12	Release of final version
2.1	2018-04-25	Updated diagram scalings; Nomenclature of product qualification grade was changed; MSL level changed from 1 to 3

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