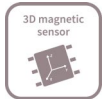


# TLE493D-A2B6

## Low Power 3D Hall Sensor with I<sup>2</sup>C Interface



## User Manual

### About this document

#### Scope and purpose

This document provides product information and descriptions regarding:

- I<sup>2</sup>C Registers
- I<sup>2</sup>C Interface
- Diagnostic

#### Intended audience

This document is aimed at engineers and developers of hard and software using the sensor TLE493D-A2B6.

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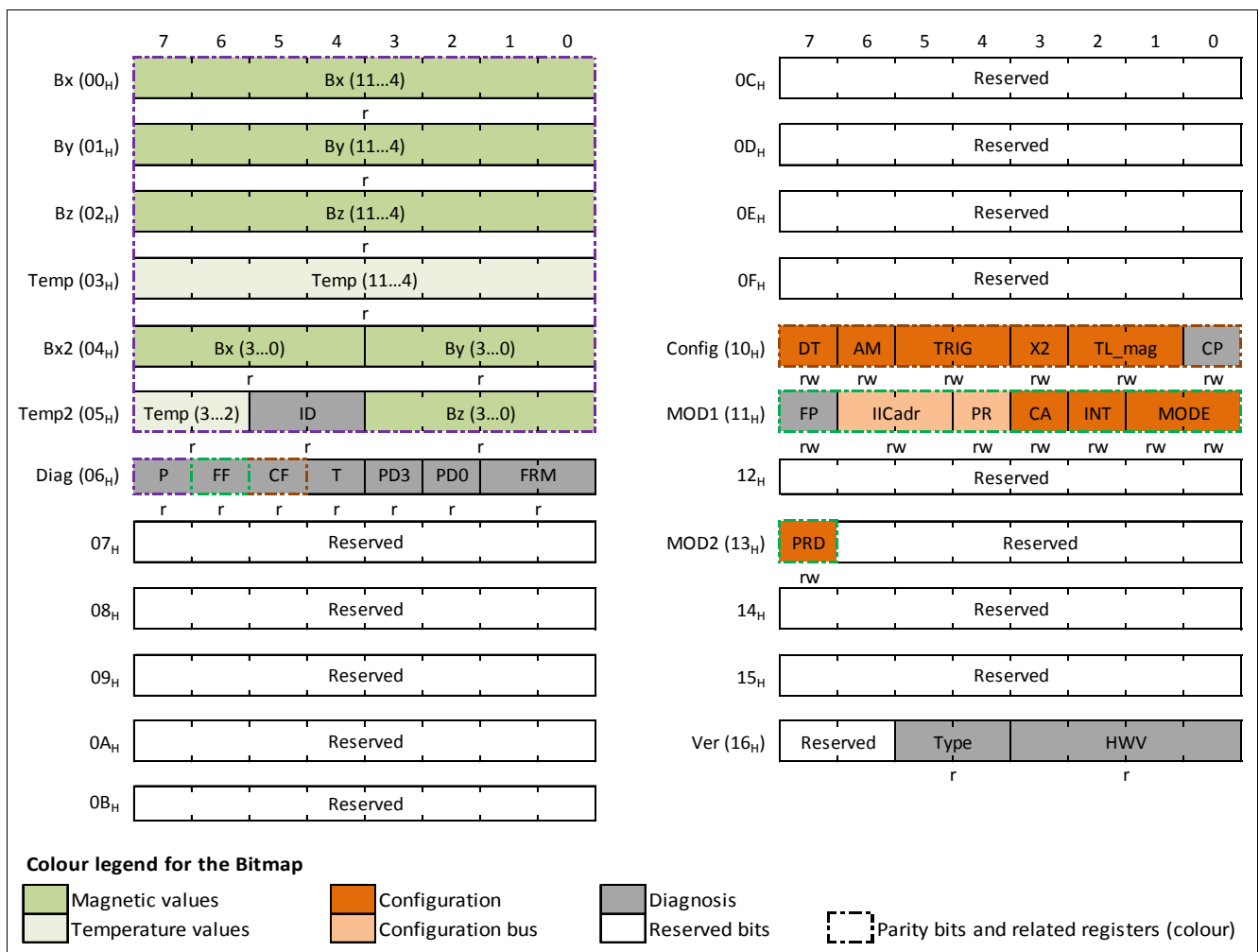
# 1 I<sup>2</sup>C Registers

The TLE493D-A2B6 includes several registers that can be accessed via Inter-Integrated Circuit interface (I<sup>2</sup>C) to read data as well as to write and configure settings.

## 1.1 Registers overview

A bitmap overview is presented in **Figure 1**. Basically the following sections are available:

- measurement data (green bits in registers 00<sub>H</sub> till 05<sub>H</sub>)
- sensor status and diagnostics (grey bits in registers 05<sub>H</sub>, 06<sub>H</sub>, 10<sub>H</sub> and 11<sub>H</sub>)
- configuration parameters such as the power mode (orange bits in registers 10<sub>H</sub>, 11<sub>H</sub> and 13<sub>H</sub>)



**Figure 1** TLE493D-A2B6 Bitmap

The diagnostic register 06<sub>H</sub> contains parity information as a diagnostic mechanism. The bitmap illustrates this and marks the relationship of the sections to this flags with different colored lines/frames around the bit contents.

**Table 1 Registers overview**

Register name	Register long name	Address
<b>Bx, By and Bz</b>	<b>Magnetic values MSBs</b>	00 <sub>H</sub> , 01 <sub>H</sub> , 02 <sub>H</sub>
<b>Temp</b>	<b>Temperature value MSBs</b>	03 <sub>H</sub>
<b>Bx2</b>	<b>Magnetic values LSBs</b>	04 <sub>H</sub>
<b>Temp2</b>	<b>Temperature and magnetic LSBs and device address</b>	05 <sub>H</sub>
<b>Diag</b>	<b>Sensor diagnostic and status register</b>	06 <sub>H</sub>
<b>Config</b>	<b>Configuration register</b>	10 <sub>H</sub>
<b>MOD1</b>	<b>Power mode, interrupt, address, parity</b>	11 <sub>H</sub>
<b>MOD2</b>	<b>Low Power Mode update rate</b>	13 <sub>H</sub>
<b>Ver</b>	<b>Version register</b>	16 <sub>H</sub>

## 1.2 Register descriptions

The I<sup>2</sup>C registers can be read or written at any time. It is recommended to read measurement data in a synchronized fashion, i.e. after an interrupt pulse (/INT). This avoids reading inconsistent sensor or diagnostic data, especially in fast mode. Additionally, several flags can be checked to ensure the register values are consistent and the ADC was not running at the time of readout.

### 1.2.1 Bit types

The TLE493D-A2B6 contains read bits, write bits and reserved bits.

**Table 2 Bit Types**

Abbreviation	Function	Description
r	Read	Read-only bits
rw	Read Write	Readable and writable bit
	Reserved	Bits that must keep the default values (read prior to write required)

### 1.2.2 Measurement data and registers combined in the I<sup>2</sup>C parity bit “P”

The I<sup>2</sup>C communication of the registers in this chapter is protected with the parity bit “P”, described in the Diag register with the address 06<sub>H</sub>. See also [Figure 1](#) - parity bits and related registers.

To make sure all data is consistent, the registers from 00<sub>H</sub> to 06<sub>H</sub> should be read with the same I<sup>2</sup>C command. Otherwise, the sampled data (X, Y, Z, Temperature) may correspond to different conversion cycles.

## TLE493D-A2B6

### I<sup>2</sup>C Registers

#### Magnetic values MSBs

Register names	Address	Reset Value
Bx, By and Bz	00 <sub>H</sub> 01 <sub>H</sub> 02 <sub>H</sub>	80 <sub>H</sub>

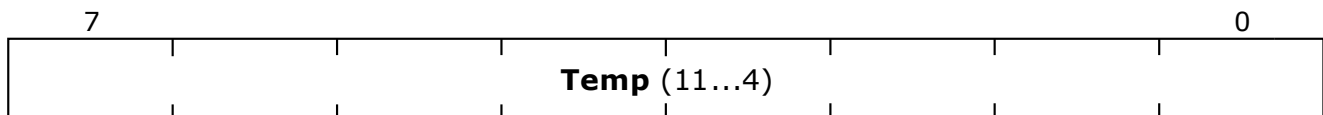


Field	Bits	Type	Description
Bx, By and Bz	7:0	r	<b>Bx, By and Bz values</b> Signed value as two's complement from the HALL probes in the x, y and z-direction of the magnetic field. Contains the eight Most Significant Bits. If Bz is deactivated the Bz value is the reset value.

Back to [TLE493D-A2B6 Bitmap](#).

#### Temperature value MSBs

Register name	Address	Reset Value
Temp	03 <sub>H</sub>	80 <sub>H</sub>

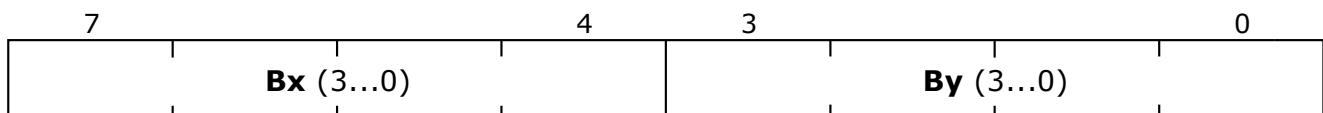


Field	Bits	Type	Description
Temp	7:0	r	<b>Temperature value</b> Signed value as two's complement. If the temperature measurement is deactivated, the Temp value is the reset value.

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#### Magnetic values LSBs

Register name	Address	Reset Value
Bx2	04 <sub>H</sub>	00 <sub>H</sub>



## TLE493D-A2B6

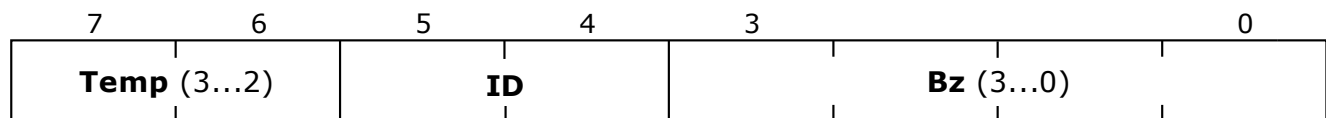
### I<sup>2</sup>C Registers

Field	Bits	Type	Description
<b>Bx</b>	7:4	r	<b>Bx value</b> Signed value as two's complement from the HALL probes in the x-direction of the magnetic field. Contains the four Least Significant Bits.
<b>By</b>	3:0	r	<b>By value</b> Signed value as two's complement from the HALL probes in the y-direction of the magnetic field. Contains the four Least Significant Bits.

Back to [TLE493D-A2B6 Bitmap](#).

### Temperature and magnetic LSBs and device address

Register name	Address	Reset Value
Temp2	05 <sub>H</sub>	00 <sub>H</sub>



Field	Bits	Type	Description
<b>Temp</b>	7:6	r	<b>Temperature value</b> Signed value as two's complement. If the temperature measurement is deactivated, the Temp value is the reset value.
<b>ID</b>	5:4	r	<b>ID</b> Readback of the sensor ID, from <b>lICadr</b> . $\mu$ C shall verify the address sent by the sensor. See <a href="#">Table 4</a> .
<b>Bz</b>	3:0	r	<b>Bz value</b> Signed value as two's complement from the HALL probes in the z-direction of the magnetic field. Contains the four Least Significant Bits. If Bz is deactivated the Bz value is 0 <sub>H</sub> .

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### 1.2.3 Configuration registers combined in the I<sup>2</sup>C parity flag “CF”

The I<sup>2</sup>C communication of the registers in this chapter is protected by the parity bit **CF**, which is described in the Diag register with the address 06<sub>H</sub>. See also [Figure 1](#) - parity bits and related registers.

#### Configuration register

Register name	Address	Reset Value
Config	10 <sub>H</sub>	00 <sub>H</sub>

7	6	5	4	3	2	1	0
<b>DT</b>	<b>AM</b>	<b>TRIG</b>		<b>X2</b>	<b>TL_mag</b>		<b>CP</b>

Field	Bits	Type	Description
<b>DT</b>	7	rw	<b>Disable Temperature</b> If 0 <sub>B</sub> temperature measurement is enabled. If 1 <sub>B</sub> temperature measurement is disabled. This means the Bx, By and Bz channels are measured. The Temp channel is disabled and contains the reset value until a new conversion with Temp is done.
<b>AM</b>	6	rw	<b>X/Y Angular Measurement</b> If 0 <sub>B</sub> the Bz measurement is enabled. If 1 <sub>B</sub> and the DT bit = 1 <sub>B</sub> the Bz measurement is disabled. This means the Bx and By channel is measured. The channels Bz and Temp contain the reset values until a new conversion with Bz and Temp is done. Note: If the DT bit = 0 <sub>B</sub> , the AM bit don't care.
<b>TRIG</b>	5:4	rw	<b>Trigger options</b> If PR bit = 1 <sub>B</sub> (1-byte read protocol), the TRIG bits define the trigger mode of the device: If 00 <sub>B</sub> no ADC trigger on read. If 01 <sub>B</sub> ADC trigger on read before first MSB. If 1x <sub>B</sub> ADC trigger on read after register 05 <sub>H</sub> . If PR bit = 0 <sub>B</sub> these bits have no effect.
<b>X2</b>	3	rw	<b>Short-range sensitivity</b> When this bit is set, the sensitivity of the Bx, By, and Bz ADC-conversion is doubled by a longer ADC integration time. The Temp result will not change, neither in sensitivity nor conversion time. See <a href="#">Table 3</a> .
<b>TL_mag</b>	2:1	rw	<b>Magnetic temperature compensation</b> There are two bits for setting the sensitivity over temperature of the sensor to compensate a magnet temperature coefficient. If 00 <sub>B</sub> → TC <sub>0</sub> (no compensation) If 01 <sub>B</sub> → TC <sub>1</sub> If 10 <sub>B</sub> → TC <sub>2</sub> If 11 <sub>B</sub> → TC <sub>3</sub>
<b>CP</b>	0	rw	<b>Configuration parity</b> The register 10 <sub>H</sub> is even parity protected with this bit. On startup or reset, this parity is OK and the <b>CF</b> bit in the status register 06 <sub>H</sub> is set.

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**Table 3** X2 bit

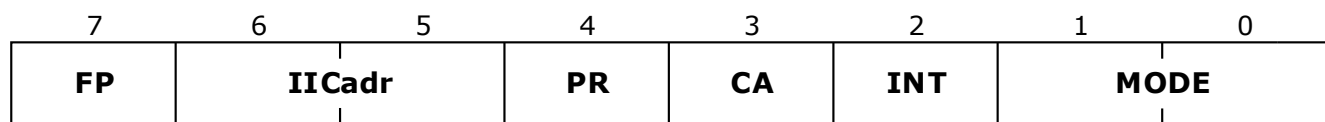
X2 bit	Bx (11 ... 0)	By (11 ... 0)	Bz (11 ... 0)	T (11 ... 2)
0 <sub>B</sub>	Bx full-range	By full-range	Bz full-range	T full-range
1 <sub>B</sub>	Bx short-range	By short-range	Bz short-range	T full-range

### 1.2.4 Mode registers combined in the I<sup>2</sup>C parity flag “FF”

The I<sup>2</sup>C communication of the registers in this chapter is protected with the parity bit “FF”, described in the Diag register with the address 06<sub>H</sub>. See also [Figure 1](#) - parity bits and related registers.

#### Power mode, interrupt, address, parity

Register name	Address	Reset Value
MOD1	11 <sub>H</sub>	00 <sub>H</sub>



Field	Bits	Type	Description
FP	7	rw	<b>Fuse parity</b> The registers 11 <sub>H</sub> and 13 <sub>H</sub> (bit 7) are odd parity protected with this bit. If this parity bit is incorrect please see <a href="#">FF</a> bit. To exit this state a sensor reset is necessary.
IICadr	6:5	rw	<b>I<sup>2</sup>C address</b> Bits can be set to 00 <sub>B</sub> , 01 <sub>B</sub> , 10 <sub>B</sub> or 11 <sub>B</sub> to define the slave address in bus configuration. See <a href="#">Table 4</a> and data sheet.
PR	4	rw	<b>I<sup>2</sup>C 1-byte or 2-byte read protocol</b> If 0 <sub>B</sub> this is the 2-byte read protocol: <start> <I <sup>2</sup> Cadr.> <reg.adr.> <data of reg.adr.> <data of reg.adr.+1> .... <stop> If 1 <sub>B</sub> this is the 1-byte read protocol: <start> <I <sup>2</sup> Cadr.> <data of reg.00 <sub>H</sub> > <data of reg.01 <sub>H</sub> > .... <stop> See <a href="#">Chapter 2.1.3</a>
CA	3	rw	<b>Collision avoidance</b> Clock stretching only in master-controlled and low-power mode, not in fast mode. The CA bit interacts with the <a href="#">INT</a> bit, see <a href="#">Table 5</a> and <a href="#">Chapter 2.2</a> .



Field	Bits	Type	Description
INT	2	rw	<b>Interrupt enabled</b> If 1 <sub>B</sub> /INT disabled If 0 <sub>B</sub> /INT enabled: After a completed measurement and ADC-conversion, an /INT pulse will be generated. For bus configurations /INT timing constraints between I <sup>2</sup> C data transfers and interrupt pulses must be monitored and aligned. The INT bit interacts with the CA bit, see <a href="#">Table 5</a> .
MODE	1:0	rw	<b>Power mode</b> If 00 <sub>B</sub> Low Power Mode: Cyclic measurements and ADC-conversions with a update rate, defined in the PRD registers. “No ADC trigger” must be used, see <a href="#">Table 6</a> and <a href="#">TRIG</a> . If 01 <sub>B</sub> Master Controlled Mode (Power Down mode): Measurement triggering depends on the PR bit and is possible with I <sup>2</sup> C sub address byte (see <a href="#">Table 6</a> ) or <a href="#">TRIG</a> bits. If 10 <sub>B</sub> is reserved and must not be used. If 11 <sub>B</sub> Fast Mode: The measurements and ADC-conversions are running continuously. It is recommended to set INT = 0 <sub>B</sub> and use a I <sup>2</sup> C clock speed ≥ 800 kHz.

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**Table 4 Device address overview**

The addresses are selected to ensure a minimum Hamming distance of 4 between them.

Address write	Address read	IICadr (bit-6)	IICadr (bit-5)	ID (bit-5)	ID (bit-4)
6A <sub>H</sub> <sup>1)</sup>	6B <sub>H</sub> <sup>1)</sup>	0 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>
44 <sub>H</sub>	45 <sub>H</sub>	0 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>	1 <sub>B</sub>
F0 <sub>H</sub>	F1 <sub>H</sub>	1 <sub>B</sub>	0 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>
88 <sub>H</sub>	89 <sub>H</sub>	1 <sub>B</sub>	1 <sub>B</sub>	1 <sub>B</sub>	1 <sub>B</sub>

1) Default address after start up or reset.

**Table 5 /INT (interrupt) and clock stretching**

In case the microcontroller tries to read sensor data the clock stretching pulls the SCL /INT line to low, as long as the measurement and ADC-conversion is not finished.

CA	INT	Configuration
0 <sub>B</sub>	0 <sub>B</sub>	/INT is enabled and will not be transmitted between <START> and <STOP>. /INT collision avoidance active.
0 <sub>B</sub>	1 <sub>B</sub>	/INT disabled. Clock stretching enabled. Suppress sensor read out during ongoing ADC conversion. This configuration must not be used with the “read” trigger-bits (7:5) = 010 <sub>B</sub> or 011 <sub>B</sub> (see <a href="#">Table 6</a> ) or with the trigger option <a href="#">TRIG</a> bit = 01 <sub>B</sub> .
1 <sub>B</sub>	0 <sub>B</sub>	/INT is enabled and will be transmitted between <START> and <STOP>. /INT may collide with I <sup>2</sup> C clock from microcontroller.
1 <sub>B</sub>	1 <sub>B</sub>	/INT disabled. Clock stretching disabled. Unsynchronized sensor readouts may collide with ADC conversion.

## TLE493D-A2B6

### I<sup>2</sup>C Registers

#### Low Power Mode update rate

Register name	Address	Reset Value
MOD2	13 <sub>H</sub>	(bits 7:5) 000 <sub>B</sub>

7	6					0
<b>PRD</b>			Reserved			

Field	Bits	Type	Description
PRD	7	rw	<b>Update rate settings</b> If 0 <sub>B</sub> $f_{Update}$ = fast. If 1 <sub>B</sub> $f_{Update}$ = slow.
Reserved	6:0		<b>Factory settings</b>

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### 1.2.5 Diagnostic, status and version registers

The device provides diagnostic and status information in register 06<sub>H</sub> and version information in register 16<sub>H</sub>.

#### Sensor diagnostic and status register

Register name	Address	Reset Value
Diag	06 <sub>H</sub>	60 <sub>H</sub>

7	6	5	4	3	2	1	0
<b>P</b>	<b>FF</b>	<b>CF</b>	<b>T</b>	<b>PD3</b>	<b>PDO</b>	<b>FRM</b>	

Field	Bits	Type	Description
P	7	r	<b>Bus parity</b> This bit adds up to an odd parity of the registers 00 <sub>H</sub> through 05 <sub>H</sub> (including 05 <sub>H</sub> ), described in <a href="#">Chapter 1.2.2</a> . The parity bit is generated during the I <sup>2</sup> C readout. The address byte, register byte and acknowledge bits are not included in the parity sum. If the parity calculated by the microcontroller after I <sup>2</sup> C reads is incorrect, these values must be treated as invalid.

Field	Bits	Type	Description
<b>FF</b>	6	r	<p><b>Fuse parity flag</b> Provides a flag from the internal fuse parity check of registers 11<sub>H</sub> and 13<sub>H</sub> (bit 7). This parity check includes the <b>FP</b> bit. If 1<sub>B</sub> parity is OK. If 0<sub>B</sub> the parity is not correct. The sensor must be considered defective and must no longer be used. A sensor with an invalid fuse parity disconnects its SDA. It will automatically go to low-power mode and only uses the /INT signal to communicate the error (collision avoidance is enabled).</p>
<b>CF</b>	5	r	<p><b>Configuration parity flag</b> Provides a flag from the internal configuration parity check of register 10<sub>H</sub>. This parity check includes the <b>CP</b> bit. After startup or after reset the <b>CP</b> bit is true. If 1<sub>B</sub> parity is OK. If 0<sub>B</sub> parity is not OK.</p>
<b>T</b>	4	r	<p><b>T bit</b> If 1<sub>B</sub> data in registers 00<sub>H</sub> till 05<sub>H</sub> are invalid measurement data. If 0<sub>B</sub> data in registers 00<sub>H</sub> till 05<sub>H</sub> are valid measurement data.</p>
<b>PD3</b>	3	r	<p><b>Power-down flag 3</b> If 1<sub>B</sub> ADC-conversion of Temp is completed and valid measurement data can be read out. Thus it must be 1<sub>B</sub> at readout. If 0<sub>B</sub> ADC-conversion of Temp is running and read measurement data are invalid. Any readout with PD3 bit = 0<sub>B</sub> should be considered invalid. At startup, this is 0<sub>B</sub> until one ADC conversion has been performed. The value then changes to 1<sub>B</sub>.</p>
<b>PD0</b>	2	r	<p><b>Power-down flag 0</b> If 1<sub>B</sub> the ADC conversion of Bx is completed and valid measurement data can be read out. Thus it must be 1<sub>B</sub> at readout. If 0<sub>B</sub> the ADC conversion of Bx is running and read measurement data are invalid. Any readout with PD0 bit = 0<sub>B</sub> should be considered invalid. At startup, this is 0<sub>B</sub> until one ADC conversion has been performed. The value then changes to 1<sub>B</sub>.</p>
<b>FRM</b>	1:0	r	<p><b>Frame counter</b> Increments at every updated ADC-conversion, once a X/Y/Z/T or X/Y/Z or X/Y conversion is completed and the new measurement data have been stored in the registers 00<sub>H</sub> till 05<sub>H</sub>. The microcontroller shall check if bits change in consecutive conversion runs.</p>

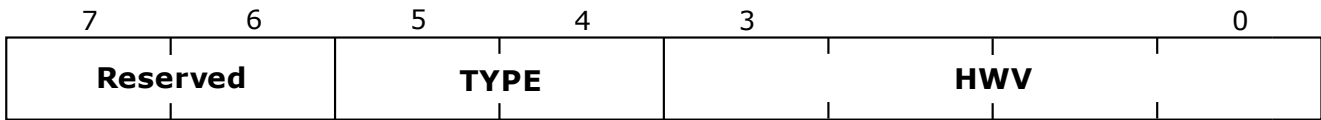
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## TLE493D-A2B6

### I<sup>2</sup>C Registers

#### Version register

Register name	Address	Reset Value
Ver	16 <sub>H</sub>	C9 <sub>H</sub> , D9 <sub>H</sub> or E9 <sub>H</sub>



Field	Bits	Type	Description
Reserved	7:6		Factory settings
TYPE	5:4	r	Chip feature If 11 <sub>B</sub> : device without Wake Up feature.
HWV	3:0	r	Hardware revision If 9 <sub>H</sub> it is the B21 design step.

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## 2 I<sup>2</sup>C Interface

The TLE493D-A2B6 uses Inter-Integrated Circuit (I<sup>2</sup>C) as the communication interface with the microcontroller.

**The I<sup>2</sup>C interface has three main functions:**

- Sensor configuration.
- Transmit measurement data.
- Interrupt handling.

**This sensor provides two I<sup>2</sup>C read protocols:**

- 16-bit read frame (μC is driving data), so called **2-byte read command**.
- 8-bit read frame (μC is driving data), so called **1-byte read command**.

### 2.1 I<sup>2</sup>C protocol description

The TLE493D-A2B6 provides one I<sup>2</sup>C write protocol, based on 2 bytes and two I<sup>2</sup>C read protocols. Default is the 2-byte read protocol. With the **PR** bit it can be selected, if the 1-byte read protocol or the 2-byte read protocol is used.

#### 2.1.1 General description

- The interface conforms to the I<sup>2</sup>C fast mode specification (400kBit/sec max.), but can be driven faster according to the data sheet.
- The TLE493D-A2B6 does not support “repeated starts”. Each addressing requires a start condition.
- The interface can be accessed in any power mode.
- The data transmission order is Most Significant Bit (MSB) first, Least Significant Bit (LSB) last.
- A I<sup>2</sup>C communication is always initiated with a start condition and concluded with a stop condition by the master (microcontroller). During a start or stop condition the SCL line must stay “high” and the SDA line must change its state: SDA line falling = start condition and SDA line rising = stop condition.
- Bit transfer occur when the SCL line is “high”.
- Each byte is followed by one ACK bit. The ACK bit is always generated by the recipient of each data byte.
  - If no error occurs during the data transfer, the ACK bit will be set to “low”.
  - If an error occurs during the data transfer, the ACK bit will be set to “high”.
  - If the communication is finished (before the Stop condition), the ACK bit must be set to “high”.

#### 2.1.2 I<sup>2</sup>C write command

Write I<sup>2</sup>C communication description:

- The purpose of the sensor address is to identify the sensor with which communication should occur. The sensor address byte is required independently of the number of sensors connected to the microcontroller.
- The register address identifies the register in the bitmap (according to **Figure 1**) with which the first data byte will be written.
- Data bytes are transmitted as long as the SCL line generates pulses. Each additional data byte increments the register address until the stop condition occurs.
- Bytes transmitted beyond the register address frame are ignored and the corresponding ACK bit is sent “high”, indicating an error.

I<sup>2</sup>C Interface

The I<sup>2</sup>C write communication frame consists of:

- The start condition.
- The sensor address, according to [Table 4](#).
- Write command bit = “low” (read = “high”).
- Acknowledge ACK.
- Trigger bits, according to [Table 6](#).
- The register address, according to [Figure 1](#).
- Acknowledge ACK.
- Writing of one or several bytes to the sensor, each byte followed by an acknowledge ACK.
- The stop condition.

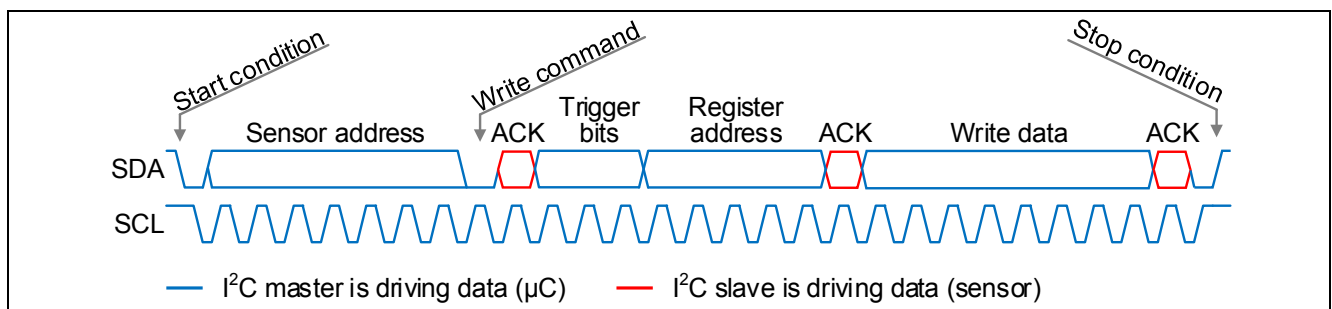


Figure 2 General I<sup>2</sup>C write frame format: Write data from microcontroller to sensor

Trigger bits in the I<sup>2</sup>C protocol

The trigger bits are used in Power Down Mode. The Power Down Mode is used in the Master Controlled Mode, when no measurement is running. Thus the trigger bits are relevant for the Master Controlled Mode as well.

For a more silent measurement environment it is recommended to separate the measurement and the communication as much as possible, by using the trigger bits = 001<sub>B</sub> or trigger bits = 100<sub>B</sub> and communicate between two measurements with reduced overlap of measurement and communication.

Table 6 I<sup>2</sup>C trigger bits

Read/Write command	Trigger-bit 7	Trigger-bit 6	Trigger-bit 5	Trigger command
0 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>	no ADC trigger
0 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>	1 <sub>B</sub>	ADC trigger after write frame is finished, <a href="#">Figure 4</a>
0 <sub>B</sub>	0 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>	no ADC trigger
0 <sub>B</sub>	0 <sub>B</sub>	1 <sub>B</sub>	1 <sub>B</sub>	ADC trigger after write frame is finished, <a href="#">Figure 4</a>
0 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>	no ADC trigger
0 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>	1 <sub>B</sub>	ADC trigger after write frame is finished, <a href="#">Figure 4</a>
0 <sub>B</sub>	1 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>	no ADC trigger
0 <sub>B</sub>	1 <sub>B</sub>	1 <sub>B</sub>	1 <sub>B</sub>	must not be used
1 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>	no ADC trigger
1 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>	1 <sub>B</sub>	no ADC trigger
1 <sub>B</sub>	0 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>	ADC trigger before first MSB, <a href="#">Figure 3</a>
1 <sub>B</sub>	0 <sub>B</sub>	1 <sub>B</sub>	1 <sub>B</sub>	ADC trigger before first MSB, <a href="#">Figure 3</a>

Table 6 I<sup>2</sup>C trigger bits (cont'd)

Read/Write command	Trigger-bit 7	Trigger-bit 6	Trigger-bit 5	Trigger command
1 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>	0 <sub>B</sub>	ADC trigger after register 05 <sub>H</sub> , <a href="#">Figure 5</a>
1 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>	1 <sub>B</sub>	ADC trigger after register 05 <sub>H</sub> , <a href="#">Figure 5</a>
1 <sub>B</sub>	1 <sub>B</sub>	1 <sub>B</sub>	0 <sub>B</sub>	ADC trigger after register 05 <sub>H</sub> , <a href="#">Figure 5</a>
1 <sub>B</sub>	1 <sub>B</sub>	1 <sub>B</sub>	1 <sub>B</sub>	must not be used

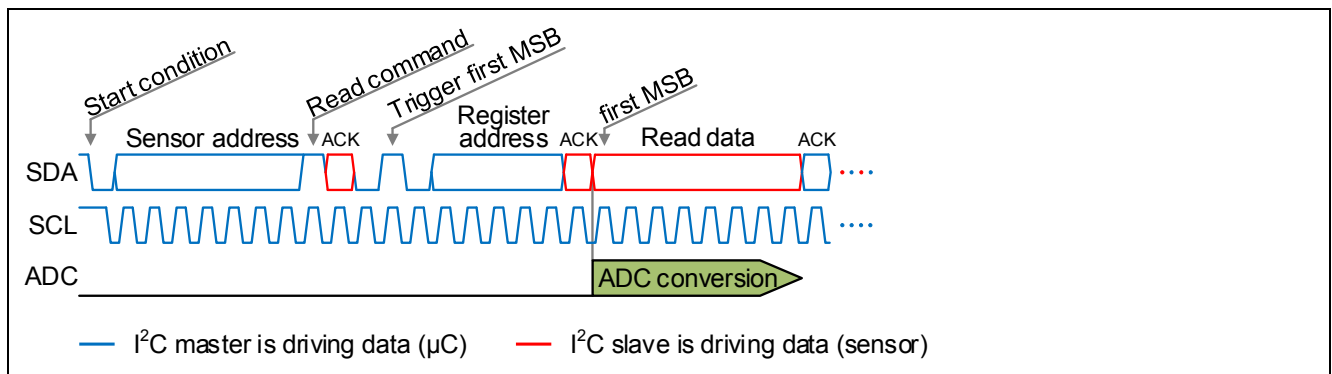


Figure 3 ADC trigger before sending first MSB of data registers, I<sup>2</sup>C trigger bits 010<sub>B</sub>.

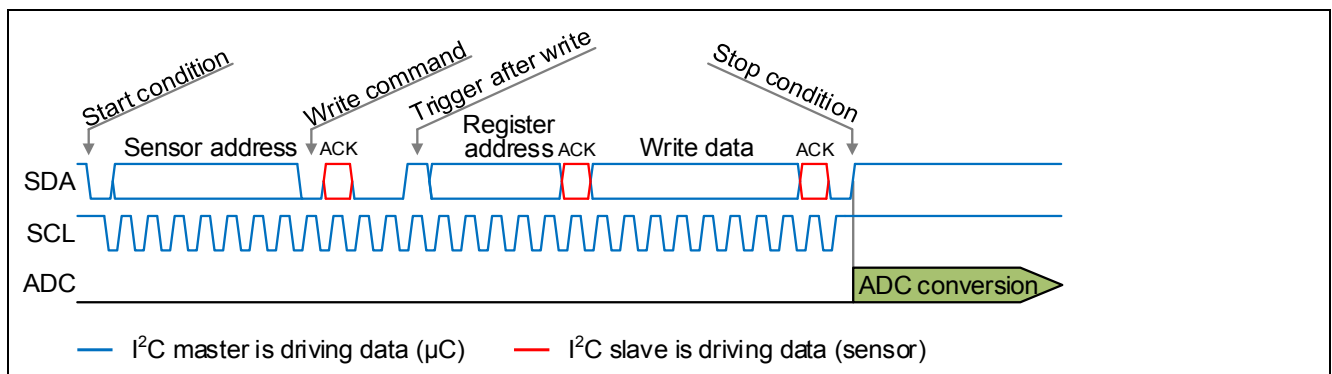


Figure 4 ADC trigger after write frame is finished, I<sup>2</sup>C trigger bits 001<sub>B</sub>.

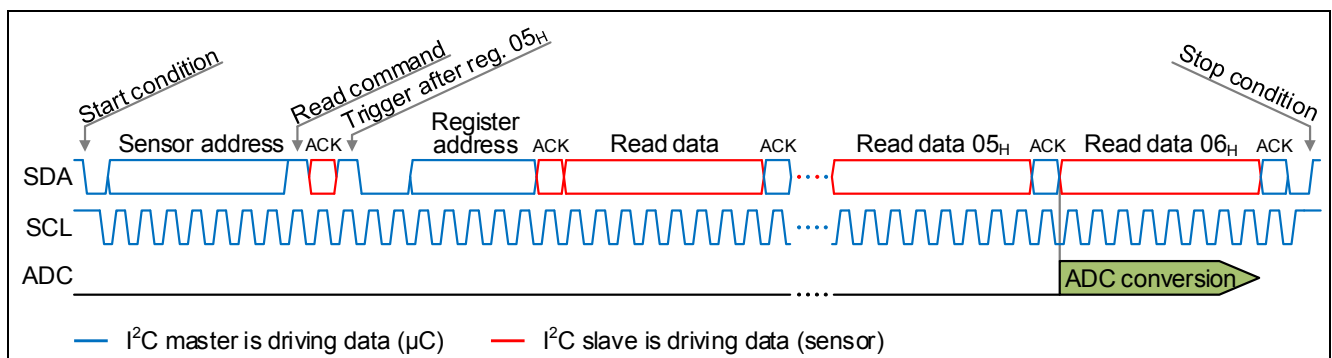


Figure 5 ADC trigger after register 05<sub>H</sub>, I<sup>2</sup>C trigger bits 100<sub>B</sub>.

**Example I<sup>2</sup>C write communication**

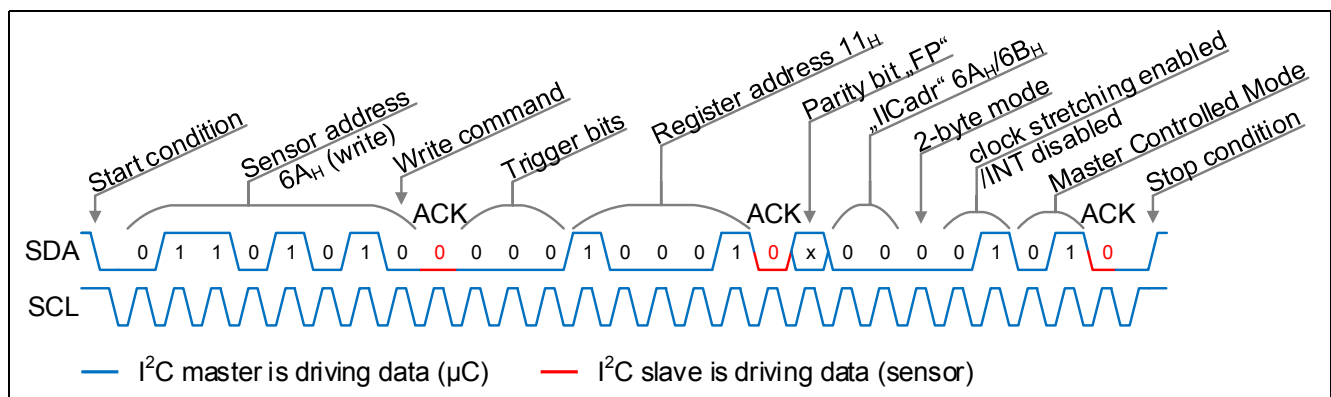
An example of a write communication is provided in [Figure 6](#).

In this example the sensor with the address 6A<sub>H</sub> / 6B<sub>H</sub> (see [Table 4](#)) should be configured for:

- Master Controlled Mode,
- /INT disabled,
- Clock stretching enabled,
- No trigger of a measurement.
- Other settings should be kept as is.

Implementation:

- The microcontroller generates a start condition.
- Configuration changes can only be performed with a write command. The address for write operation of this sensor is 6A<sub>H</sub> = 01101010<sub>B</sub>.
- If the sensor detects no error, the ACK = 0<sub>B</sub> is transmitted back to the microcontroller.
- No measurement is performed if the trigger bits = 000<sub>B</sub>.
- The register to change the required settings is 11<sub>H</sub> according the bitmap [Figure 1](#) = 10001<sub>B</sub>.
- If the sensor detects no error, the ACK = 0<sub>B</sub> is transmitted back to the microcontroller.
- The parity bit “FP” is the odd parity of the registers 11<sub>H</sub> and 13<sub>H</sub> (bits 7:5), see [FP](#) register, thus it is not possible to quantify it in this example.
- The sensor address should not be changed, i.e. the sensor address 6A<sub>H</sub> / 6B<sub>H</sub> should be kept. Thus the [IICadr](#) bits = 00<sub>B</sub>, see [IICadr](#) registers.
- The 2-byte protocol should be kept as is. Thus the [PR](#) bit = 0<sub>B</sub>.
- In order to enable clock stretching and disable /INT the [CA](#) bit must be set to 0<sub>B</sub> and the [INT](#) bit must be set to 1<sub>B</sub> (see [Table 5](#)).
- To use the Master Controlled Mode the [MODE](#) bits must be set to 01<sub>B</sub>.
- If the sensor detects no error the ACK = 0<sub>B</sub> is transmitted back to the microcontroller.
- The microcontroller generates the stop condition.



**Figure 6 Example I<sup>2</sup>C frame format 2-byte: Write data from microcontroller to sensor**



### 2.1.3 I<sup>2</sup>C read commands

Read I<sup>2</sup>C communication description:

- The purpose of the sensor address is to identify the sensor with which communication should occur. The sensor address byte is required independently of the number of sensors connected to the microcontroller.
- Only available in the 2-byte read command: The register address identifies the register in the bitmap (according [Figure 1](#)) from which the first data byte will be read.  
In the 1-byte read command the read out starts always at the register address 00<sub>H</sub>.
- As many data bytes will be transferred as long as pulses are generated by the SCL line. Each additional data byte increments the register address. Until the stop condition occurs.
- If bytes are read beyond the register address frame the sensor keeps the SDA = 1<sub>B</sub>.
- If the microcontroller reads data and does not acknowledge the sensor data (ACK = 1<sub>B</sub>) the sensor keeps the SDA = 1<sub>B</sub> until the next stop condition.

#### 2.1.3.1 2-byte read command

The I<sup>2</sup>C read communication frame consists of:

- The start condition.
- The sensor address, according to [Table 4](#).
- Read command bit = “high” (write = “low”).
- Acknowledge ACK.
- Trigger bits, according to [Table 6](#).
- The register address, according to [Figure 1](#).
- Acknowledge ACK.
- Reading of one or several bytes from the sensor, each byte followed by an acknowledge ACK.
- The stop condition.

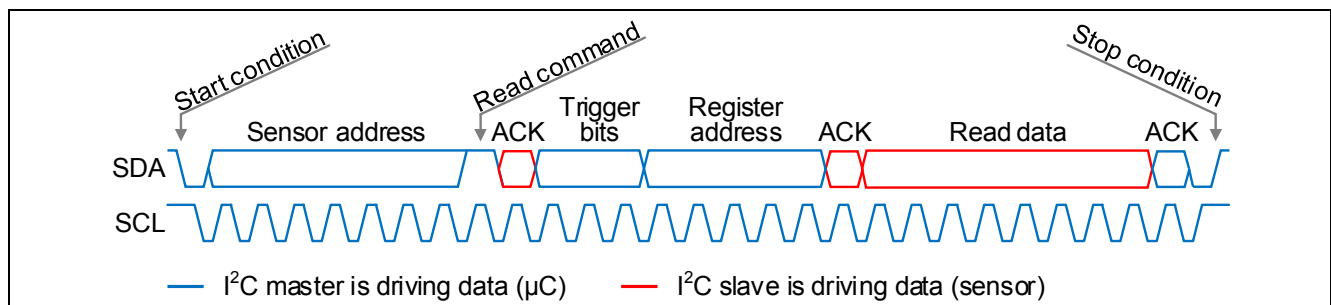


Figure 7 General I<sup>2</sup>C frame format 2-byte: Read data from sensor to microcontroller

#### 2.1.3.2 1-byte read command

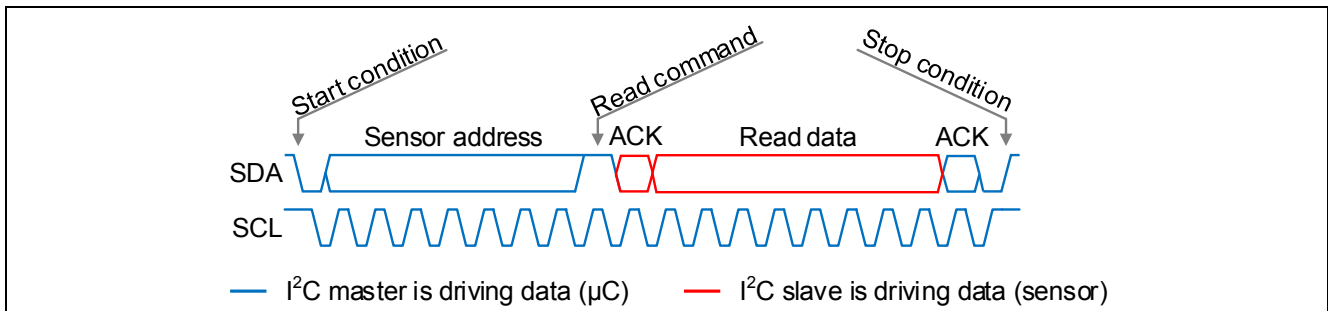
The 1-byte read mode can be entered, by configuring the [PR](#) bit with an write communication. E.g. with the write cycle:

- start condition
- 6A<sub>H</sub> (sensor address)
- 11<sub>H</sub> (register address)
- XXX1 XXXX<sub>B</sub> ([PR](#) bit = 1<sub>B</sub>)
- stop condition

**I<sup>2</sup>C Interface**

The I<sup>2</sup>C communication frame consists of:

- The start condition.
- The sensor address, according to [Table 4](#).
- Read command bit = “high” (write = “low”).
- Acknowledge ACK.
- Reading of one or several bytes from the sensor, each byte followed by an acknowledge ACK.
- The stop condition.



**Figure 8** General I<sup>2</sup>C frame format 1-byte: Read data from sensor to microcontroller

**Example I<sup>2</sup>C 1-byte read communication**

An example of a read communication is provided in [Figure 9](#).

In this example, the sensor with the address  $6A_H / 6B_H$  (see [Table 4](#)) should read out the measurement values, registers  $00_H - 05_H$  and the diagnostic register  $06_H$ :

Implementation:

- The microcontroller generates a start condition.
- The address for read operation of this sensor is  $6B_H = 01101011_B$ . This address value must be transmitted by the microcontroller to the sensor.
- If the sensor detects no error, the  $ACK = 0_B$  is transmitted back to the microcontroller.
- The microcontroller must go on clocking the SCL line.
- The sensor transmits 8 data bits of register  $00_H$  to the microcontroller.
- If the microcontroller detects no error the  $ACK = 0_B$  is transmitted back to the sensor.
- The microcontroller must go on clocking the SCL line.
- The sensor transmits 8 data bits of register  $01_H$  to the microcontroller.
- ...
- After transmitting the register  $06_H$  the microcontroller transmits a NACK.
- The microcontroller generates the stop condition.

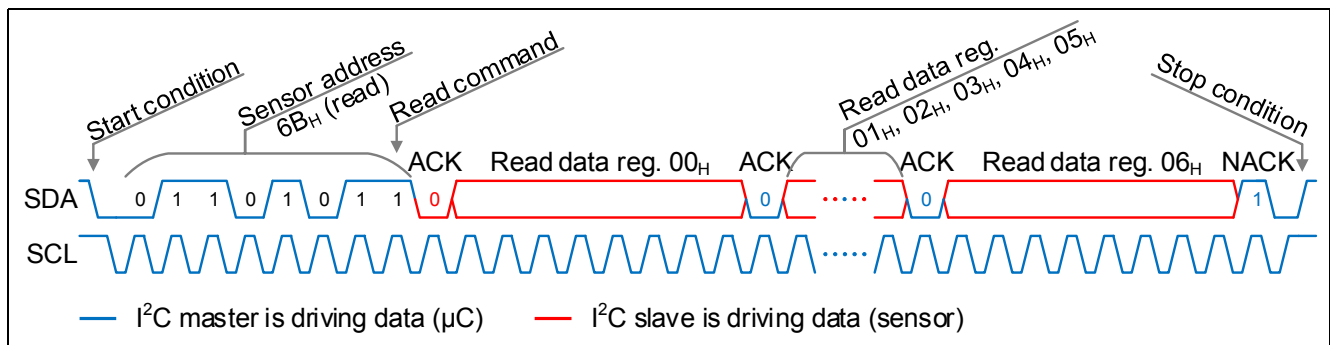


Figure 9 Example I<sup>2</sup>C frame format 1-byte: Read data from sensor to microcontroller

## 2.2 Collision avoidance and clock stretching

Using the configuration bits **CA** and **INT**, collision avoidance and clock stretching can be configured. An overview is given in **Table 5**. An example without collision avoidance and clock stretching is shown in **Figure 10**. In this example:

- the sensor interrupt disturbs the I<sup>2</sup>C clock, causing an additional SCL pulse which shifts the data read out by one bit.
- the data read out starts when the ADC conversion is running.

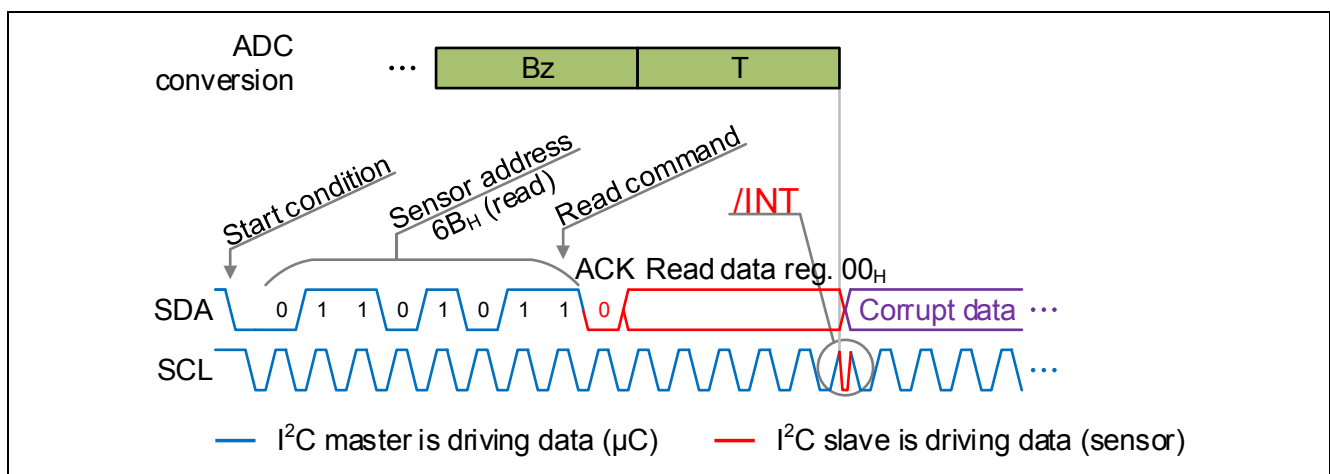


Figure 10 Example without collision avoidance **CA** bit = 1<sub>B</sub> and **INT** bit = 0<sub>B</sub>

### 2.2.1 Collision avoidance (**CA** bit = 0<sub>B</sub> and **INT** bit = 0<sub>B</sub>)

In a bus configuration combined with an activated interrupt signal /INT it must be assured, that during any communication no interrupt /INT occurs. With collision avoidance enabled, the sensor monitors for any start/stop condition, even if it does not detect a valid bus address. The interrupt signal /INT is omitted whenever a start condition is detected, as shown in **Figure 11**, in contrast to **Figure 10**. Only after a stop condition is detected, the interrupt signal /INT is generated by the sensor.

It is strongly recommended to use the collision avoidance feature whenever the interrupt signal /INT is used.

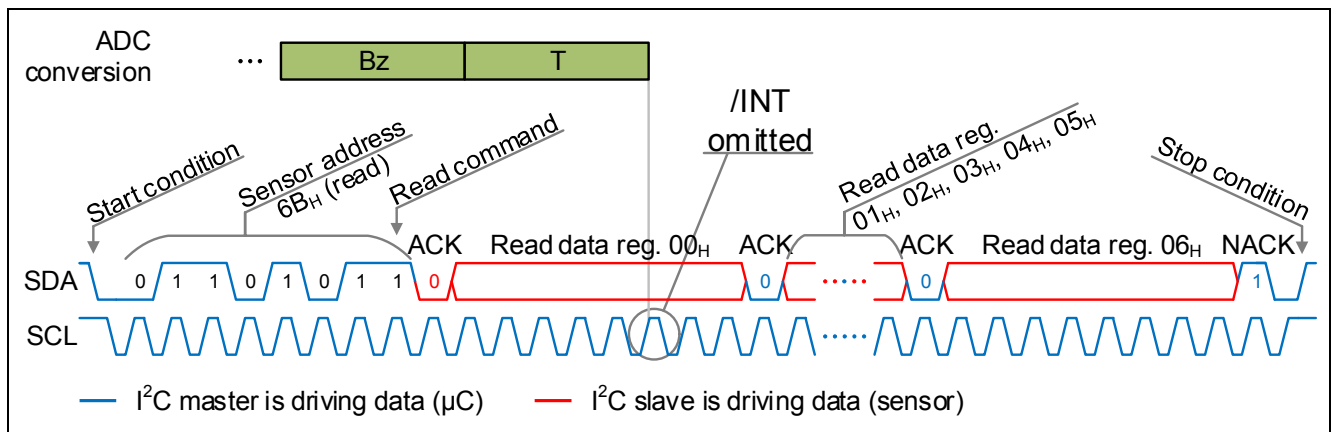


Figure 11 Example with collision avoidance CA bit = 0<sub>B</sub> and INT bit = 0<sub>B</sub>

### 2.2.2 Clock stretching (CA bit = 0<sub>B</sub> and INT bit = 1<sub>B</sub>)

With the clock stretching feature, the data read out starts after the ADC conversion is finished. Thus it can be avoided that during an ADC conversion old or corrupted measurement results are read out, which may occur when the ADC is writing to a register while this is being read out by the microcontroller. The clock stretching feature is shown in Figure 12 in combination with a 1-byte read command. Clock stretching can also be used with a 2-byte read command.

The sensor pulls the SCL line to low during the following situation:

- An ADC conversion is in progress.
- The sensor is addressed for register read (writes are never affected by clock stretching).
- The sensor is about to transmit the valid ACK in response to the I<sup>2</sup>C addressing of the microcontroller.

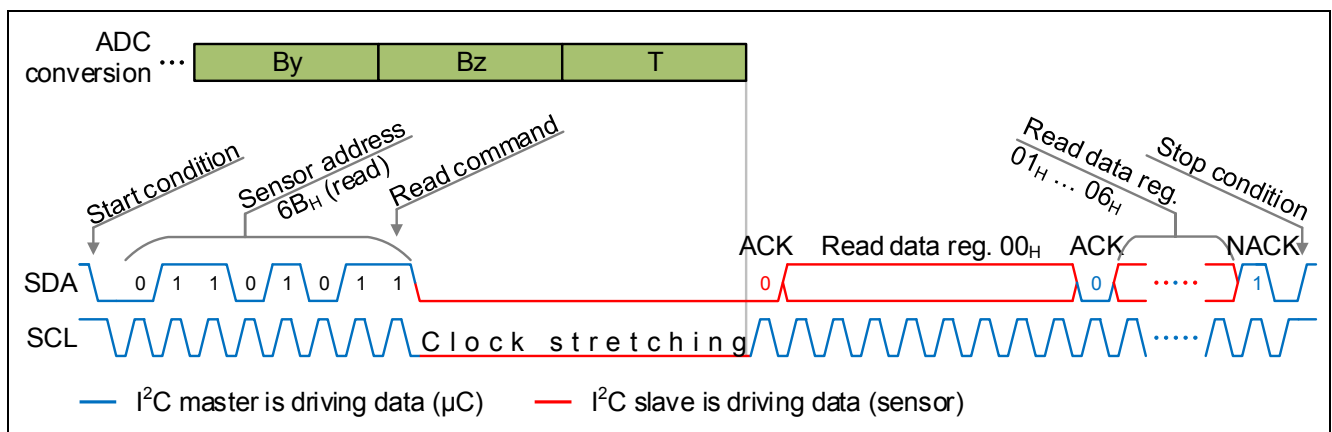


Figure 12 Example with clock stretching CA bit = 0<sub>B</sub> and INT bit = 1<sub>B</sub>

### 2.3 Sensor reset by I<sup>2</sup>C

If the microcontroller is reset, the communication with the sensor may be corrupted, possibly causing the sensor to enter an incorrect state. The sensor can be reset via the I<sup>2</sup>C interface by sending the following command sequence from the microcontroller to the sensor:

- Start condition,
- sending FF<sub>H</sub>,
- stop condition.
- Start condition,
- sending FF<sub>H</sub>,
- stop condition.
- Start condition,
- sending 00<sub>H</sub>,
- stop condition.
- Start condition,
- sending 00<sub>H</sub>,
- stop condition.
- 30μs delay.

After a reset, the sensor must be reconfigured to the desired settings. The reset sequence uses twice the identical data to assure a proper reset, even when an unexpected /INT pulse occurs.

Spikes can be interpreted as bus signals causing an action. E.g. when the collision avoidance feature is active and if the SDA line spikes together with SCL line this could be interpreted as start condition, blocking further /INT pulses until a stop condition appears on the bus. In such a case the sensor must be reset in order to initialize it. If the sensor does not respond after the reset, it must be considered defective.

Such spikes may occur as the sensor powers up. Because of this we recommend to using the reset sequence after each power up before configuring the sensor.

If the microcontroller resets during an ongoing I<sup>2</sup>C communication, the SDA line could get stuck low. This would block the I<sup>2</sup>C bus and is a well-known limitation of the I<sup>2</sup>C interface. To recover from this situation please use the reset sequence described in this chapter.

## 2.4 Sensor Initialization and Readout example

To ensure that both the microcontroller and the sensor are synchronized and properly initialized, it is recommended to apply the I<sup>2</sup>C reset and upload the fuse register settings each time the microcontroller is reset, see [Figure 13](#).

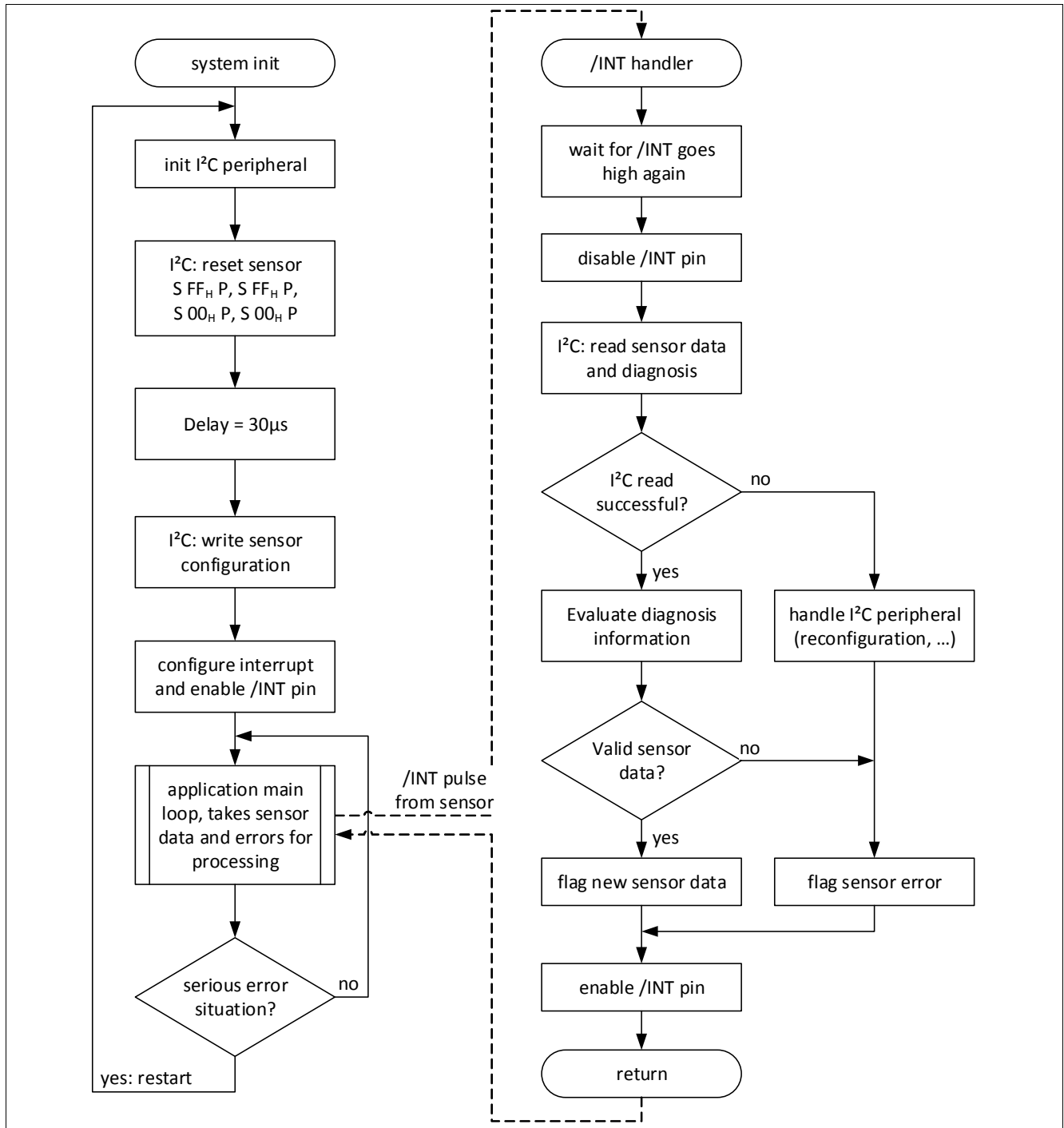


Figure 13 Microcontroller software flowchart for TLE493D-A2B6

## 2.5 Loss of V<sub>DD</sub> impact on I<sup>2</sup>C bus

If the SDA or SCL line is pulled “low” and the sensor is disconnected from the V<sub>DD</sub> supply line, the affected I<sup>2</sup>C line will most likely get a stuck in the Low state and will interfere with the communication on the bus.

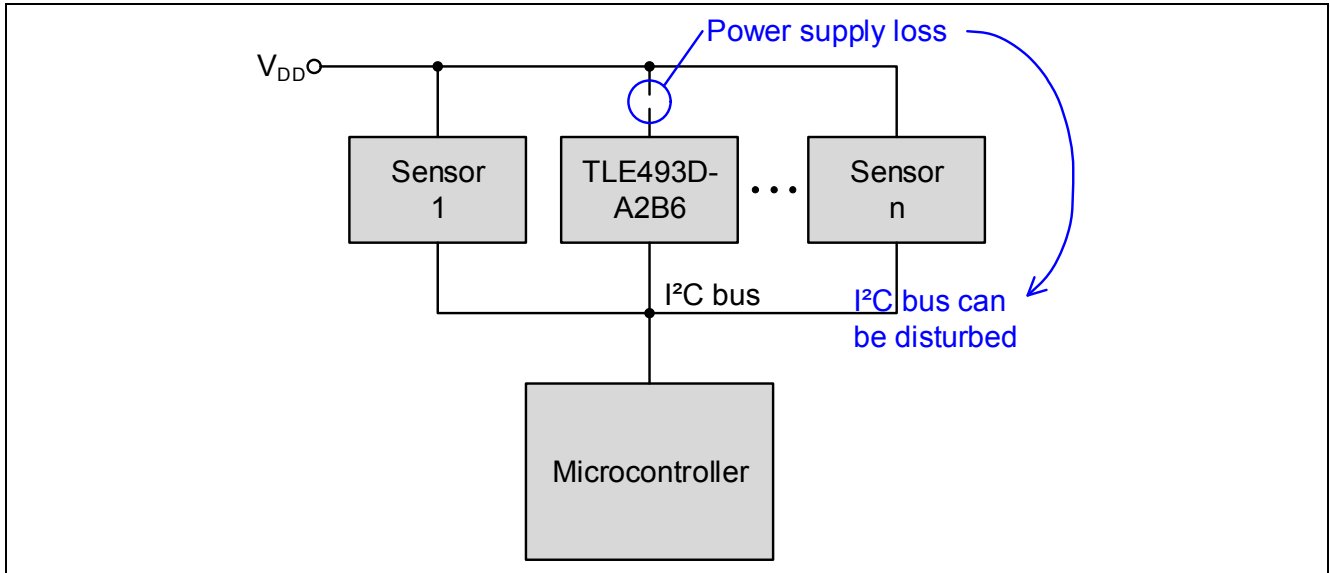


Figure 14 Example of I<sup>2</sup>C bus and a TLE493D-A2B6 with disconnected V<sub>DD</sub>

When V<sub>DD</sub> is pulled to GND the SDA and SCL line will not disturb the bus.

### 3 Diagnostic

The sensor TLE493D-A2B6 provides diagnostic functions. These functions are running in the background, providing results, which can be checked by the microcontroller for the verification of the measurement results.

To ensure the integrity of received data the following diagnostic functions are available.

#### 3.1 Parity bits and parity flags

##### Parity bits:

- **FP** (mode parity bit)
- **CP** (configuration parity bit)
- **P** (bus parity bit)

##### Parity flags:

- **FF** (mode parity flag)
- **CF** (configuration parity flag)

#### 3.2 Power-down flags

During measurements and during ADC conversion, the sensor monitors if the supply voltage is correct and if the conversion is finished. This is indicated by the **PD3** and **PD0** registers.

#### 3.3 Frame Counter

The frame counter **FRM** registers are incremented by one when a conversion is completed.



## 4 Terminology

### A

ACK	Acknowledge
ADC	Analog/Digital Converter
adr	address

### E

EMC	Electromagnetic Compatibility
-----	-------------------------------

### G

GND	Ground
-----	--------

### I

ID	IDentification
I <sup>2</sup> C (I2C)	Inter-Integrated Circuit
/INT	Interrupt pin, Interrupt signal

### L

LSB	Least Significant Bit
-----	-----------------------

### M

Magnetic field	Magnetic flux density that the sensor measures.
min	minimum
MSB	Most Significant Bit
max	maximum

### P

PCB	Printed Circuit Board
-----	-----------------------

### R

reg	register
-----	----------

### S

SCL	Clock pin
SDA	Data pin
Sensor	Refers to the TLE493D-A2B6 product
Sensor module	Refers to the TLE493D-A2B6 product and all the passive elements in the customer's module
Supply	Refers to the sensor supply pins V <sub>DD</sub> and GND (the unused pins are assumed to be connected to GND as well).

### V

V <sub>DD</sub>	Supply voltage
-----------------	----------------

### μ

μC	Microcontroller
----	-----------------

## 5 Revision history

Revision	Date	Changes
Ver. 1.11	2019-05-28	Register <b>MODE</b> updated.
Ver. 1.1	2018-09-20	<b>TRIG</b> updated. <b>MOD2</b> updated. <b>Table 5</b> updated. <b>Trigger bits in the I<sup>2</sup>C protocol</b> updated. <b>Table 6</b> updated and <b>Figure 4</b> accordingly. <b>Figure 5</b> updated. At the end of a data read out a NACK is transferred before the stop condition (according to the standard and the product). This was updated: <b>Chapter 2.1.1</b> , <b>Figure 9</b> , <b>Figure 11</b> , <b>Figure 12</b> Editorial changes.
Ver. 0.1	2018-04-20	Initial release.

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