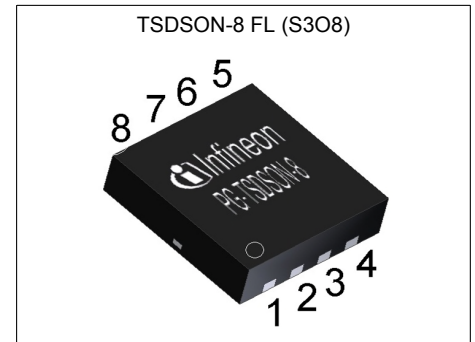


# MOSFET

## OptiMOS™ 5 Power-MOSFET, 30 V

### Features

- Optimized for high performance Wireless charger
- Very low  $FOM_{QOSS}$  for high frequency SMPS
- Low  $FOM_{SW}$  for high frequency SMPS
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Very low on-resistance  $R_{DS(on)}$  @  $V_{GS}=4.5$  V
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



RoHS

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	30	V
$R_{DS(on),max}$	4.4	m $\Omega$
$I_D$	17	A
$Q_{OSS}$	7.2	nC
$Q_G(0V..4.5V)$	5.2	nC

Type / Ordering Code	Package	Marking	Related Links
BSZ0589NS	PG-TSDSON-8 FL	0589NS	-

<sup>1)</sup> J-STD20 and JESD22

## Table of Contents

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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	17 10	A	$V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_A=100\text{ °C}$
Pulsed drain current <sup>1)</sup>	$I_{D,pulse}$	-	-	68	A	$T_A=25\text{ °C}$
Avalanche current, single pulse <sup>2)</sup>	$I_{AS}$	-	-	20	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	20	mJ	$I_D=20\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	2.1	-	W	$T_A=25\text{ °C}$ , $R_{thJA}=60\text{ K/W}$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	4.6	K/W	-
Device on PCB, 6 cm <sup>2</sup> cooling area <sup>3)</sup>	$R_{thJA}$	-	-	60	K/W	-

## 3 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2	V	$V_{DS}=V_{GS}$ , $I_D=250\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=24\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=24\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	4.4 3.5	5.3 4.4	m $\Omega$	$V_{GS}=4.5\text{ V}$ , $I_D=8\text{ A}$ $V_{GS}=10\text{ V}$ , $I_D=8\text{ A}$
Gate resistance <sup>4)</sup>	$R_G$	-	1	1.7	$\Omega$	-
Transconductance	$g_{fs}$	28	56	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$ , $I_D=10\text{ A}$

<sup>1)</sup> See Diagram 3 for more detailed information

<sup>2)</sup> See Diagram 13 for more detailed information

<sup>3)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

<sup>4)</sup> Defined by design. Not subject to production test.

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance <sup>1)</sup>	$C_{iss}$	-	700	950	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=15\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>1)</sup>	$C_{oss}$	-	220	300	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=15\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	16	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=15\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	2.3	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=8\text{ A}$ , $R_{G,ext}=1.6\ \Omega$
Rise time	$t_r$	-	2.4	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=8\text{ A}$ , $R_{G,ext}=1.6\ \Omega$
Turn-off delay time	$t_{d(off)}$	-	13	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=8\text{ A}$ , $R_{G,ext}=1.6\ \Omega$
Fall time	$t_f$	-	2.0	-	ns	$V_{DD}=15\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=8\text{ A}$ , $R_{G,ext}=1.6\ \Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	1.7	-	nC	$V_{DD}=15\text{ V}$ , $I_D=8\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	1.1	-	nC	$V_{DD}=15\text{ V}$ , $I_D=8\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge	$Q_{gd}$	-	1.3	-	nC	$V_{DD}=15\text{ V}$ , $I_D=8\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	$Q_{sw}$	-	1.9	-	nC	$V_{DD}=15\text{ V}$ , $I_D=8\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total	$Q_g$	-	5.2	-	nC	$V_{DD}=15\text{ V}$ , $I_D=8\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	2.4	-	V	$V_{DD}=15\text{ V}$ , $I_D=8\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	11	15	nC	$V_{DD}=15\text{ V}$ , $I_D=8\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	4.8	-	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Output charge	$Q_{oss}$	-	7.2	-	nC	$V_{DD}=15\text{ V}$ , $V_{GS}=0\text{ V}$

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	2.1	A	$T_A=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	68	A	$T_A=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.71	1.1	V	$V_{GS}=0\text{ V}$ , $I_F=2.1\text{ A}$ , $T_J=25\text{ °C}$
Reverse recovery charge	$Q_{rr}$	-	10	-	nC	$V_R=15\text{ V}$ , $I_F=30\text{ A}$ , $di_F/dt=400\text{ A}/\mu\text{s}$

<sup>1)</sup> Defined by design. Not subject to production test.

<sup>2)</sup> See "Gate charge waveforms" for parameter definition

### 4 Electrical characteristics diagrams

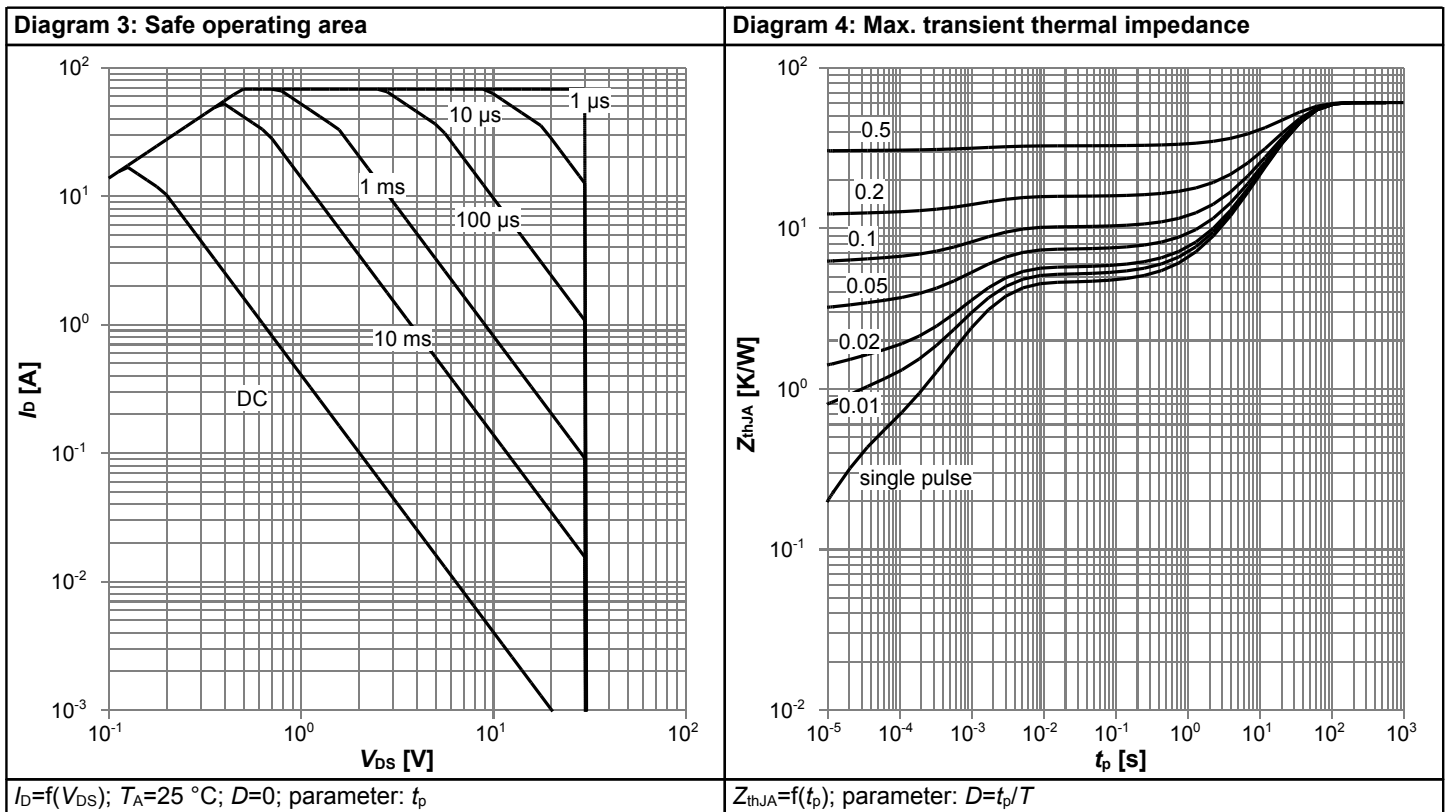
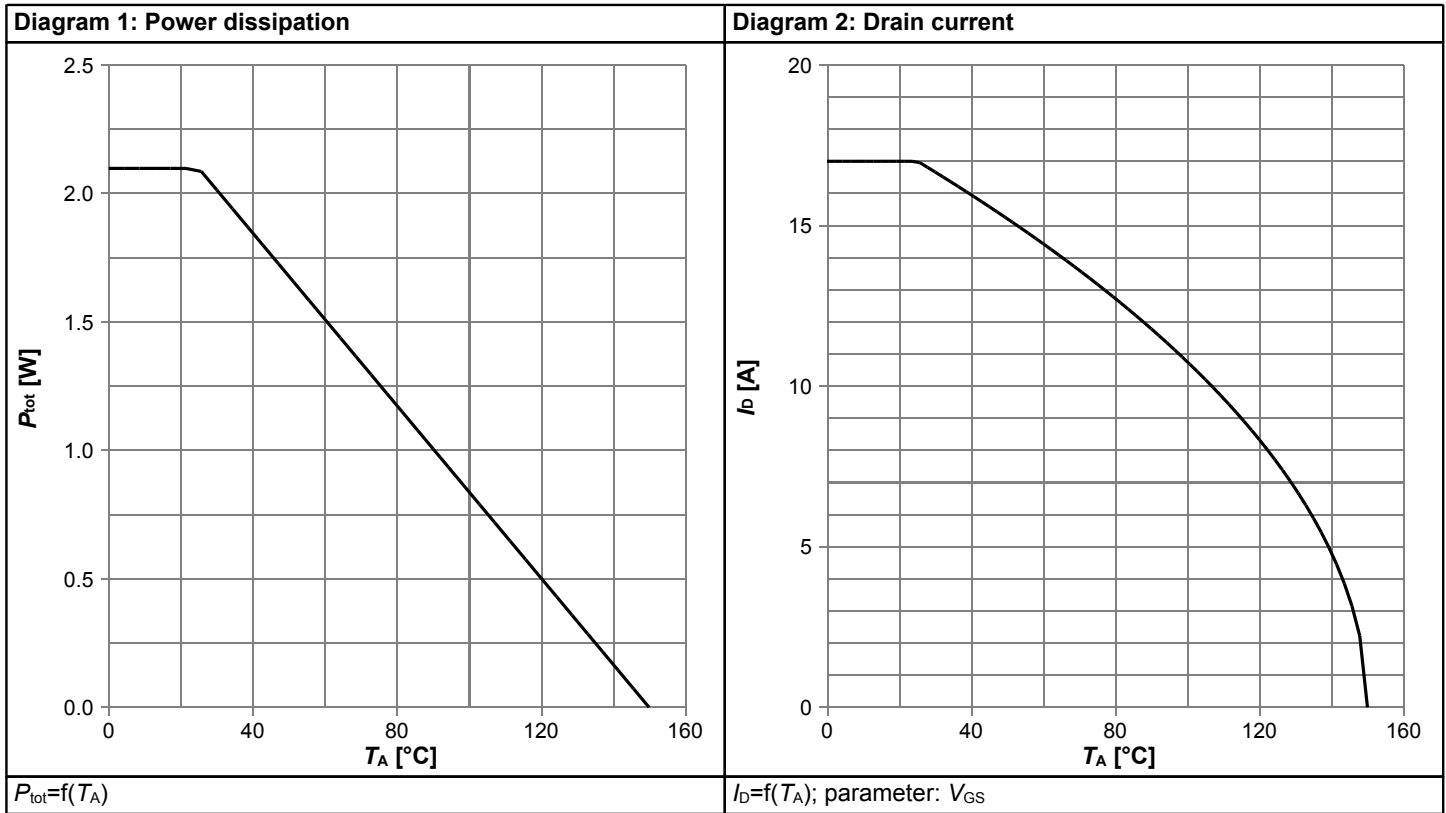
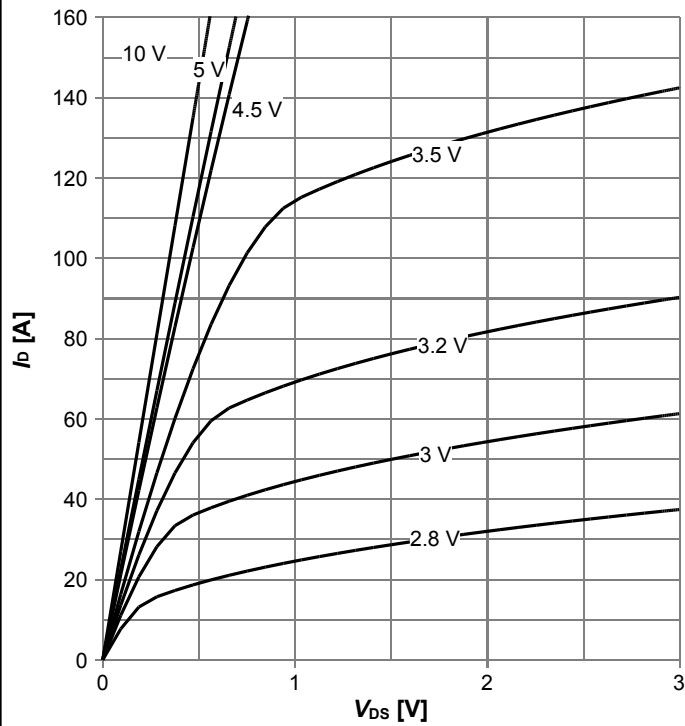
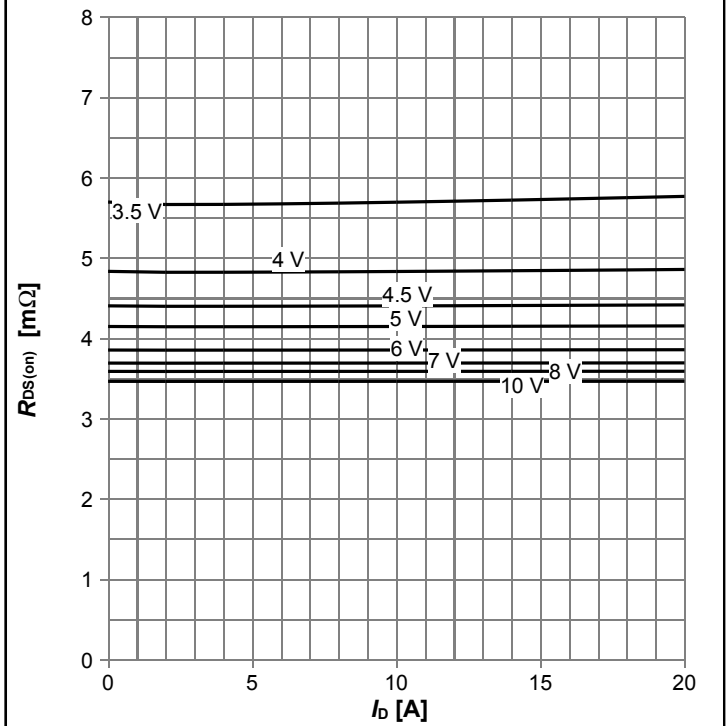


Diagram 5: Typ. output characteristics



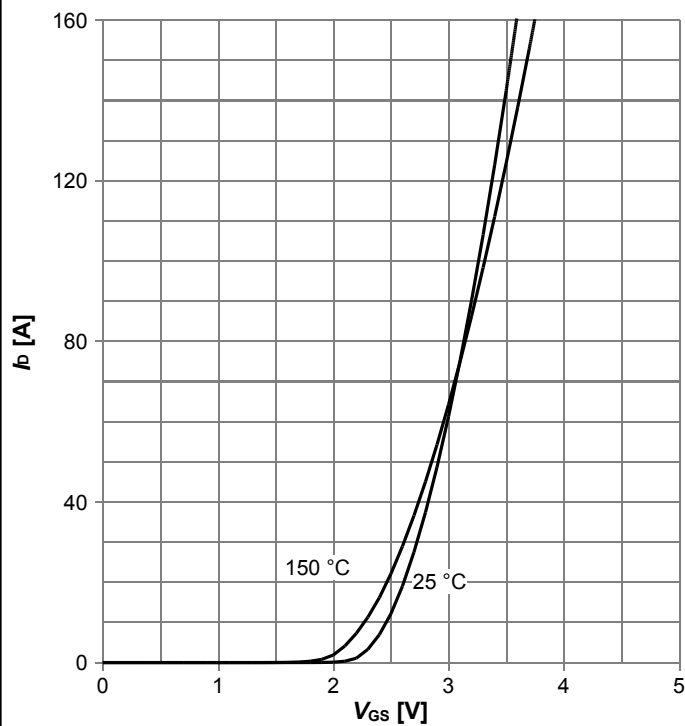
$I_D = f(V_{DS}); T_j = 25\text{ °C};$  parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



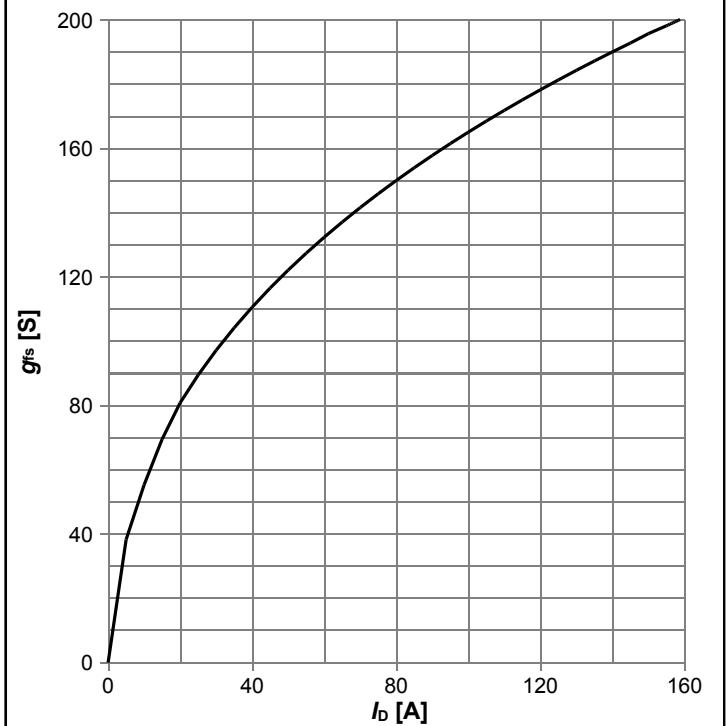
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C};$  parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



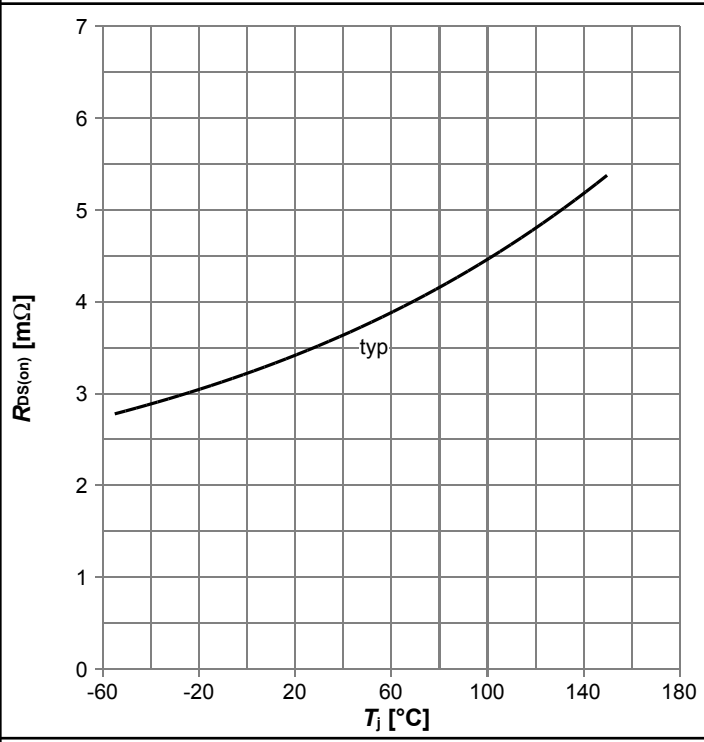
$I_D = f(V_{GS}); |V_{DS}| > 2 \cdot I_D \cdot R_{DS(on)max};$  parameter:  $T_j$

Diagram 8: Typ. forward transconductance



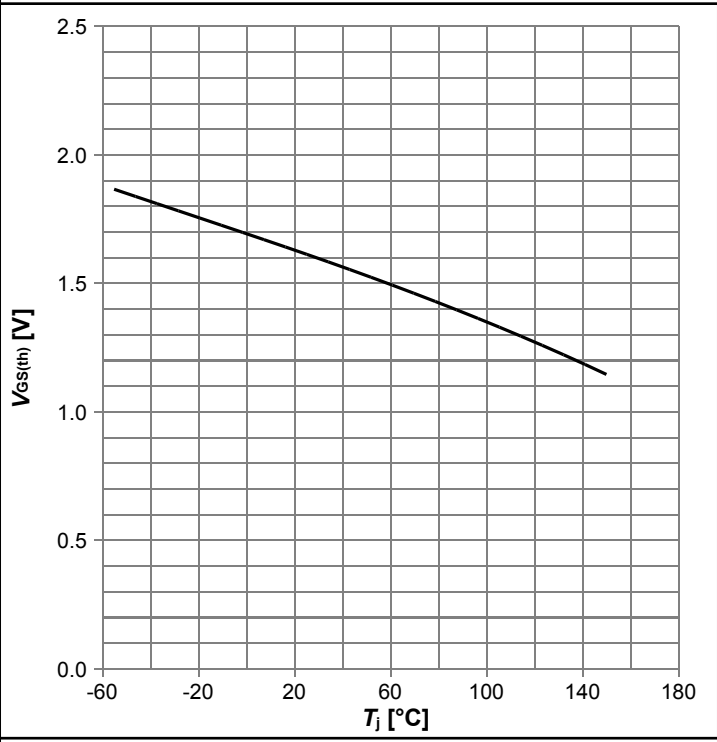
$g_{fs} = f(I_D); T_j = 25\text{ °C}$

Diagram 9: Drain-source on-state resistance



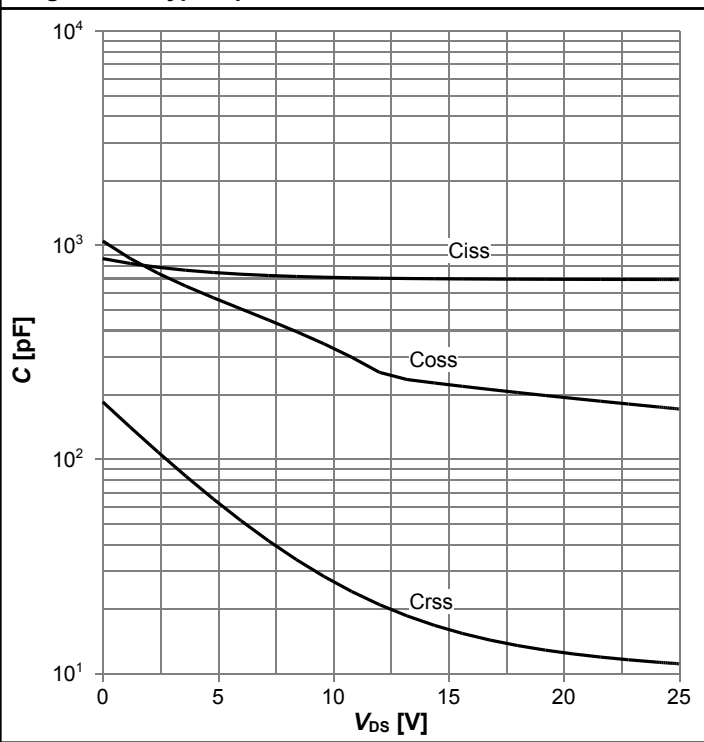
$R_{DS(on)}=f(T_j)$ ;  $I_D=8$  A;  $V_{GS}=10$  V

Diagram 10: Typ. gate threshold voltage



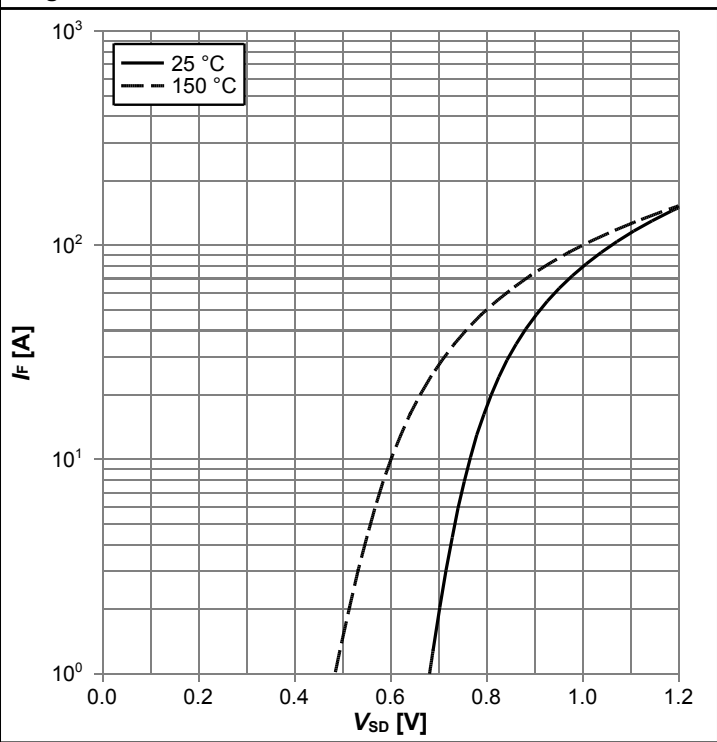
$V_{GS(th)}=f(T_j)$ ;  $V_{GS}=V_{DS}$ ;  $I_D=250$  μA

Diagram 11: Typ. capacitances



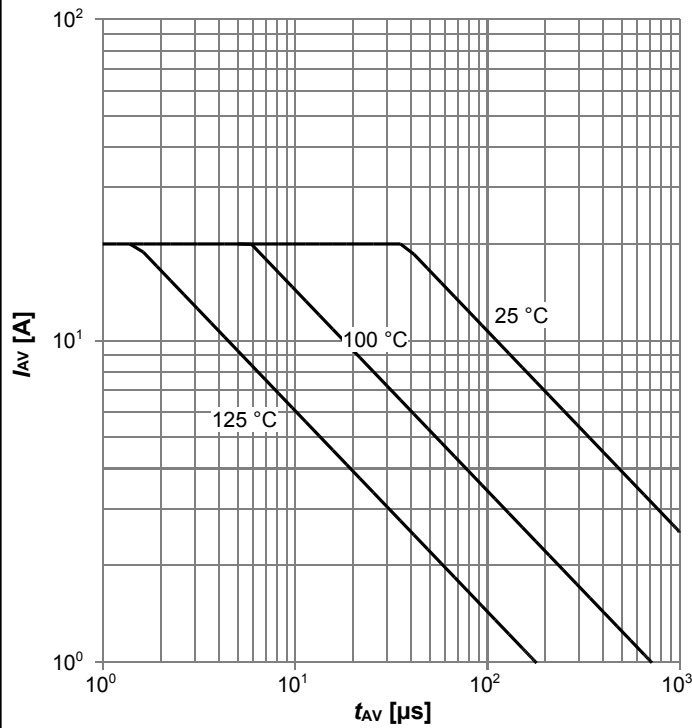
$C=f(V_{DS})$ ;  $V_{GS}=0$  V;  $f=1$  MHz

Diagram 12: Forward characteristics of reverse diode



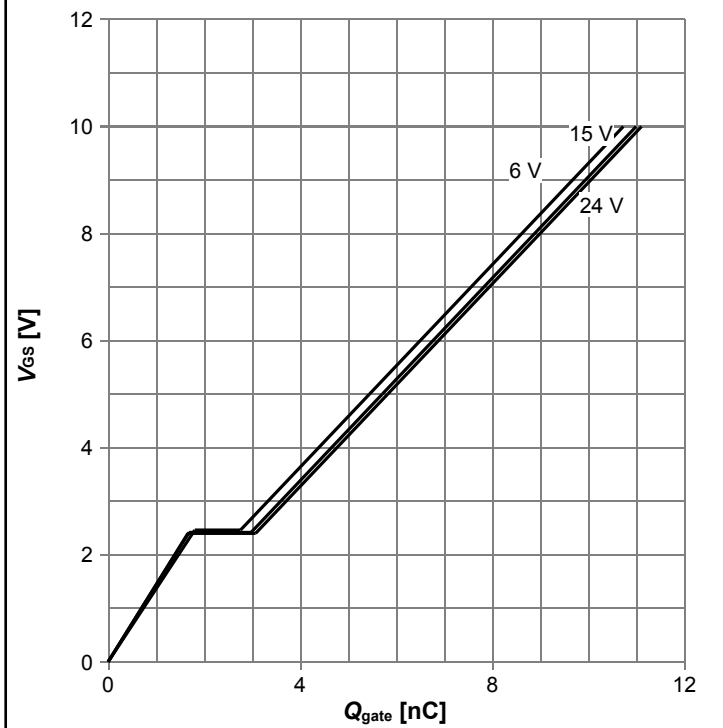
$I_F=f(V_{SD})$ ; parameter:  $T_j$

Diagram 13: Avalanche characteristics



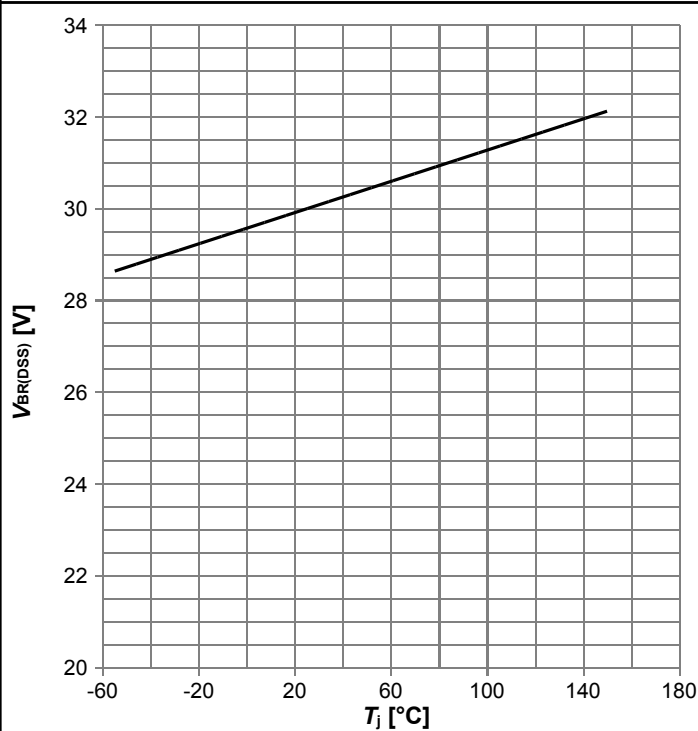
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j(start)}$

Diagram 14: Typ. gate charge



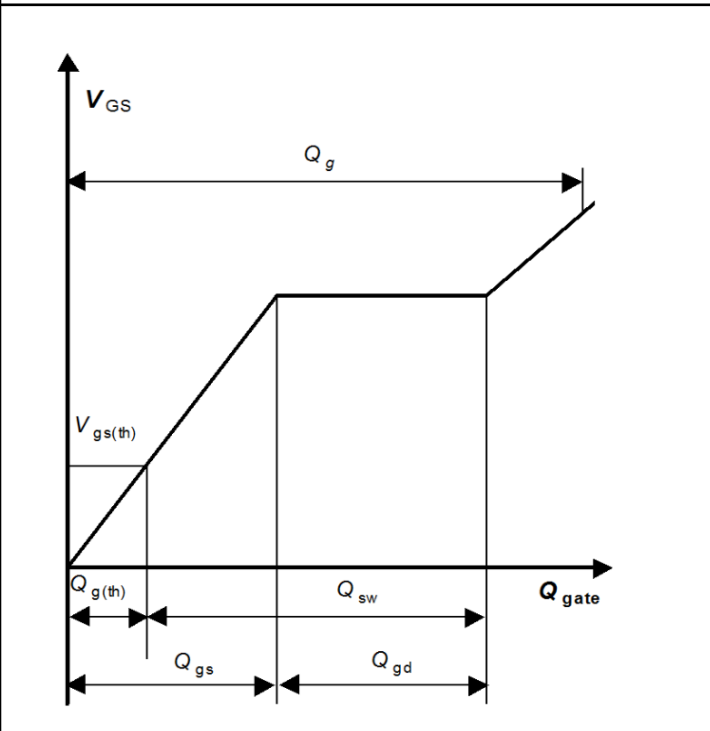
$V_{GS}=f(Q_{gate}); I_D=8$  A pulsed; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage



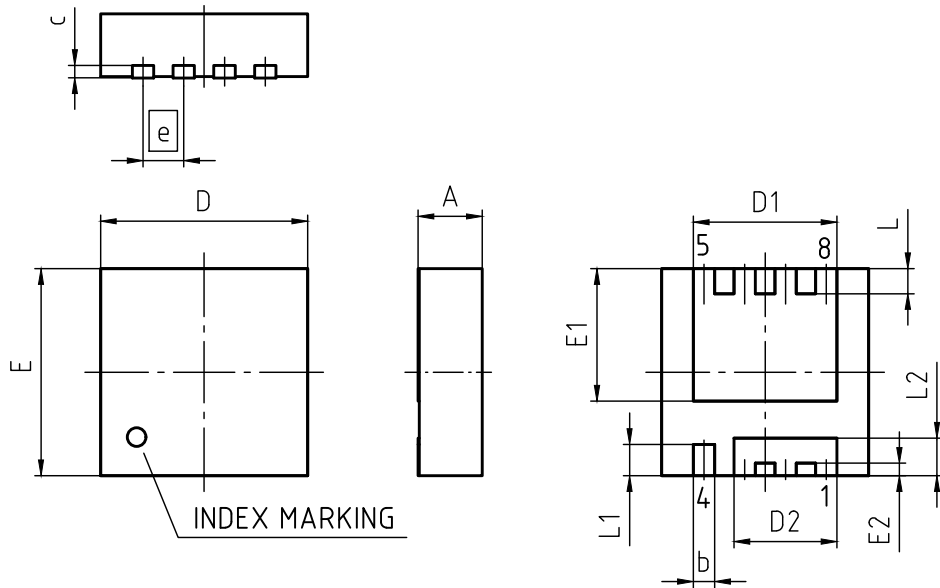
$V_{BR(DSS)}=f(T_j); I_D=1$  mA

Diagram Gate charge waveforms





## 5 Package Outlines



PACKAGE - GROUP NUMBER: <b>PG-TSDSON-8-U03</b>		
REVISION: 03	DATE: 20.10.2020	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
<b>A</b>	0.90	1.10
<b>b</b>	0.24	0.44
<b>c</b>	(0.20)	
<b>D</b>	3.20	3.40
<b>D1</b>	2.19	2.39
<b>D2</b>	1.54	1.74
<b>E</b>	3.20	3.40
<b>E1</b>	2.01	2.21
<b>E2</b>	0.10	0.30
<b>e</b>	0.65	
<b>L</b>	0.30	0.50
<b>L1</b>	0.40	0.60
<b>L2</b>	0.50	0.70
<b>aaa</b>	0.06	

Figure 1 Outline PG-TSDSON-8 FL, dimensions in mm

## Revision History

BSZ0589NS

**Revision: 2020-11-16, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-07-11	Release of final version
2.1	2020-11-16	Update package drawing

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