

TLE 4206-4G

H-Bridge Driver  
Headlight Beam Controller

Data Sheet

Rev. 1.0, 2010-08-05

Automotive Power

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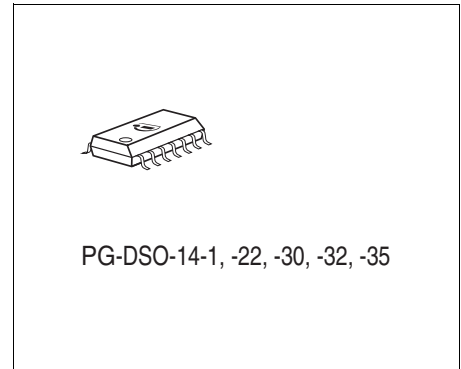
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## 1 Overview

### Features

- Ideal for manual and automatic-static headlight beam control applications with DC motor loads
- Delivers up to 0.8 A continuous
- Range low-voltage detection with hysteresis; Lower switch-off threshold @ 1.34V typ
- Low saturation voltage; typ. 1.2 V total @ 25 °C; 0.4 A
- Output protected against short circuit
- Over temperature protection with hysteresis
- Over- and under voltage lockout
- Internal clamp diodes
- Thermally enhanced SO package
- Green Product (RoHS compliant)
- AEC Qualified



**PG-DSO-14-22**

### Description

The TLE 4206-4G is a protected H-Bridge Driver designed specifically for automotive headlight beam control applications with DC-brush motor loads. The part is built using Infineon's bipolar high voltage power technology DOPL.

The standard enhanced power PG-DSO-14-22 package meets the application requirements and saves PCB-board space and costs.

The servo-loop-parameter pos.- and neg. Hysteresis, pos.- and neg. deadband and angle-amplification are programmable with external resistors. An internal window-comparator controls the input line. In case of fault conditions, like short circuit to GND, short circuit to supply-voltage, and broken wire, the TLE 4206-4G stops the motor immediately and enters active braking (brake high). The device also incorporates integrated features like over- and under voltage-lockout, short-circuit-protection and over-temperature-protection.

The TLE 4206-4G is a derivate of the TLE 4206-2G. The Range pin not only offers short circuit protection at the reference potentiometer but also determines the potentiometer's voltage range of operation. The TLE 4206-4G considers a smaller window of operation by way of increasing the lower Range Switch off and on thresholds to serve a larger variety of reference potentiometer strokes.

Type	Package	Marking
TLE 4206-4G	PG-DSO-14-22	TLE4206-4G

## 2 Block Diagram

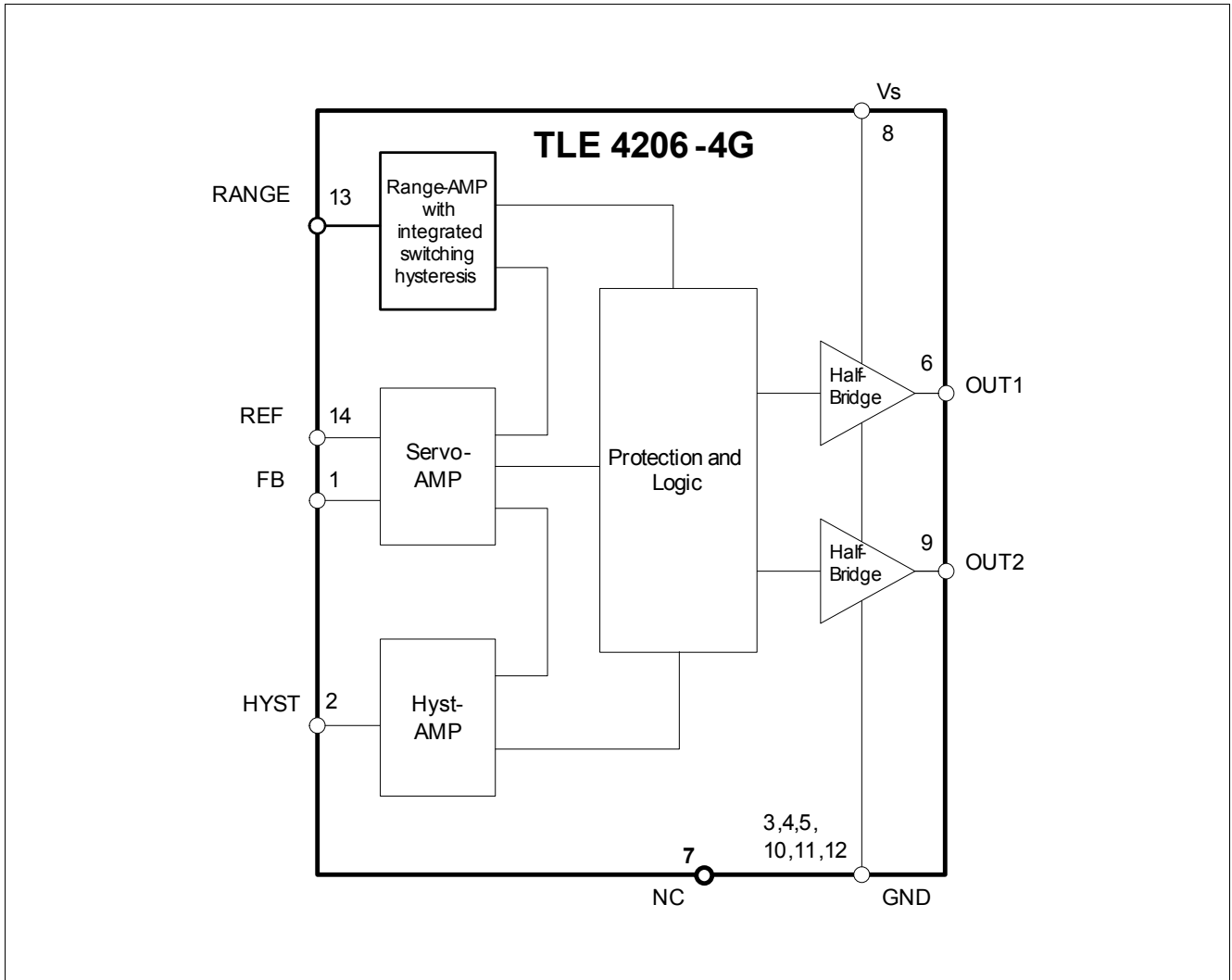


Figure 1 Block Diagram

### 3 Pin Configuration

#### 3.1 Pin Assignment

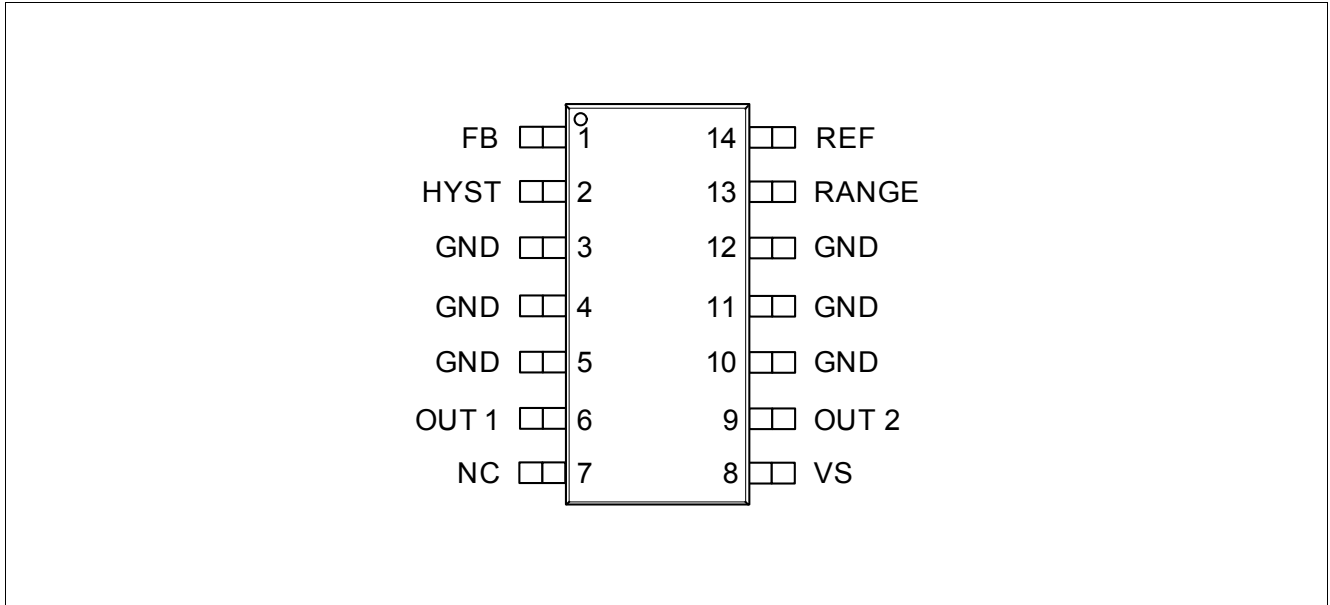


Figure 2 Pin Configuration

#### 3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	FB	Feedback Input
2	HYST	Hysteresis I/O
3, 4, 5, 10, 11, 12	GND	Ground
6	OUT1	Power Output 1
7	NC	Not Connected. This pin can be left open or connected to ground.
8	$V_s$	Power Supply Voltage
9	OUT2	Power Output 2
13	RANGE	Range Input
14	REF	Reference Input

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings <sup>1)</sup>

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
<b>Voltages</b>						
4.1.1	Supply voltage	$V_{S1}$	-0.3	45	V	–
4.1.2	Supply voltage	$V_{S2}$	-1	–	V	$t < 0.5\text{ s}$ ; $I_S > -2\text{ A}$
4.1.3	Logic input voltages (FB, REF, RANGE, HYST)	$V_I$	-0.3	20	V	–
<b>Currents</b>						
4.1.4	Output current (OUT1, OUT2)	$I_{OUT}$	–	–	A	internally limited
4.1.5	Output current (Diode)	$I_{OUT\_DIODE}$	-1	1	A	–
4.1.6	Input current (FB, REF, RANGE, HYST)	$I_{IN}$	-2 -6	2 6	mA mA	– $t < 2\text{ ms}$ ; $t/T < 0.1$
<b>Temperatures</b>						
4.1.7	Junction Temperature	$T_j$	-40	150	°C	–
4.1.8	Storage Temperature	$T_{stg}$	-50	150	°C	–
<b>ESD Susceptibility</b>						
4.1.9	ESD resistivity of OUT and $V_S$ pin to GND	$V_{ESD}$	-2	2	kV	HBM <sup>2)</sup>
4.1.10	ESD Resistivity logic pins to GND	$V_{ESD5,7}$	-2	2	kV	HBM <sup>2)</sup>

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to EIA/JESD 22-A114B

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Operating Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply voltage	$V_{S\_OP}$	8	18	V	After $V_S$ rising above $V_{UV\ ON}$
4.2.2	Supply voltage increasing	$V_{S\_INC}$	-0.3	$V_{UV\ ON}$	V	Outputs in tristate
4.2.3	Supply voltage decreasing	$V_{S\_DEC}$	-0.3	$V_{UV\ OFF}$	V	Outputs in tristate
4.2.4	Output current	$I_{OUT1-2}$	-0.8	0.8	A	–
4.2.5	Input current (FB, REF)	$I_{IN\_op}$	-50	500	$\mu A$	–
4.2.6	Junction temperature	$T_j$	-40	150	$^{\circ}C$	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

## 4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Soldering Point <sup>1)</sup>	$R_{thJSP}$	–	25	–	K/W	measured to pin 5
4.3.2	Junction to Ambient <sup>1)</sup> minimal-footprint	$R_{thJA\_minfoot}$	–	130	–	K/W	<sup>2)</sup>
4.3.3	Junction to Ambient <sup>1)</sup> additional 600 mm <sup>2</sup> CU area	$R_{thJA\_600mm2}$	–	65	–	K/W	<sup>3)</sup>

1) Not subject to production test, specified by design.

2) JESD 51-2, 51-3, FR4 76.2 mm × 114.3 mm × 1.5 mm, 70  $\mu m$  Cu, minimal footprint; Ta=27°C

3) JESD 51-2, 51-3, FR4 76.2 mm × 114.3 mm × 1.5 mm, 70  $\mu m$  Cu, 600 mm<sup>2</sup> CU cooling area connected to Pins: 3, 4, 5, 10, 11, 12; Ta=27°C

## 4.4 Electrical Characteristics

### Electrical Characteristics

$V_S = 8\text{ V to }18\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$ ,  $I_{OUT1-2} = 0\text{ A}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		

#### Current Consumption

4.4.1	Supply current	$I_{S\_no\ load}$	–	12	20	mA	no load connected
4.4.2	Supply current	$I_{S\_0.4A}$	–	20	30	mA	$I_{OUT1} = 0.4\text{ A};$ $I_{OUT2} = -0.4\text{ A}$
4.4.3	Supply current	$I_{S\_0.8A}$	–	35	50	mA	$I_{OUT1} = 0.8\text{ A};$ $I_{OUT2} = -0.8\text{ A}$

#### Over- and Under Voltage Lockout

4.4.4	UV Switch ON voltage	$V_{UV\ ON}$	–	7.4	8	V	$V_S$ increasing
4.4.5	UV Switch OFF voltage	$V_{UV\ OFF}$	6.3	6.9	–	V	$V_S$ decreasing
4.4.6	UV ON/OFF Hysteresis	$V_{UVHY}$	–	0.5	–	V	$V_{UV\ ON} - V_{UV\ OFF}$
4.4.7	OV Switch OFF voltage	$V_{OV\ OFF}$	–	20.5	23	V	$V_S$ increasing
4.4.8	OV Switch ON voltage	$V_{OV\ ON}$	17.5	20	–	V	$V_S$ decreasing
4.4.9	OV ON/OFF Hysteresis	$V_{OVHY}$	–	0.5	–	V	$V_{OV\ OFF} - V_{OV\ ON}$

#### Outputs OUT1-2, Saturation Voltages

4.4.10	Source (upper) $I_{OUT} = -0.2\text{ A}$	$V_{SAT\ U\ 0.2A}$	–	0.85	1.15	V	$T_j = 25\text{ °C}$
4.4.11	Source (upper) $I_{OUT} = -0.4\text{ A}$	$V_{SAT\ U\ 0.4A}$	–	0.90	1.20	V	
4.4.12	Sink (upper) $I_{OUT} = -0.8\text{ A}$	$V_{SAT\ U\ 0.8A}$	–	1.10	1.50	V	
4.4.13	Sink (lower) $I_{OUT} = 0.2\text{ A}$	$V_{SAT\ L\ 0.2A}$	–	0.15	0.23	V	
4.4.14	Sink (lower) $I_{OUT} = 0.4\text{ A}$	$V_{SAT\ L\ 0.4A}$	–	0.25	0.40	V	
4.4.15	Sink (lower) $I_{OUT} = 0.8\text{ A}$	$V_{SAT\ L\ 0.8A}$	–	0.45	0.75	V	
4.4.16	Total drop, $I_{OUT} = 0.2\text{ A}$	$V_{SAT\ 0.2A}$	–	1.0	1.4	V	$V_{SAT} = V_{SAT\ U} + V_{SAT\ L}$
4.4.17	Total drop, $I_{OUT} = 0.4\text{ A}$	$V_{SAT\ 0.4A}$	–	1.2	1.7	V	
4.4.18	Total drop, $I_{OUT} = 0.8\text{ A}$	$V_{SAT\ 0.8A}$	–	1.6	2.5	V	

#### Outputs OUT1-2, Clamp Diodes

4.4.19	Forward voltage; upper	$V_{FU}$	–	1	1.5	V	$I_F = 0.4\text{ A}$
4.4.20	Upper leakage current	$I_{LKU}$	–	–	5	mA	
4.4.21	Forward voltage; lower	$V_{FL}$	–	0.9	1.4	V	

#### Input-Interface, Input REF

4.4.22	Quiescent voltage	$V_{REFq}$	–	200	–	mV	$I_{REF} = 0\text{ }\mu\text{A}$
4.4.23	Input resistance	$R_{REF}$	–	6	–	k $\Omega$	$0\text{ V} < V_{REF} < 0.5\text{ V}$



General Product Characteristics

Electrical Characteristics (cont'd)

$V_S = 8\text{ V to }18\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$ ,  $I_{OUT1-2} = 0\text{ A}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		

**Input-Interface, Input FB**

4.4.24	Quiescent voltage	$V_{FBq}$	–	200	–	mV	$I_{FB} = 0\text{ }\mu\text{A}$
4.4.25	Input resistance	$R_{FB}$	–	6	–	k $\Omega$	$0\text{ V} < V_{FB} < 0.5\text{ V}$

**Input-Interface, Input/Output HYST**

4.4.26	Current Amplification $A_{HYST} = I_{HYST} / (I_{REF} - I_{FB})$	$A_{HYST}$	0.8	0.95	1.1	–	$-20\text{ }\mu\text{A} < I_{HYST} < -10\text{ }\mu\text{A}$ ; $10\text{ }\mu\text{A} < I_{HYST} < 20\text{ }\mu\text{A}$ ; $I_{REF} = 250\text{ }\mu\text{A}$ ; $V_{HYST} = V_S / 2$
4.4.27	Current Offset	$I_{HYSTIO}$	-2	0.35	3	$\mu\text{A}$	$I_{REF} = I_{FB} = 250\text{ }\mu\text{A}$ ; $V_{HYST} = V_S / 2$
4.4.28	Threshold voltage High	$V_{HYH} / V_S$	–	52	–	%	–
4.4.29	Deadband voltage High	$V_{DBH} / V_S$	–	50.4	–	%	–
4.4.30	Deadband voltage Low	$V_{DBL} / V_S$	–	49.6	–	%	–
4.4.31	Threshold voltage Low	$V_{HYL} / V_S$	–	48	–	%	–
4.4.32	Hysteresis Window	$V_{HYW} / V_S$	3	4	5	%	$(V_{HYH} - V_{HYL}) / V_S$
4.4.33	Deadband Window	$V_{DBW} / V_S$	0.4	0.8	1.2	%	$(V_{DBH} - V_{DBL}) / V_S$

**Input-Interface, Input RANGE**

4.4.34	Input current	$I_{RANGE}$	-1	–	1	$\mu\text{A}$	$0\text{ V} < V_{RANGE} < V_S$
4.4.35	Switch-OFF voltage High	$V_{OFFH}$	-25	0	100	mV	refer to $V_S$
4.4.36	Switch-OFF voltage Low	$V_{OFFL}$	1240	1340	1440	mV	refer to GND, $V_{RANGE}$ decreasing
4.4.37	Switch-ON voltage Low	$V_{ONL}$	1320	1424	1520	mV	refer to GND, $V_{RANGE}$ increasing
4.4.38	Low-threshold hysteresis	$V_{OFFLHYS}$	–	84	–	mV	see <a href="#">Figure 6</a>

**Thermal Shutdown**

4.4.39	Thermal shutdown junction temperature <sup>1)</sup>	$T_{jSD}$	150	175	200	$^{\circ}\text{C}$	–
4.4.40	Thermal switch-on junction temperature	$T_{jSO}$	120	–	170	$^{\circ}\text{C}$	–
4.4.41	Temperature hysteresis	$\Delta T$	–	30	–	K	–

1) Not subject to production test, specified by design.

## 5 Application Information

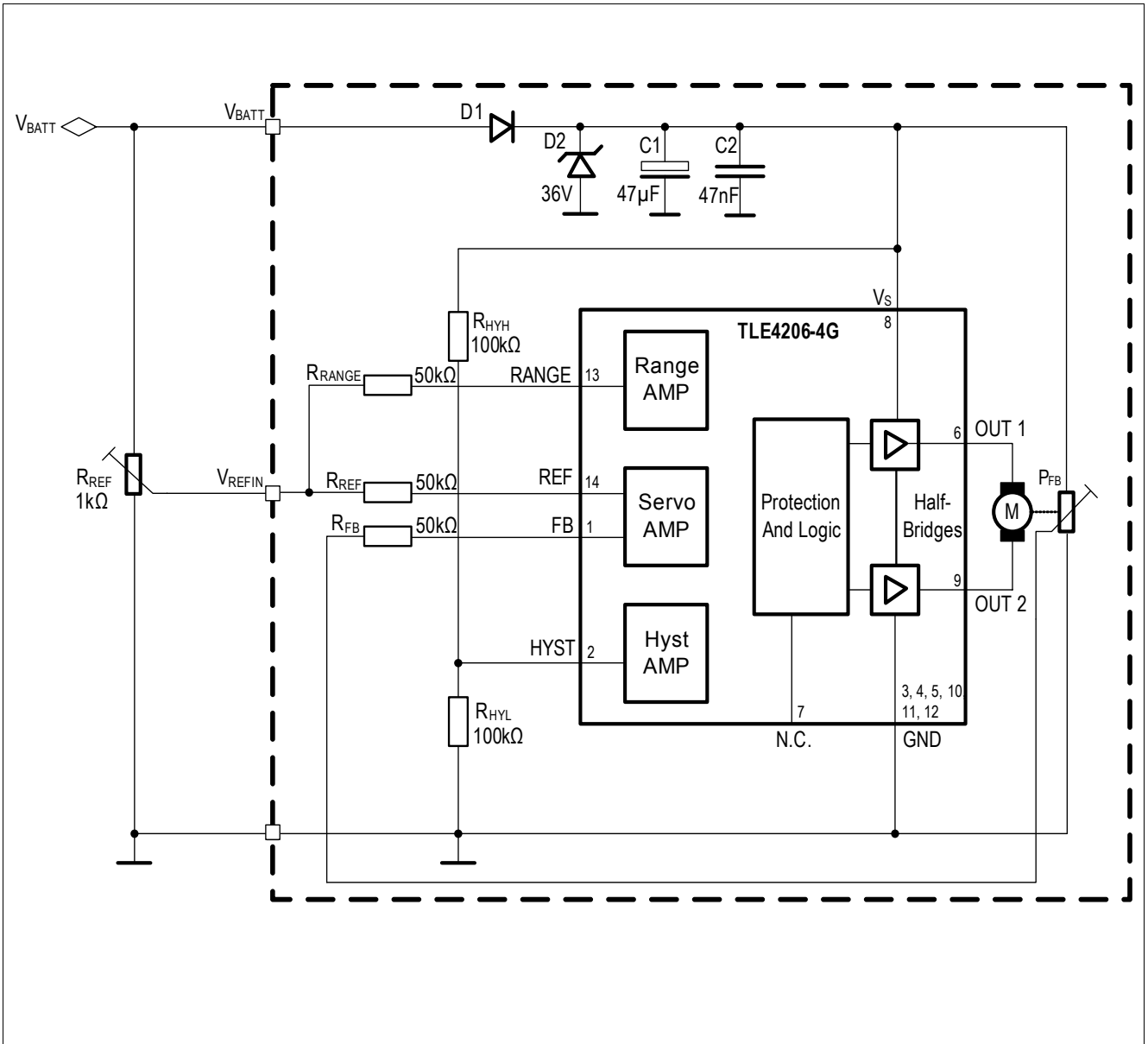


Figure 3 Application Circuit for Manual Headlight Beam Adjustment

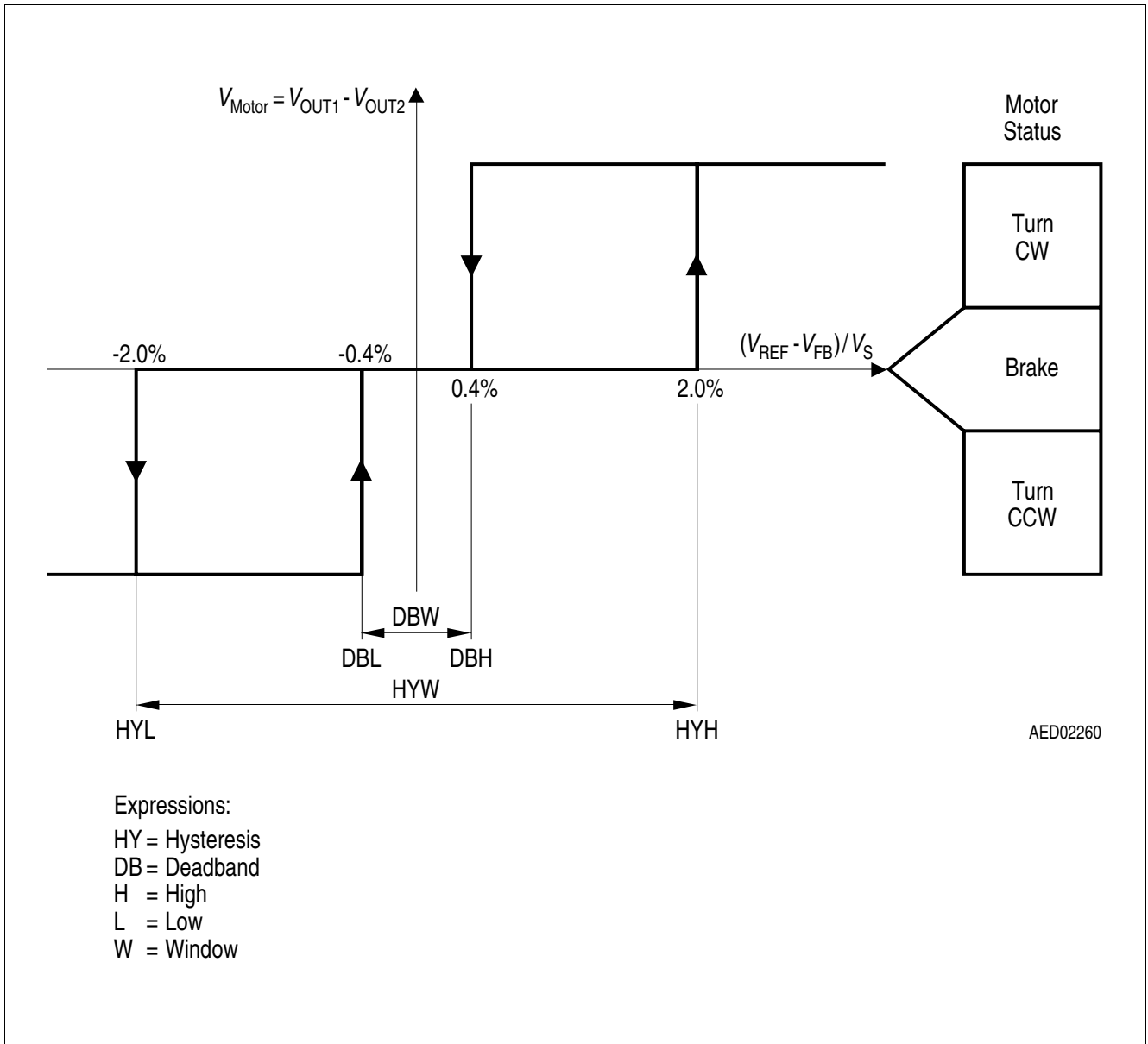


Figure 4 Hysteresis, Phaselag and Deadband-Definitions

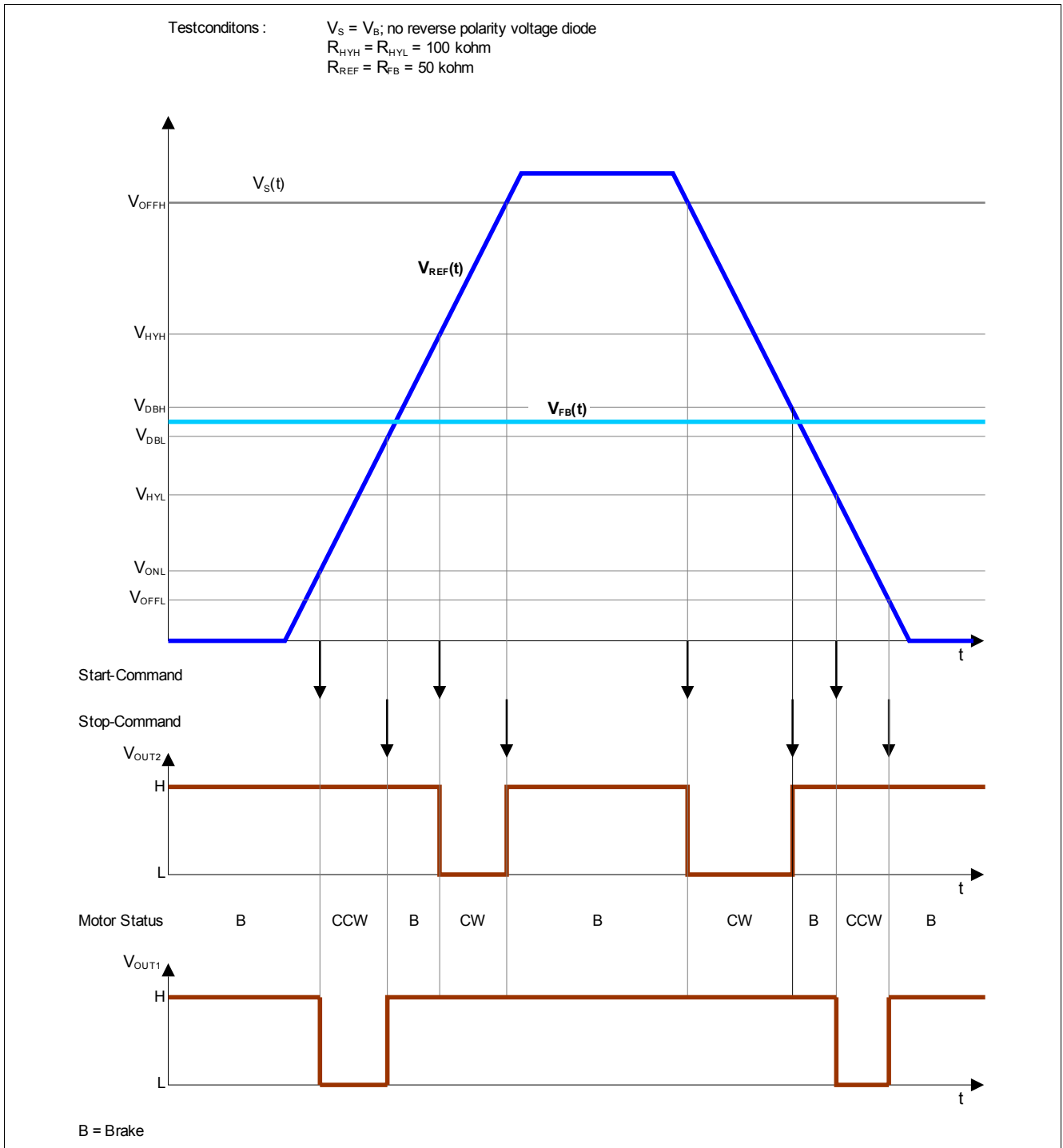


Figure 5 Motor Operation

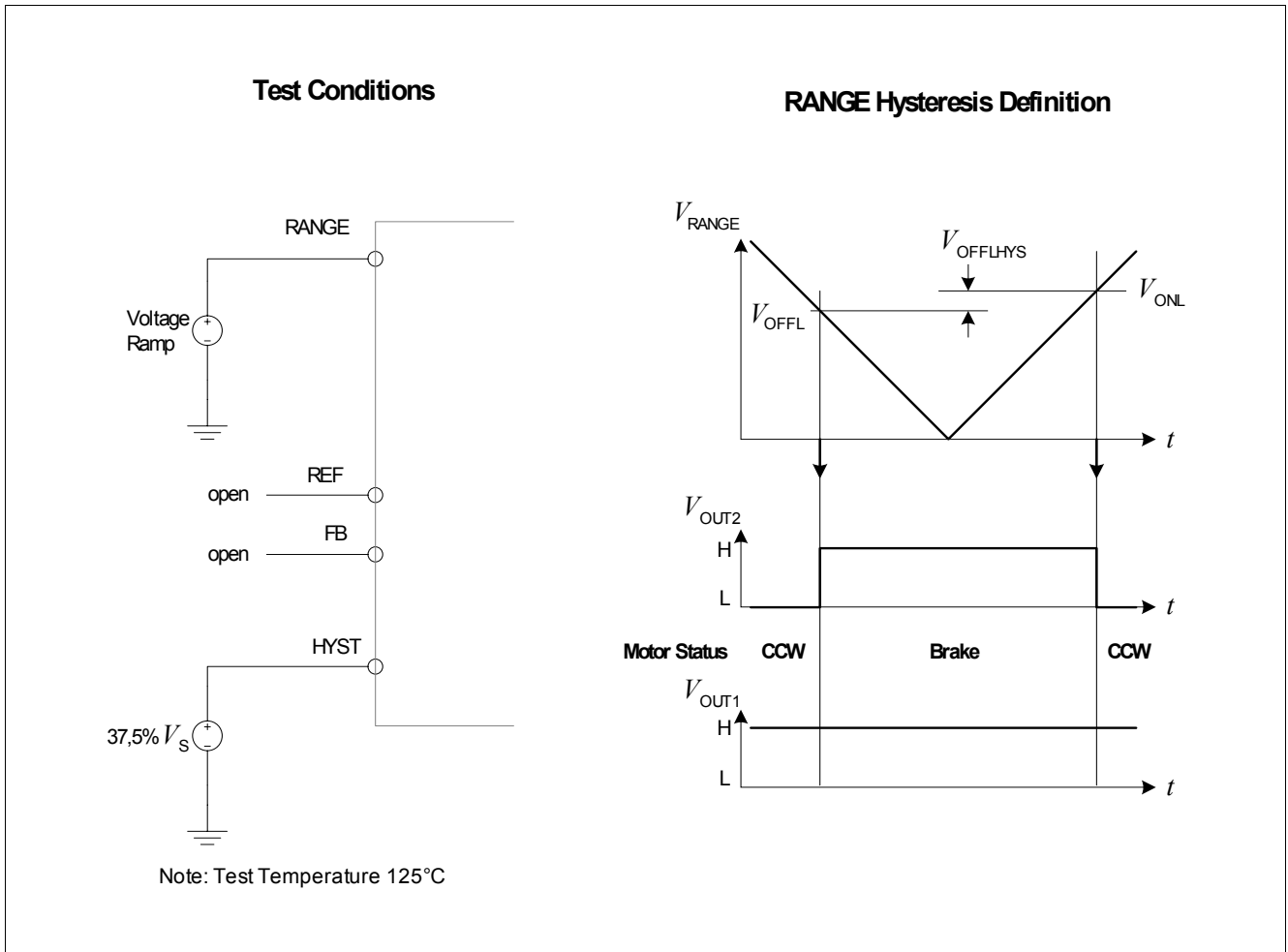


Figure 6 RANGE Hysteresis and Test Conditions

## 6 Package Outlines

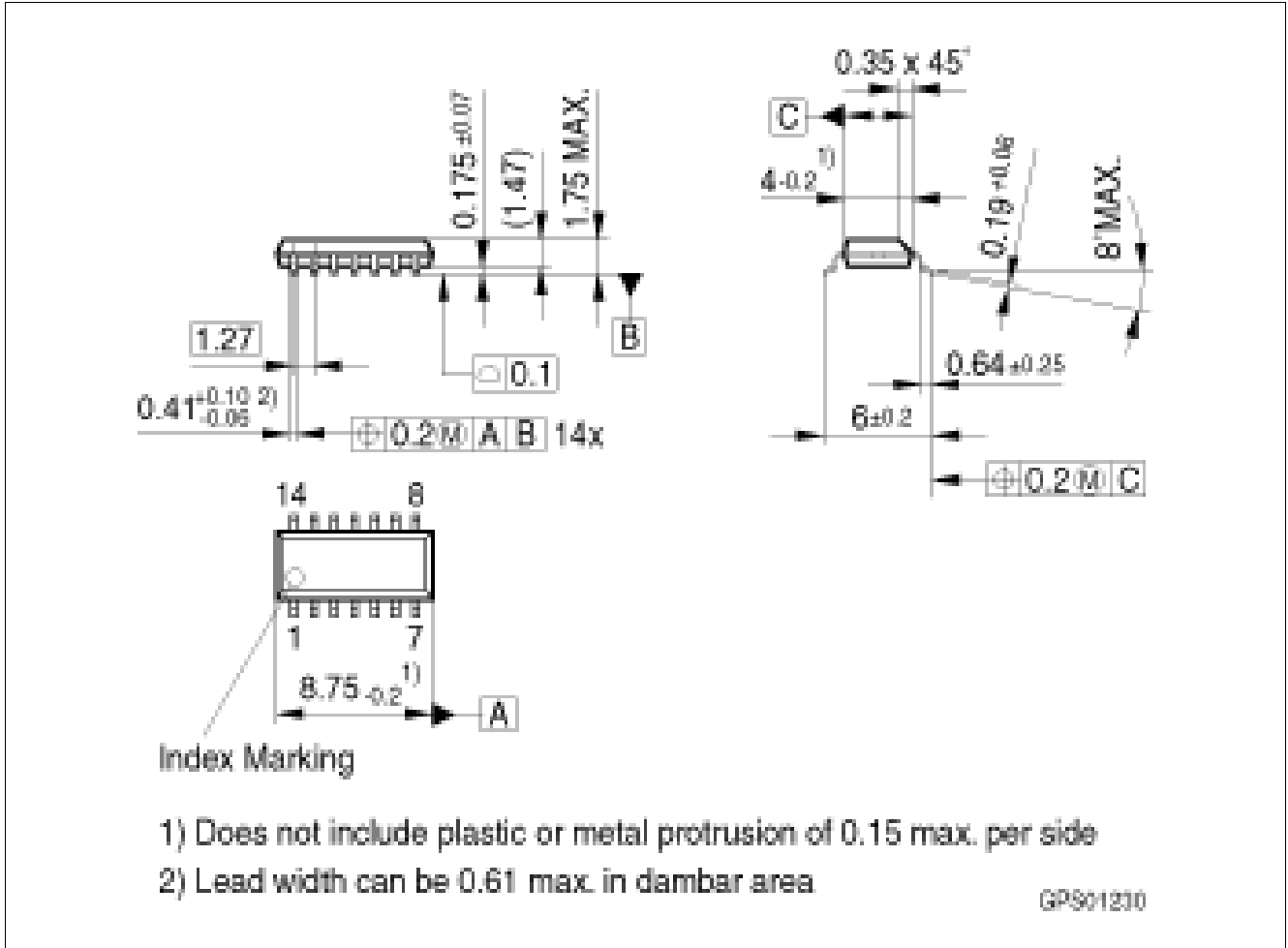


Figure 7 PG-DSO-14-22 (Plastic/Plastic Green - Dual Small Outline Package)

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

## 7 Revision History

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TLE 4206-4G

**Revision History: Rev. 1.0, 2010-08-05**

Previous Version(s): None

Revision	Page	Subjects (major changes since last revision)
1.0	All	Final Data Sheet Release

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