OptiMOS™-5 Power-Transistor

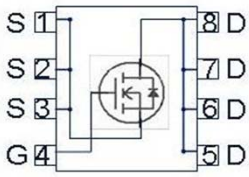
Product Summary

V_{DS}	100	V
$R_{DS(on)}$	4	mΩ
I_D	100	A

Features

- N-channel - Enhancement mode - Normal level
- AEC qualified
- MSL1 up to 260°C peak reflow
- 100% Avalanche tested
- Feasible for automatic optical inspection (AOI)

PG-TDSON-8



Type	Package	Marking
IAUC100N10S5N040	PG-TDSON-8	5N1N040

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current[1]	I_D	T_C=25°C, V_{GS}=10V	100	A
		T_C=100°C, V_{GS}=10V	100	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25°C	400	
Avalanche energy, single pulse	E_{AS}	I_D=50A	234	mJ
Avalanche current, single pulse	I_{AS}	-	100	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	T_C=25°C, T_J =175°C	167	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}	-	-	-	0.9	K/W

Electrical characteristics, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D= 1mA	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D= 90µA	2.2	3.0	3.8	
Zero gate voltage drain current	I_{DSS}	V_{DS}=100V, V_{GS}=0V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=100V, V_{GS}=0V, T_j=125°C[2)]	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=6V, I_D=25A	-	4.2	5.6	mΩ
		V_{GS}=10 V, I_D=50 A	-	3.4	4	
Gate resistance[2)]	R_G		-	1.3	-	Ω

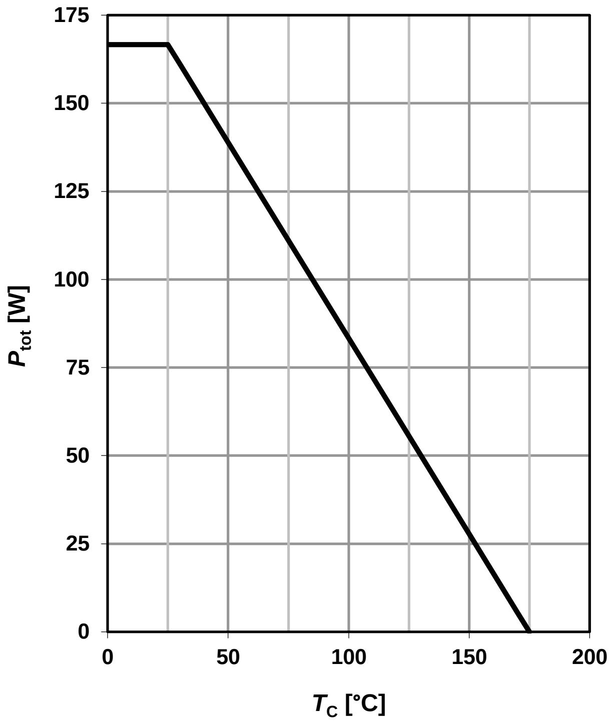
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2)]						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=50V, f=1MHz	-	4000	5200	pF
Output capacitance	C_{oss}		-	660	860	
Reverse transfer capacitance	C_{rss}		-	28	42	
Turn-on delay time	$t_{d(on)}$	V_{DD}=50V, V_{GS}=10V, I_D=100A, R_G=3.5Ω	-	10	-	ns
Rise time	t_r		-	5	-	
Turn-off delay time	$t_{d(off)}$		-	19	-	
Fall time	t_f		-	14	-	
Gate Charge Characteristics[2)]						
Gate to source charge	Q_{gs}	V_{DD}=50V, I_D=50A, V_{GS}=0 to 10V	-	20	26	nC
Gate to drain charge	Q_{gd}		-	13	20	
Gate charge total	Q_g		-	60	78	
Gate plateau voltage	$V_{plateau}$		-	4.6	-	V
Reverse Diode						
Diode continous forward current[2)]	I_S	T_C=25°C	-	-	100	A
Diode pulse current[2)]	$I_{S,pulse}$		-	-	400	
Diode forward voltage	V_{SD}	V_{GS}=0V, I_F=50A, T_j=25°C	-	0.9	1.1	V
Reverse recovery time[2)]	t_{rr}	V_R=50V, I_F=50A, di_F/dt=100A/µs	-	54	-	ns
Reverse recovery charge[2)]	Q_{rr}		-	90	-	nC

1) Current is limited by package; with an R_{thJC} =0.9K/W the chip is able to carry 140A at 25°C.

2) Defined by design. Not subject to production test.

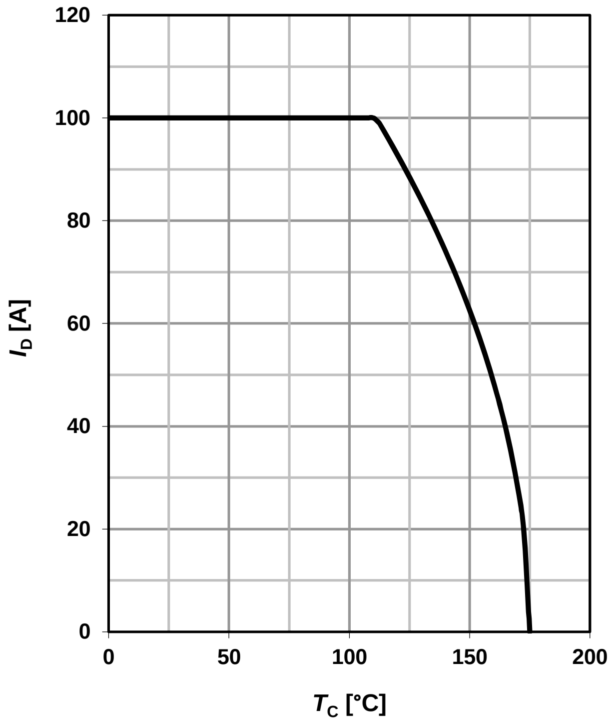
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V



2 Drain current

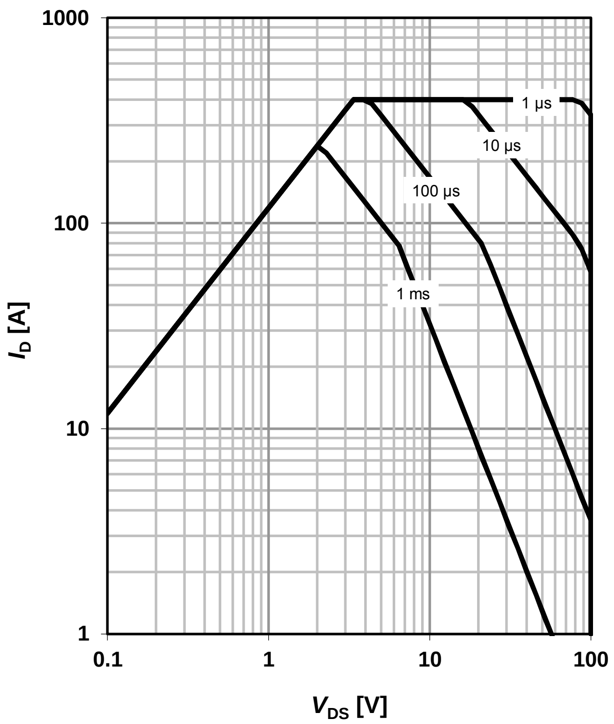
$I_D = f(T_C)$; $V_{GS} \geq 6$ V



3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$

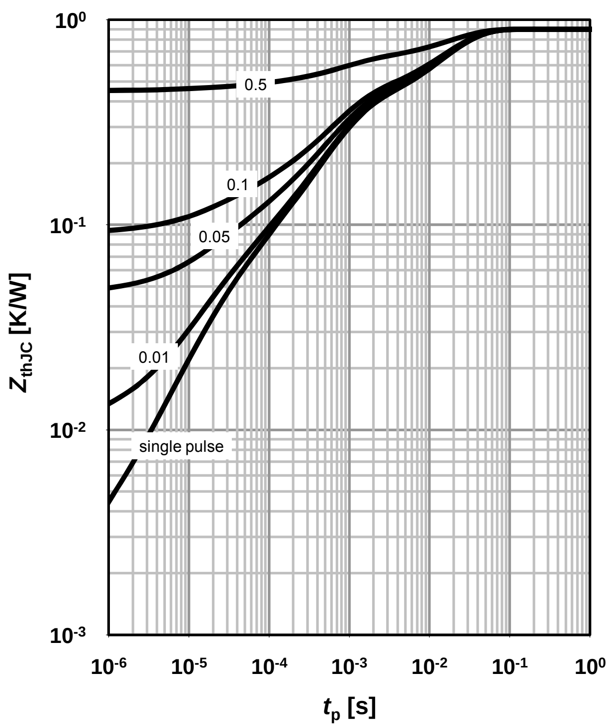
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

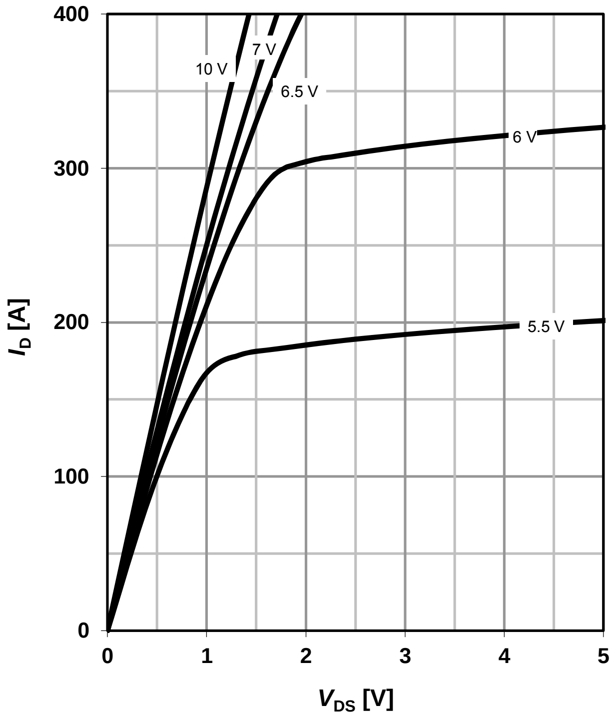
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C

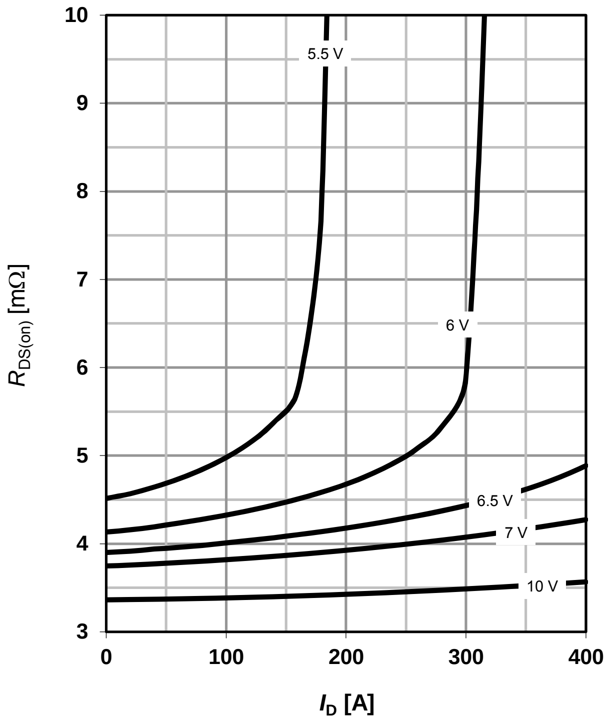
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = (I_D)$; $T_j = 25$ °C

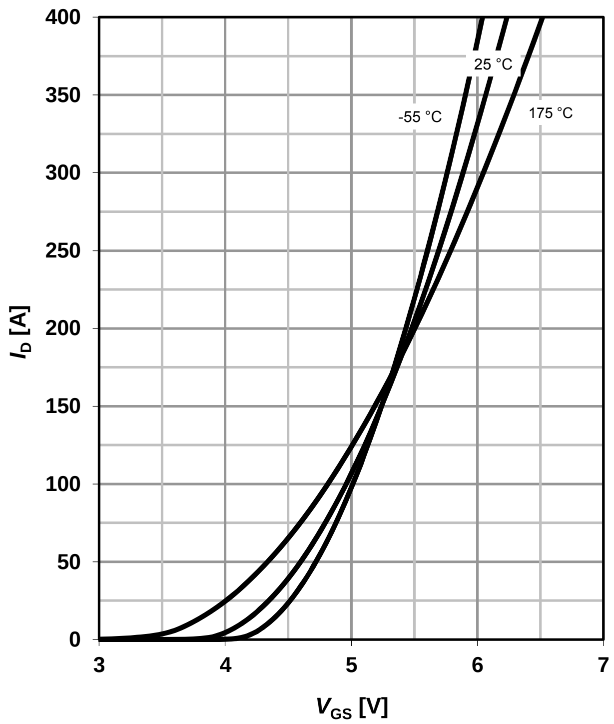
parameter: V_{GS}



7 Typ. transfer characteristics

$I_D = f(V_{GS})$; $V_{DS} = 6$V

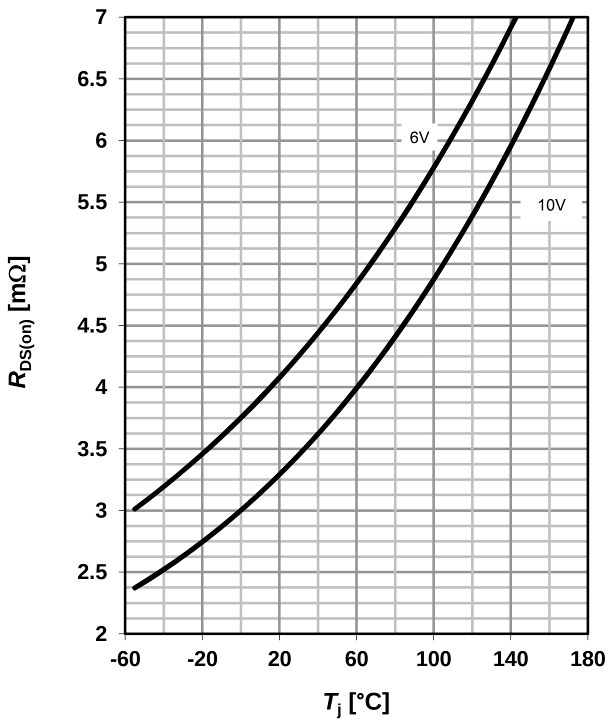
parameter: T_j



8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j)$; $I_D = 50$ A; $V_{GS} = 10$ V

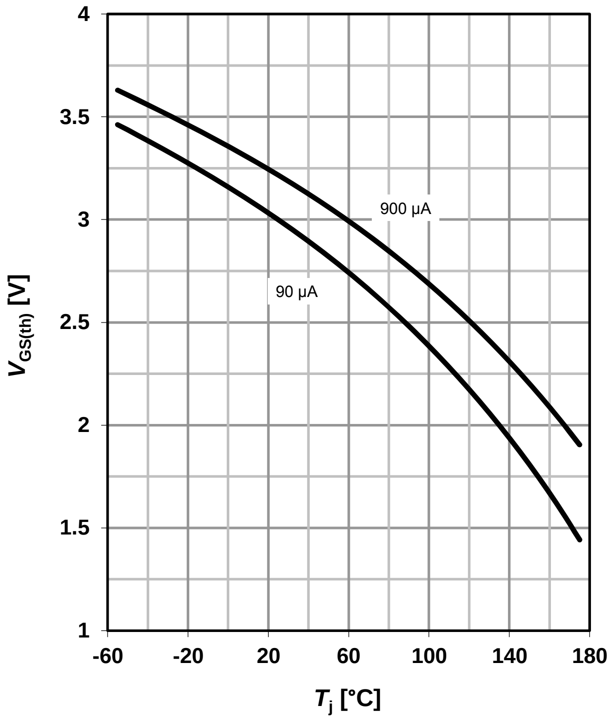
$I_D = 25$ A; $V_{GS} = 6$ V



9 Typ. gate threshold voltage

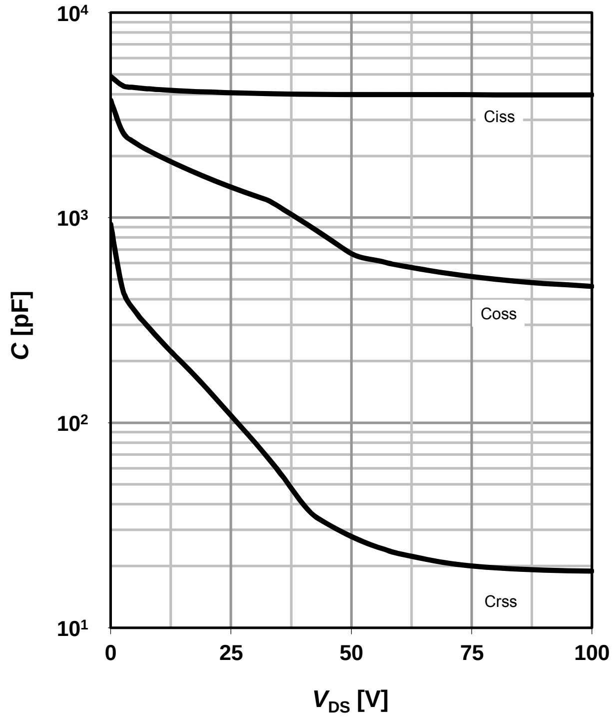
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

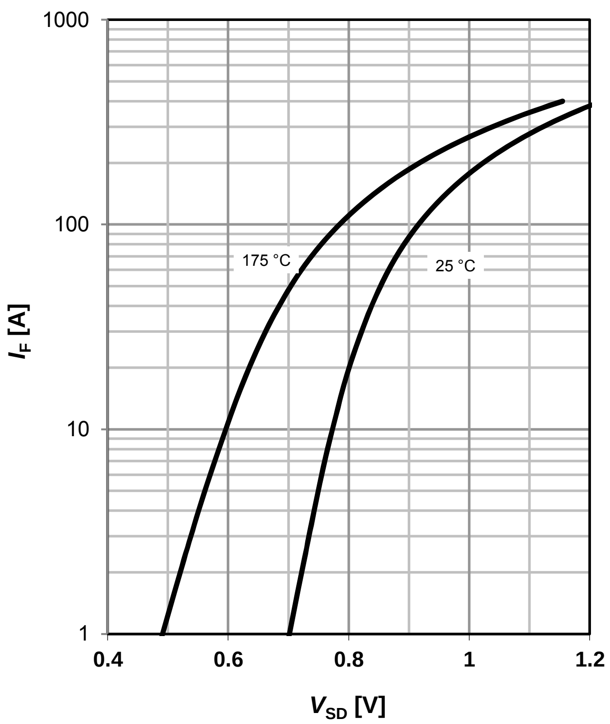
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



11 Typical forward diode characteristicis

IF = $f(V_{SD})$

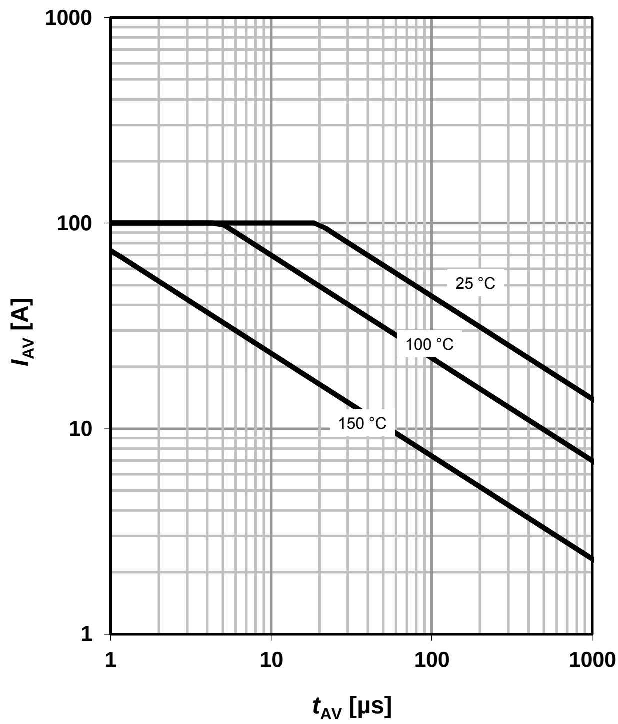
parameter: T_j



12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$

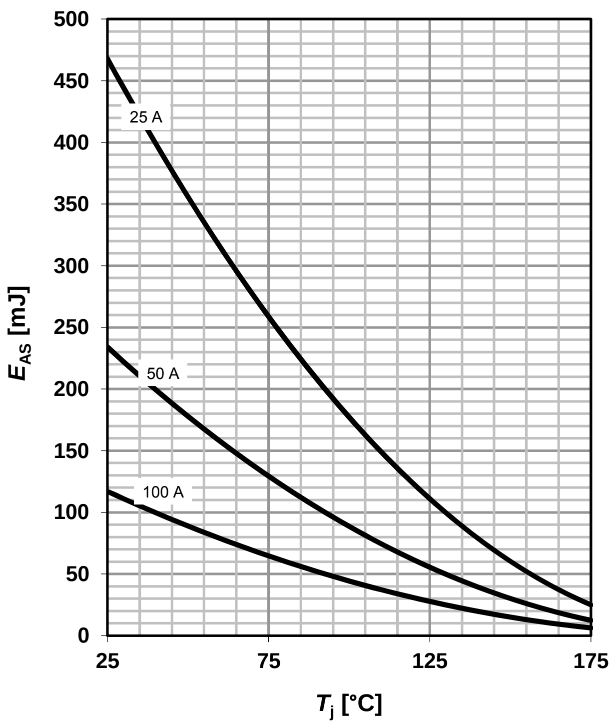
parameter: $T_{j(start)}$



13 Typical avalanche energy

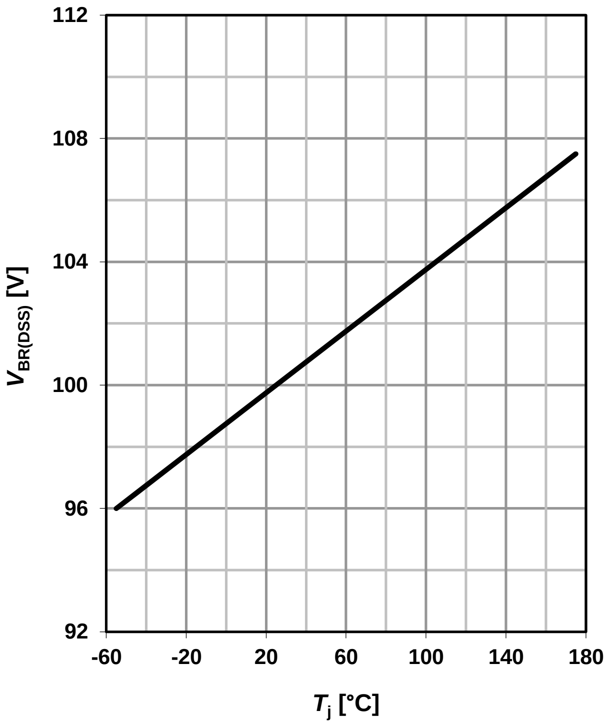
$E_{AS} = f(T_j)$

parameter: I_D



14 Drain-source breakdown voltage

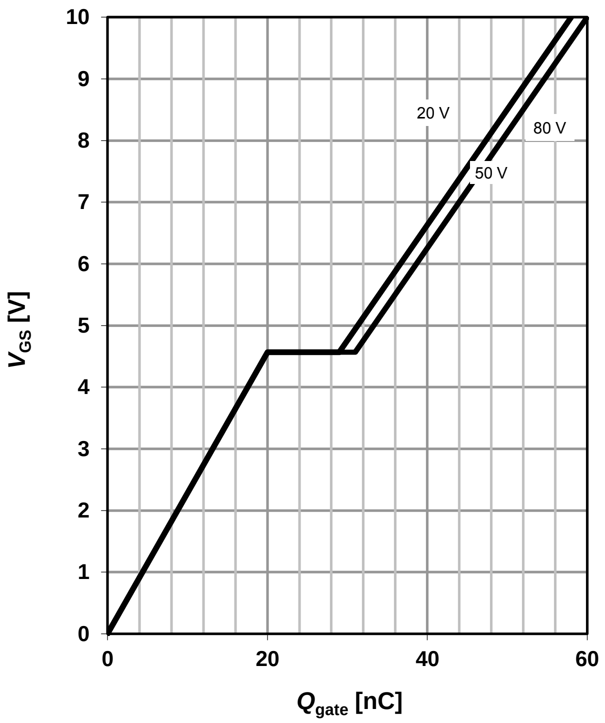
$V_{BR(DSS)} = f(T_j)$; $I_D = 1$ mA



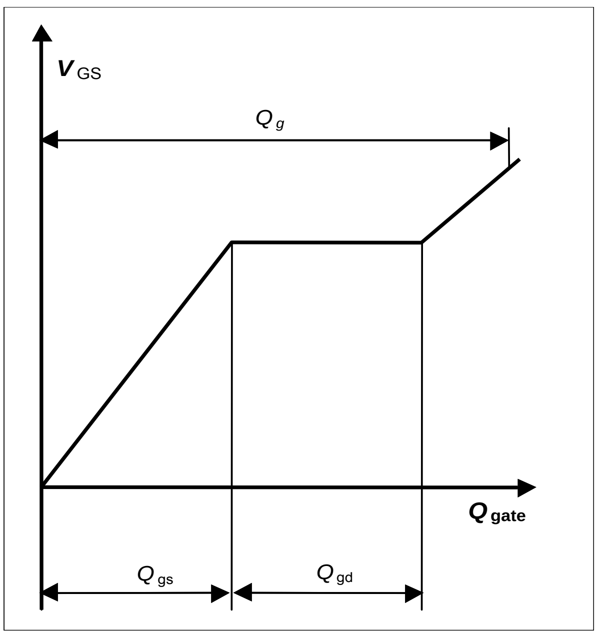
15 Typ. gate charge

$V_{GS} = f(Q_{gate})$; $I_D = 50$ A pulsed

parameter: V_{DD}



16 Gate charge waveforms



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Revision History

Version	Date	Changes
Revision 1.0	2018-06-12	Final Data Sheet