TVS Diodes

Transient Voltage Suppressor Diodes

BGF120A

Dual Channel Ultra-Low Capacitance ESD Diode

Datasheet

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Final

Power Management & Multimarket

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Page or Item	**Subjects (major changes since previous revision)**
Rev. 1.4, 2012-09-17	
12	Package outline updated

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Last Trademarks Update 2011-11-11

1 BGF120A Dual Channel Ultra-Low Capacitance ESD Diode

1.1 Features

- ESD /transient protection of high-speed data and RF antenna lines exceeding:
  – IEC61000-4-2 (ESD): 18 kV (contact)
- Max. reverse working voltage: 5.3 V
- Ultra-low capacitance:
  – < 0.75 pF (max.) in bi-directional configuration
  – < 1.5 pF (max.) in uni-directional configuration
- Very low reverse current: < 1 nA (typ.)
- Small leadless plastic package with 0.75 mm x 0.75 mm size (typ.) and 0.66 mm height (max.)
- 400 µm pad pitch and 40 µm Sn solder depot on pads
- RoHS and WEEE compliant package

1.2 Application

- USB 2.0, 10/100/1000 Ethernet, Firewire, DVI, HDMI, S-ATA
- RF antenna protection e.g. GPS, FM radio, mobile TV

1.3 Description

The BGF120A can be used for 2 lines uni-directional or 1 line bi-directional ESD and surge protection up to 20 kV contact discharge according to IEC61000-4-2. The capacitance of the device is less then 0.75 pF (max.) in bi-directional configuration and less than 1.5 pF (max.) in uni-directional configuration. Maximum reverse working voltage is 5.3 V (uni-directional) or ±5.3 V (bi-directional). The reverse leakage current is less than 1 nA (typ.). The leadless plastic package has 0.75 mm x 0.75 mm typical size and maximum height of 0.66 mm. The pads have 400 µm pitch and offer 40 µm Sn for high reliability soldering

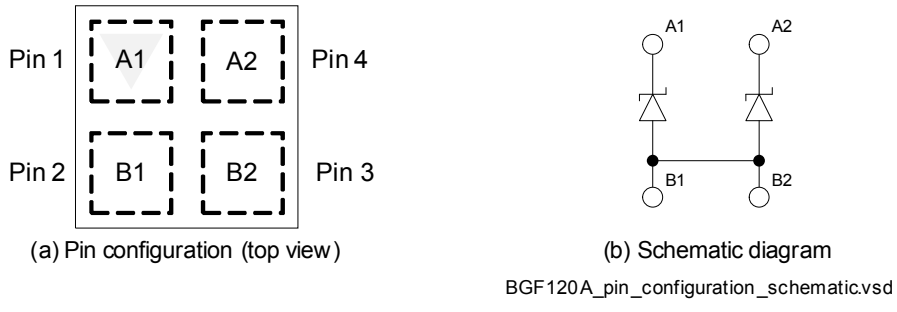

Figure 1-1 Pin Configuration and Schematic Diagram

Type	Package	Configuration	Marking code
BGF120A	TSLP-4-8	2 lines, uni-directional[1)]	A

1) Or 1 line, bi-directional between A1 and A2, if B1, B2 are not connected

2 Electrical Characteristics

Table 2-1 Maximum Ratings T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operating temperature range	T_{OP}	-40	-	+125	°C	
Storage temperature range	T_{STG}	-65	-	+150	°C	
Contact discharge[1)]	V_{ESD}	-	-	18	kV	

1) V_{ESD} according to IEC61000-4-2

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 2-2 DC Electrical Characteristics T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	-	-	5.3	V	
Breakdown voltage	V_{BR}	6	-	-	V	I_{BR} = 1 mA
Reverse current	I_R	-	<1	50	nA	V_R = 5.3V

Table 2-3 DC Electrical Characteristics T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance[1)] A1 or A2 to B1/B2 A1 to A2, B1/B2 n.c.	C_L	 - -	 - -	 1.5 0.75	pF	V_R = 0 V, f = 1 MHz
Series inductance per diode	L_S	-	0.25	-	nH	

1) Total capacitance line to ground

Table 2-4 ESD Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse clamping voltage[1)] A1 or A2 vs B1, B2	V_{CL}	-	22	-	V	I_{TLP} = 16 A,
A1 or A2 vs B1, B2		-	31	-		I_{TLP} = 30 A,
Forward clamping voltage[1)] A1 or A2 vs B1, B2	V_{FC}	-	-14	-	V	I_{TLP} = -16 A,
A1 or A2 vs B1, B2		-	-20	-		I_{TLP} = -30 A,
Dynamic resistance[1)] positive pulse A1 or A2 vs. B1, B2 negative pulse A1 or A2 vs B1, B2	R_{DYN}	- -	0.7 0.5	- -	Ω	

1) ANSI/ESD STM5.5.1 - Electrostatic Discharge Sensitive Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, $t_{r\ =\ 0.6\ ns,}$ I_{TLP} and V_{TLP} averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP characteristic between I_{PP1} = 10 A and I_{PP2} = 30 A. Please refer to Application Note AN210**[1]**.

3 Typical Characteristics

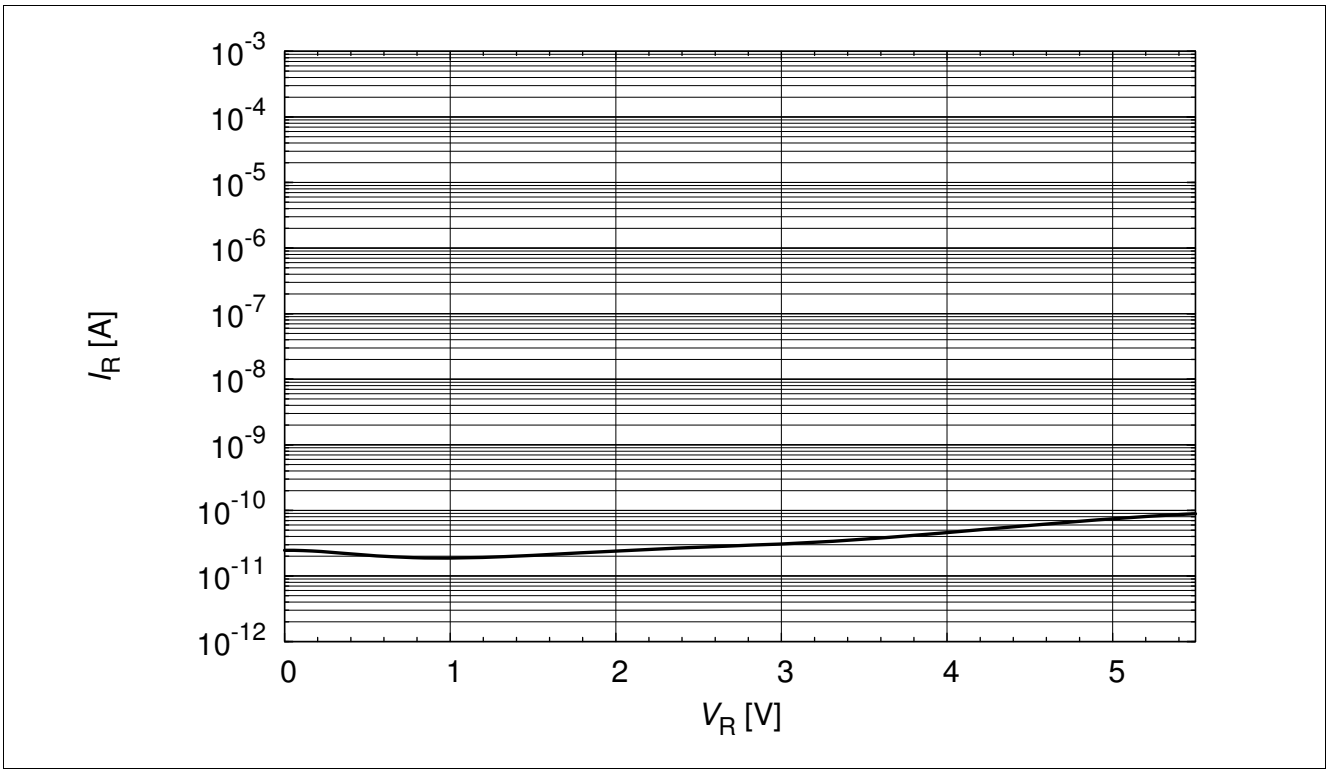

Figure 3-1 Reverse current I_R = f(V_R)

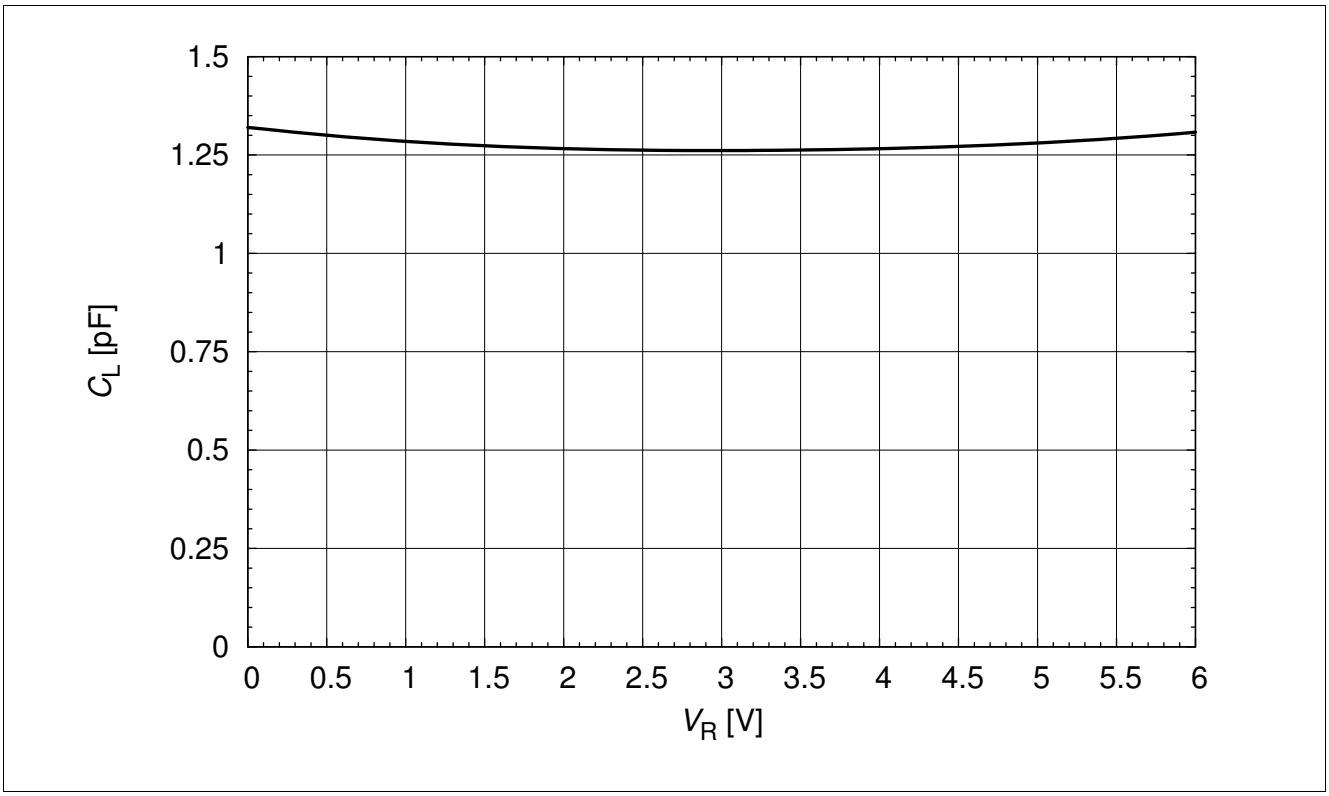

Figure 3-2 Capacitance A1vs. B1, A2 vs. B2, $C_{L(A1,B1)}$ = $C_{L(A2,B2)}$ = f(V_R)

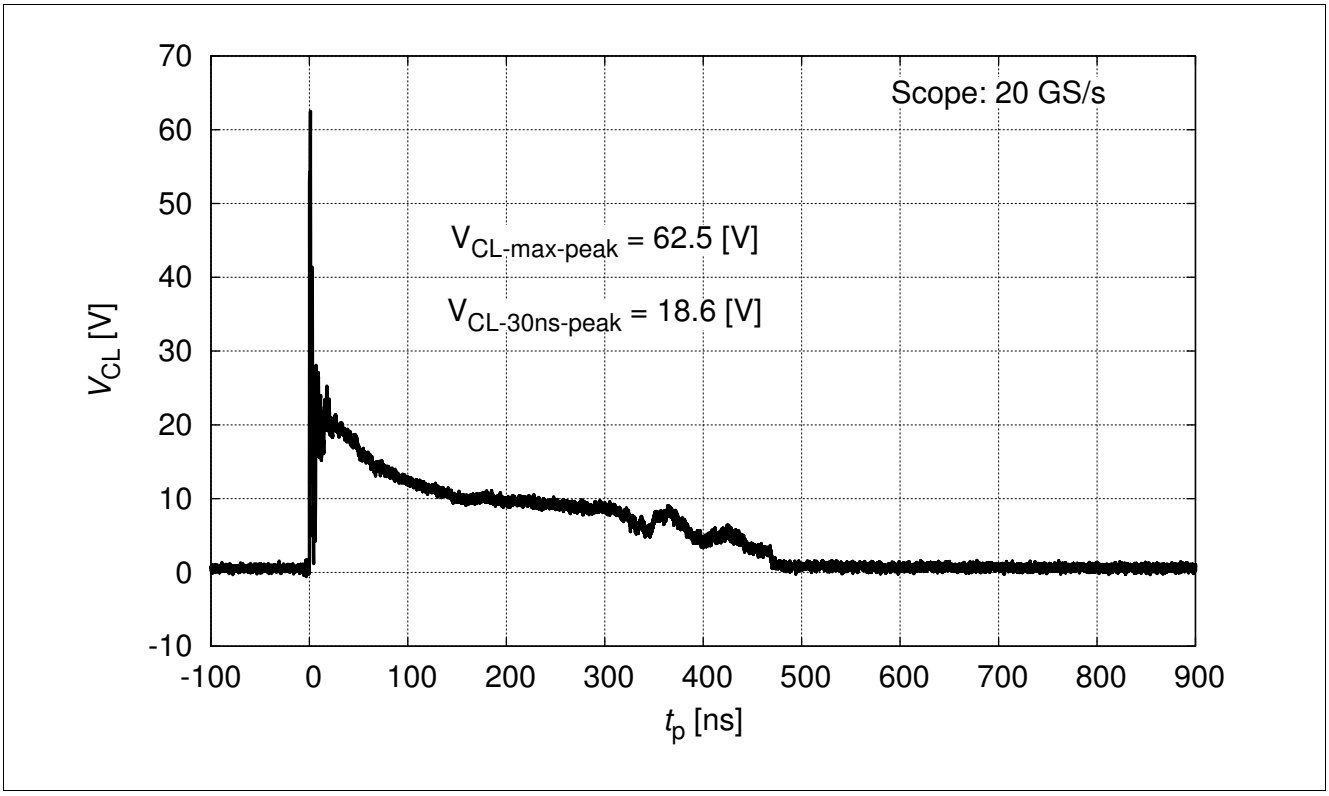

Figure 3-3 Clamping voltage at +8 kV discharge according IEC61000-4-2 (R = 330 Ω, C = 150 pF)

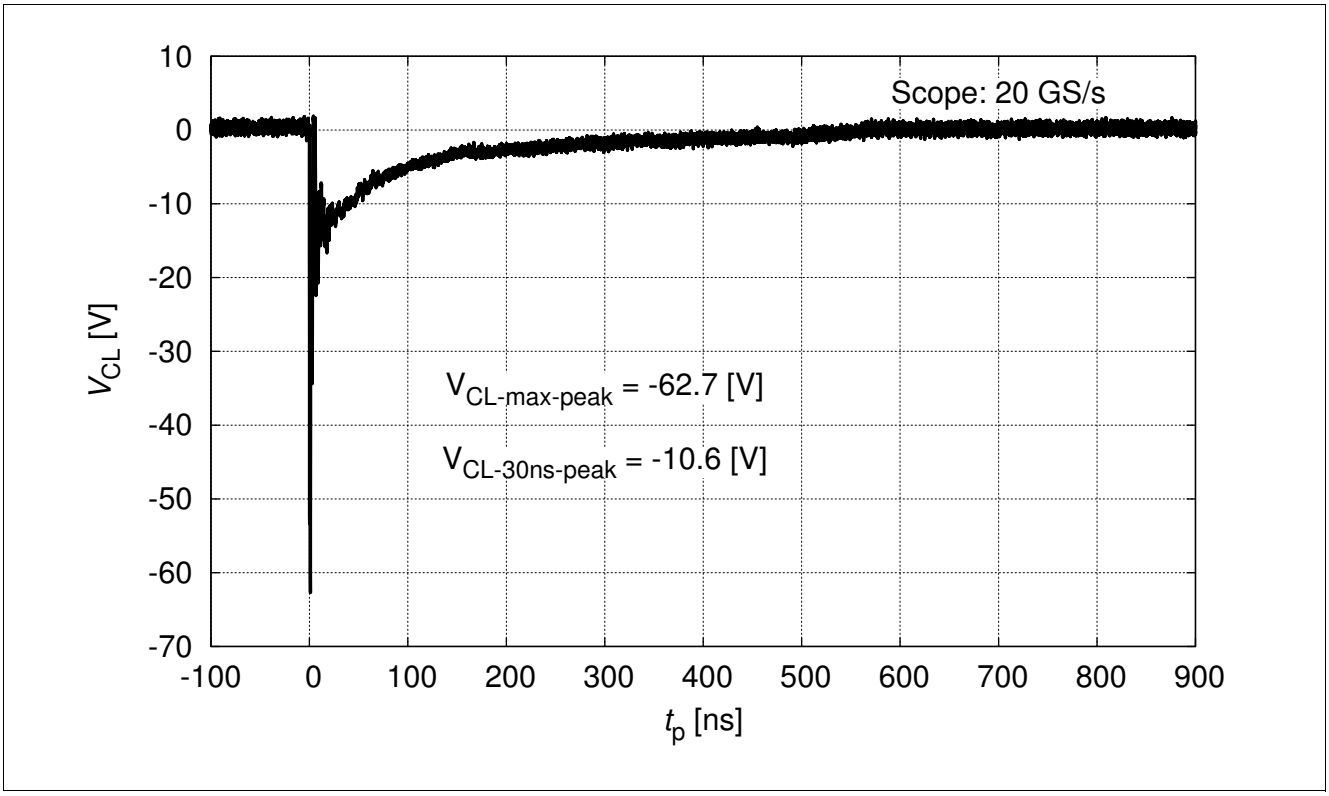

Figure 3-4 Clamping voltage at -8 kV discharge according IEC61000-4-2 (R = 330 Ω, C = 150 pF)

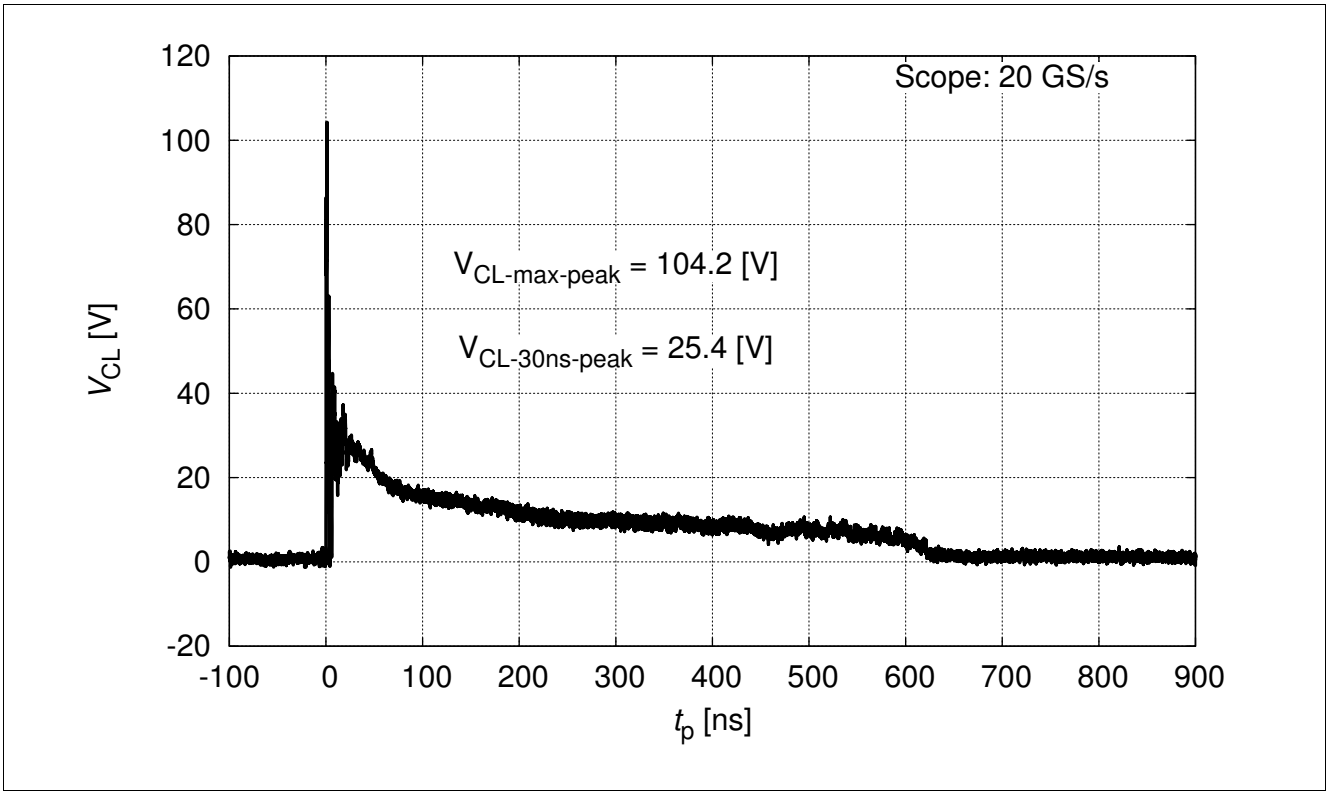

Figure 3-5 Clamping voltage at +15 kV discharge according IEC61000-4-2 (R = 330 Ohm, C = 150 pF)

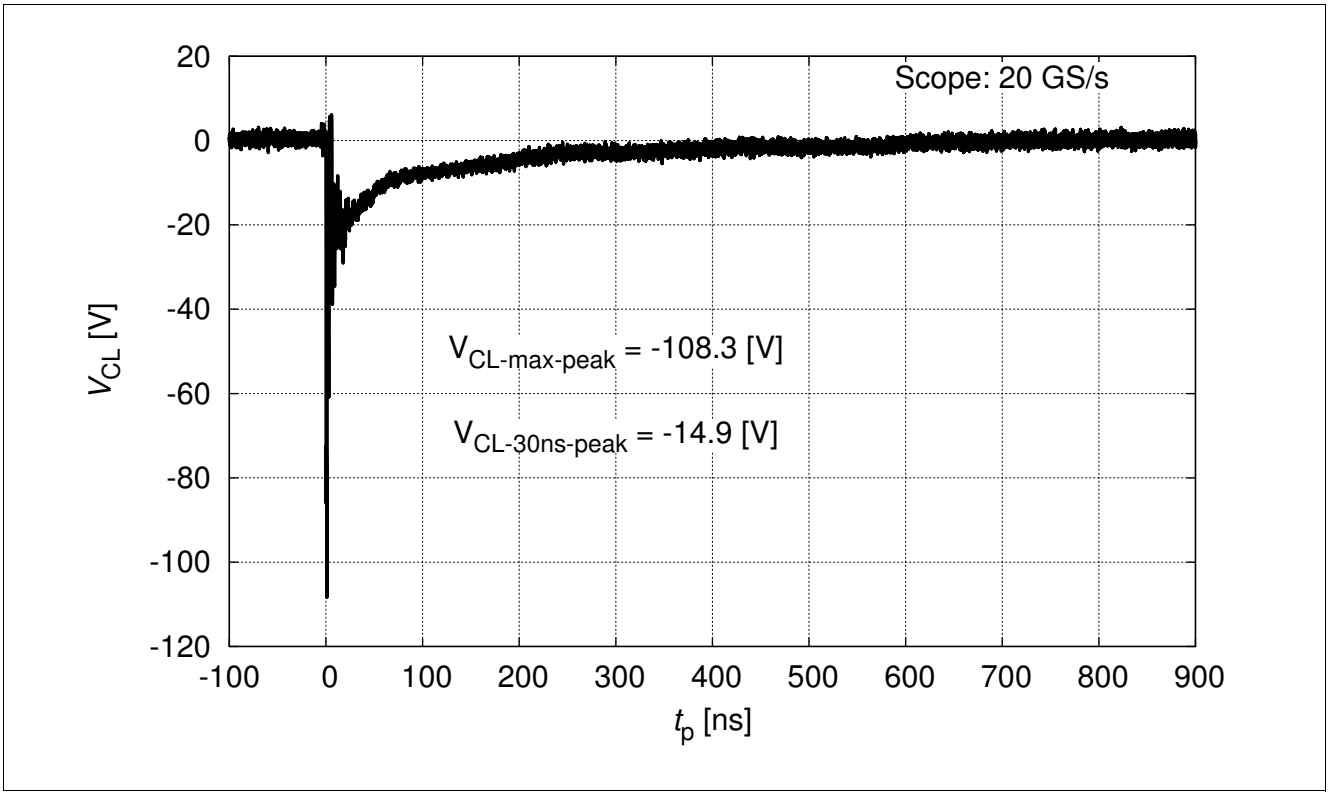

Figure 3-6 Clamping voltage at -15 kV discharge according IEC61000-4-2 (R = 330 Ω, C = 150 pF)

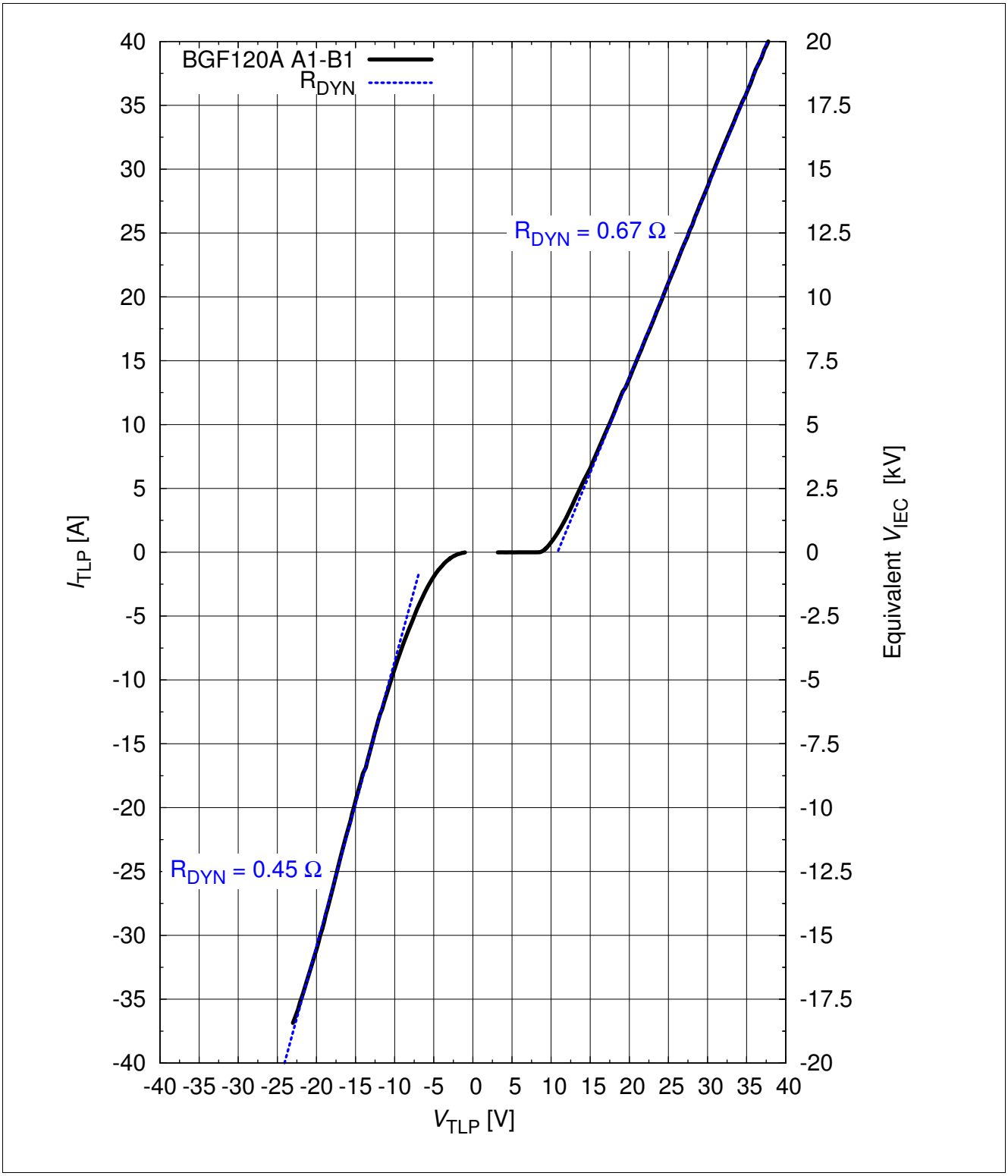

Figure 3-7 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ according ANSI/ESD STM5.5.1- Electrostatic Dischange Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 0.6 ns, I_{TLP} and V_{TLP} averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using squares fit to ELP characterisitic between I_{TLP1} = 10 A and I_{TLP2} = 30 A. Please refer to Application Note AN210 [1]

4 Application and Signal Routing

Application example for high-speed data line protection (uni-directional)

This low parasitic capacitance dual channel TVS diode array can be used either in a 2 channel uni-directional configuration or in a single channel bi-directional configuration. Due to the low capacitance and low inductance the configurations are perfect fit for ultra high-speed interfaces, such as USB2.0/3.0, S-ATA, DVI or HDMI ports.

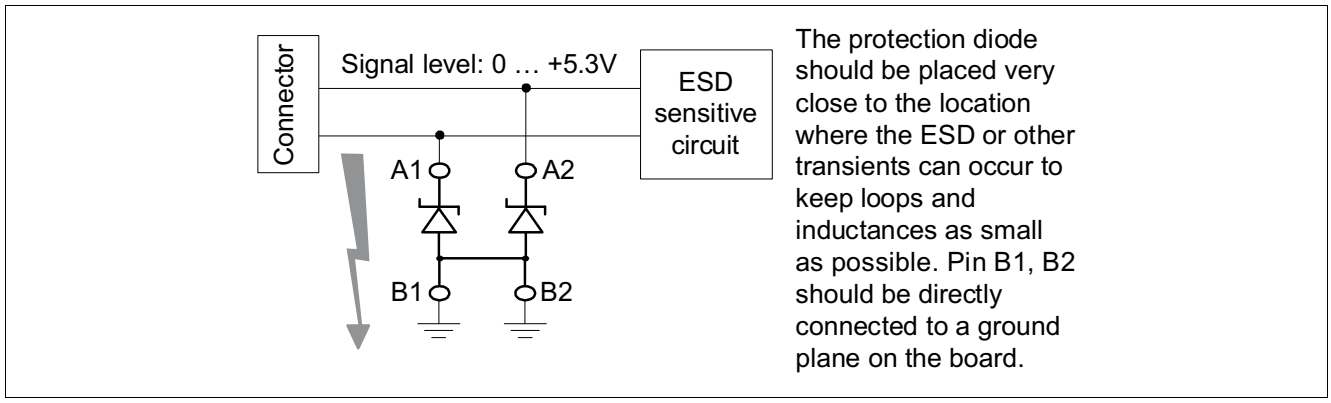

Figure 4-1 Application example for high-speed data line protection (uni-directional)

Application example for RF antenna line (bi-directional)

Connecting pin A1(A2) to the signal line and A2(A1) to GND and leaving pin B1/B2 floating even further reduces the parasitics to 0.75 pF only and correspondingly enable the user to add reliable ESD protection to RF antennas in e.g. GPS, FM radio or mobile TV applications without influence of the RF circuitry.

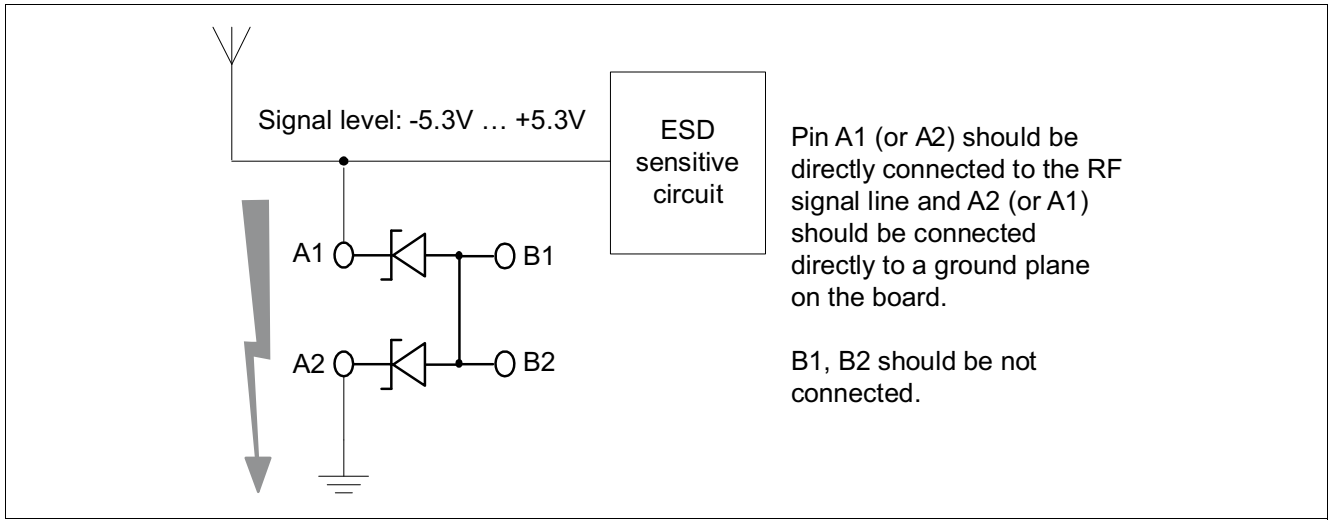

Figure 4-2 Application example for RF antenna line (bi-directional)

5 Package

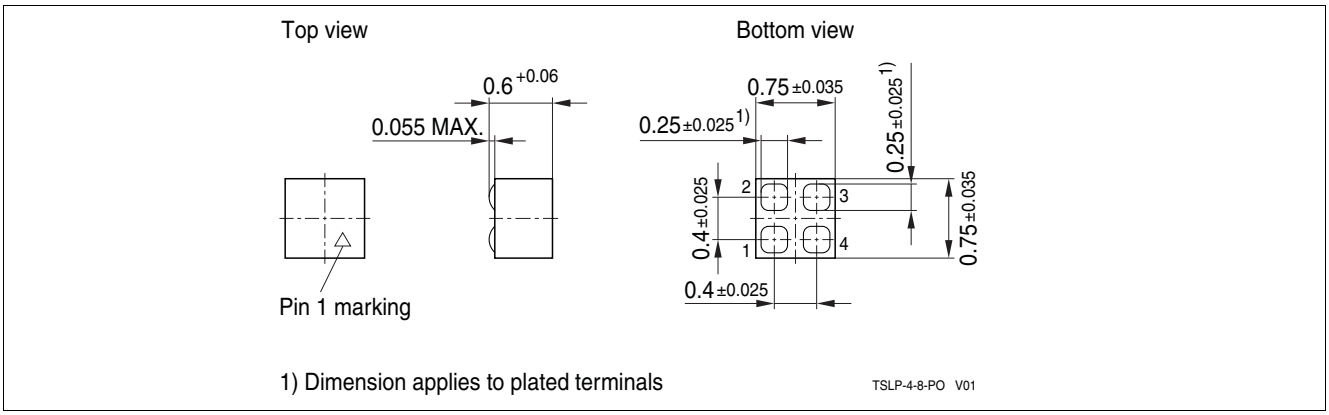

Figure 5-1 Package outline for TSLP-4-8 (dimension in mm)

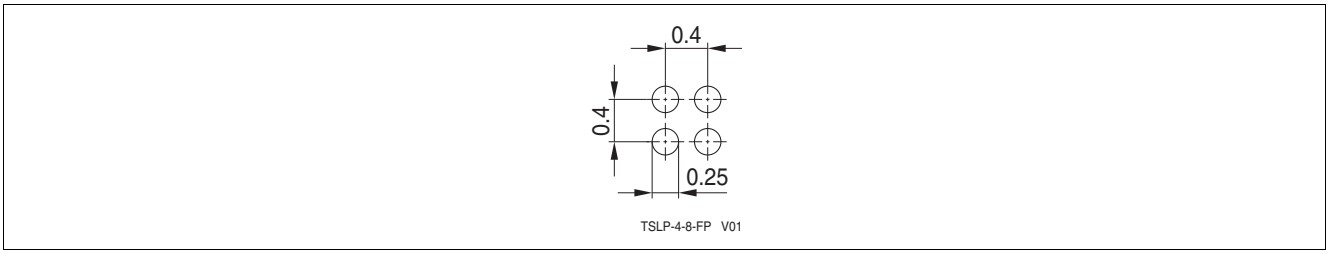

Figure 5-2 Package footprint for TSLP-4-8 (dimension in mm)

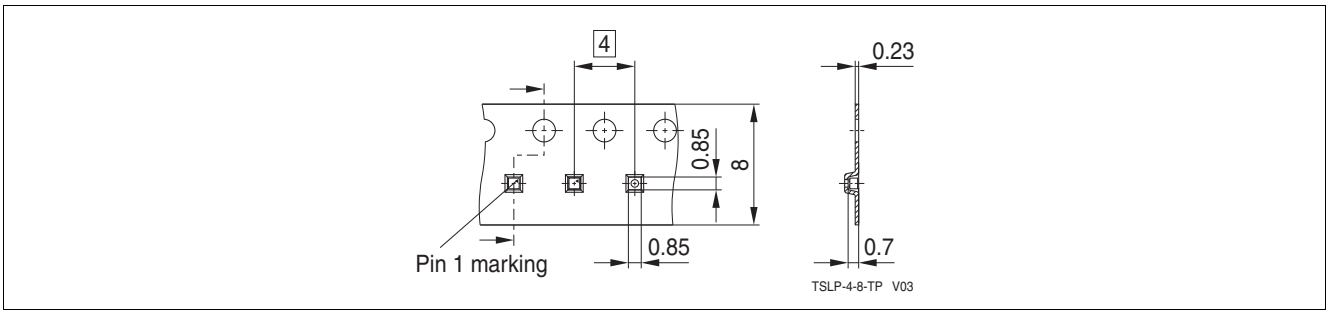

Figure 5-3 Tape and Reel Information for TSLP-4-8 (dimension in mm)

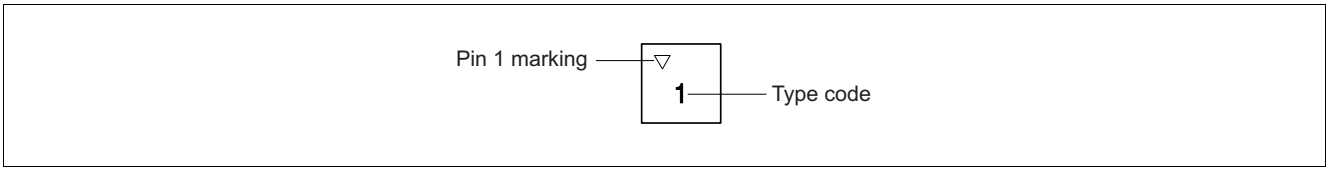

Figure 5-4 Marking (example) for TSLP-4-8

References

[1] Infineon Technologies AG, “Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology”, Application Note 210, RF and Protection Devices, April 22, 2010, Rev.1.0

[2] Infineon Technologies AG, “Recommendation for PCB Assembly of Infineon TSLP and TSSLP Packages”.

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