

SiC

Silicon Carbide Diode

5th Generation thinQ!TM

650V SiC Schottky Diode

IDL12G65C5

Final Data Sheet

Rev. 2.0, 2013-12-05

Power Management & Multimarket

5th Generation thinQ!™ SiC Schottky Diode

IDL12G65C5

1 Description

ThinQ!™ Generation 5 represents Infineon leading edge technology for the SiC Schottky Barrier diodes. The Infineon proprietary diffusion soldering process, already introduced with G3 is now combined with a new, more compact design and thin-wafer technology. The result is a new family of products showing improved efficiency over all load conditions, resulting from both the improved thermal characteristics and a lower figure of merit ($Q_c \times V_f$).

The new thinQ!™ Generation 5 has been designed to complement our 650V CoolMOS™ families: this ensures meeting the most stringent application requirements in this voltage range.

Features

- Revolutionary semiconductor material - Silicon Carbide
- Benchmark switching behavior
- No reverse recovery/ No forward recovery
- Temperature independent switching behavior
- High surge current capability
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target applications
- Breakdown voltage tested at 27 mA²⁾
- Optimized for high temperature operation

Benefits

- System efficiency improvement over Si diodes
- System cost / size savings due to reduced cooling requirements
- Enabling higher frequency / increased power density solutions
- Higher system reliability due to lower operating temperatures
- Reduced EMI

Applications

- Switch mode power supply
- Power factor correction
- Solar inverter
- Uninterruptible power supply

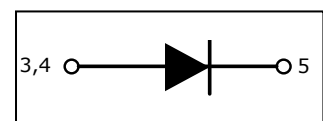
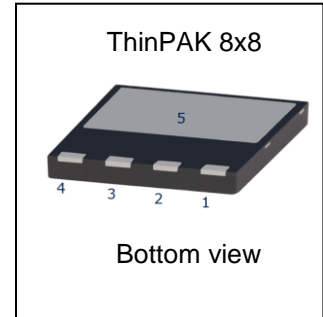
Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DC}	650	V
$Q_C; V_R=400V$	18	nC
$E_C; V_R=400V$	4.1	μJ
$I_F @ T_C < 145^\circ C$	12	A

Table 2 Pin Definition

Pin 1	Pin 2	Pin 3	Pin 4	Pin 5
n.c.	n.c.	A	A	C

Type / ordering Code	Package	Marking
IDL12G65C5	PG-VSON-4	D1265C5



Related Links

- <http://www.infineon.com/sic>
- [ThinPAK Webpage](#)
- [ThinPAK Application Note](#)

1) J-STD20 and JEDEC22

2) All devices tested under avalanche conditions for a time period of 10ms

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2 Maximum ratings

Table 3 Maximum ratings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Continuous forward current	I_F	–	–	12	A	$T_C < 145^\circ\text{C}$, $D=1$
Surge non-repetitive forward current, sine halfwave	$I_{F,SM}$	–	–	57		$T_C = 25^\circ\text{C}$, $t_p=10\text{ ms}$
		–	–	50		$T_C = 150^\circ\text{C}$, $t_p=10\text{ ms}$
Non-repetitive peak forward current	$I_{F,max}$	–	–	505		$T_C = 25^\circ\text{C}$, $t_p=10\text{ }\mu\text{s}$
i ² t value	$\int i^2 dt$	–	–	16.5	A ² s	$T_C = 25^\circ\text{C}$, $t_p=10\text{ ms}$
		–	–	12.6		$T_C = 150^\circ\text{C}$, $t_p=10\text{ ms}$
Repetitive peak reverse voltage	V_{RRM}	–	–	650	V	$T_j = 25^\circ\text{C}$
Diode dv/dt ruggedness	dv/dt	–	–	100	V/ns	$V_R=0..480\text{ V}$
Power dissipation	P_{tot}	–	–	138	W	$T_C = 25^\circ\text{C}$
Operating and storage temperature	$T_j; T_{stg}$	-55	–	150	°C	

3 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	–	0.7	0.9	K/W	SMD version, device on PCB, 6cm ² cooling area ¹⁾
Thermal resistance, junction-ambient	R_{thJA}	–	–	45		

1) Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70μm) for drain connection. PCB is vertical without air stream cooling.

4 Electrical characteristics

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
DC blocking voltage	V_{DC}	650	–	–	V	$I_R = 0.19 \text{ mA}, T_j = 25^\circ\text{C}$
Diode forward voltage	V_F	–	1.5	1.7		$I_F = 12 \text{ A}, T_j = 25^\circ\text{C}$
		–	1.8	2.1		$I_F = 12 \text{ A}, T_j = 150^\circ\text{C}$
Reverse current	I_R	–	0.65	190	μA	$V_R = 650 \text{ V}, T_j = 25^\circ\text{C}$
		–	0.16	68		$V_R = 600 \text{ V}, T_j = 25^\circ\text{C}$
		–	2.4	1350		$V_R = 650 \text{ V}, T_j = 150^\circ\text{C}$

Table 6 AC characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Total capacitive charge	Q_c	–	18	–	nC	$V_R = 400 \text{ V}, di/dt = 200 \text{ A}/\mu\text{s}, I_F \leq I_{F,MAX}, T_j = 150^\circ\text{C}.$
Total Capacitance	C	–	360	–	pF	$V_R = 1 \text{ V}, f = 1 \text{ MHz}$
		–	48	–		$V_R = 300 \text{ V}, f = 1 \text{ MHz}$
		–	47	–		$V_R = 600 \text{ V}, f = 1 \text{ MHz}$

5 Electrical characteristics diagrams

Table 7

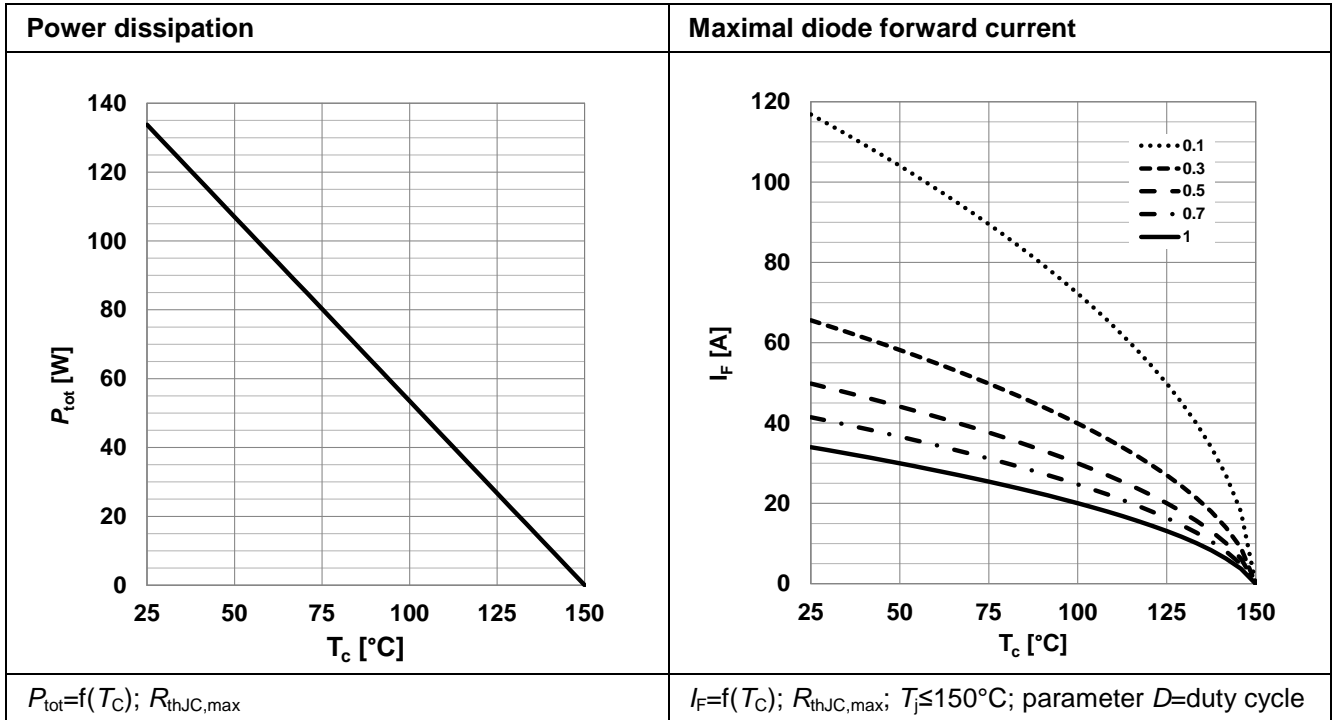


Table 8

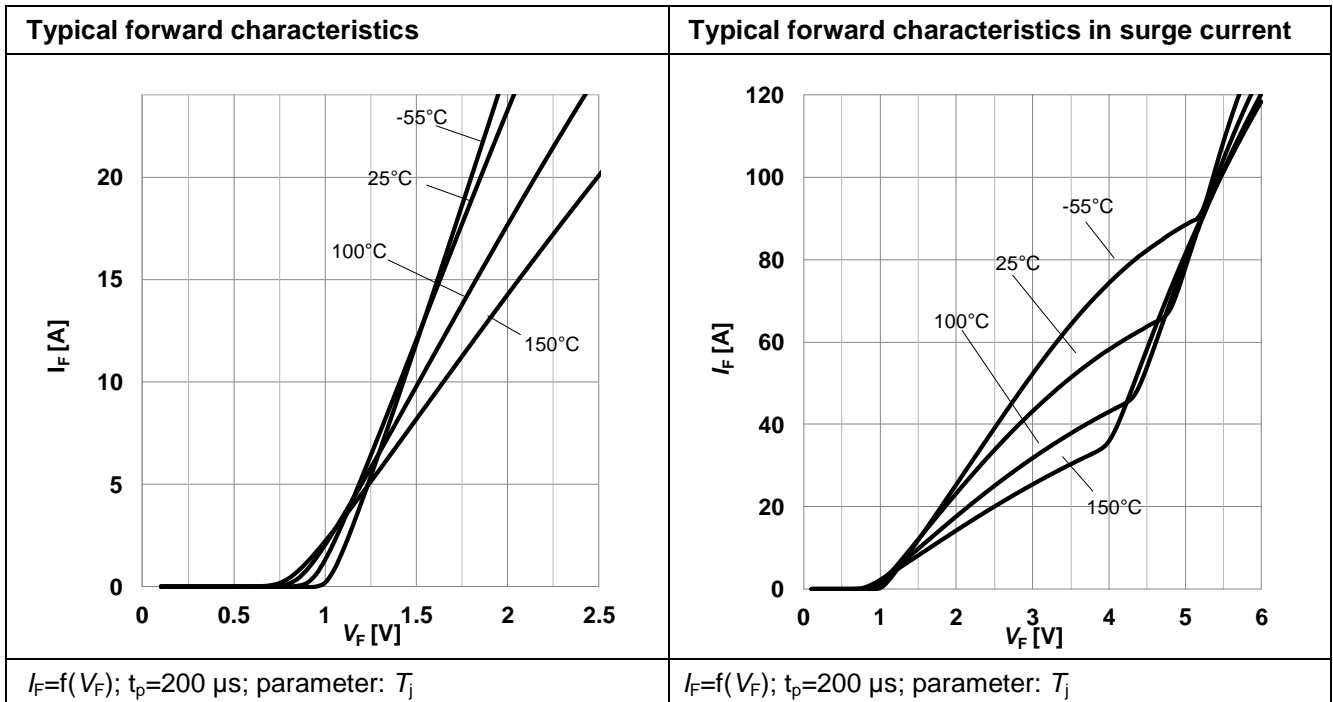


Table 9

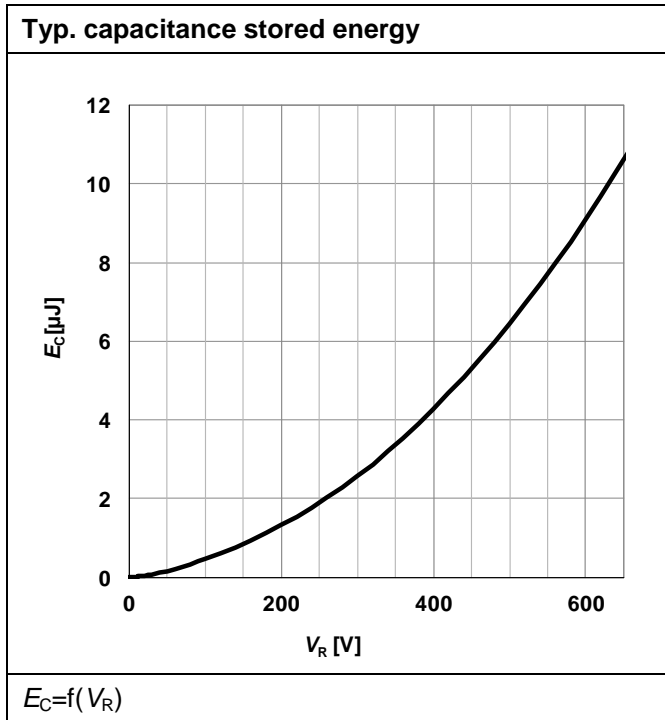
Typ. capacitance charge vs. current slope ¹⁾	Typ. reverse current vs. reverse voltage
$Q_C=f(dI_F/dt); T_j=150^\circ\text{C}; V_R=400\text{ V}; I_F \leq I_{F,max}$	$I_R=f(V_R); \text{parameter: } T_j;$

1) Only capacitive charge, guaranteed by design.

Table 10

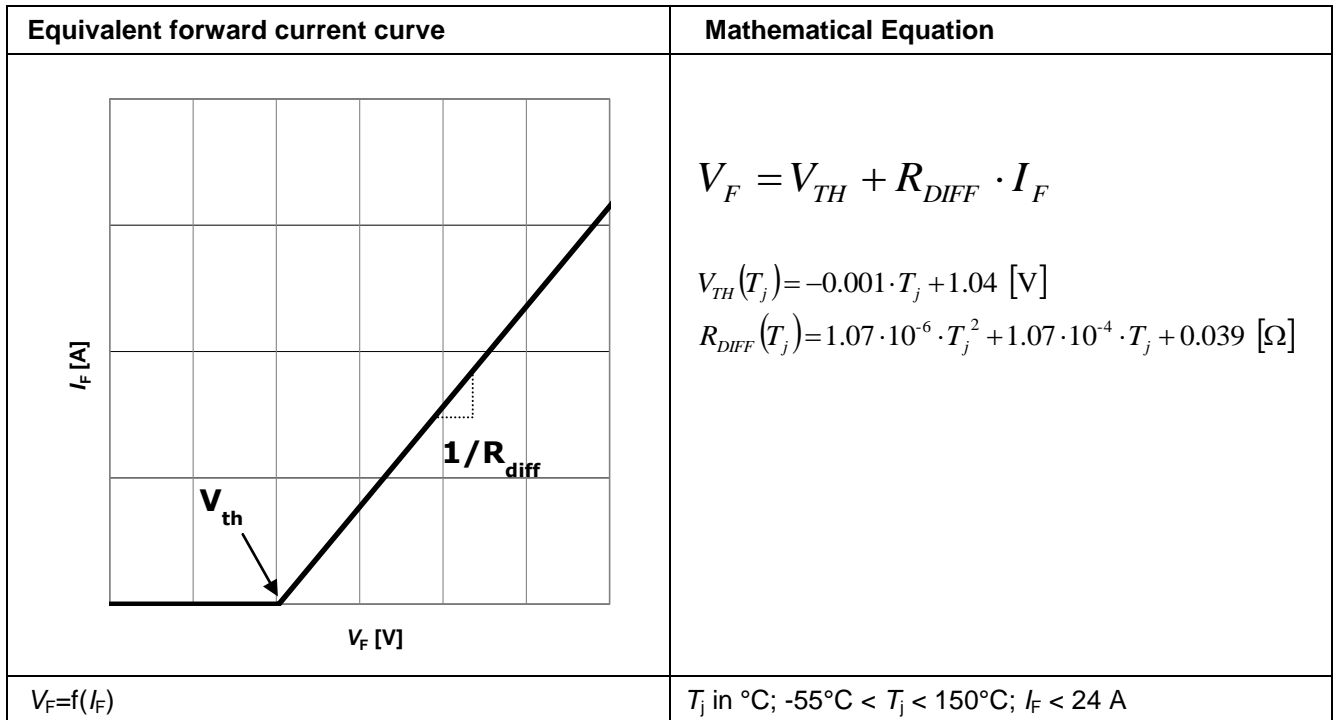
Max. transient thermal impedance	Typ. capacitance vs. reverse voltage
$Z_{th,jc}=f(t_p); \text{parameter: } D=t_p/T$	$C=f(V_R); T_j=25^\circ\text{C}; f=1\text{ MHz}$

Table 11



6 Simplified Forward Characteristics Model

Table 12



7 Package outlines

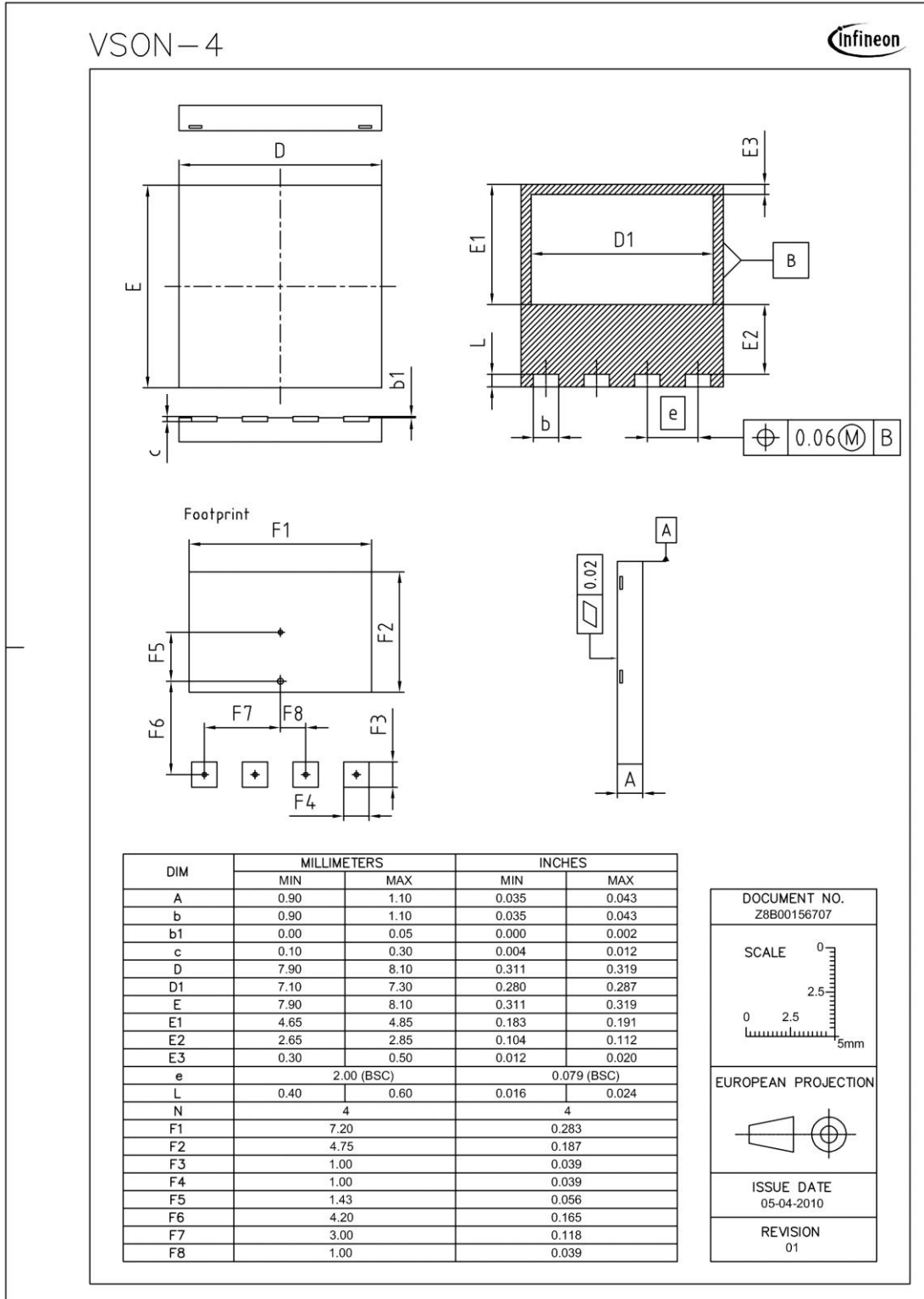


Figure 1 Outlines ThinPAK 8x8, dimensions in mm/inches

8 Revision History

5th Generation thinQ!TM SiC Schottky Diode

Revision History: 2013-12-05, Rev. 2.0

Previous Revision:

Revision	Subjects (major changes since last version)
2.0	Release of the data sheet

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