

MOSFET

600V CoolMOS™ G7 SJ Power Device

The C7 GOLD series (G7) for the first time brings together the benefits of the C7 GOLD CoolMOS™ technology, 4 pin Kelvin Source capability and the improved thermal properties of the DDPAK package to enable a possible SMD solution for high current topologies such as PFC up to 3kW.

Features

- C7 Gold gives best in class FOM $R_{DS(on)} * E_{oss}$ and $R_{DS(on)} * Q_g$.
- Suitable for hard and soft switching (PFC and high performance LLC)
- C7 Gold technology enables best in class $R_{DS(on)}$ in smallest footprint.
- DDPAK package has inbuilt 4th pin Kelvin Source configuration and low parasitic source inductance (~3nH).
- DDPAK package is MSL1 compliant, total Pb-free and has easy visual inspection leads.
- DDPAK SMD package combined with lead free die attach process enables improved thermal performance (R_{th}).

Benefits

- C7 Gold FOM $R_{DS(on)} * Q_g$ is 15% better than previous C7 600V enabling faster switching leading to higher efficiency.
- Possibility to increase economies of scales by usage in PFC and PWM topologies in the application.
- C7 Gold can reach 50mΩ in DDPAK 115mm² footprint, whereas previous BIC C7 600V was 40mΩ in 150mm² D²PAK footprint.
- Reducing parasitic source inductance by Kelvin Source improves efficiency by faster switching and ease of use due to less ringing.
- DDPAK package is easy to use and has the highest quality standards.
- Improved thermals enable SMD DDPAK package to be used in higher current designs than has been previously possible.

Potential applications

PFC stages and PWM stages (TTF, LLC) for high power/performance SMPS e.g. Computing, Server, Telecom, UPS and Solar.

Product validation

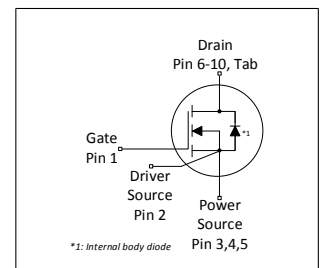
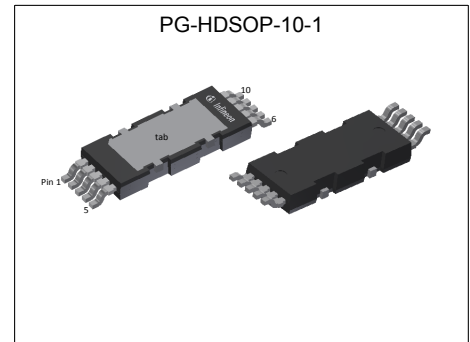
Fully qualified according to JEDEC for Industrial Applications

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS@T_{j,max}}$	650	V
$R_{DS(on),max}$	102	mΩ
$Q_{g,typ}$	34	nC
$I_{D,pulse}$	66	A
$I_{D,continuous}$ @ $T_j < 150^\circ C$	32	A
$E_{oss@400V}$	4	μJ
Body diode di/dt	740	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPDD60R102G7	PG-HDSOP-10	60R102G7	see Appendix A



RoHS

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1 Maximum ratings

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	23 15	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	66	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	78	mJ	$I_D=4.4\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.39	mJ	$I_D=4.4\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	4.4	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	139	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	n.a.	Ncm	-
Continuous diode forward current	I_S	-	-	23	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	66	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	25	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 6.7\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di/dt	-	-	740	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 6.7\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.9	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm ² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Reflow soldering temperature	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	$V_{DS}=V_{GS}, I_D=0.39mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=600V, V_{GS}=0V, T_j=25^\circ\text{C}$ $V_{DS}=600V, V_{GS}=0V, T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.088 0.220	0.102 -	Ω	$V_{GS}=10V, I_D=7.8A, T_j=25^\circ\text{C}$ $V_{GS}=10V, I_D=7.8A, T_j=150^\circ\text{C}$
Gate resistance	R_G	-	0.8	-	Ω	$f=1\text{MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1320	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250\text{kHz}$
Output capacitance	C_{oss}	-	27	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250\text{kHz}$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	50	-	pF	$V_{GS}=0V, V_{DS}=0\dots400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	516	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0\dots400V$
Turn-on delay time	$t_{d(on)}$	-	18	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=7.8A,$ $R_G=5.3\Omega$; see table 9
Rise time	t_r	-	5	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=7.8A,$ $R_G=5.3\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	60	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=7.8A,$ $R_G=5.3\Omega$; see table 9
Fall time	t_f	-	4	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=7.8A,$ $R_G=5.3\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{GS}	-	7	-	nC	$V_{DD}=400V, I_D=7.8A, V_{GS}=0$ to 10V
Gate to drain charge	Q_{gd}	-	12	-	nC	$V_{DD}=400V, I_D=7.8A, V_{GS}=0$ to 10V
Gate charge total	Q_g	-	34	-	nC	$V_{DD}=400V, I_D=7.8A, V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	5.0	-	V	$V_{DD}=400V, I_D=7.8A, V_{GS}=0$ to 10V

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.8	-	V	$V_{GS}=0V, I_F=7.8A, T_j=25^\circ C$
Reverse recovery time	t_{rr}	-	305	-	ns	$V_R=400V, I_F=7.8A, di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	3.1	-	μC	$V_R=400V, I_F=7.8A, di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	22	-	A	$V_R=400V, I_F=7.8A, di_F/dt=100A/\mu s$; see table 8

4 Electrical characteristics diagrams

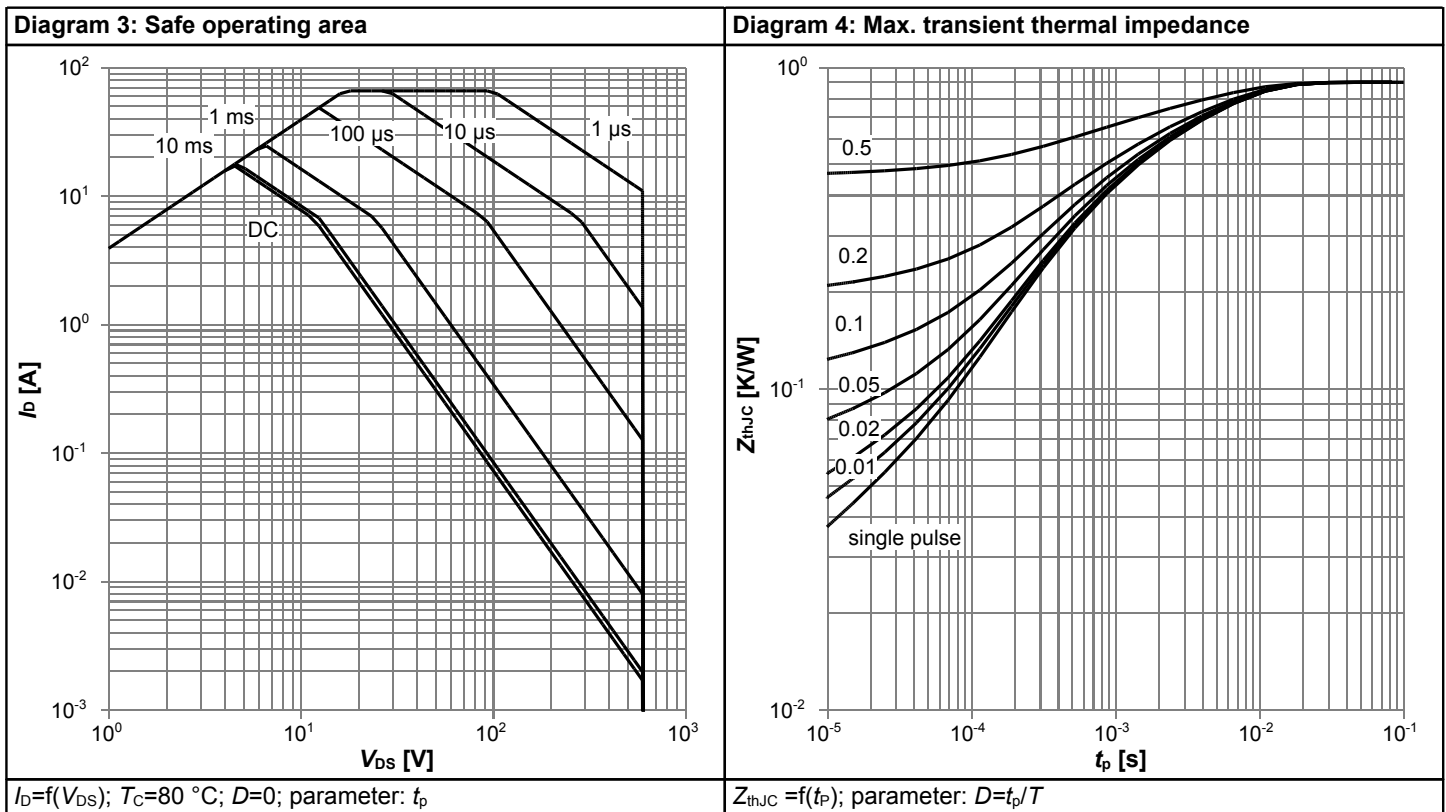
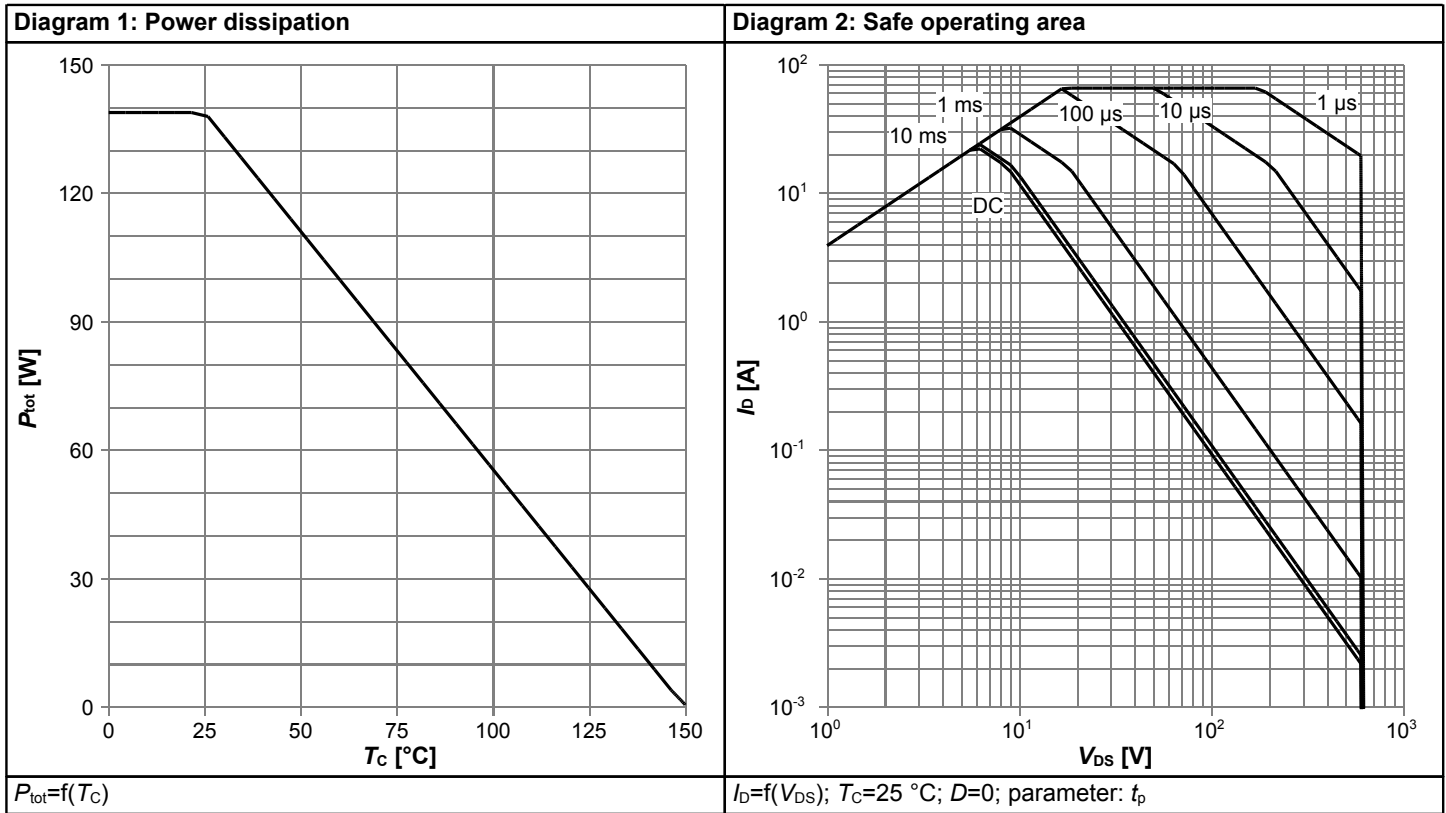
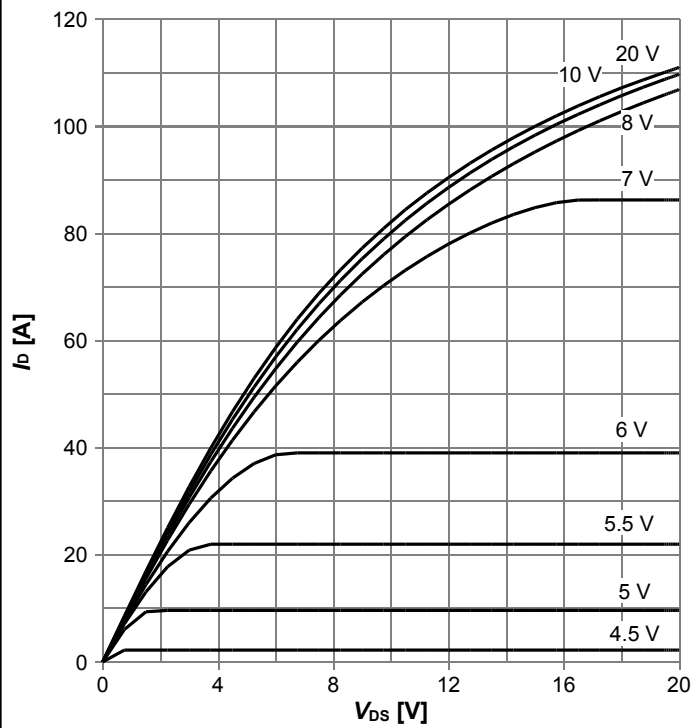
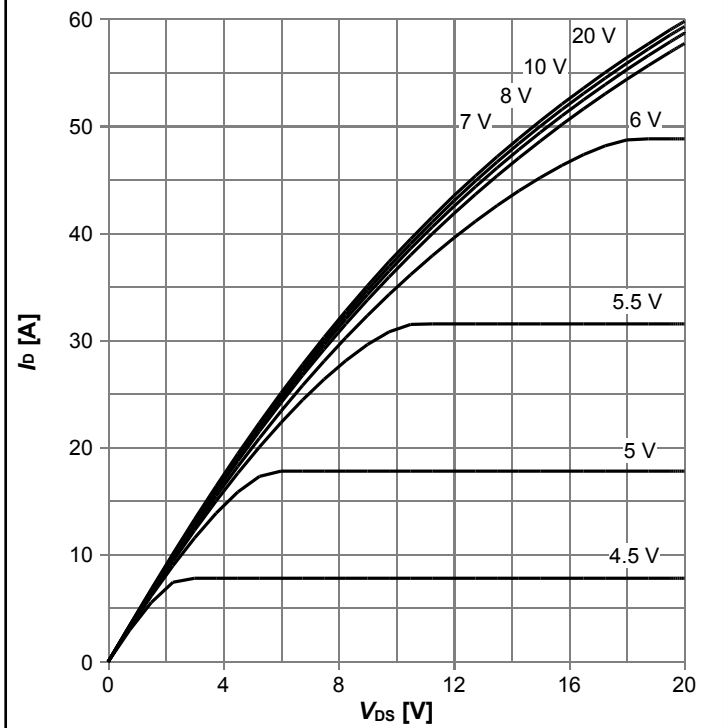


Diagram 5: Typ. output characteristics



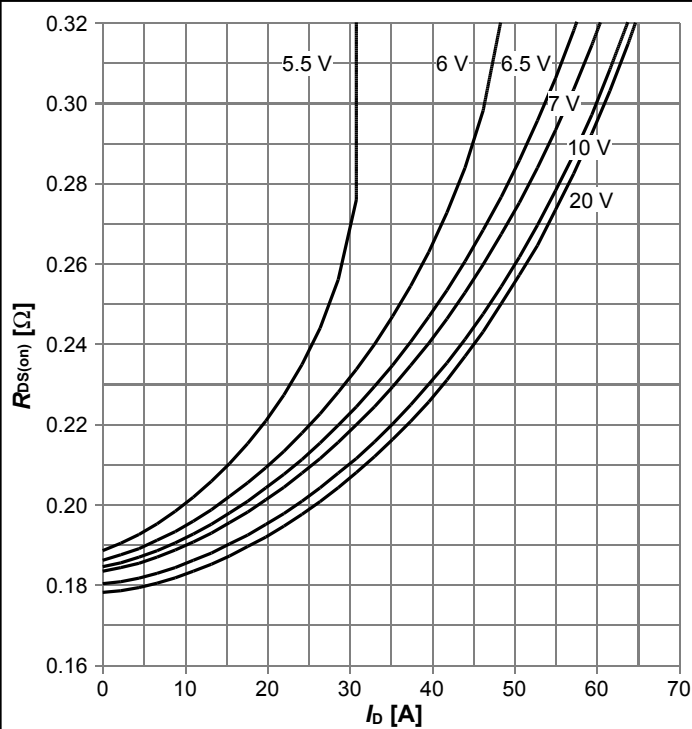
$I_D = f(V_{DS})$; $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



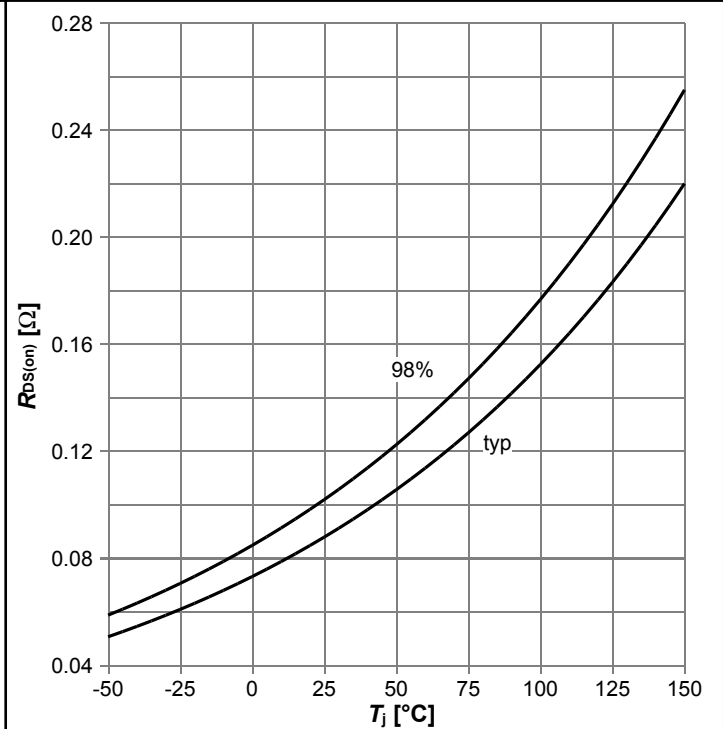
$I_D = f(V_{DS})$; $T_j = 125\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



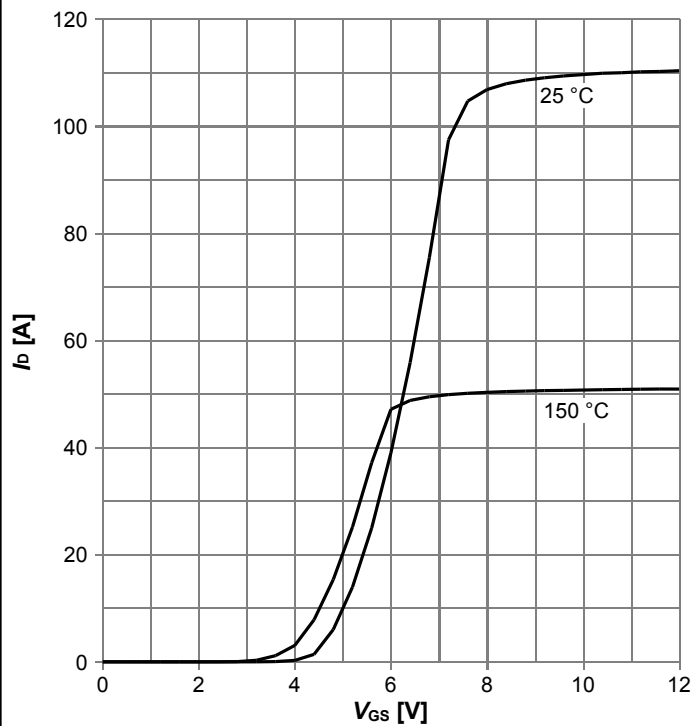
$R_{DS(on)} = f(I_D)$; $T_j = 125\text{ °C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



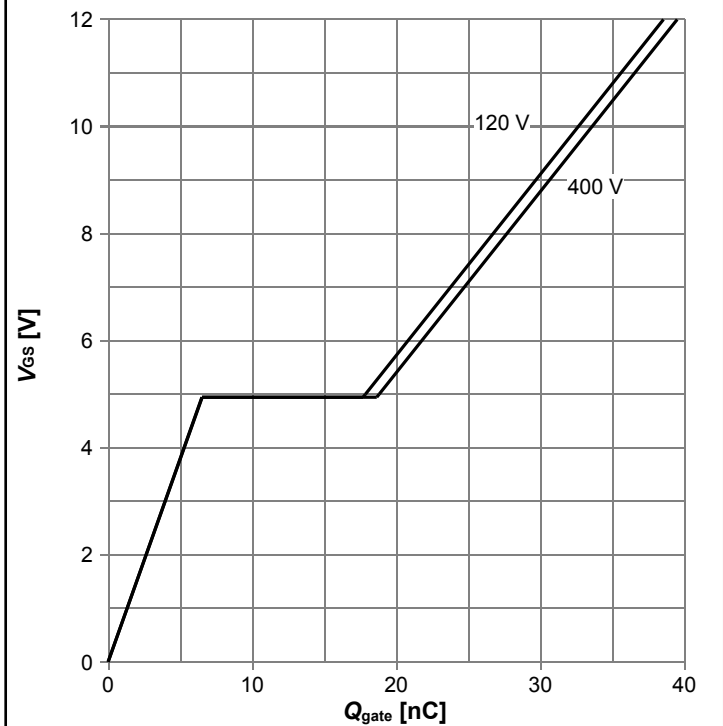
$R_{DS(on)} = f(T_j)$; $I_D = 7.8\text{ A}$; $V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics



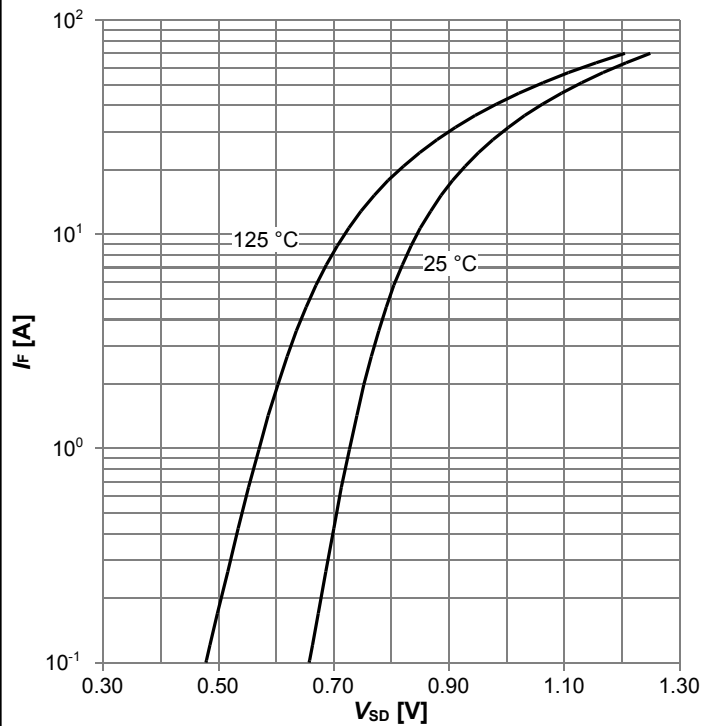
$I_D = f(V_{GS})$; $V_{DS} = 20V$; parameter: T_j

Diagram 10: Typ. gate charge



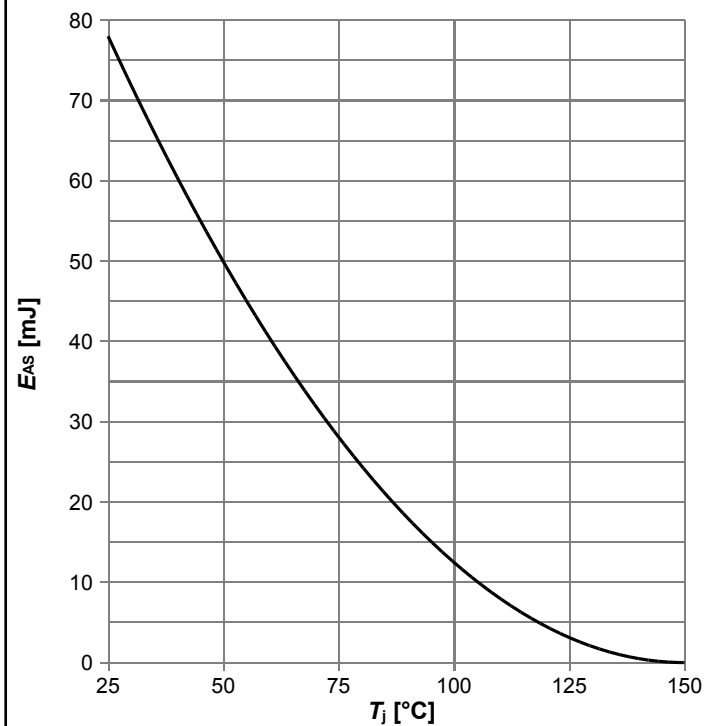
$V_{GS} = f(Q_{gate})$; $I_D = 7.8$ A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



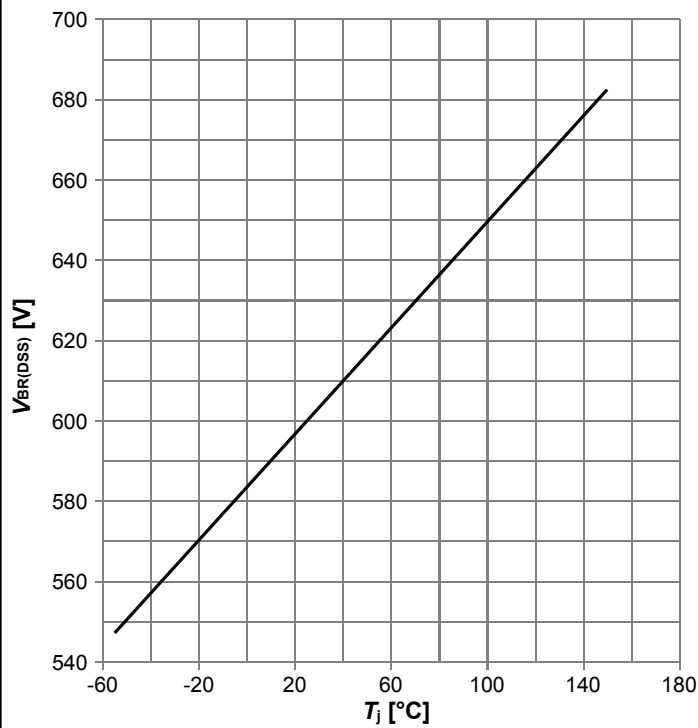
$I_F = f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



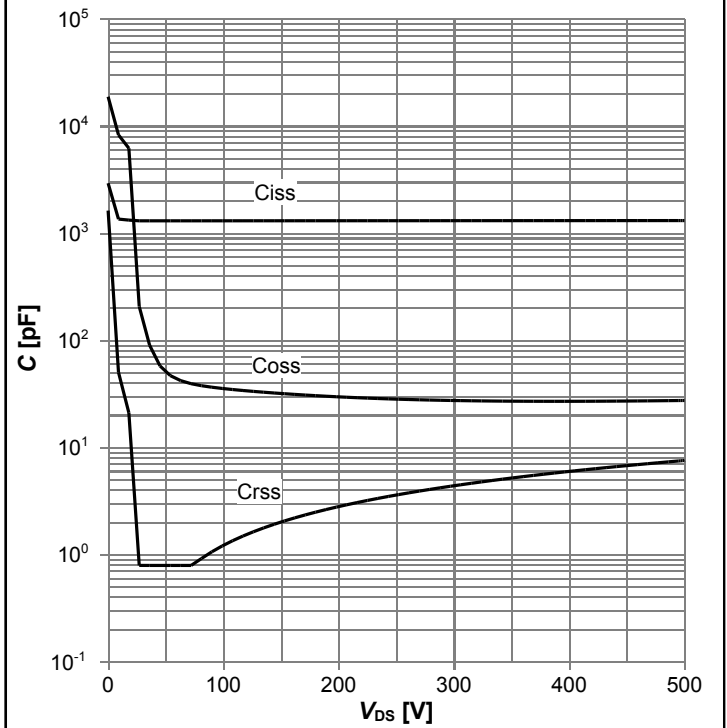
$E_{AS} = f(T_j)$; $I_D = 4.4$ A; $V_{DD} = 50$ V

Diagram 13: Drain-source breakdown voltage



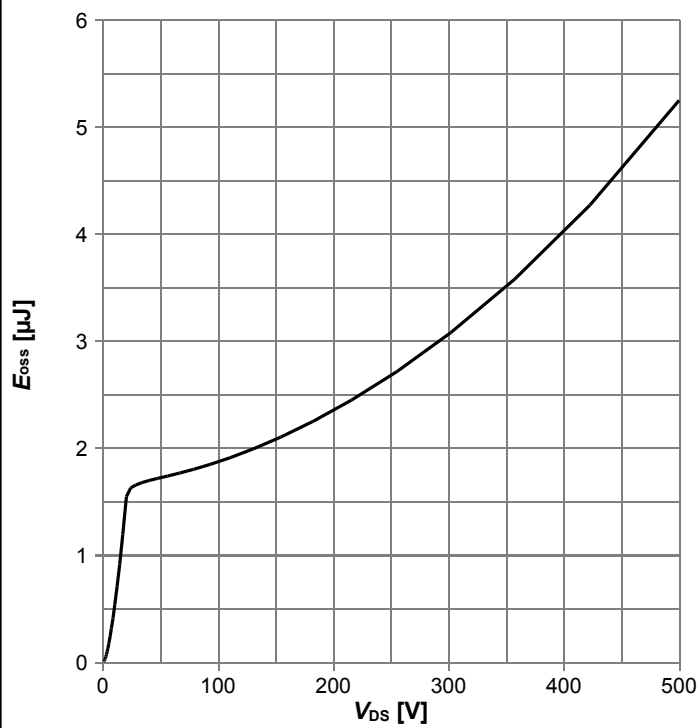
$V_{BR(DSS)}=f(T_j); I_D=1\text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=250\text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics



Table 9 Switching times



Table 10 Unclamped inductive load



6 Package Outlines

PG-HDSOP-10-1

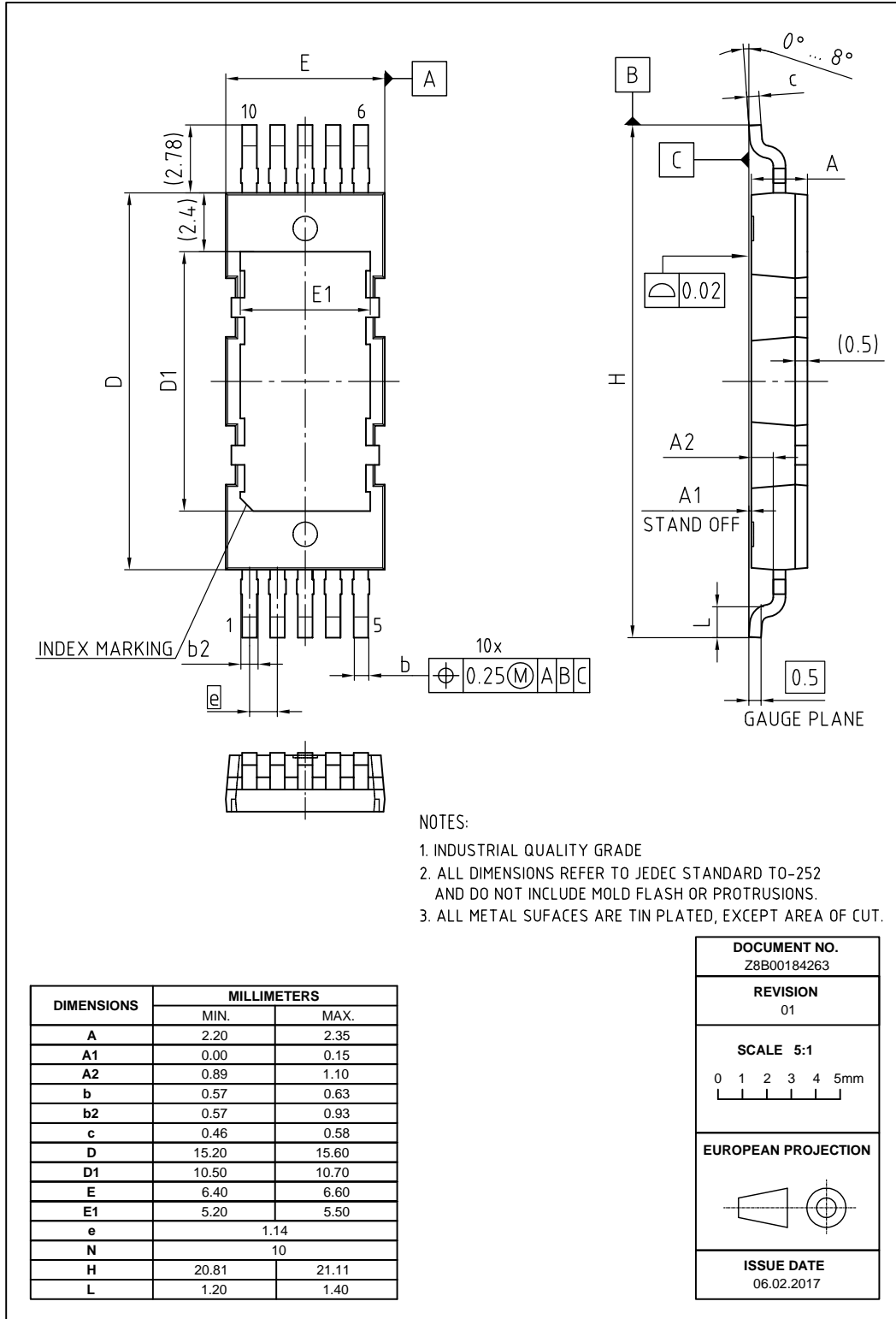


Figure 1 Outline PG-HDSOP-10, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- IFX CoolMOS™ G7 Webpage: www.infineon.com
- IFX CoolMOS™ G7 application note: www.infineon.com
- IFX CoolMOS™ G7 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPDD60R102G7

Revision: 2020-10-27, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2018-01-05	Release of final version
2.1	2020-10-27	Content update diagram 2,3,4,7,8 and format update

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