3300 W CCM bi-directional totem pole with 650 V CoolSiC™ and XMC™

EVAL_3K3W_TP_PFC_SIC

About this document

Authors

Matteo-Alessandro Kutschak

David Meneses Herrera

Scope and purpose

This document presents a system solution based on Infineon superjunction (SJ) (CoolMOS™) and wide band-gap (CoolSiC™) power semiconductors, drivers and microcontroller for a bridgeless totem-pole Power Factor Corrector (PFC) with bi-directional capability. The EVAL_3K3W_TP_PFC_SIC board is intended for those applications which require the highest efficiency (99 percent) and high power density (73 W/in^3), such as high-end servers and telecoms. In addition, the bi-directional power flow capability would allow this design to be used in battery chargers or battery formation applications. The totem pole implemented in the EVAL_3K3W_TP_PFC_SIC board operates in Continuous Conduction Mode (CCM) in both rectifier (PFC) and inverter mode, with full digital control implementation on the Infineon XMC™ 1000 series microcontroller.

The Infineon components used in the 3300 W bridgeless bi-directional totem-pole board are as follows:

- 600 V CoolMOS™ C7 SJ MOSFET and 650 V CoolSiC™ silicon carbide MOSFET
- 2EDF7275F isolated gate drivers (EiceDRIVER™)
- XMC1404 microcontroller
- ICE5QSAG CoolSET™ QR Flyback controller
- 950 V CoolMOS™ P7 SJ MOSFET

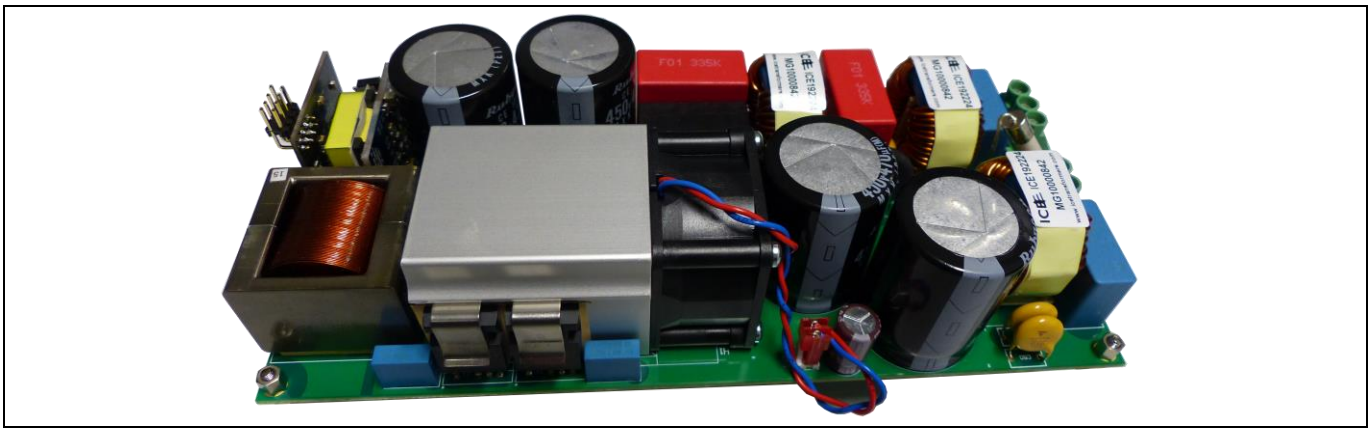

Figure 1 3300 W bridgeless totem-pole PFC with CoolSiC™, CoolMOS™ and XMC™ control

Table of contents

1 System description

The EVAL_3K3W_TP_PFC_SIC board is a system solution enabled by Infineon Technologies power semiconductors as well as drivers and microcontroller. The evaluation board consists of a bridgeless totem-pole topology and it is intended for high-end applications in which the highest efficiency is required. Furthermore, the totem-pole topology is simple and offers a reduced part count and full utilization of the PFC inductor and switches [1]. For these reasons, totem-pole PFC enables high power density at a limited system cost for high-performance systems. In addition, the EVAL_3K3W_TP_PFC_SIC board provides reverse power flow (inverter operation for grid-connected applications) due to the inherent bi-directional power flow capability of the totem-pole topology.

The totem-pole topology in PFC applications with CCM operation is feasible by using wide band-gap semiconductors [1]. In this case, the Infineon CoolSiC™ MOSFET in TO-247 four-pin package is used to push the efficiency to 99 percent at half-load (Figure 2). The converter operates exclusively at high-line (176 Vrms minimum, 230 Vrms nominal) in CCM with 65 kHz switching frequency.

Note: Due to production variations and measurement set-up, efficiency variations up to ±0.2 percent can be seen in the result shown.

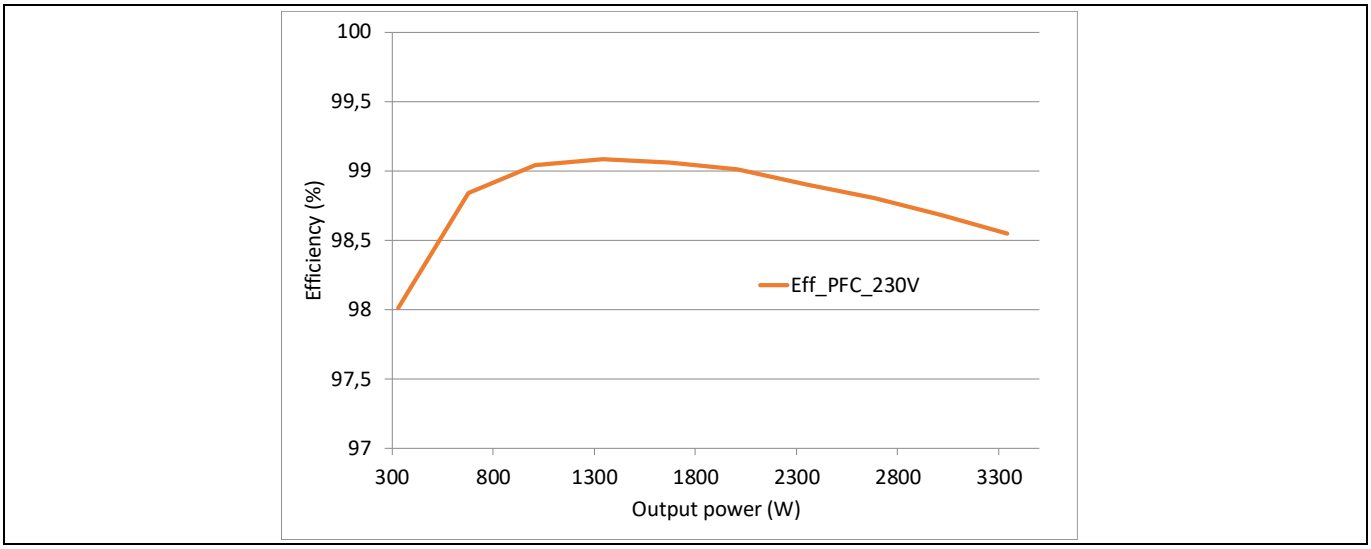

Figure 2 Measured efficiency at 230 V (with applied line filter in the power analyzer) of the 3300 W totem-pole PFC with 64 mΩ CoolSiC™ and 17 mΩ CoolMOS™

The PFC function to achieve bulk voltage regulation while demanding high-quality current from the grid is implemented with an Infineon XMC1404 microcontroller [2]. Further detail on PFC control implementation in the XMC™ 1000 family can be found in the application notes of other Infineon PSU and PFC evaluation boards with classic boost or dual boost topologies [3][4][5].

The 3300 W bridgeless bi-directional (PFC/AC-DC and inverter/AC-DC) totem-pole presented in this application note is a system solution developed with Infineon power semiconductors as well as Infineon drivers and controllers. The Infineon devices used in the implementation of the EVAL_3K3W_TP_PFC_SIC board are listed below.

- 64 mΩ 650 V CoolSiC™ (IMZA65R048M1) in TO-247 four-pin package, as totem-pole PFC high-frequency switches

- 17 mΩ 600 V CoolMOS™ C7 (IPW60R017C7) in TO-247 package, for the totem-pole PFC return path (low-frequency bridge)
- 2EDF7275F isolated gate drivers (EiceDRIVER™)
- ICE5QSAG QR Flyback controller and 950 V CoolMOS™ P7 (IPU95R3K7P7) for the bias auxiliary supply
- XMC1404 microcontroller for PFC control implementation

A simplified block diagram of the bridgeless topology with the mentioned devices from the Infineon portfolio is shown in Figure 3. The diode bridge in front of the totem-pole PFC converter is meant to be a current path for start-up or surge conditions and it is not part of the current path during the steady-state converter operation. The power flow direction, which will select the converter operation – forward power flow or PFC operation versus reverse power flow or inverter operation – can be selected by a switch connected to the XMC™ microcontroller as a digital input pin.

Note: *The power flow or operation mode is selected before the application starts and the power flow cannot be reverted during operation. Therefore, the EVAL_3K3W_TP_PFC_SIC board is able to operate as either PFC or inverter but the current version of the SW does not provide dynamic change of operation mode.*

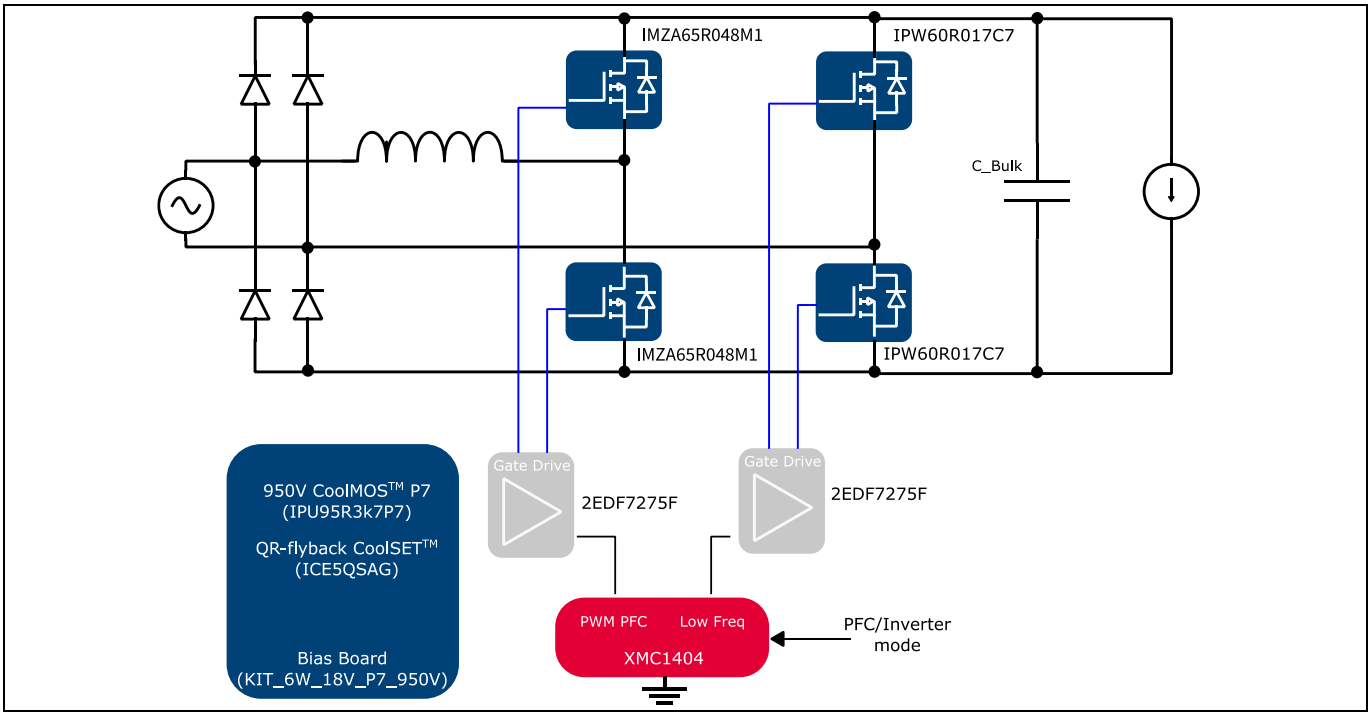

Figure 3 **3300 W bridgeless totem-pole PFC board (EVAL_3K3W_TP_PFC_SIC) simplified diagram showing the topology and the Infineon semiconductors used**

This document will describe the EVAL_3K3W_TP_PFC_SIC board implementation, as well as the specifications and main test results. For further information on Infineon semiconductors visit the Infineon website, the Infineon evaluation board search, and the websites for the different implemented components:

- CoolMOS™ power MOSFET
- CoolSiC™ MOSFET
- Gate driver ICs
- QR CoolSET™ (bias board KIT_6W_18V_P7_950V)
- XMC™ microcontrollers

1.1 Board description

Figure 4 shows the placement of the different sections of the EVAL_3K3W_TP_PFC_SIC bridgeless totem-pole bi-directional PFC with Infineon 650 V CoolSiC™ silicon carbide MOSFET. The board is 208 mm long, with a width of 89 mm and a height of 40 mm (1U), for a power density of 73 W/in^3.

Inmediately after the AC input connector, a two-stage EMI filter is placed as well as a fuse and NTC in-rush current limiter, together with the input relay. The DC output connector is placed on the same side of the board as the AC connector. Close to the output connector, a single-stage filter (with differential and common mode paths) is placed to guarantee proper aquisition of the output variables in efficiency measurements.

On the other side of the board, two daughter cards are introduced. They are the bias board and the control card. The bias board uses a QR CoolSET™ controller and 950 V P7 CoolMOS™ switch to generate the required voltages for the control card, driving, relay and fan supply. The control card implements the required current, voltage and polarity sensing. The full digital control is implemented in the Infineon XMC™ microcontroller, which is in charge of the proper operation of the bridgeless totem-pole topology.

The rest of the board is occupied by the bridgeless totem-pole itself, which comprises the PFC choke, the bulk capacitor and a bridge with 650 V CoolSiC™ MOSFET and 600 V C7 CoolMOS™. The bulk capacitance is designed to comply with the hold-up time shown in Table 1. The semiconductors in TO-247 package are mounted on a heatsink with attached fan, which blows air toward the PFC choke. The choke is designed with high-flux material in EQ shape in order to comply with the height requirement, high efficiency performance and high power density.

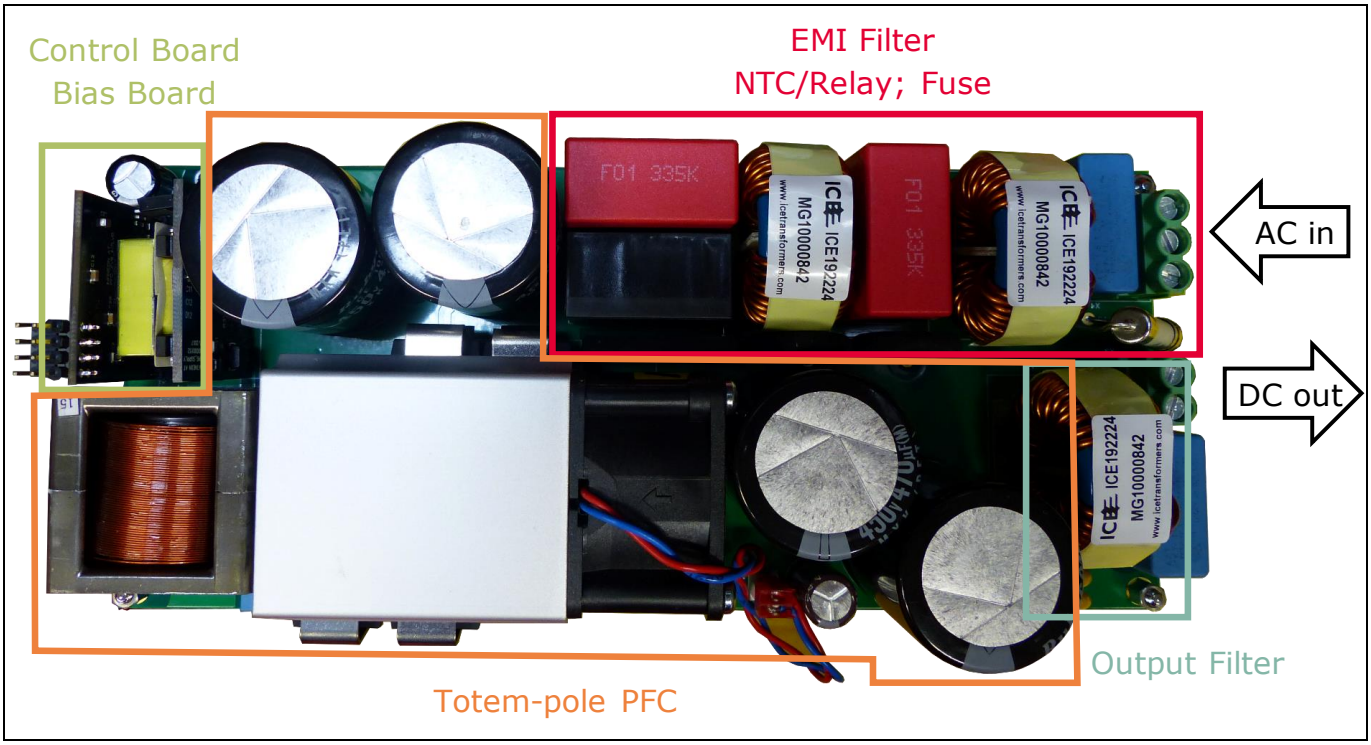

Figure 4 Placement of the different sections in the 3300 W bridgeless totem-pole PFC with Infineon 650 V CoolSiC™ and 600 V C7 CoolMOS™ MOSFETs and XMC™ control

1.2 Signal conditioning for digital control of totem-pole CCM PFC

The evaluation board EVAL_3K3W_TP_PFC_SIC implements CCM average current mode control with Duty Feed-Forward (DFF) for both PFC and inverter operation. It follows a control structure similar to that implemented for a classic PFC presented in [2] and [4] or the dual boost introduced in [5].

Unlike the classic PFC in which the AC voltage is rectified by the diode bridge, in the bridgeless totem-pole PFC converter the inductor current is both positive and negative. The most simple and cost-effective way to sense this current is to use a shunt resistor in series with the inductor as shown in Figure 5. In addition, in the EVAL_3K3W_TP_PFC_SIC board, the control reference (GND_iso in Figure 5) is placed in the AC-line after the shunt resistor. Therefore, the Current Sense voltage (CS+) is positive and negative according to the positive reference current shown by the red arrow in Figure 5.

Since the ADC of the microcontroller used for the control implementation (XMC1404 from Infineon Technologies [2]) only allows input voltages between zero and the supply voltage (Vcc_XMC in Figure 5), an offset is included together with the CS gain in order to properly use the input spam of the ADC. In this case the offset is 2.5 V, which corresponds to half the supply voltage for the XMC™ controller used. The differential gain (Ki) is adjusted to consider not only inductor average current but also the switching frequency ripple, since this signal is used for CCM average current control and peak current limitation [2].

In the totem-pole operation, for both PFC and inverter power flow, the return path transistors (HS_SR and LS_SR on Figure 5) are switched at the AC zero crossing according to the AC polarity: HS_SR for positive AC and LS_SR for negative AC cycle. The polarity of the input voltage is set according to the control reference GND_iso. Since the control reference is in one of the AC input rails, the polarity detection is significantly simplified and the internal ESD diode protection of the XMC™ controller is used to transform the input capacitor voltage into a digital signal.

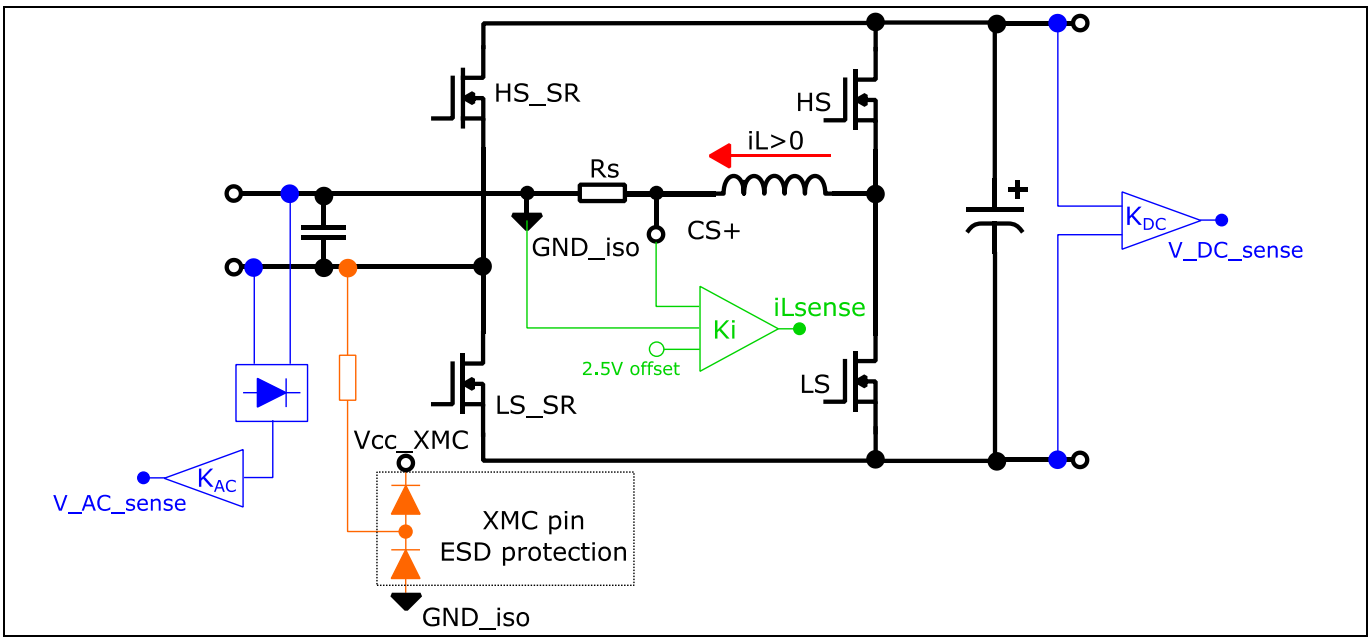

Figure 5 Block diagram of the sensing circuitry required for bi-directional totem-pole control with XMC™ and control reference in the AC rail in series with the PFC choke

Due to the control reference location, the bulk voltage sense requires a differential amplifier with gain K_{DC}, as shown in Figure 5. In the case of the of AC voltage sensing, the control reference location allows simple sensing. In this case, the voltage has been rectified (positive ADC input is required) and adapted to the ADC input range with a differential gain K_{AC}.

Since the AC voltage is used for the current reference generation in the selected average current mode structure (Figure 6), the current reference is a full wave rectified sinusoidal sequence. However, the current sense after the ADC is a sinusoidal sequence with offset at half of the ADC spam. Therefore, the ADC result from the CS first requires the offset to be removed and then rectified according to the AC polarity signal and the operation mode: current in inverter mode is 180 degrees out of phase with the AC voltage, while current in PFC mode is in phase with the AC voltage. These two steps, together with extra gain, are implemented by software in the XMC™ controller.

The current loop controller and structure is kept the same for inverter operation. However, since the bulk voltage is controlled by a DC-DC converter in DC-AC operation, the V_{loop_output} signal is substituted by a value sent by the DC-DC stage which is the target power to be delivered into the grid.

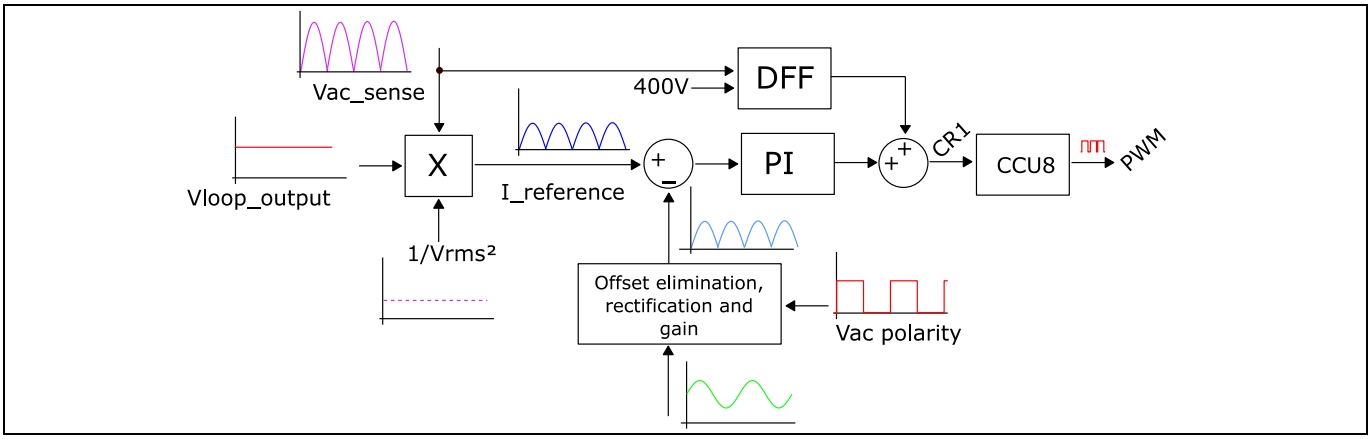

Figure 6 Current loop structure with duty feed-forward and the required current manipulation

1.3 Graphical user interface (GUI)

The XMC™ controller includes a serial communication interface (UART) and a specific protocol, which allows communication from a computer to the microcontroller. The user interface for Windows (Figure 7) has been developed to communicate with the controller using XMC™ Link (UART to USB conversion).

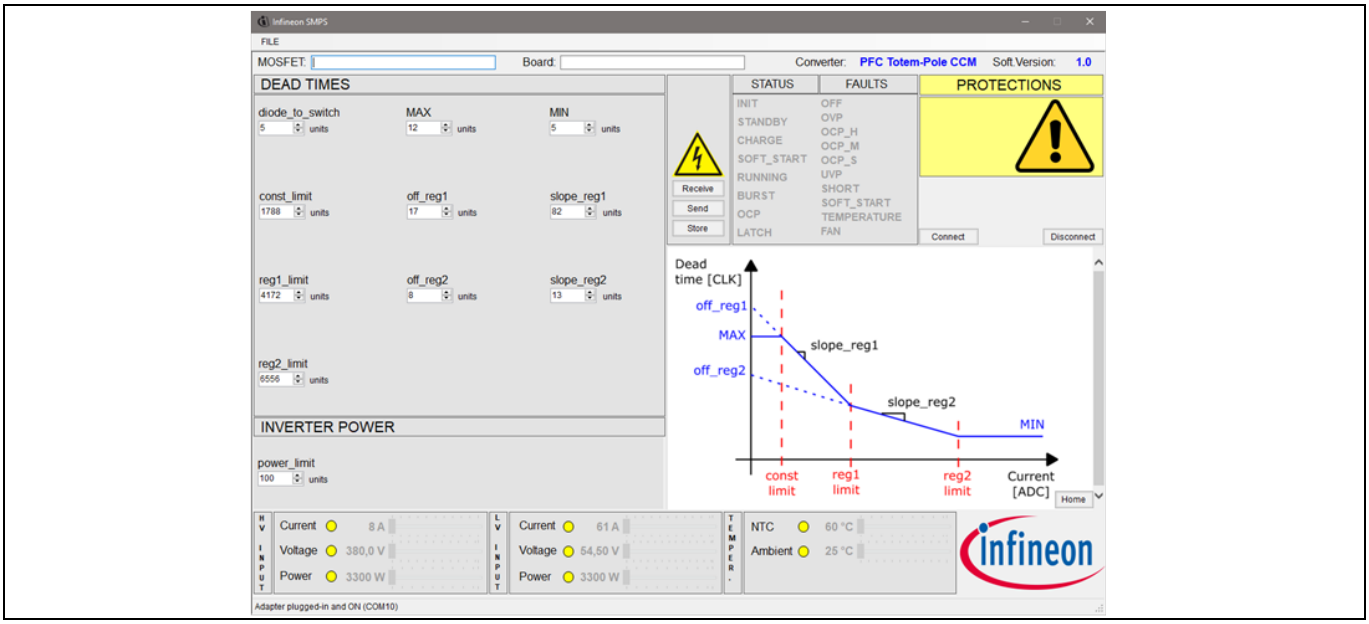

Figure 7 GUI for dead-time optimization and power target in inverter operation in the EVAL_3K3W_TP_PFC_SIC board

Two main sets of parameters can be updated in the controller using the GUI:

- Dead-time between low-side and high-side CoolSiC™ switches in the totem-pole topology. The dead-time can be modified in the controller following two linear regions with minimum and maximum limitation (Figure 7).
- Power command, which sets the current level in inverter operation. This emulates the command sent by the DC-DC stage in the final application. Figure 8 shows the relationship between the power command in the GUI and the output power for different AC voltages.

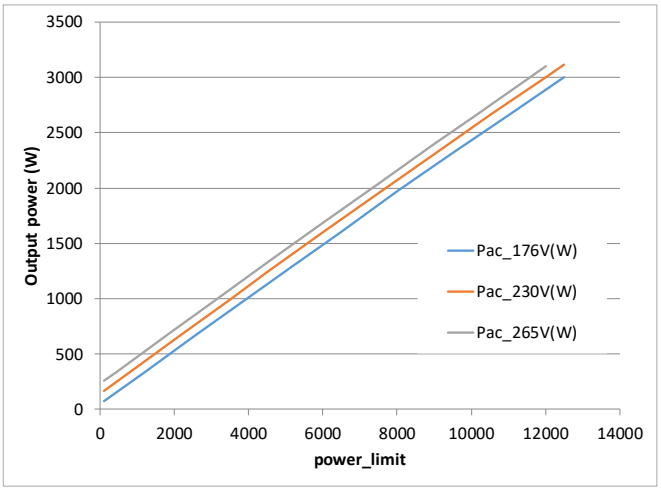

Figure 8 Measured output power (AC) according to the power_limit parameter from the GUI

The GUI shown is intended for development of the totem-pole platform, and the other functions displayed in Figure 7 are not available.

2 PFC (AC-DC operation) specification and test results

This chapter presents the specifications, performance and behavior of the 3300 W bridgeless totem pole with average current mode control in CCM for PFC operation. The results shown have been obtained with 64 mΩ 650 V CoolSic™ devices in TO-247 four-pin package and 17 mΩ 600 V CoolMOS™ in TO-247 as low-frequency switches. Table 1 shows the demonstrator performance and specifications under several steady-state and dynamic conditions. The converter operates at 65 kHz switching frequency and only for high-line AC input (176 V minimum RMS voltage).

Table 1 Summary of specifications and test conditions for the 3300 W bi-directional totem-pole board in PFC mode

Test		Conditions	Specification	
Efficiency test		230 Vrms, 50 Hz/60 Hz	η_{pk} = 99 percent at 1650 W (50 percent load)	
Current THD		230 Vrms, 50 Hz/60 Hz	THDi less than 10 percent from 10 percent load	
Power factor		230 Vrms, 50 Hz/60 Hz	PF more than 0.95 from 20 percent load	
Rated DC voltage			400 V	
Steady-state V_{out} ripple		230 Vrms, 50 Hz/60 Hz, 100 percent load	$\lvert\Delta V_{out}\rvert$ less than 20 $V_{pk\text{-}pk}$	
In-rush current		230 Vrms, 50 Hz/60 Hz, measured on the first AC cycle	I_{in_peak} less than 30 A	
Power line disturbance	AC lost (hold-up time)	230 Vrms, 50 Hz, 10 ms at 100 percent load, 20 ms at 50 percent load	V_{out_min} = 300 V (UVP)	No damage: * PFC soft-start if bulk voltage under 300 V * PFC soft-start if AC out of range for certain time
	Voltage sag	200 Vrms, 50 Hz/60 Hz, different sag conditions, 100 percent load		
Brown-out	AC voltage		174 V on; 168 V off	
Load transient		7.4 A (90 percent) ↔ 0.8 A (10 percent), 0.2 A/µs	V_{out_min} = 300 V (UVP) V_{out_max} = 450 V (OVP)	
OCP			Peak current limit 40 A	
			AVG current limit 28 A	

2.1 Performance and steady-state waveforms

The performance of the bi-directional totem pole presented in this document has been tested using the board EVAL_3K3W_BIDI_PSFB [6] as load in PFC operation and voltage supplier for inverter mode. This board is a bi-directional ZVS phase-shift full-bridge converter which can be used together with the presented bi-directional bridgeless PFC to build a full system solution using Infineon Technologies components. This set-up allows the use of the high–frequency isolation transformer present in the DC-DC stage to properly interface a voltage source to a grid emulator equipment, and it has been used to test the bi-directional capability and the steady-state performance of the bi-directional totem-pole. The presented measurements in this section comply with the specifications presented in Table 1 and have been obtained with a WT3000 power analyzer.

Figure 9 shows the efficiency measurements for PFC operation at different AC voltages. The efficiency results are the same regardless of the AC frequency (50 Hz/60 Hz) and do not include the fan consumption.

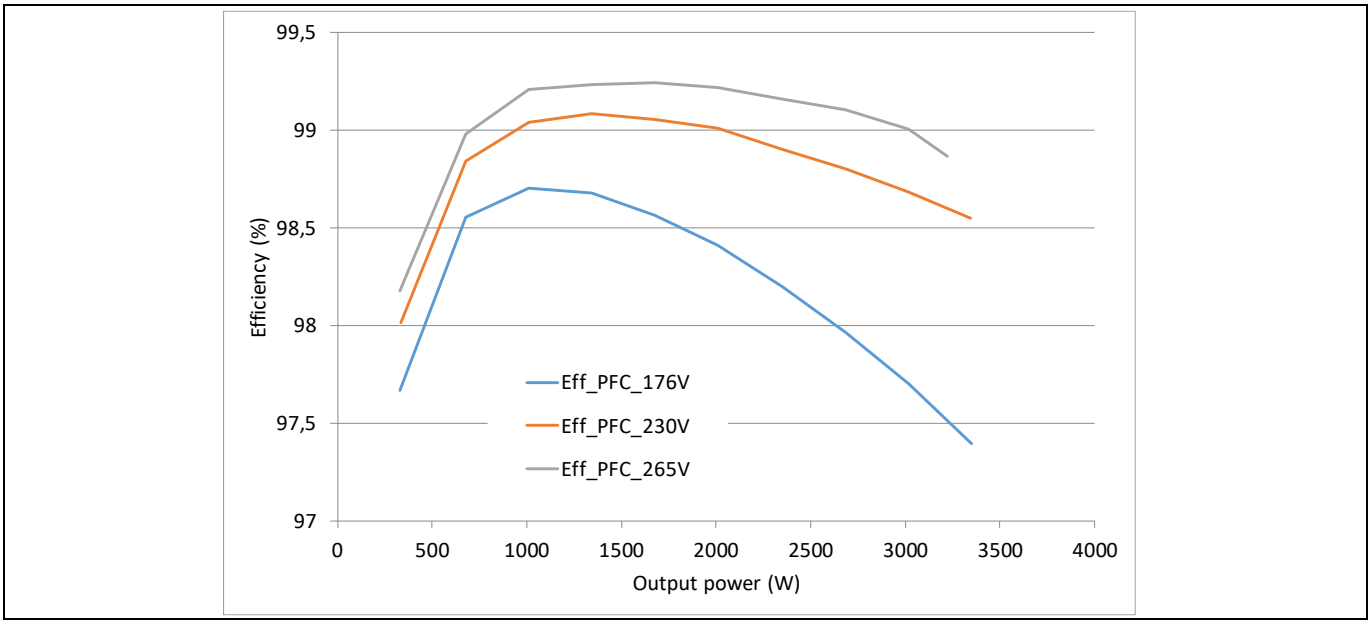

Figure 9 Measured efficiency (with applied line filter in the power analyzer) at different RMS voltages (50/60 Hz) for PFC operation

Figure 9 depicts the Total Harmonic Distortion (THD) and power factor measured at different AC voltages at 50 Hz and 60 Hz for PFC operation. As can be seen, the results for THD and power factor have small differences. These differences are within the measurement accuracy of the equipment used.

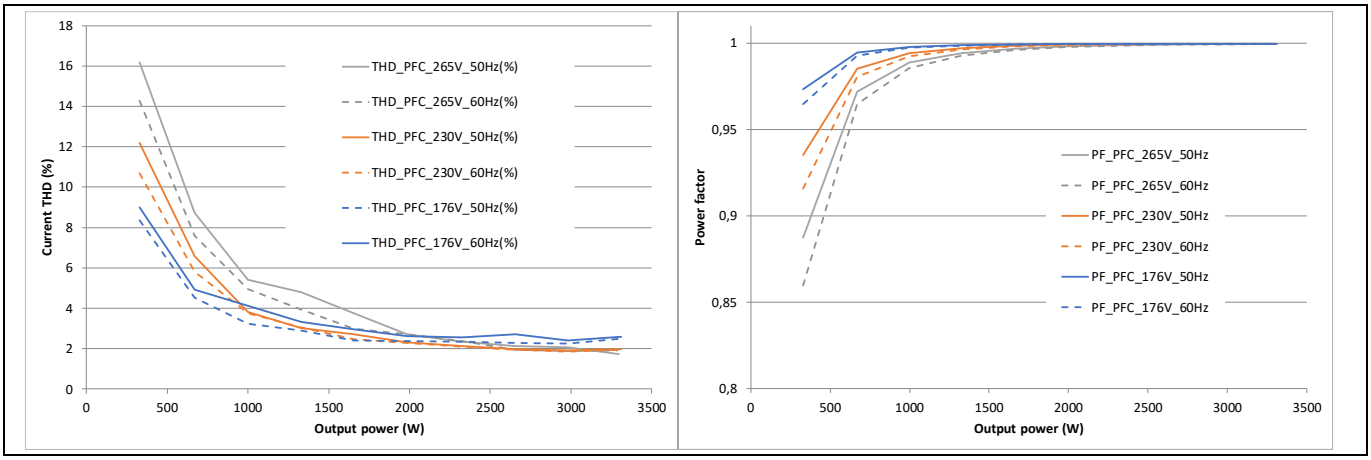

Figure 10 Measured THD and power factor at different RMS voltages for 50 Hz and 60 Hz in PFC operation

Figure 11 and Figure 12 show the PFC operation for different AC voltages in amplitude and frequency as well as power levels.

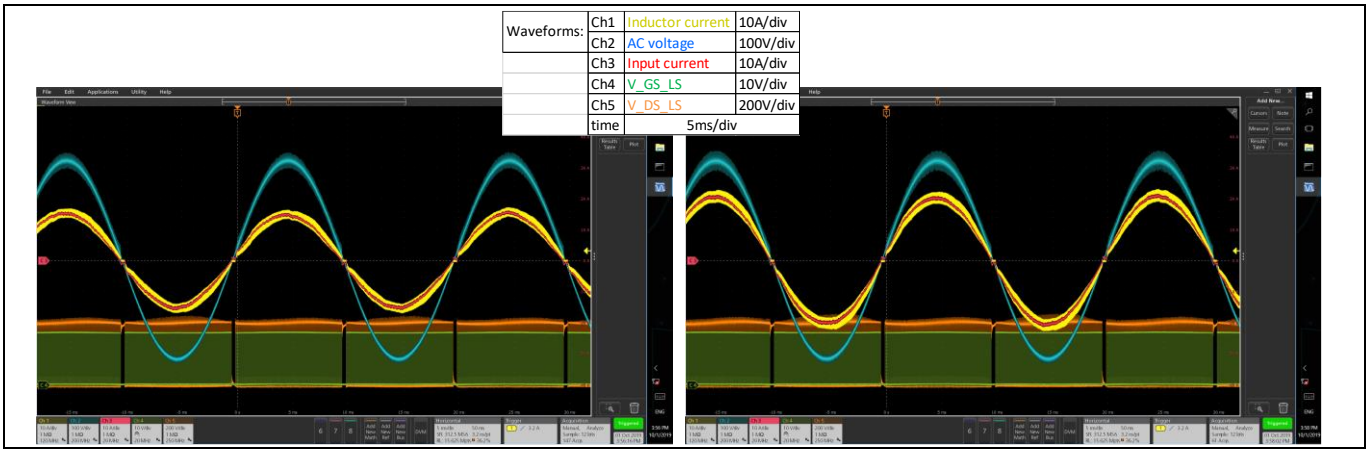

Figure 11 Steady-state waveforms at 230 V, 50 Hz AC voltage, 50 percent load (left) and 100 percent load (right)

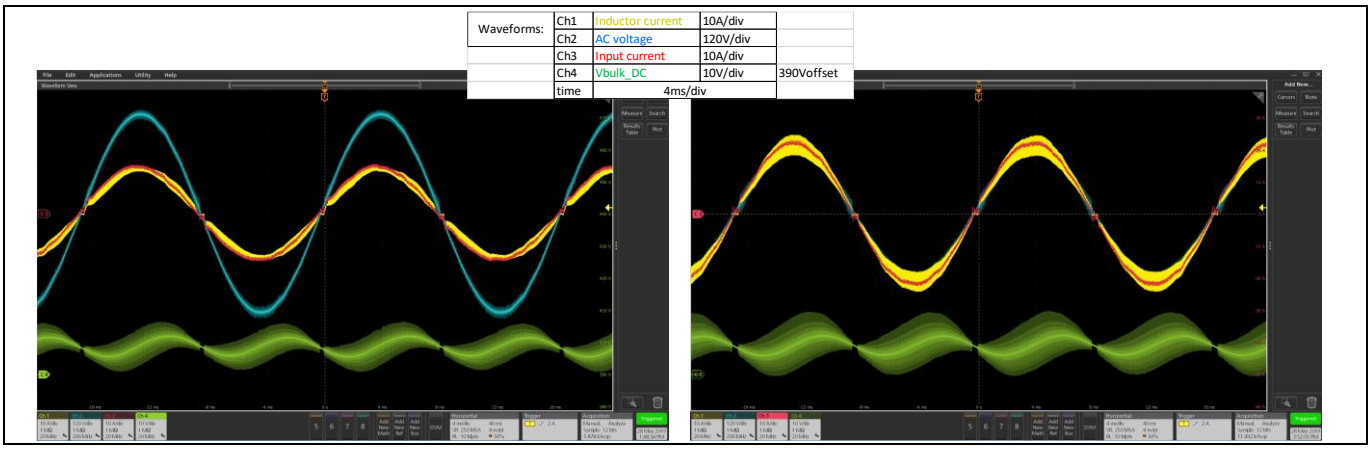

Figure 12 Steady-state waveforms at 265 V (left) and 176 V (right) for 60 Hz AC voltage and 80 percent load (2.7 kW)

2.2 Power line disturbance

Two main line disturbance conditions can occur when connected to the grid. On one side the AC can be lost during a certain time – Line Cycle Drop-Out (LCDO) – and, on the other side, the AC voltage can suddenly decrease to an abnormal value – voltage sag. This section introduces the test conditions for both disturbances as well as the EVAL_3K3W_TP_PFC_SIC bridgeless board performance when those conditions are applied. For these tests of the PFC operation a programmable AC source and a high-voltage electronic load have been used.

2.2.1 Line Cycle Drop-Out

The 3300 W totem-pole CCM PFC operates exclusively in high-line. Therefore the ACLCDO capability is tested from 230 to 0 V. Different timing, related to the specified hold-up time and the line frequency, is applied as shown in Table 2. The test results (Figure 13 and Figure 14) show that the output voltage is within the specified dynamic variation regardless of the start angle of the voltage drop-out. In case the drop-out is longer than specified, output voltage under-voltage (300 V) can be triggered and a turn-off and restart of the unit will occur.

Table 2 Applied voltage cycles for LCDO test at different loads with 50 Hz AC input voltage

		1st to 10th time (100 ms period)	
Applied voltage	230 V AC	0 V AC	230 V AC
Timing at different load conditions	50 percent load	20 percent (20 ms)	80 percent (80 ms)
	100 percent load	10 percent (10 ms)	90 percent (90 ms)

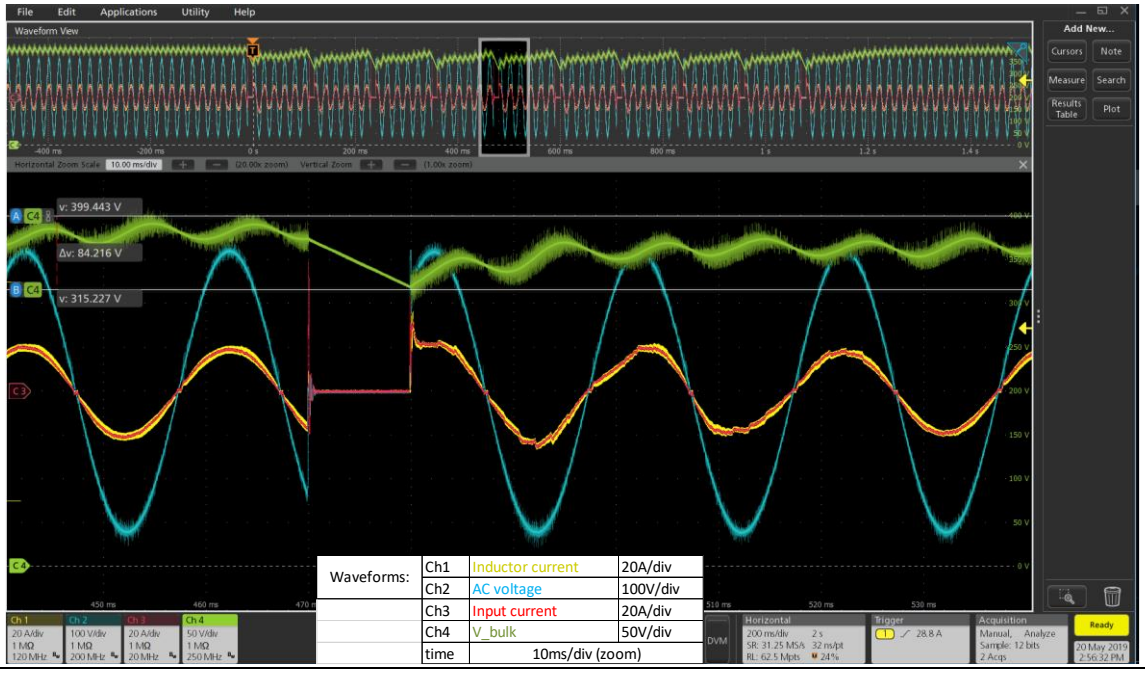

Figure 13 Detail of the fifth repetition in a 10 ms LCDO test at 230 V AC, 50 Hz and 100 percent load with starting angle of 45 degrees

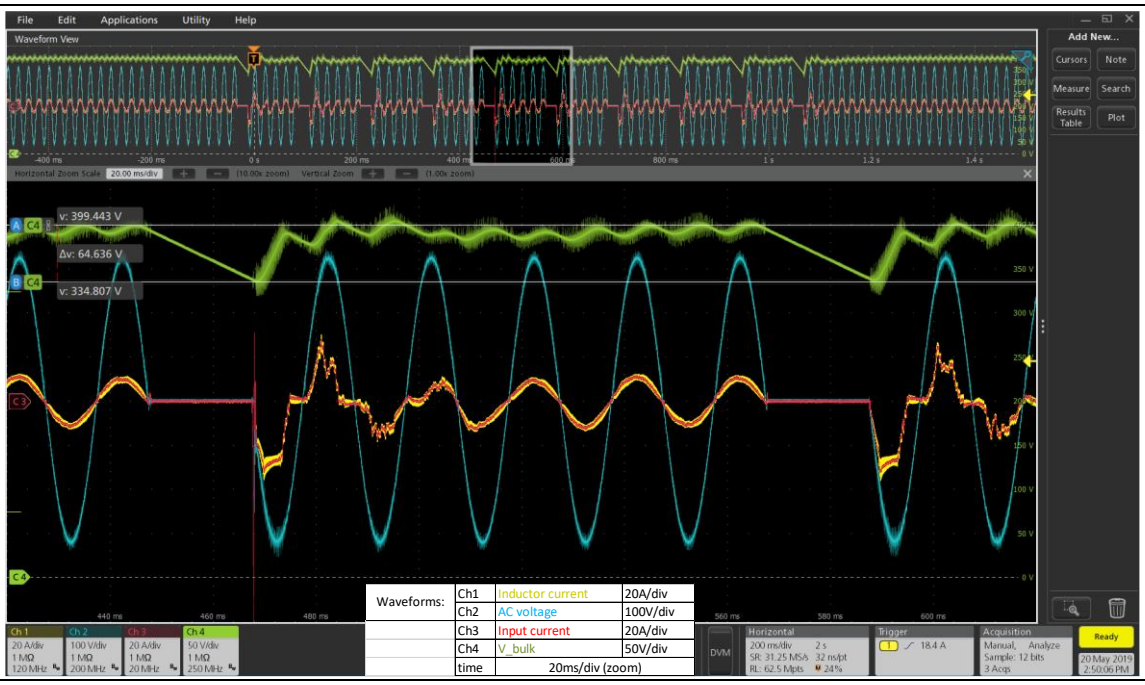

Figure 14 Detail of the fifth and sixth repetition in a 20 ms LCDO test at 230 V AC, 50 Hz and 50 percent load with starting angle of 0 degrees

2.2.2 Voltage sag

For high-line, two different voltage sag conditions are considered and tested, corresponding with Table 3.

Table 3 Voltage sag conditions for high-line applied to the EVAL_3K3W_TP_PFC_SIC board

		1st to 10th time	
	Steady AC input	Voltage sag (time)	Period
AC input	200 V AC	130 V AC (0.5 s)	5 s
	200 V AC	150 V AC (2 s)	20 s

Figure 15 shows the totem-pole PFC behavior with 130 V voltage sag during 500 ms. As can be seen by the V_{DS} waveform, the output voltage cannot be regulated to 400 V in this condition since the inductor average current is limited to 28 A. Not only is average current limitation applied in the EVAL_3K3W_TP_PFC_SIC board for both power flow modes but also peak current limitation, which is set to 40 A (Figure 16).

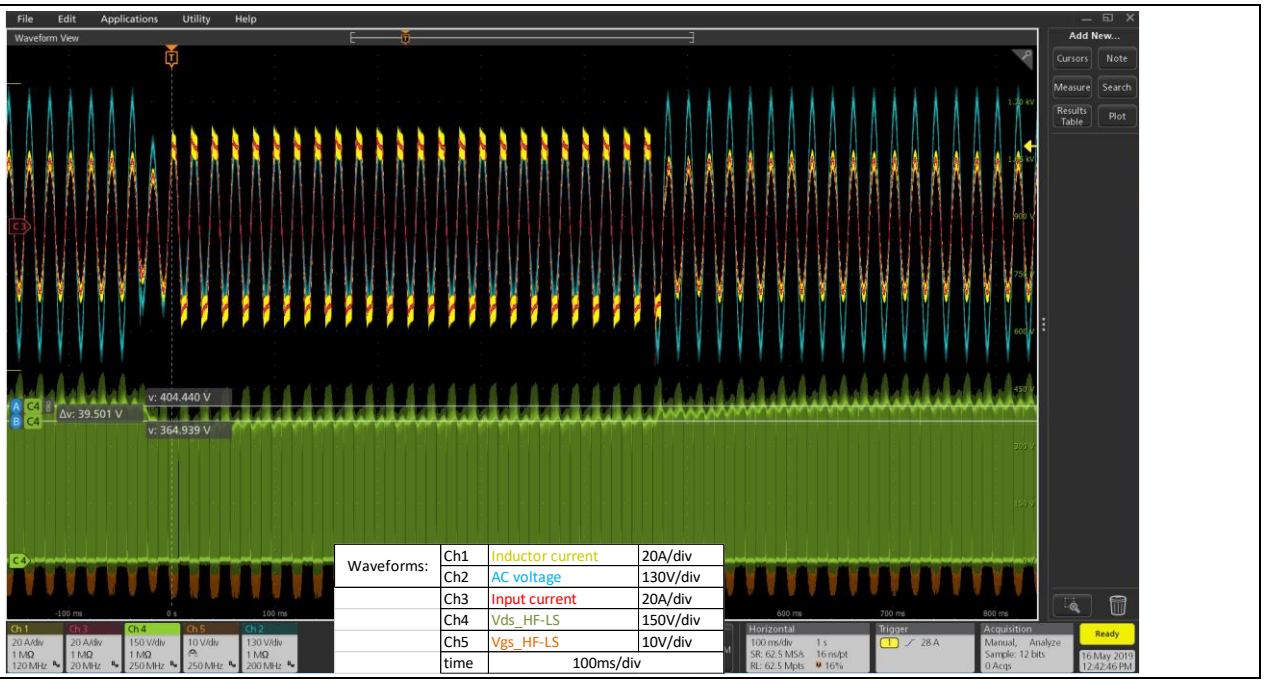

Figure 15 Main waveforms during a 500 ms and 130 Vrms voltage sag at full load

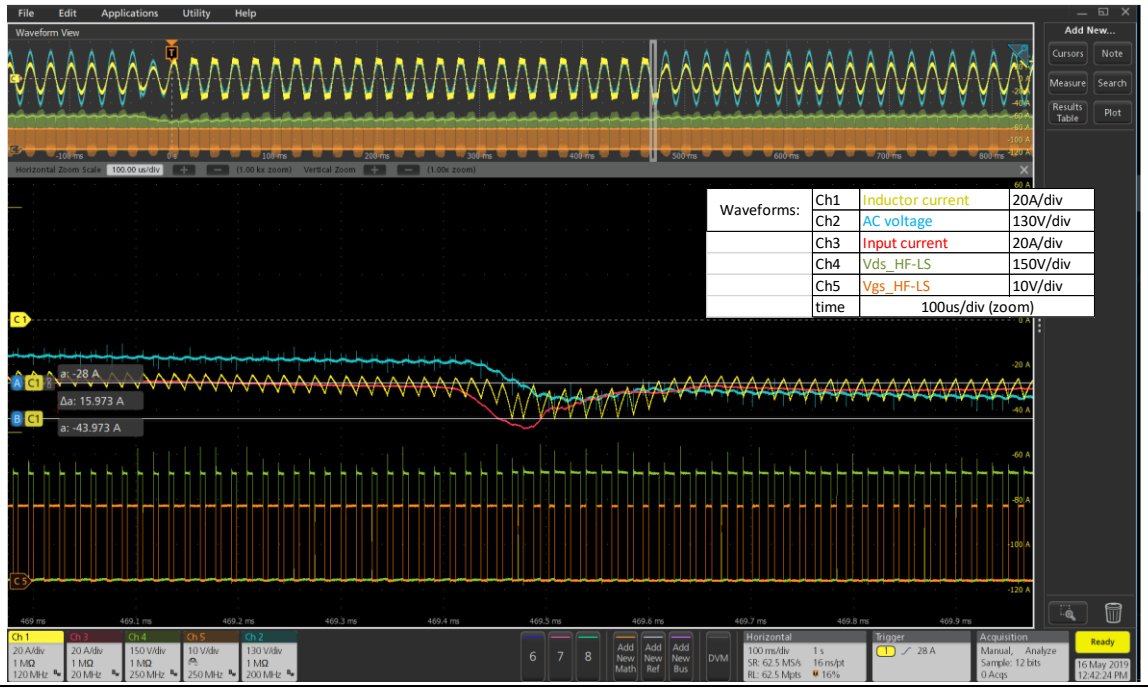

Figure 16 Peak current limitation when returning to nominal voltage after 130 V voltage sag in PFC mode

However, if the voltage is under the nominal range for longer than specified in the table, the PFC turns off and restarts with soft-start after an idle time. Figure 17 shows this behavior when a voltage sag to 130 V is applied for longer than 500 ms (750 ms) at full load.

Note: The electronic load used during the test is configured in such a way that it demands current only when the voltage applied is over 300 V, which is the under-voltage setting of the bridgeless PFC.

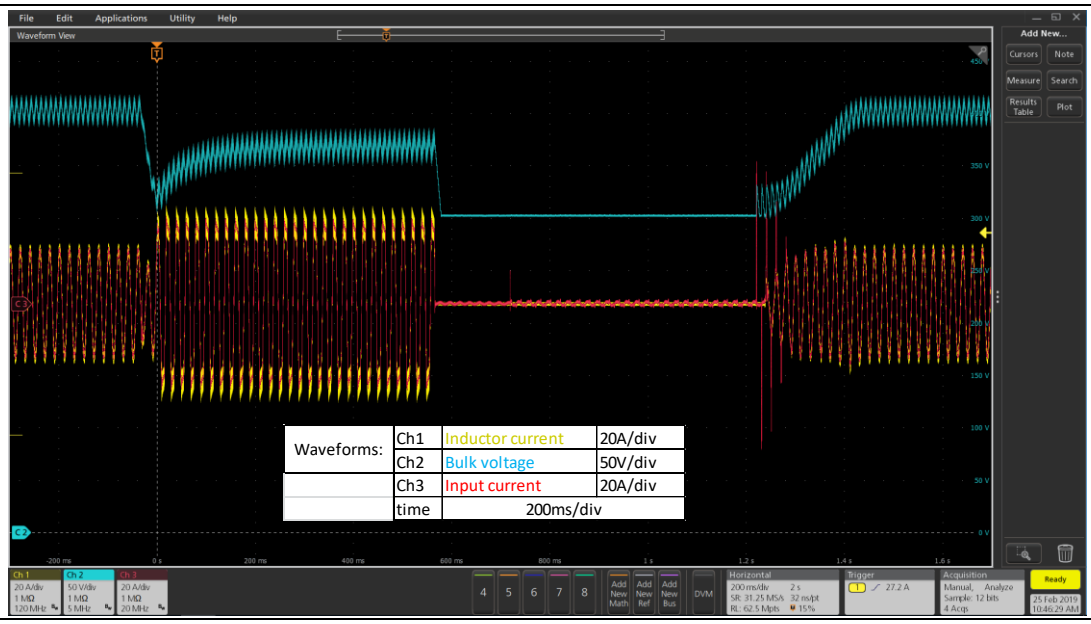

Figure 17 PFC resumes operation after 130 Vrms voltage sag applied for 750 ms at full load

A similar behavior can be seen when 150 V is applied for 2s (Figure 18). The average inductor current, i.e. input current, is limited to 28 A (Figure 18). In this case the demanded current is lower and therefore the average current limitation occurs for a shorter time, and thus the bulk voltage decreases less than in the 130 V case.

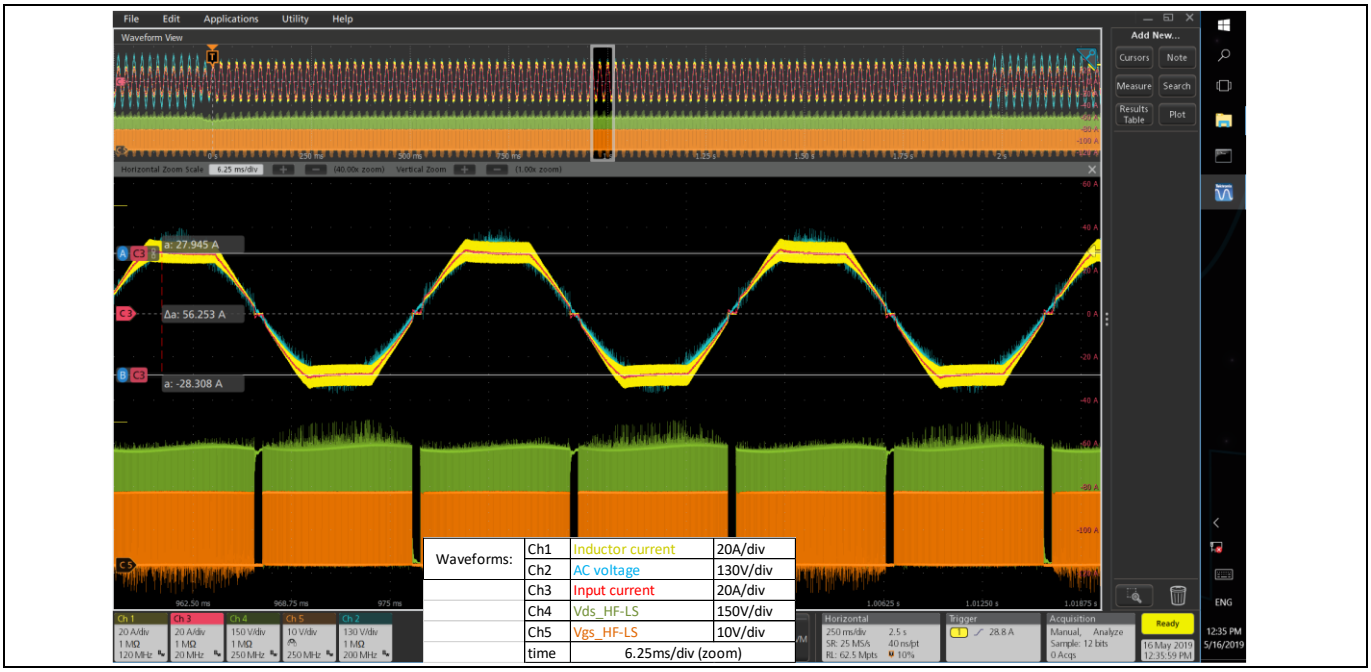

Figure 18 Detail of the voltage sag operation at 150 V for 2 s

2.3 Output voltage dynamic behavior

In addition to power line disturbance, two other dynamic perturbances can affect the performance of the power supply shown: load and input voltage variation.

2.3.1 Load-transient response in PFC mode

As specified in Table 1, 10 percent load (0.8 A) to 90 percent load (7.4 A) steps (and vice versa) with 0.2 A/µs slope are considered in PFC mode. Figure 19 and Figure 20 show the EVAL_3K3W_TP_PFC_SIC board behavior under these load steps. The implemented voltage loop has a 35 Hz crossover frequency. In this SW version of the totem-pole control, neither extra gain nor non-linear current variation have been implemented.

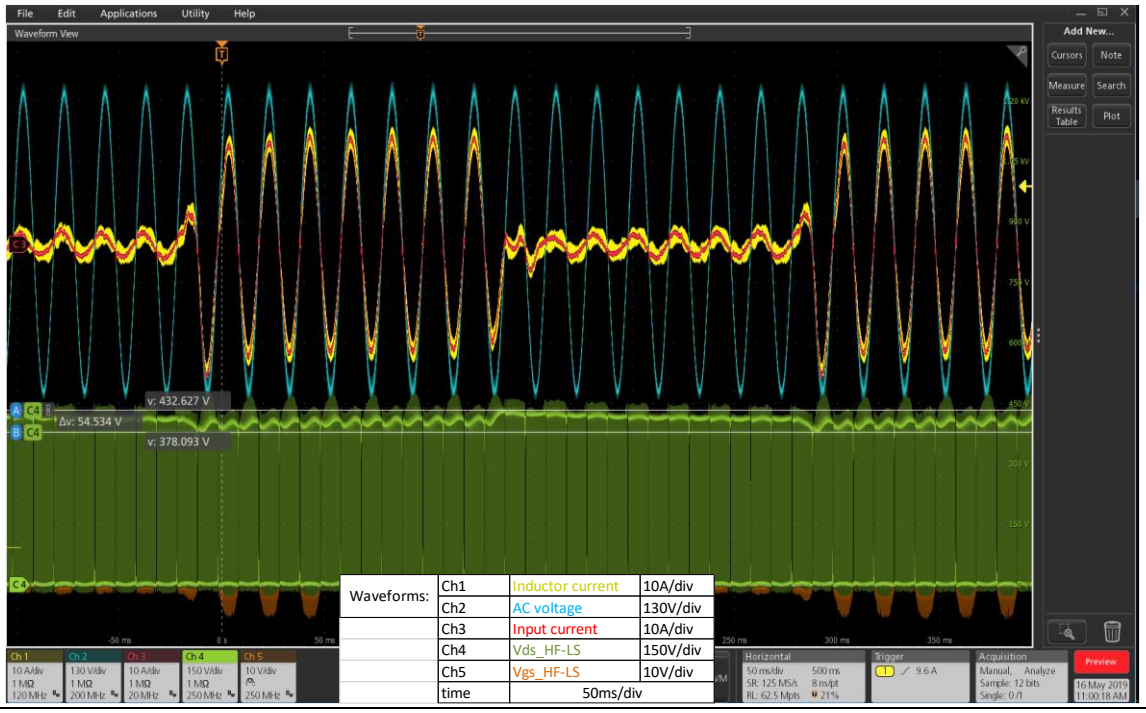

Figure 19 **3.3 kW SiC totem-pole CCM PFC response for 10 percent to 90 percent load steps every 150 ms with 0.2 A/µs current slope**

The output voltage dynamic range for the specified load variation is within 375 V and 430 V. When the load is removed (Figure 20) the overshoot reaches 440 V, which is under the over-voltage setting (450 V), and the converter manages to reduce the voltage without PWM interruption. Furthermore, the converter regulates the output voltage under no-load conditions by making the average inductor current close to zero. This is possible since negative inductor current is allowed in a totem-pole configuration with complementary PWM signals, i.e. if the MOSFET in diode function is not turned off when the inductor current gets close to zero to emulate the diode behavior.

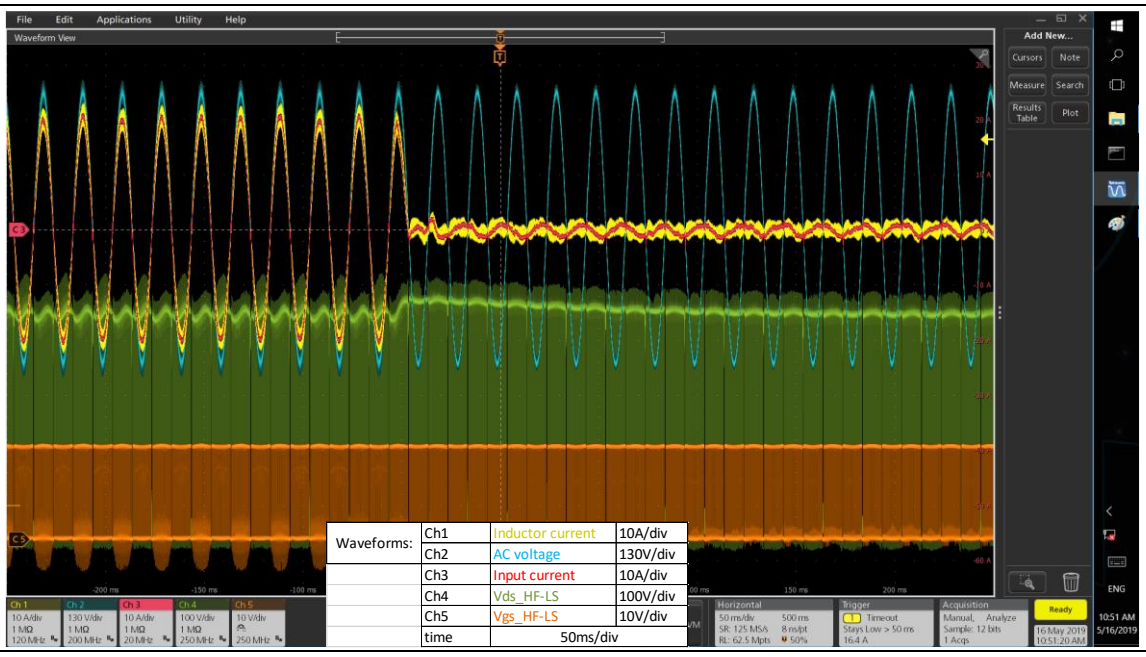

Figure 20 **3.3 kW SiC totem-pole CCM PFC response at full load to no-load step with 0.2 A/µs current slope**

2.3.2 AC voltage variation in PFC mode

Input voltage variations, as seen in the power line disturbance section, can modify the bulk voltage. This can also occur when the input voltage varies even within the normal operation range, as shown in Figure 21. In this condition, the bulk voltage is in the range 330 to 430 V, as shown by the test result.

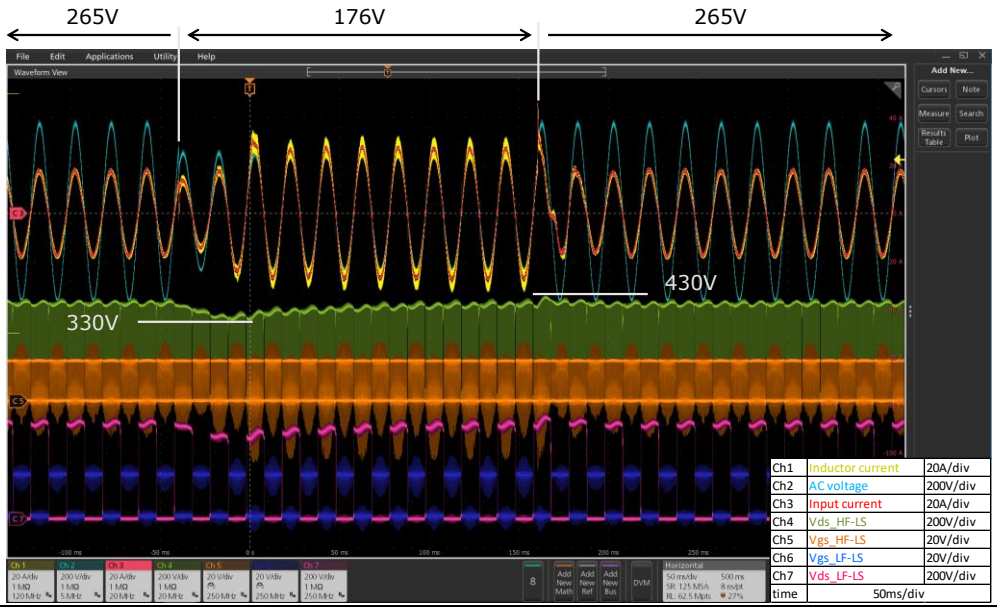

Figure 21 Maximum (265 Vrms) to minimum (176 Vrms) line voltage variation at full-load operation

As introduced in section 2.2.2, a sudden increase in the input voltage leads to an immediate increase in the inductor current until the voltage loop and the line feed-forward reduce the current demand. Figure 22 shows this effect when the AC voltage changes from 176 to 265 V. The sudden change of the inductor current leads to peak current limitation, which is set to 40 A for both positive and negative AC.

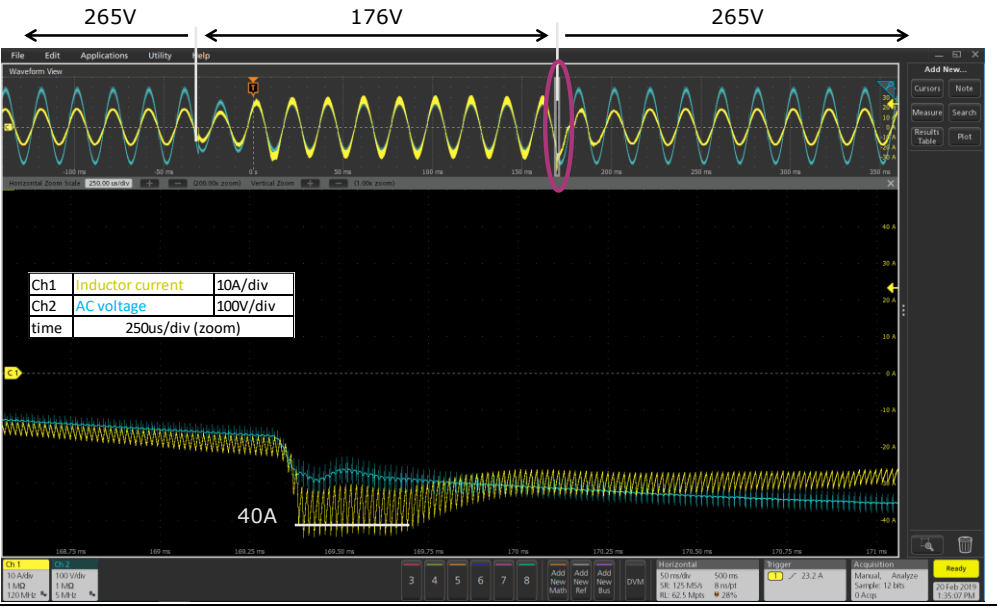

Figure 22 Detail of the inductor peak current cycle-by-cycle limitation when the input voltage changes from 176 to 265 V

2.4 In-rush current and PFC start-up

Figure 23 shows the start-up of the bridgeless totem pole in PFC mode for full-load operation. The test has been performed with programmable AC source and high-voltage electronic load. The load is configured with a 350 V threshold to start sinking current. This threshold emulates the behavior of the DC-DC converter, which would be the load for the PFC (Figure 24).

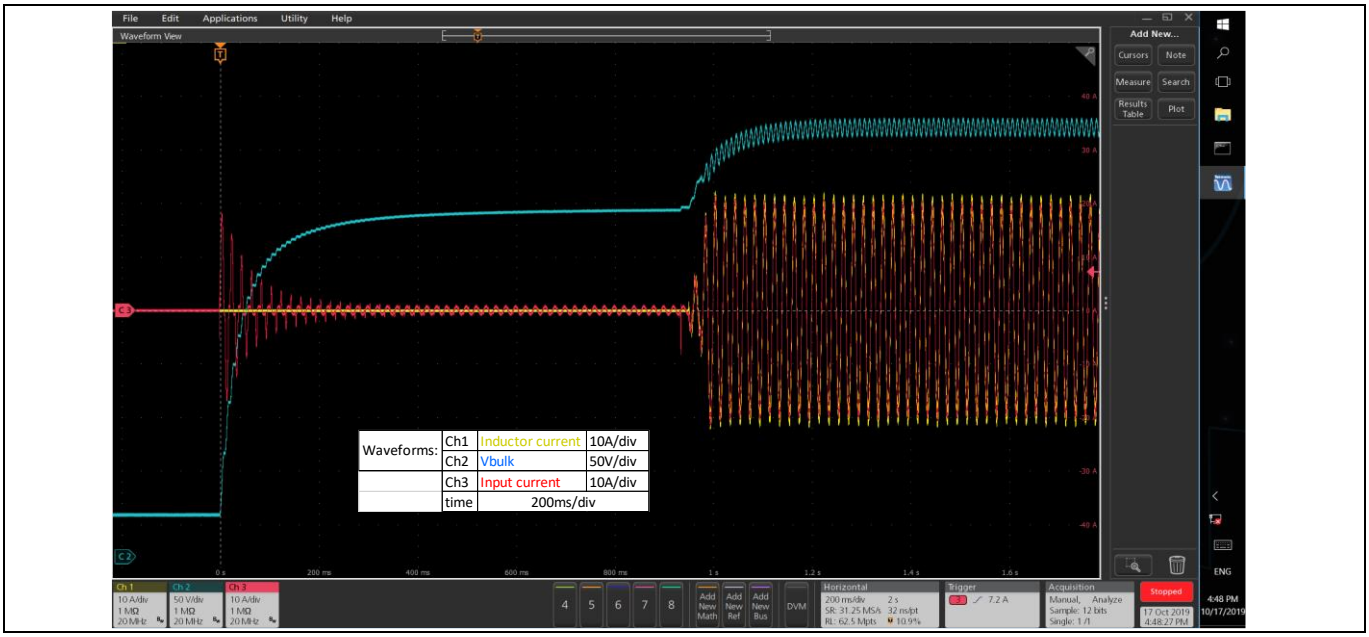

Figure 23 EVAL_3K3W_TP_PFC_SIC start-up at full load for 230 V, 50 Hz input voltage

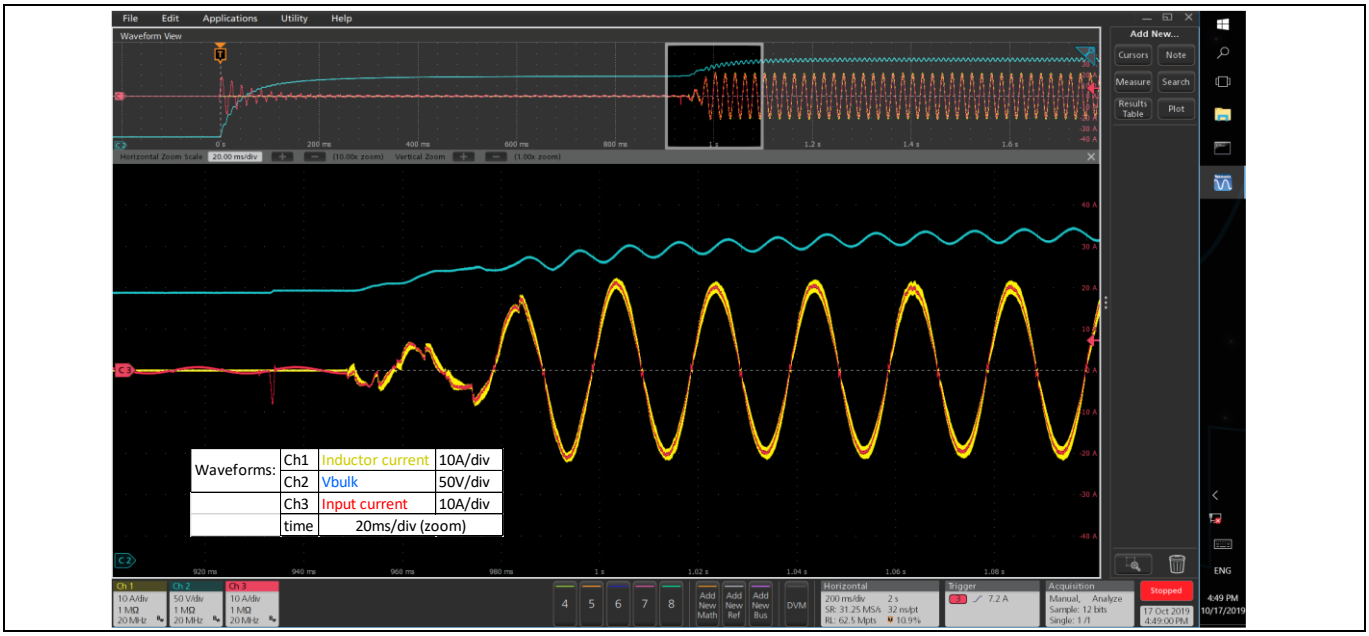

Figure 24 Detail of the bulk voltage soft-start from AC peak voltage to steady-state voltage after relay is closed (230 V/50 Hz)

The in-rush current when connecting to the AC source is limited with a NTC. This resistor is short-circuited by a parallel relay before start-up if the input and output voltage conditions to start the bridgeless PFC are met. The

in-rush current is measured at the first AC cycle and it is independent of the output load. Figure 25 shows the in-rush current at full-load start-up. According to the measurement the in-rush current is significantly under the specified 30 A in Table 1.

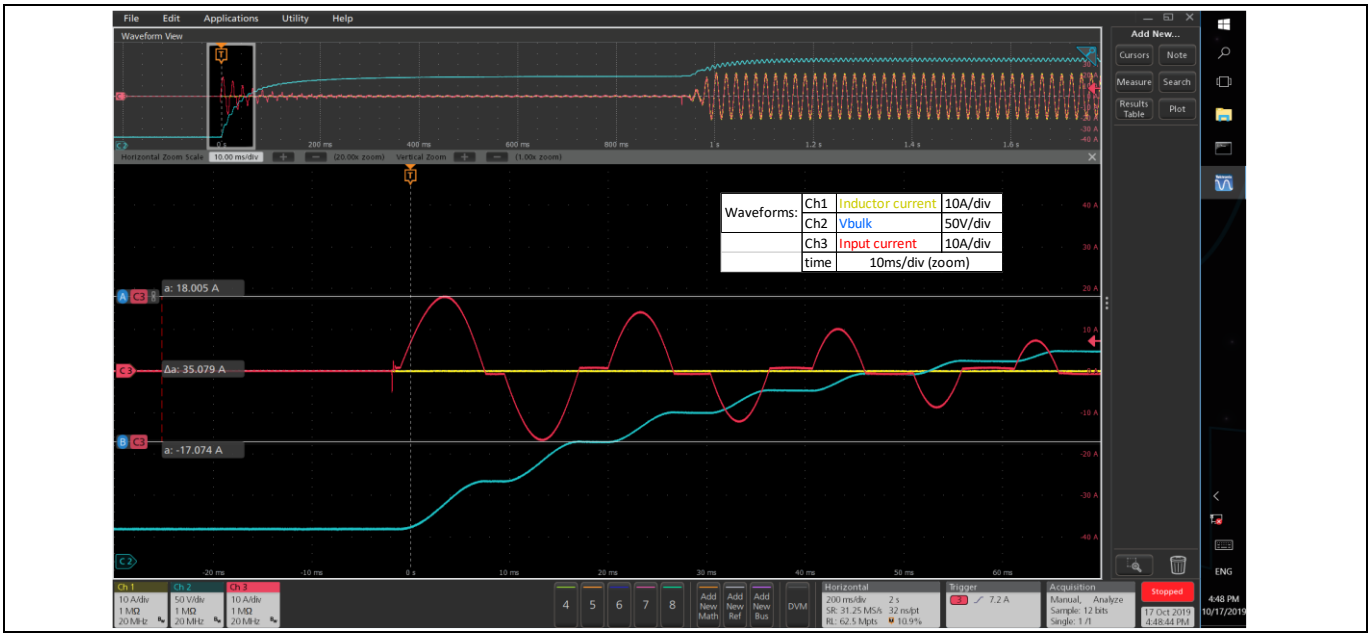

Figure 25 In-rush current of EVAL_3K3W_TP_PFC_SIC at full-load start-up

3 Inverter (DC-AC operation) specification and test results

The bridgeless totem-pole topology offers inherent bi-directional power flow capability, which has been explored in the EVAL_3K3W_TP_PFC_SIC. The inverter operation mode can be selected before the application starts by choosing the “INV” option in the available switch (SW1) on the main board.

Note: The power flow or operation mode is selected before the application starts and the power flow cannot be reverted during operation in this version of the SW. Therefore, the EVAL_3K3W_TP_PFC_SIC board is able to operate as either PFC or inverter but the SW is not ready for dynamic change of operation mode.

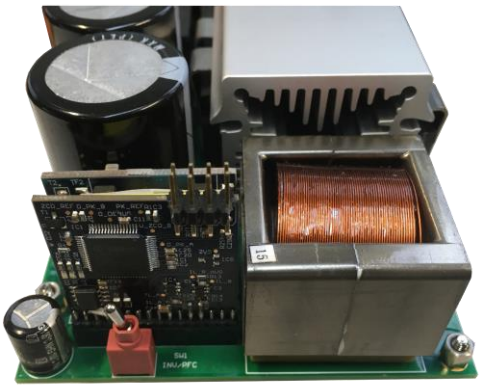

Figure 26 Switch to select the operation mode (PFC or inverter) in the EVAL_3K3W_TP_PFC_SIC

The inverter operates at 65 kHz switching frequency for high-line AC input (176 V minimum RMS voltage), as in the rectifier operation. The specifications in inverter operation regarding efficiency, THD, PF, AC voltage ranges and OCP are the same as those shown in Table 1. Table 4 shows those specifications which are different for inverter operation.

Table 4 Summary of specifications and test conditions for the 3300 W bi-directional totem-pole board in inverter mode

Test		Conditions	Specification
Rated DC voltage			400 V
AC voltage		Relay off after 100 ms	174 V on; 168 V off
DC voltage			Low range: 390 V on, 350 V off/latching
			High range: 410 V on, 450 V off/latching
Load transient			Soft change between received power commands
Power line disturbance	AC lost	230 Vrms, 50 Hz, 2 ms, load independent	Inverter resumes operation with soft-start after AC returns to range
	Voltage sag	100 ms under 170 V, load independent	Inverter off and restarts after a defined time with soft-start when AC returns to range

As introduced in section 2.1, the EVAL_3K3W_TP_PFC_SIC board has been tested using EVAL_3K3W_BIDI_PSFB as the voltage supplier for inverter mode (Figure 27).

Note: Since the DC-DC board has been designed as stand-alone, changes in the control loop have been implemented to operate with the SiC bridgeless totem pole as a load.

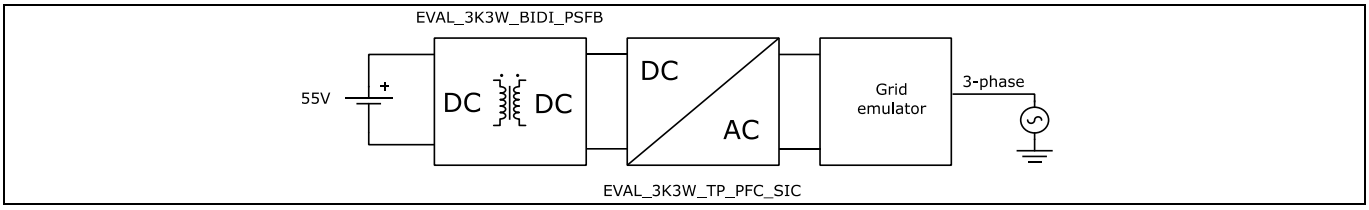

Figure 27 EVAL_3K3W_BIDI_PSFB and EVAL_3K3W_TP_PFC_SIC set-up for inverter test connected to a grid emulator

3.1 Performance and steady-state waveforms

The totem-pole bi-directional converter with Infineon CoolSiC™ presented in this application note has been tested in steady-state up to 3 kW output power. The power limitation is necessary because of the thermal limitation of EVAL-3K3W_BIDI_PSFB operating in boost mode [6]. Figure 28 shows the efficiency measurements (without fan consumption) for inverter operation at different AC voltages at 50 Hz. AC current performance for inverter operation of the bi-directional totem pole is presented in Figure 29.

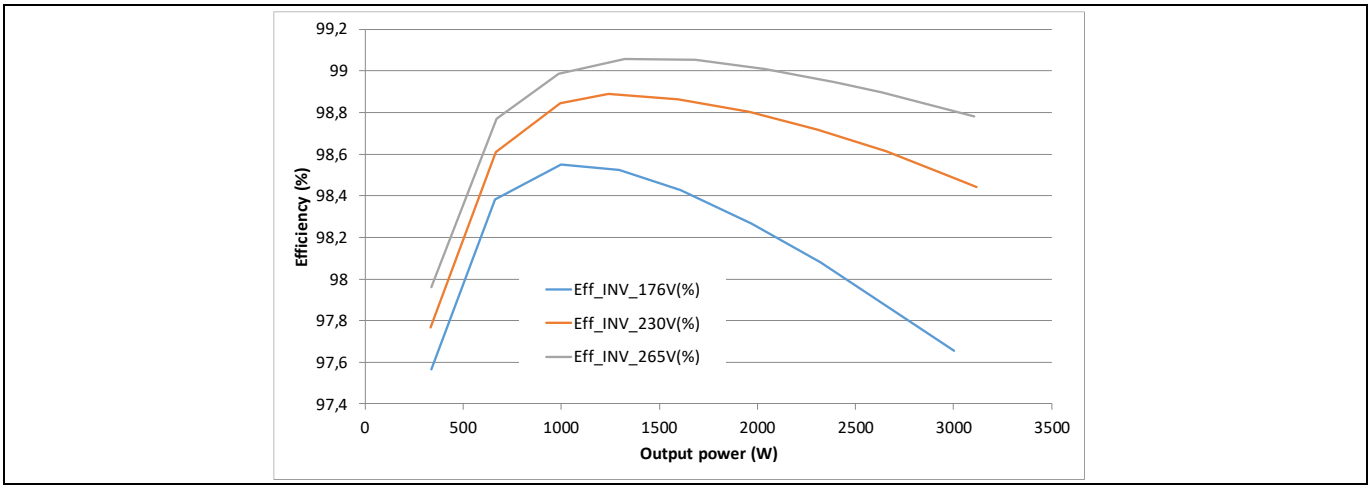

Figure 28 Measured efficiency for inverter operation of the EVAL_3K3W_TP_PFC_SIC board at different RMS voltages (50 Hz)

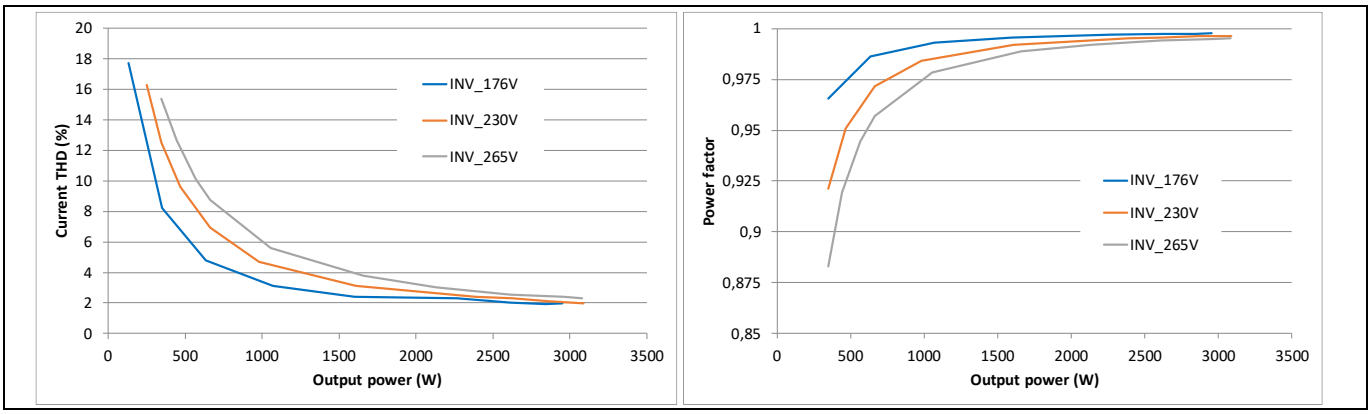

Figure 29 Measured THD (left) and power factor (right) for inverter operation of EVAL_3K3W_TP_PFC_SIC board at different RMS voltages (50 Hz)

The inductor current of the bridgeless totem-pole topology in inverter operation is 180 degrees out of phase in comparison with the PFC operation. Therefore, current is actually injected into the AC grid. This main difference can be seen in Figure 30, which shows the main waveforms of the EVAL_3K3W_TP_PFC_SIC board in rectifier and inverter operation for the same power level, 50 percent load.

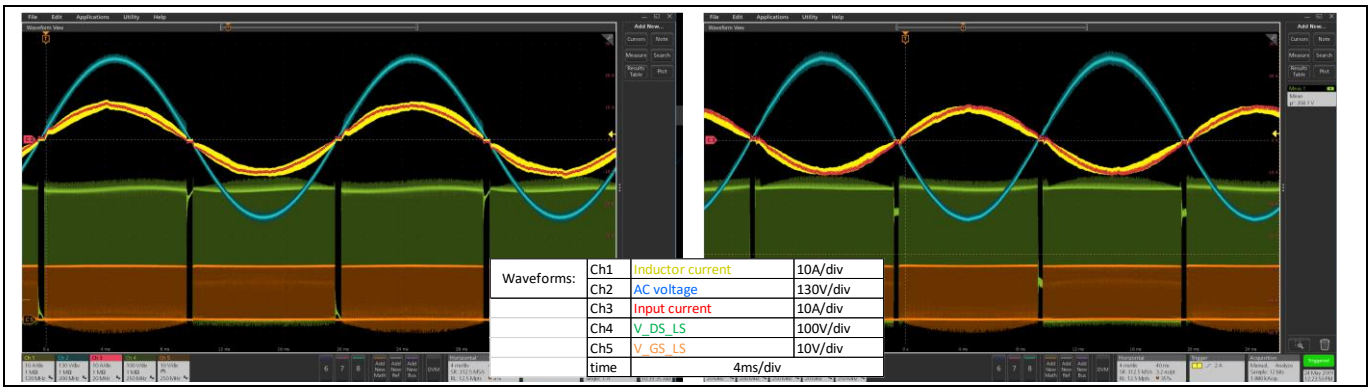

Figure 30 Steady-state waveforms at 230 V 50 Hz for 50 percent load (1.65 kW) in PFC (left) and inverter (right) mode

3.2 Inverter mode load change

In inverter mode, the EVAL_3K3W_TP_PFC_SIC board behaves as a current source connected between two voltage sources: the bulk voltage and the AC grid. In that case, the power to be injected into the grid is set by the DC-DC stage, which also regulates the bulk voltage (input voltage for the inverter). Therefore, the DC-DC stage would send a power command to the DC-AC converter, which in the presented tests has been substituted by a power command sent from the computer using a GUI (section 1.3).

When a new power command is received, the power is modified following a ramp as shown in Figure 31, where a power change from 300 W to 2500 W is received. A similar behavior would be observed in case of a power command reduction.

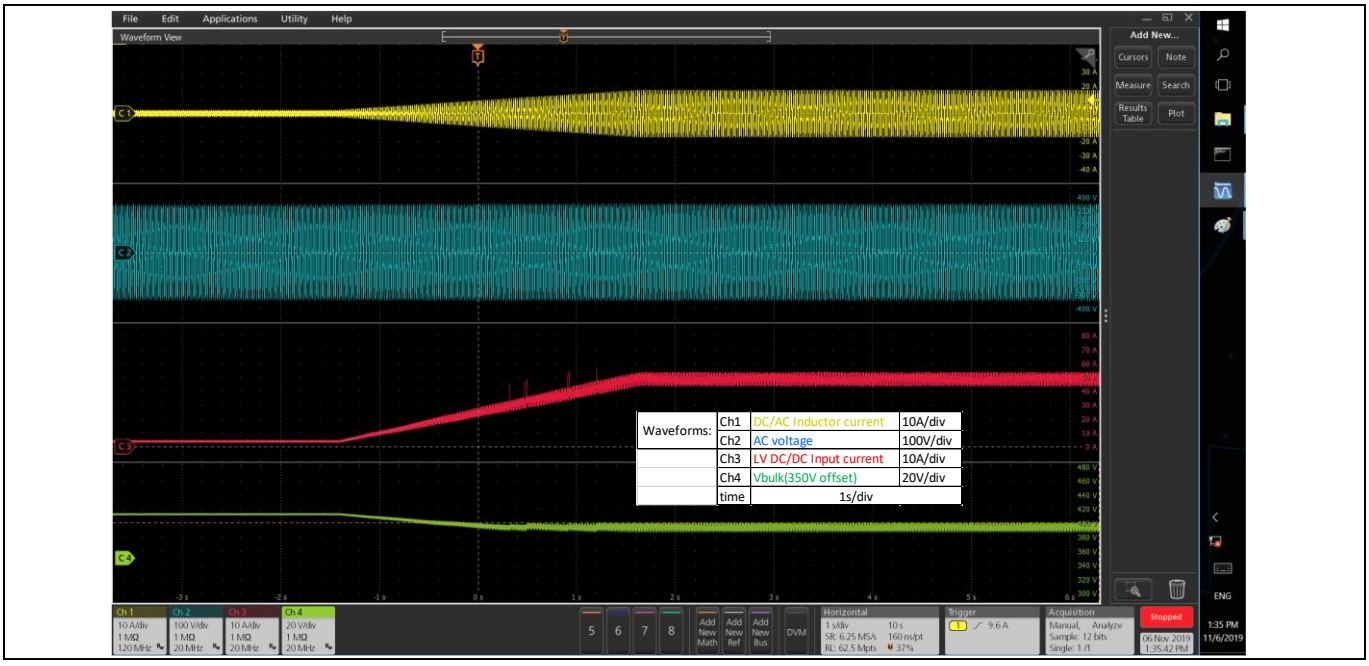

Figure 31 Load increase (300 W to 2.5 kW) in inverter mode; 230 V, 50 Hz AC voltage

3.3 Power line disturbance and AC voltage variation

3.3.1 Inverter mode LCDO

In the case of inverter operation, the hold-up time does not apply since the DC-DC stage is controlling the bulk voltage, i.e. the supply voltage to the DC-AC stage. Therefore, when an AC voltage loss is detected (AC close to zero for more than 2 ms) the inverter prepares for soft-start operation when the voltage returns. This behavior, which is independent of the injected power, can be seen in Figure 32 for a 20 ms line drop-out to 0 V, or in Figure 33 when the AC goes to 0 V for 50 ms.

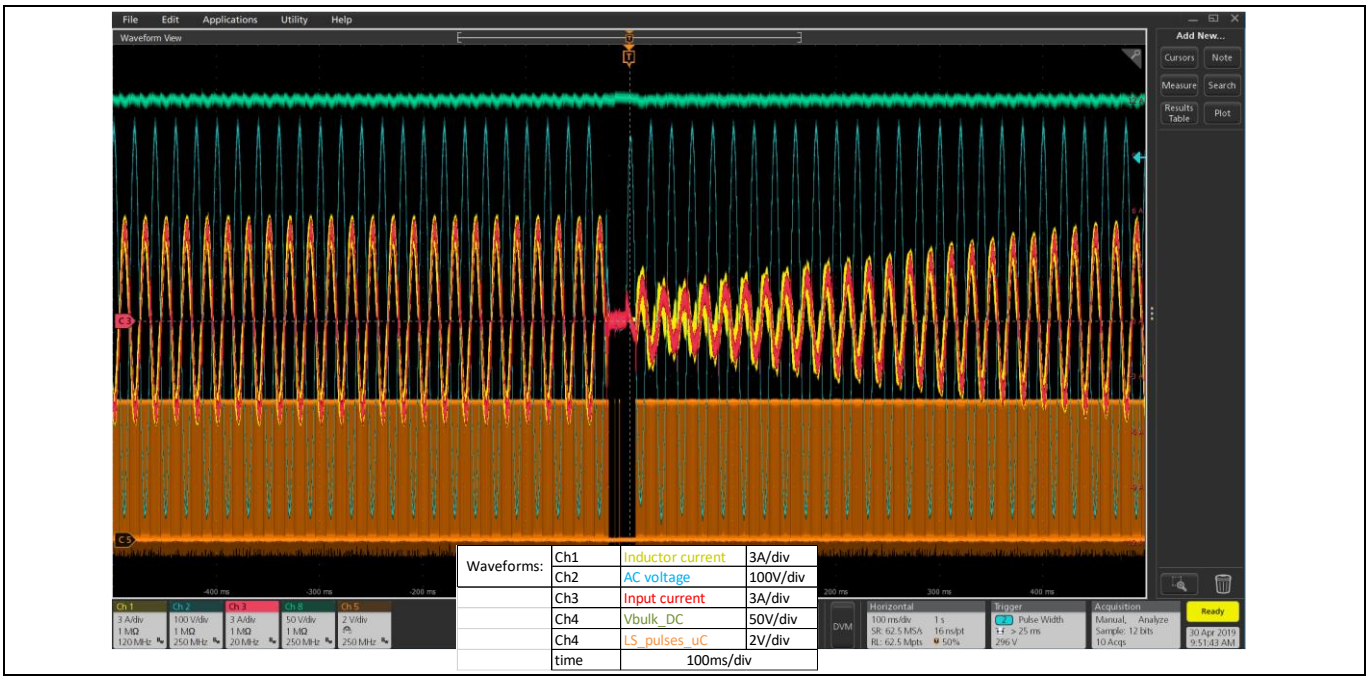

Figure 32 Inverter behavior under AC-line drop-out of 20 ms for 800 W power

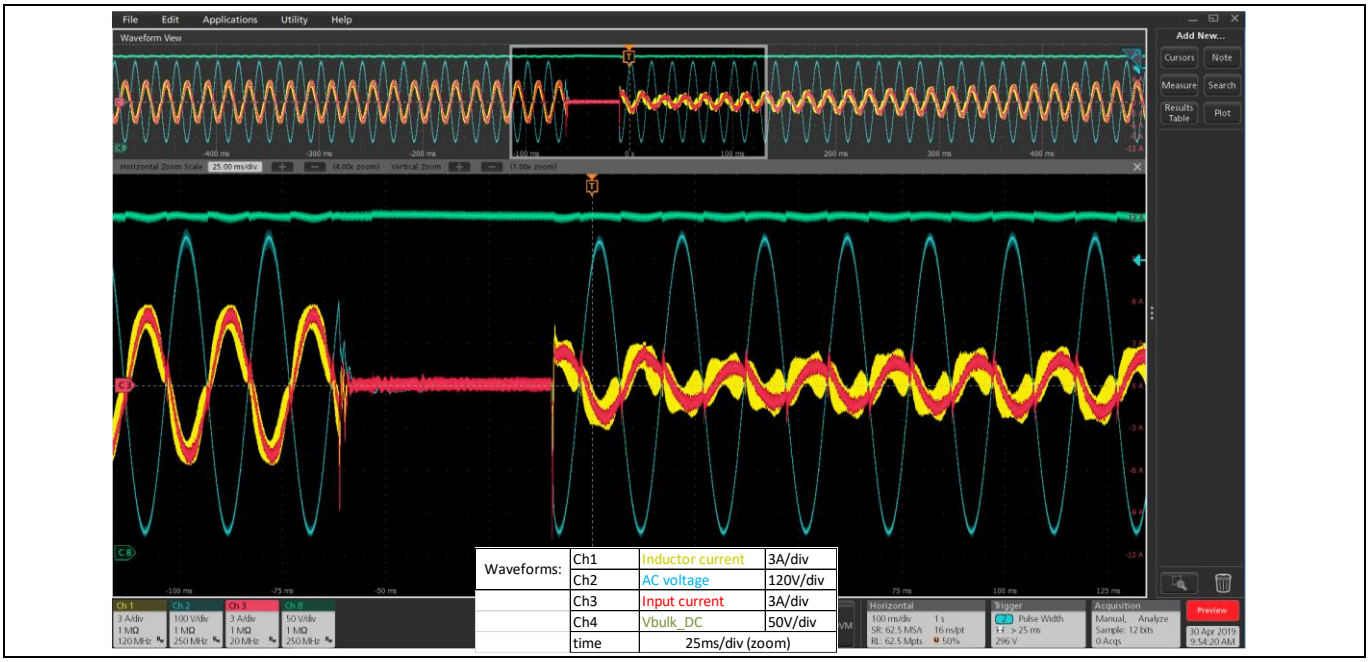

Figure 33 Detail of the inverter behavior under AC-line drop-out of 50 ms for 800 W power

3.3.2 Voltage sag and AC voltage variation

The behavior shown previously occurs when the AC voltage drops to zero. In case the AC voltage is under the AC voltage limit specified in Table 4, the inverter will stop operation and open the NTC relay. After a defined time the inverter resumes operation with soft-start after closing the relay, provided that the AC voltage has returned to the nominal range. Figure 34 shows a voltage sag from 230 to 115 V for 200 ms with 2.5 kW injected into the grid emulator, in which the sequence shown can be recognized.

Figure 34 115 V/200 ms voltage sag from 230 V at 2.5 kW inverter operation

In case the AC voltage is out of range for a time shorter than 100 ms, when the AC voltage returns to range a higher current is momentarily demanded by the inverter. This increase in the current, together with the slow voltage loop of the DC-DC supplying the bulk voltage, produces an over-current in the DC-DC low-voltage side. This over-current can trigger Over-Current Protection (OCP) in the DC-DC stage. Figure 35 – left, shows a successful voltage sag of 100 ms from 230 to 115 V with 380 W output power. However, when the power is increased to 880 W the increase in the AC current during the transition transfers into an increase in the low-voltage current and DC-DC OCP (68 A) is triggered. After that, the DC-DC converter stops and bulk voltage reaches down to 350 V, and thus the DC-AC totem-pole latches operation.

Figure 35 115 V voltage sag from 230 V applied during 100 ms at 380 W (left) and 880 W (right)

The same behavior can be expected even with variations within the normal AC range. Figure 36 shows two examples of 265 to 176 V steps in the AC voltage for different power levels. When the power increases, OCP in the DC-DC stage can also be triggered, as shown above.

Figure 36 265 to 176 V AC voltage variation for 960 W (left) and 1200 W (right) in inverter operation

4 Thermal measurements

The board shown in this document (EVAL_3K3W_TP_PFC_SIC) is not provided with an enclosure. The implemented thermal concept uses a low-power fan attached to the main heatsink, in which the power semiconductors dissipate their generated losses. The PFC choke is behind the heatsink and also receives the airflow from the implemented fan.

As can be seen, especially for AC voltages in the lower part of the range, the hotspot of the board is the PFC choke. As introduced above, the PFC choke is implemented with a high-flux EQ core and helical flat wire. The obtained form factor of this design enables high efficiency and increased power density, while keeping the height requirement. The main disadvantage is the heat dissipation, since there are only two small contacts to dissipate the winding heat through the PCB and the enclosed core limits the airflow from the implemented fan. Therefore, a more powerful fan in an enclosed environment might be required in the final application.

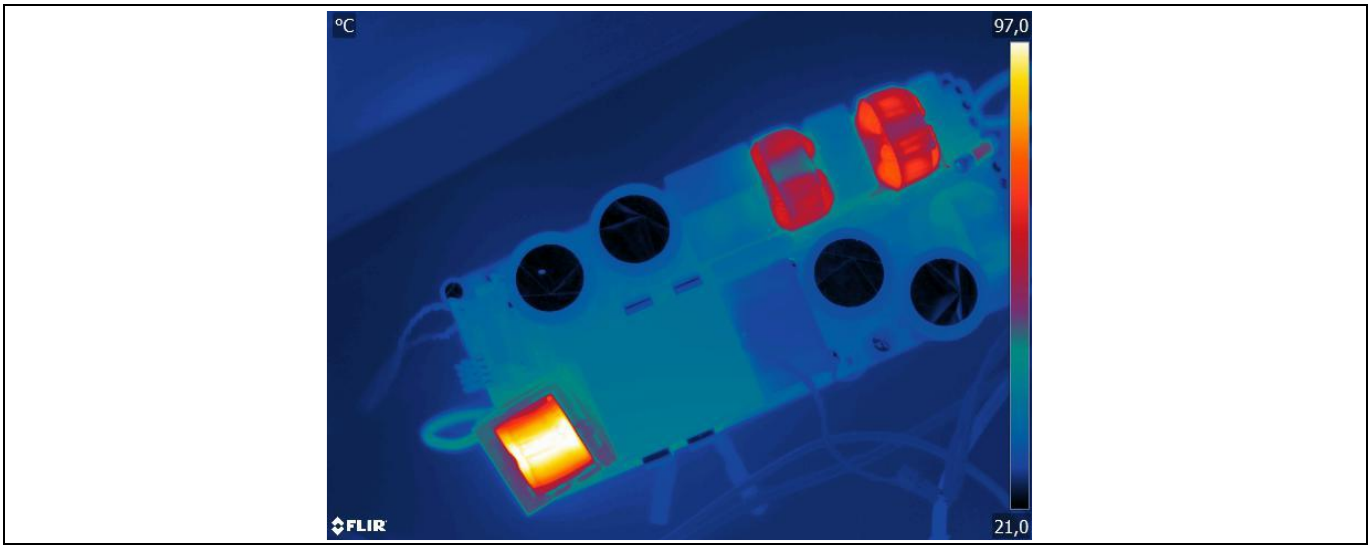

Figure 37 Thermal capture at room temperature of EVAL_3K3W_TP_PFC_SIC at nominal input (230 V) and full-load (3.3 kW) conditions for PFC operation

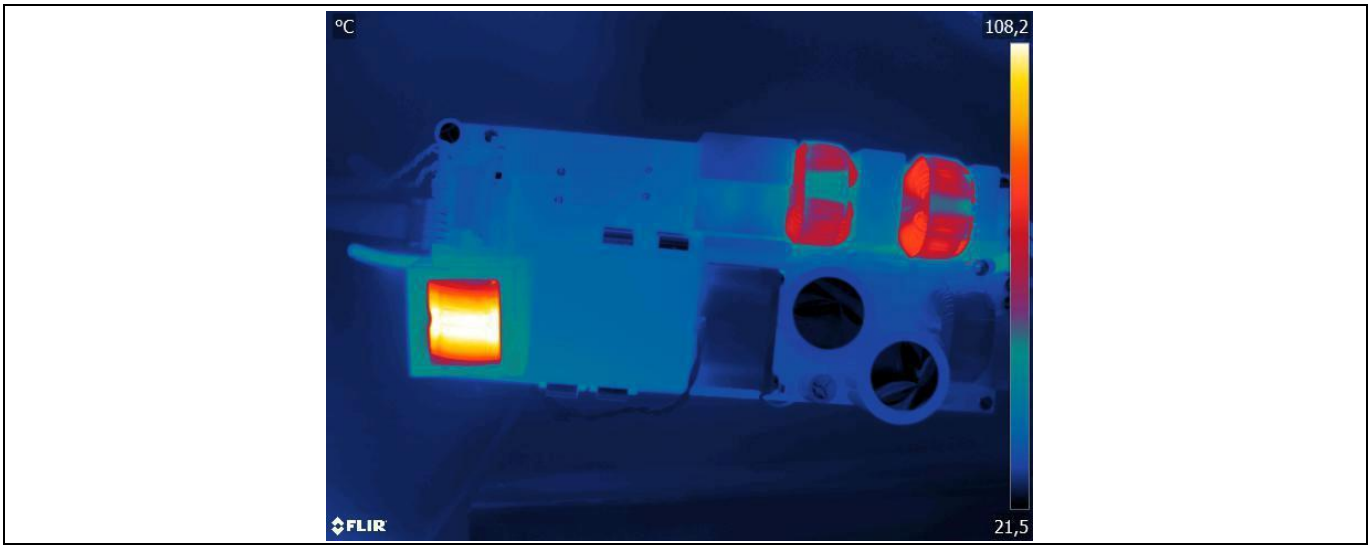

Figure 38 Thermal capture at room temperature of EVAL_3K3W_TP_PFC_SIC at minimum AC voltage (176 V) and full-load (3 kW) conditions for inverter operation

5 Summary

This document introduced an Infineon system solution for bridgeless totem-pole PFC, which achieves a peak efficiency of 99 percent with a 1U form factor and a power density of 73 W/in^3. The totem-pole PFC topology is enabled by using an Infineon 650 V CoolSiC™ silicon carbide MOSFET. The combination of the wide band-gap switches and 600 V CoolMOS™ C7 enables high performance in a compact form factor, as presented in this application note. The bridgeless topology implements full digital control on an XMC™ 1000 series Infineon microcontroller.

The EVAL_3K3W_TP_PFC_SIC board has been tested using programmable AC source and electronic load to demonstrate the power line disturbance behavior or dynamic load conditions in PFC operation. But the bi-directional DC-DC phase-shift full-bridge board from Infineon (EVAL_3K3W_BIDI_PSFB) has also been used for both the PFC and inverter test.

Digital control enables the utilization of the inherent bi-directional power flow capability of the bridgeless totem-pole topology of EVAL_3k3W_TP_PFC_SIC. The power flow must be selected before starting the board, by using an incorporated switch in the main board. The bi-directional solution presented in this document is not prepared for dynamic change in the power flow.

The performance of the board in PFC operation complies with power line disturbance and hold-up time. In the case of inverter operation, the dynamic load and power line disturbance behavior has been adapted by introducing soft transitions. The interaction with the DC-DC converter and the influence of AC variations in inverter operation is also discussed in the application note.

6 Schematics

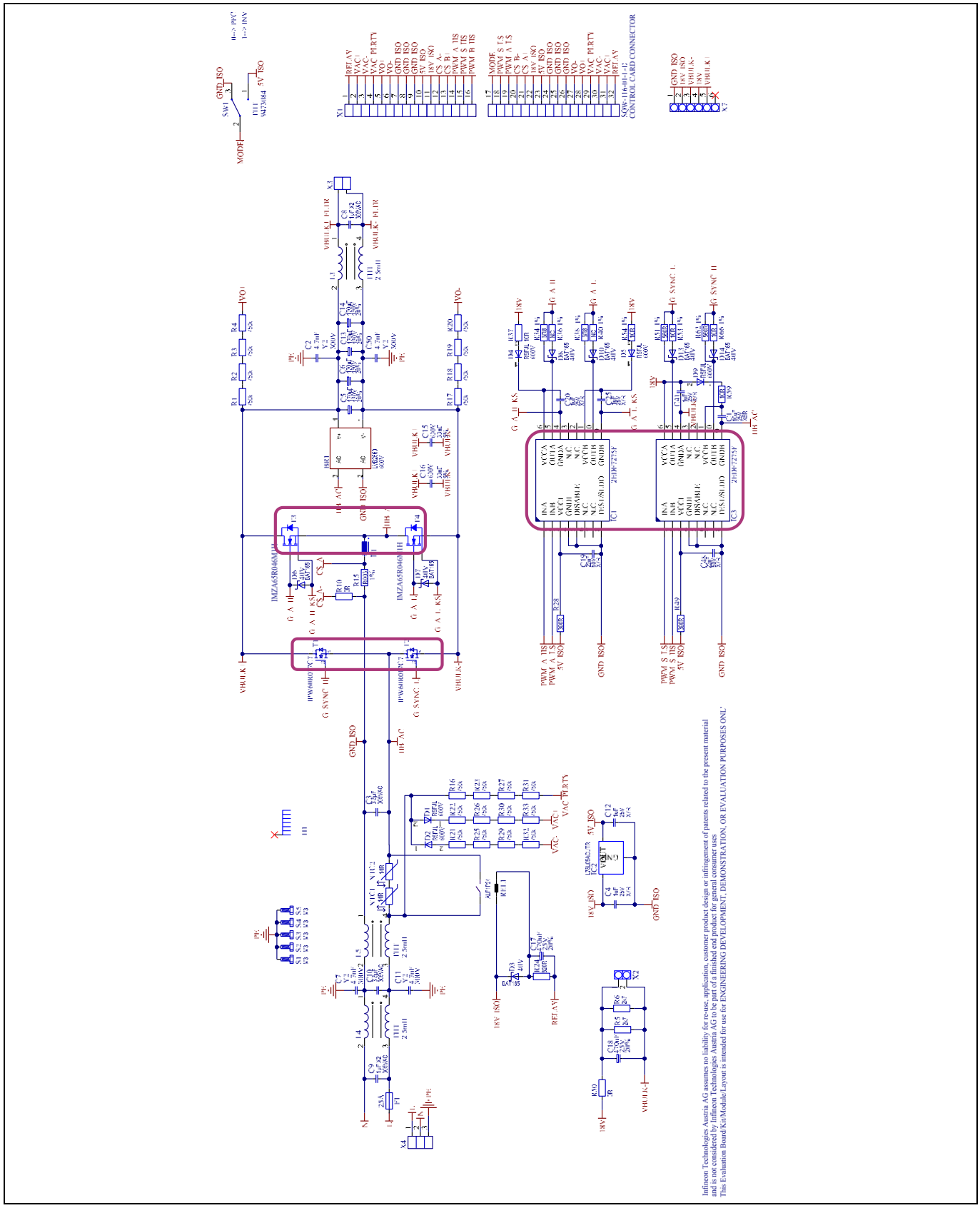

Figure 39 **EVAL_3K3W_TP_PFC_SIC main board schematic, which includes control board, bias board and fan connectors, as well as the PFC/inverter selection switch. Infineon devices are highlighted.**

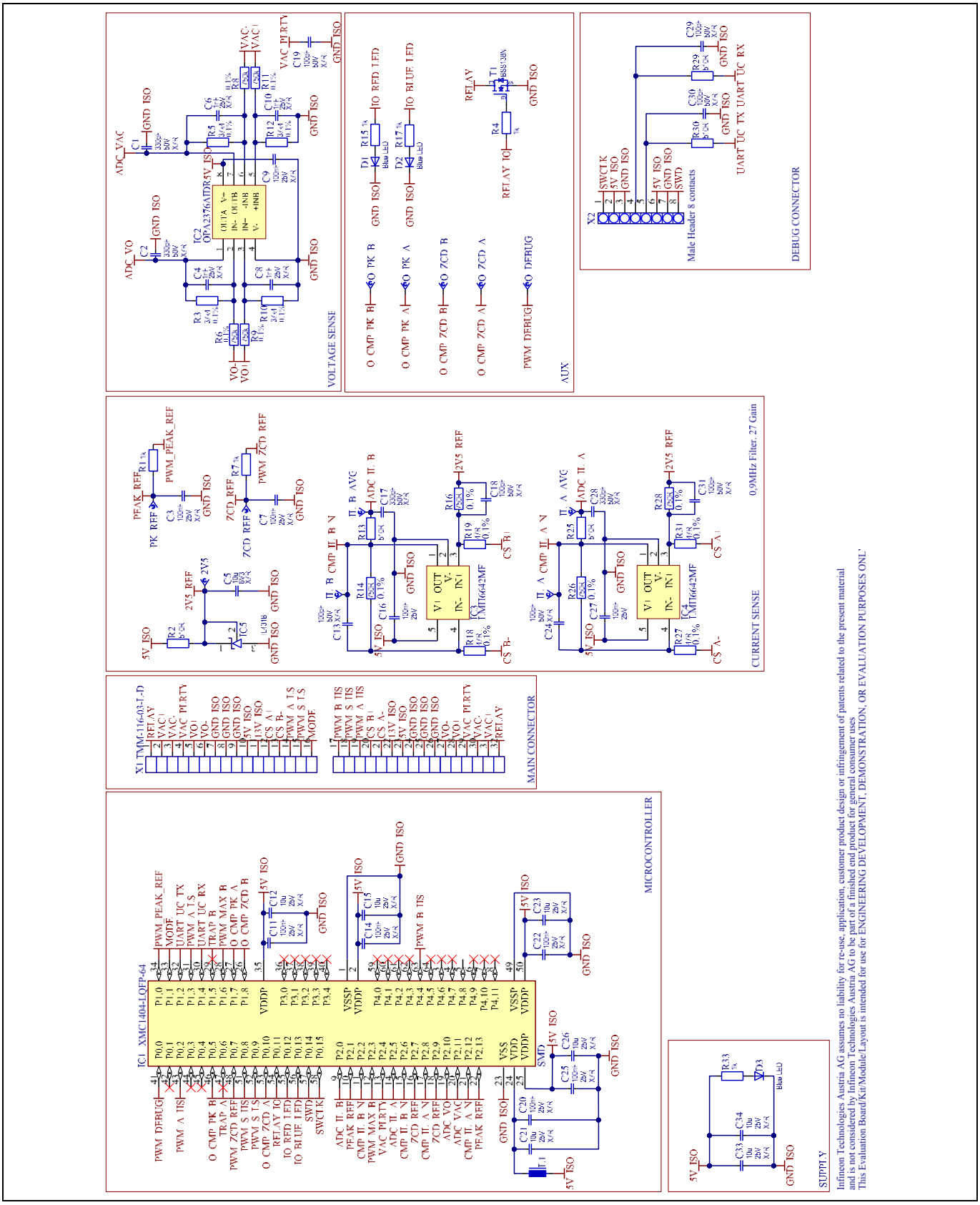

Figure 40 Control card schematic in EVAL_3K3W_TP_PFC_SIC with XMC1404

7 Bill of Materials (BoM)

Table 5 Main board components in EVAL_3K3W_TP_PFC_SIC

Designator	Value	Tolerance	Voltage	Description
T1, T2	**IPW60R017C7**		**600 V**	**MOSFET**
T3, T4	**IMZA65R048M1**		**650 V**	**N-channel MOSFET**
IC1, IC3	**2EDF7275F**			**Integrated circuit**
BR1	LVB2560		600 V	Bridge diode
C1	10 µF	X5R	25 V	Ceramic capacitor
C2, C7, C11, C50	4.7 nF	Y2	300 V	Ceramic capacitor
C3, C10	3.3 µF	10 percent	305 V AC	Foil capacitor
C4, C12, C20, C41	1 µF	X7R	25 V	Ceramic capacitor
C5, C6, C13, C14	470 µF	20 percent	450 V	Polarized capacitor
C8, C9	1 µF X2	20 percent	305 V AC	Foil capacitor
C15, C16	33 nF	5 percent	630 V	Foil capacitor
C17	470 µF	20 percent	25 V	Polarized capacitor
C19, C48	22 nF	X7R	50 V	Ceramic capacitor
C25	1 µF	X7R	25 V	Ceramic capacitor
D1, D2, D4, D5, D9	RSFJL		600 V	Diode
D3, D6, D7, D8, D10, D13, D14	BAT165		40 V	Schottky diode
F1	25 A			Fuse
H1	LAM4K05024		24 V	Heatsink
IC2	L78L05ACUTR			Integrated circuit
L1	500 µH			Inductor
L3, L4, L5	2.5 mH			Inductor
NTC1, NTC2	14 R	25 percent		NTC resistor
R1, R2, R3, R4, R16, R17, R18, R19, R20, R21, R22, R23, R25, R26, R27, R29, R30, R31, R32, R33	750 k	1 percent		Resistor
R5, R6	2k7	1 percent		Resistor
R10	0 R	1 percent		Resistor
R15	R003	1 percent		Resistor
R24	820 R	1 percent		Resistor
R28, R49	390 R	1 percent		Resistor
R34, R38	6R8	1 percent		Resistor
R37, R54, R59	10 R	1 percent		Resistor
R50	0 R	1 percent		Resistor
R51, R62	560 R	1 percent		Resistor
R53, R66	10 R	1 percent		Resistor
REL1	ALF1P24		24 V	Relais
SW1	2AS1T2A1M2RES			Toggle switch
X1	SQW-116-01-L-D			Pin header 2 x 16
X2				Female header, 2 contacts
X3	MKDS 5/3-6,35 – 1714955			AC connector
X4	MKDS 5/3-6,35 – 1714968			DC connector

Table 6 Control board components in EVAL_3K3W_TP_PFC_SIC

Designator	Value	Tolerance	Voltage	Description
IC1	**XMC1404-LQFP-64**			**Integrated circuit**
T1	**BSS138N**			**MOSFET**
C1, C2, C17, C28	330 pF	X7R	50 V	Ceramic capacitor
C3, C7, C9, C11, C14, C16, C20, C22, C25, C27	100 nF	X7R	25 V	Ceramic capacitor
C4, C6, C8, C10	1 nF	X7R	25 V	Ceramic capacitor
C5	10 µF	X7R	6V3	Ceramic capacitor
C12, C15, C21, C23, C26, C33, C34	10 µF	X7R	25 V	Ceramic capacitor
C13, C18, C19, C24, C29, C30, C31	100 pF	X7R	50 V	Ceramic capacitor
D1, D2, D3	Blue LED			LED diode
IC2	OPA2376AIDR			Integrated circuit
IC3, IC4	LMH6642MF			Integrated circuit
IC5	TL431B	0.50 percent		Integrated circuit
L1	Ferrite bead 60 Ω at 100 MHz			Inductor
R1, R4, R7, R15, R17, R33	1 k	1 percent		Resistor
R2, R13, R25, R29, R30	510 R	1 percent		Resistor
R3, R5, R10, R12	37k4	0.10 percent		Resistor
R6, R8, R9, R11	750 k	0.10 percent		Resistor
R14, R16, R26, R28	750 R	0.10 percent		Resistor
R18, R19, R27, R31	47 R	0.10 percent		Resistor
X1	TMM-116-03-L-D			Pin header 2 x 16 contacts

8 References

[1] Q. Huang and A. Q. Huang, “Review of GaN totem-pole bridgeless PFC”, in CPSS Transactions on Power Electronics and Applications, vol. 2, no. 3, pp. 187–196, Sept. 2017.

[2] “XMC1400 AA-Step Reference Manual”, August 2016. Available online.

[3] “800 W Platinum® server power supply, using 600 V CoolMOS™ C7 and digital control with XMC™”. AN_201707_PL52_022.

[4] “PFC demo board – system solution. High power density 800 W 130kHz Platinum server design”. Application note.

[5] “High-efficiency 3 kW bridgeless dual-boost PFC demo board; 90 kHz digital control design based on 650 V CoolMOS™ C7 in TO-247 4-pin”. AN_201708_PL52_025.

[6] “3300 W 54 V bi-directional phase-shift full-bridge with 600 V CoolMOS™ CFD7 and XMC™”, EVAL_3K3W_BIDI_PSFB. AN_1809_PL52_1809_081412.

Revision history

Major changes since the last revision

Page or reference	Description of change

Other Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2020-01-14

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AN_1911_PL52_1912_141352

IMPORTANT NOTICE

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

单击下面可查看定价，库存，交付和生命周期等信息

>>Infineon(英飞凌)