

# BGT24ATR12

Silicon Germanium 24 GHz Transceiver MMIC

## Data Sheet

Revision 3.1, 2014-07-15

RF & Protection Devices

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**BGT24ATR12 Silicon Germanium 24 GHz Transceiver MMIC**

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**Previous Revision: 2013-09-10, Revision 3.0**

| Page | Subjects (major changes since last revision)                   |
|------|--|
| 25   | update recommended footprint drawing (change of ground plains) |
|      |  |
|      |  |
|      |  |
|      |  |

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## 1 Features

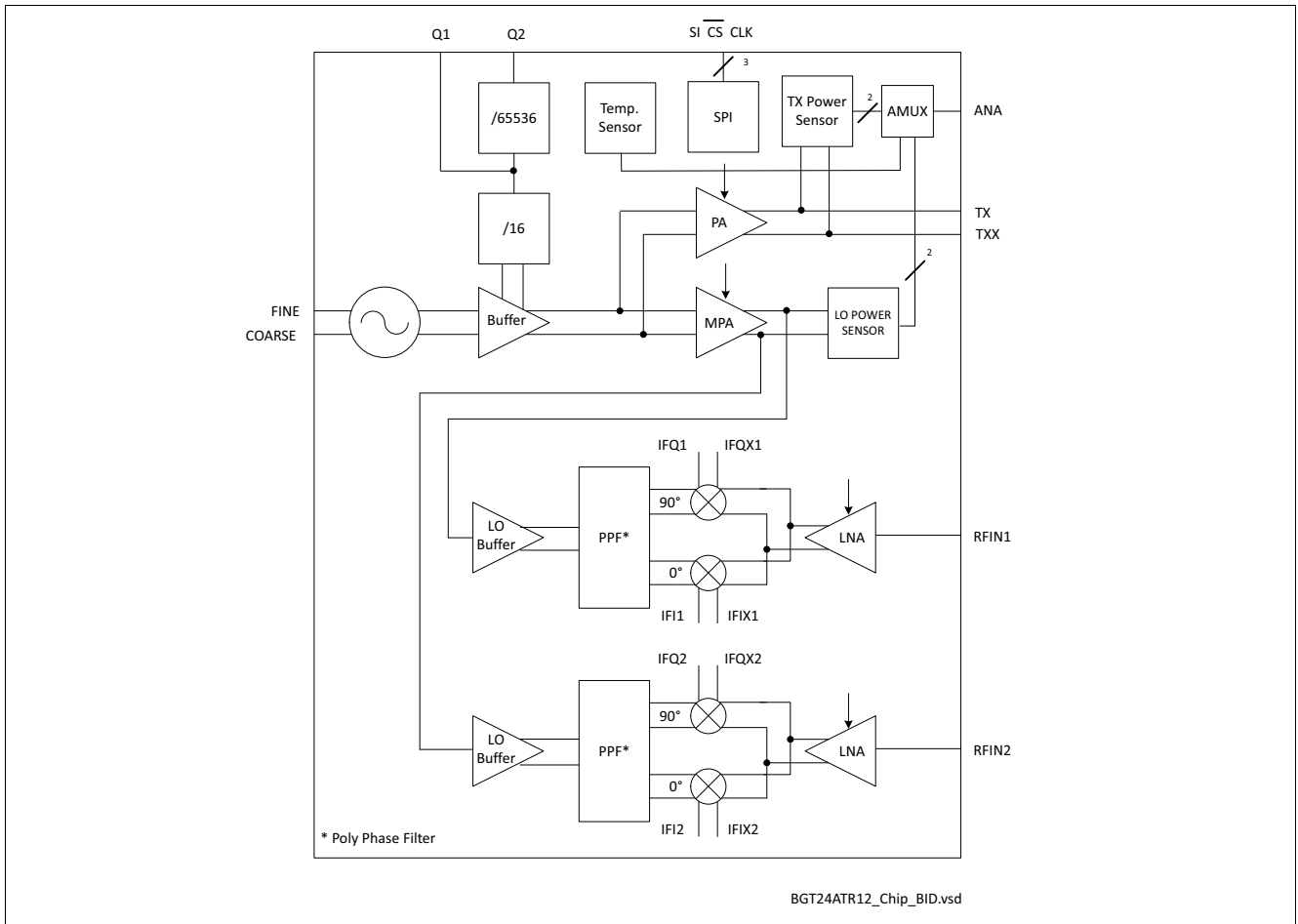
- 24 GHz ISM band transceiver MMIC with one transmitter and two receiver units
- Qualified according AEC-Q100
- Fully integrated low phase noise VCO
- Switchable prescaler with 1.5 GHz and 23 kHz output
- On chip power and temperature sensors
- Gilbert based homodyne quadrature receiver
- Single ended RF input terminals
- Low noise figure  $NF_{SSB}$ : 12 dB
- High conversion gain: 26 dB
- High 1 dB input compression point: -12 dBm
- Single supply voltage 3.3 V
- Low power consumption 690 mW
- 200 GHz bipolar SiGe:C technology b7hf200
- Fully ESD protected device
- VQFN-32-9 leadless plastic package incl. LTI feature
- Pb-free (RoHS compliant) package



### Description

The BGT24ATR12 is a Silicon Germanium MMIC for signal generation and reception, operating in the 24 GHz ISM band from 24.00 to 24.25 GHz. It is based on a 24 GHz fundamental voltage controlled oscillator. A switchable frequency prescaler is included with output frequencies of 1.5 GHz and 23 kHz. The main RF output delivers typ. 11 dBm signal power to feed an antenna. A RC polyphase filter (PPF) is used for LO quadrature phase generation of the homodyne quadrature downconversion mixer. Output power sensors as well as a temperature sensor are implemented for monitoring purposes. The device is controlled via SPI and is manufactured in a 0.18 $\mu$ m SiGe:C technology offering a cutoff frequency of 200 GHz. The MMIC is packaged in a 32 pin leadless RoHS compliant VQFN package.

| Product Name | Package  | Chip  | Marking    |
|--------------|----------|-------|------------|
| BGT24ATR12   | VQFN32-9 | T0825 | BGT24ATR12 |



**Figure 1 BGT24ATR12 Block Diagram**



## 2 Electrical Characteristics

### 2.1 Absolute Maximum Ratings

$T_A = -40\text{ °C}$  to  $125\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)<sup>1)</sup>

**Table 1 Absolute Maximum Ratings**

| Parameter   | Symbol            | Values  |      |      | Unit    | Note / Test Condition   |
|---|-------------------|---------|------|------|---------|---|
|   |                   | Min.    | Typ. | Max. |         |   |
| Supply voltage  | $V_{CC}$          | -0.3    | –    | 3.6  | V       | –   |
| DC voltage at RF Pins TX, TXX, RFIN1, RFIN2           | $VDC_{RF}$        | 0       | –    | 0    | V       | MMIC provides short circuit to GND for all RF pins                            |
| DC voltage at Pins IFI1/2, IFIX1/2, IFQ1/2, IFQX1/2   | $VDC_{IF}$        | 0       | –    | Vcc  | V       | –   |
| DC current into Pins IFI1/2, IFIX1/2, IFQ1/2, IFQX1/2 | $I_{IF}$          | -8.5    | –    | 3.5  | mA      | max. values indicate current due to short circuit to GND and Vcc respectively |
| DC voltage at Pin ANA                                 | $VDC_{ANA}$       | -0.3    | –    | 3.6  | V       | –   |
| DC current into Pin ANA (Sink)                        | $I_{ANA\ SINK}$   | 125     | 350  | 500  | $\mu$ A | max. values indicate current due to short circuit to GND and Vcc respectively |
| DC current into Pin ANA (Source)                      | $I_{ANA\ SOURCE}$ | -7      | –    | –    | mA      | –   |
| DC voltage at Pin Q1                                  | $VDC_{Q1}$        | Vcc-0.3 | –    | Vcc  | V       | –   |
| DC current into Pin Q1                                | $I_{Q1}$          | -8      | –    | 12   | mA      | –   |
| DC voltage at Pin Q2                                  | $VDC_{Q2}$        | -0.3    | –    | 3.6  | V       | –   |
| DC current into Pin Q2 enabled                        | $I_{Q2EN}$        | -3      | –    | 3    | mA      | –   |
| DC current into Pin Q2 disabled                       | $I_{Q2DIS}$       | -10     | –    | 10   | $\mu$ A | –   |
| DC voltage at SPI input Pins SI, CLK, CS              | $VDC_{SPIIN}$     | -0.3    | –    | 3.6  | V       | –   |
| DC current into SPI input Pins SI, CLK, CS            | $I_{SPIIN}$       | –       | –    | 3    | mA      | –   |
| RF input power into Pins RFIN1, RFIN2                 | $P_{RF}$          | –       | –    | 0    | dBm     | –   |
| DC voltage at Pins Fine, Coarse                       | $V_F, V_C$        | 0       | –    | 5    | V       | –   |

1) Not subject to production test, specified by design

**Table 1 Absolute Maximum Ratings (cont'd)**

| Parameter                         | Symbol     | Values |      |      | Unit | Note / Test Condition  |
|-----------------------------------|------------|--------|------|------|------|--|
|                                   |            | Min.   | Typ. | Max. |      |  |
| DC current into Pins FINE, COARSE | $I_F, I_C$ | -110   | –    | 110  | μA   | Positive currents if $V_{TUNE} > V_{CC}$ ; Negative currents if $0V \leq V_F, V_C \leq V_{CC}$ |
| Total power dissipation           | $P_{DISS}$ | –      | –    | 1050 | mW   | With BIST deactivated  |
| Junction temperature              | $T_J$      | -40    | –    | 170  | °C   | –  |
| Ambient temperature range         | $T_A$      | -40    | –    | 125  | °C   | $T_A$ = temperature at package soldering point   |
| Storage temperature range         | $T_{STG}$  | -40    | –    | 150  | °C   | –  |

**Attention: Stresses exceeding the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.**

## 2.2 Thermal Resistance

**Table 2 Thermal Resistance**

| Parameter                                | Symbol     | Values |      |      | Unit | Note / Test Condition |
|--|------------|--------|------|------|------|-----------------------|
|  |            | Min.   | Typ. | Max. |      |                       |
| Junction - soldering point <sup>1)</sup> | $R_{thJS}$ | –      | –    | 40   | K/W  | –                     |

1) For calculation of  $R_{thJS}$  please refer to application note thermal resistance

## 2.3 ESD Integrity

**Table 3 ESD Integrity**

| Parameter                         | Symbol        | Values |      |      | Unit | Note / Test Condition |
|-----------------------------------|---------------|--------|------|------|------|-----------------------|
|                                   |               | Min.   | Typ. | Max. |      |                       |
| ESD robustness, HBM <sup>1)</sup> | $V_{ESD-HBM}$ | -1     | –    | 1    | kV   | All pins              |
| ESD robustness, CDM <sup>2)</sup> | $V_{ESD-CDM}$ | -500   | –    | 500  | V    | All pins              |

- 1) According to ANSI/ESDA/JEDEC JS-001 (R = 1.5kΩ, C = 100pF) for Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM)-Component Level
- 2) According to JEDEC JESD22-C101 Field-Induced Charged Device Model (CDM), Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

## 2.4 Measured RF Characteristics

### 2.4.1 Power Supply

**Table 4** Typical Characteristics  $T_A = -40 \dots 125 \text{ }^\circ\text{C}$ , SPI-Bit 4 = low

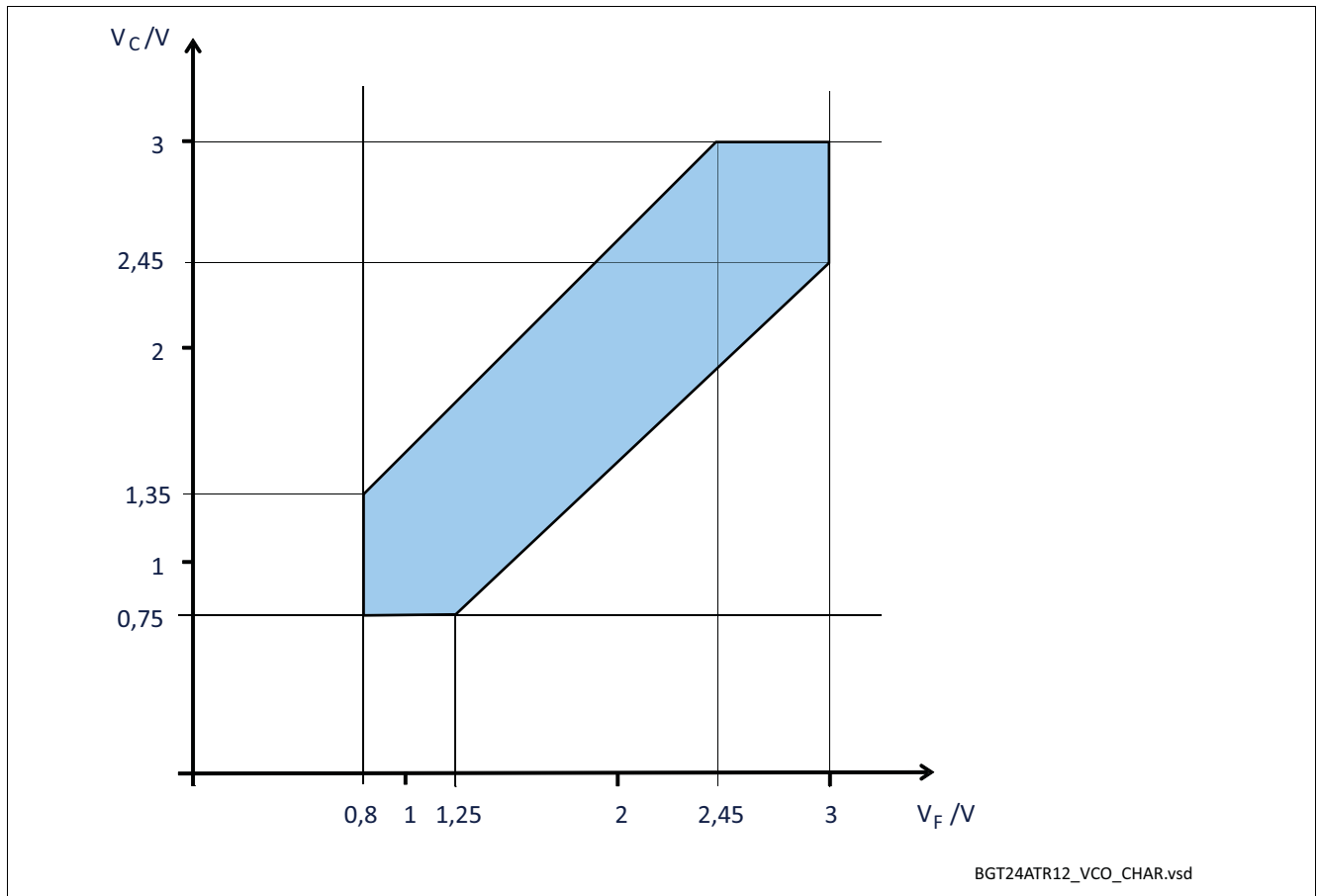
| Parameter                          | Symbol   | Values |      |       | Unit | Note / Test Condition  |
|------------------------------------|----------|--------|------|-------|------|--|
|                                    |          | Min.   | Typ. | Max.  |      |  |
| Supply voltage                     | $V_{CC}$ | 3.135  | 3.3  | 3.465 | V    | –  |
| Supply current                     | $I_{CC}$ | 150    | 210  | 270   | mA   | Max. TX output power, all prescalers are activated, LO and TX output buffer in high mode |
| Supply current - special condition | $I_{CC}$ | –      | –    | 250   | mA   | If $V_{CC,max}=3.3\text{V}$ and $T_{min}>-20^\circ\text{C}$                              |

### 2.4.2 TX Section

**Table 5** Typical Characteristics  $T_A = -40 \dots 125 \text{ }^\circ\text{C}$ ,  $f = 24.0 \dots 24.25 \text{ GHz}$ , SPI-Bit 4 = low<sup>1)</sup>

| Parameter                               | Symbol                     | Values             |      |       | Unit  | Note / Test Condition  |
|---|----------------------------|--------------------|------|-------|-------|--|
|   |                            | Min.               | Typ. | Max.  |       |  |
| VCO frequency range                     | $f_{VCO}$                  | 24.0               | –    | 24.25 | GHz   | –  |
| VCO fine tuning voltage <sup>2)</sup>   | $V_F$                      | 0.8 <sup>3)</sup>  | –    | 3.0   | V     | $0.8\text{V} \leq V_F \leq 1.25\text{V}$ for $V_{C_{MIN}}=0.75\text{V}$ ,<br>$1.25\text{V} \leq V_F \leq 3.0\text{V}$ for $V_{C_{MIN}}=0.75\text{V}+1.7\text{V}*(V_F-1.25\text{V})/1.75\text{V}$ , see Figure 2 on Page 12 |
| VCO coarse tuning voltage <sup>2)</sup> | $V_C$                      | 0.75 <sup>3)</sup> | –    | 3.0   | V     | $0.75\text{V} \leq V_C \leq 1.35\text{V}$ for $V_{F_{MIN}}=0.8\text{V}$ ,<br>$1.35\text{V} \leq V_C \leq 3.0\text{V}$ for $V_{F_{MIN}}=V_C-0.55\text{V}$ , see Figure 2 on Page 12   |
| VCO tuning slope FINE                   | $\Delta f / \Delta V_F$    | 200                | –    | 1000  | MHz/V | $24\text{GHz} \leq f \leq 24.25\text{GHz}$ see Figure 2 on Page 12   |
| VCO tuning slope COARSE                 | $\Delta f / \Delta V_C$    | 400                | –    | 2000  | MHz/V | $24\text{GHz} \leq f \leq 24.25\text{GHz}$ see Figure 2 on Page 12   |
| VCO temperature drift                   | $\Delta f / \Delta T$      | -10                | -6   | 0     | MHz/K | Min @ $T = -40^\circ\text{C}$  |
| VCO pushing                             | $\Delta f / \Delta V_{CC}$ | -350               | 60   | 350   | MHz/V | Absolute values  |

- 1) Performance based on Application Circuit Figure 3 on Page 16, Cross Section of Application Board, Compensation Structures and Application Board Layout Figure 5 on Page 22ff and Footprint Figure 9 on Page 25
- 2) At tuning pins chipinternal pull-up of  $60k\Omega \pm 20\%$  to VCC; max.- and min. temperature tuning voltage limits are chosen in a way that they can be linearly interpolated within operating temperature range
- 3) Specified min. value for temperature  $\leq 25^\circ\text{C}$ ; min. value for temperatures  $>25^\circ\text{C}$  is based on following formular  $V_{\text{CMIN}} = V_{\text{FMIN}} = 0.8\text{V} + 0.4\text{V} * (T [^\circ\text{C}] - 25^\circ\text{C}) / 100^\circ\text{C}$



**Figure 2 VCO Tuning Window**

**Table 6 Typical Characteristics  $T_A = -40 .. 125^\circ\text{C}$ ,  $f = 24.0 .. 24.25\text{ GHz}$ , SPI-Bit 4 = low<sup>1)</sup>**

| Parameter   | Symbol                              | Values |                          |      | Unit     | Note / Test Condition                                |
|---|-------------------------------------|--------|--------------------------|------|----------|--|
|   |                                     | Min.   | Typ.                     | Max. |          |  |
| VCO phase noise   | $P_N$                               | –      | -85                      | -75  | dBc/Hz   | @ 100kHz offset,<br>$V_F = V_C$                      |
| TX/TXX load impedance   | $Z_{\text{TX}}$<br>$Z_{\text{TXX}}$ | –      | 20.8-j20.2<br>19.5-j11.7 | –    | $\Omega$ | Typical value at<br>24.125GHz and<br>VSWR $\leq 2:1$ |
| Max. TX output power  | $P_{\text{TX}}$                     | 6      | 11                       | 15   | dBm      | –  |
| Max. TX output power for<br>$V_{\text{CC}} = 3.3\text{V} \pm 50\text{mV}$ | $P_{\text{TX}}$                     | 6.5    | 11                       | 14.5 | dBm      | –  |
| TX output power adjustable<br>range                                       | $a_{\text{TX}}$                     | 3      | 9                        | –    | dB       | Adjustable via SPI                                   |

**Table 6** Typical Characteristics  $T_A = -40 .. 125 \text{ }^\circ\text{C}$ ,  $f = 24.0 .. 24.25 \text{ GHz}$ , SPI-Bit 4 = low<sup>1)</sup>

| Parameter                                      | Symbol                    | Values |          |      | Unit       | Note / Test Condition   |
|--|---------------------------|--------|----------|------|------------|---|
|  |                           | Min.   | Typ.     | Max. |            |   |
| TX output power in "off" mode <sup>2)</sup>    | $P_{\text{TXoff}}$        | –      | –        | -30  | dBm        | Parameter based on IFX eval board design                            |
| Q1 Prescaler division ratio                    | $D_{\text{Q1}}$           | –      | $2^4$    | –    | –          | –   |
| Q1 Prescaler output power                      | $P_{\text{Q1}}$           | -14    | -9       | -4   | dBm        | Q1 loaded with 50 Ohm (AC- coupled)                                 |
| Q1 output impedance <sup>2)</sup>              | $Z_{\text{Q1}}$           | –      | 50       | –    | $\Omega$   | –   |
| Q2 Prescaler division ratio                    | $D_{\text{Q2}}$           | –      | $2^{20}$ | –    | –          | –   |
| Q2 Prescaler max. output voltage               | $V_{\text{maxQ2}}$        | 2.4    | –        | –    | V          | Test condition: Q2 loaded with high impedance probe (1 MOhm, 13 pF) |
| Q2 Prescaler min. output voltage               | $V_{\text{minQ2}}$        | –      | –        | 0.8  | V          | Test condition: Q2 loaded with high impedance probe (1 MOhm, 13 pF) |
| Q2 Prescaler max. output source current        | $I_{\text{maxsource Q2}}$ | 1.2    | –        | –    | mA         | Test condition: Q2 loaded with 50 Ohm to Vcc                        |
| Q2 Prescaler max. output sink current          | $I_{\text{maxsink Q2}}$   | 1.2    | –        | –    | mA         | Test condition: Q2 loaded with 50 Ohm to Vcc                        |
| Q2 Prescaler output resistance in disable mode | $R_{\text{Q2,DIS}}$       | 100    | –        | –    | k $\Omega$ | –   |

1) Performance based on Application Circuit Figure 3 on Page 16, Cross Section of Application Board, Compensation Structures and Application Board Layout Figure 5 on Page 22ff and Footprint Figure 9 on Page 25

2) Guaranteed by device design

### 2.4.3 RX Section

**Table 7 Typical Characteristics**  $T_A = -40 \dots 125 \text{ }^\circ\text{C}$ ,  $f = 24.0 \dots 24.25 \text{ GHz}$ , SPI-Bit 4 = low<sup>1)</sup>

| Parameter   | Symbol                                   | Values |                          |       | Unit     | Note / Test Condition   |
|---|--|--------|--------------------------|-------|----------|---|
|   |  | Min.   | Typ.                     | Max.  |          |   |
| RFIN frequency range  | $f_{\text{RFIN}}$                        | 24.0   | –                        | 24.25 | GHz      | –   |
| RFIN port impedance <sup>2)</sup>   | $Z_{\text{RFIN1}}$<br>$Z_{\text{RFIN2}}$ | –      | 15.9-j18.4<br>15.7-j18.9 | –     | $\Omega$ | Typical value at 24.125GHz and VSWR $\leq$ 2:1                        |
| RFIN VSWR   | VSWR                                     | –      | –                        | 2:1   | –        | At load port of off chip compensation network as proposed             |
| IF frequency range  | $f_{\text{IF}}$                          | 0      | –                        | 10    | MHz      | –   |
| IF output impedance   | $Z_{\text{IF}}$                          | 850    | 1000                     | 1150  | $\Omega$ | –   |
| Leakage LO to RFIN  | $L_{\text{LO} \rightarrow \text{RFIN}}$  | –      | –                        | -30   | dBm      | LO Signal Power @ RFIN Port, Parameter based on IFX eval board design |
| Isolation RFIN1 to RFIN2  | $I_{\text{RFIN1-RFIN2}}$                 | 30     | –                        | –     | dB       | Parameter based on IFX eval board design                              |
| Voltage conversion gain <sup>3)</sup>                                     | $G_C$                                    | 19     | 26                       | 31    | dB       | $R_{\text{LOAD,IF}} > 10 \text{ k}\Omega$                             |
| LNA gain reduction  | $\Delta G_{\text{CLG}}$                  | 3      | 5                        | 8     | dB       | –   |
| SSB noise figure  | $N_{\text{SSB}}$                         | –      | 12                       | 20    | dB       | Single sideband at $f_{\text{IF}} = 100 \text{ kHz}$                  |
| IF 1/f corner frequency   | $f_c$                                    | –      | 10                       | 20    | kHz      | –   |
| Input compression point   | $IP_{1\text{dB}}$                        | -17    | -12                      | –     | dBm      | –   |
| Input 3rd order intercept point   | $IIP3$                                   | -8     | -4                       | –     | dBm      | –   |
| Quadrat. phase imbalance  | $\varepsilon_p$                          | -10    | –                        | 10    | deg      | –   |
| Quadrat. phase imbalance over temperature and aging of both receivers     | $\Delta\varepsilon_p$                    | -8     | –                        | 8     | deg      | –   |
| Quadrat. amplitude imbalance  | $\varepsilon_A$                          | -1     | –                        | 1     | dB       | –   |
| Quadrat. amplitude imbalance over temperature and aging of both receivers | $\Delta\varepsilon_A$                    | -0.5   | –                        | 0.5   | dB       | –   |

1) Performance based on Application Circuit Figure 3 on Page 16, Cross Section of Application Board, Compensation Structures and Application Board Layout Figure 5 on Page 22ff and Footprint Figure 9 on Page 25

2) Guaranteed by device design

3) Lowest gain at high temperature, highest gain at low temperature

## 2.5 Temperature Sensor

Monitoring of the chip temperature is provided by the on-chip temperature sensor which delivers temperature-proportional voltage.

**Table 8 Typical Characteristics Temperature Sensor  $T_A = -40 .. 125\text{ }^\circ\text{C}^{1)}$**

| Parameter                  | Symbol                | Values |      |          | Unit             | Note / Test Condition |
|----------------------------|-----------------------|--------|------|----------|------------------|-----------------------|
|                            |                       | Min.   | Typ. | Max.     |                  |                       |
| Temperature range          | $T_{\text{TSENS}}$    | -40    | –    | 125      | $^\circ\text{C}$ | –                     |
| Output temperature voltage | $V_{\text{OUT,TEMP}}$ | –      | 1.50 | –        | V                | @ 25 $^\circ\text{C}$ |
| Sensitivity                | $S_{\text{TSENS}}$    | –      | 4.5  | –        | mV/K             | –                     |
| Overall accuracy error     | $Err_{\text{TSENS}}$  | –      | –    | $\pm 15$ | K                | –                     |

1) all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

## 2.6 Power Detector

For RF power indication, peak voltage detectors are connected to the output of the TX power amplifier and to the LO medium power amplifier. To eliminate temperature and supply voltage variations, a reference output  $V_{\text{REF}}$  is available through the ANA output for the TX and LO power sensor. The compensated detector output voltage is given by the difference between  $V_{\text{OUT}}$  and  $V_{\text{REF}}$  for both power sensors respectively. This voltage is proportional to the RF voltage swing at the individual amplifier outputs, its characteristic is non-directional.

**Table 9 Typical Characteristics Power Detector  $T_A = -40 .. 125\text{ }^\circ\text{C}$ ,  $V_{\text{CC}} = 3.3\text{ V}^{1)}$**

| Parameter       | Symbol                                       | Values |      |      | Unit | Note / Test Condition             |
|-----------------|--|--------|------|------|------|-----------------------------------|
|                 |  | Min.   | Typ. | Max. |      |                                   |
| Power range     | $P_{\text{PSENS}}$                           | -10    | –    | 15   | dBm  | –                                 |
| TX power sensor | $V_{\text{OUT,TX}}$ -<br>$V_{\text{REF,TX}}$ | –      | 550  | –    | mV   | @ $P_{\text{TX}} = 11\text{ dBm}$ |
| LO power sensor | $V_{\text{OUT,LO}}$ -<br>$V_{\text{REF,LO}}$ | –      | 50   | –    | mV   | @ typ. internal $P_{\text{LO}}$   |

1) all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

### 3 Application Circuit and Block Diagram

#### 3.1 Application Circuit Schematic

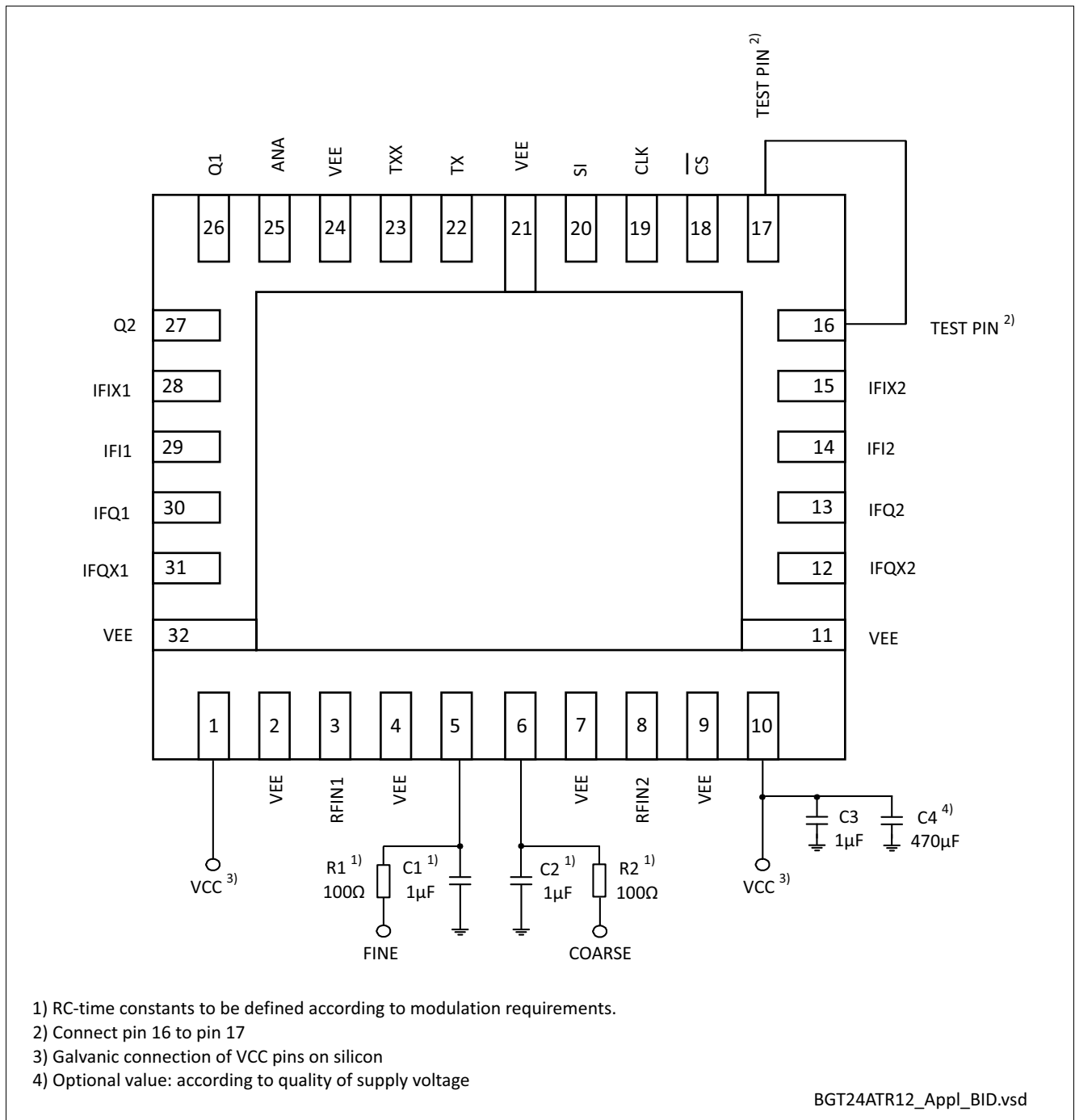


Figure 3 Application Circuit with Chip Outline (Top View)



**Table 10 Bill of Materials**

| <b>Part Number</b> | <b>Part Type</b> | <b>Manufacturer</b> | <b>Size</b> | <b>Comment</b> |
|--------------------|------------------|---------------------|-------------|----------------|
| C1 ... C4          | Chip capacitor   | Various             | Various     | –              |
| R1 ... R2          | Chip resistor    | Various             | 0402        | –              |

### 3.2 Pin Description

**Table 11 Pin Definition and Function**

| Pin No. | Name            | Function   |
|---------|-----------------|--|
| 1       | VCC             | Supply voltage   |
| 2       | VEE             | Ground   |
| 3       | RFIN1           | RF input downconverter 1                                 |
| 4       | VEE             | Ground   |
| 5       | FINE            | VCO fine tuning input                                    |
| 6       | COARSE          | VCO coarse tuning input                                  |
| 7       | VEE             | Ground   |
| 8       | RFIN2           | RF input downconverter 2                                 |
| 9       | VEE             | Ground   |
| 10      | VCC             | Supply voltage   |
| 11      | VEE             | Ground   |
| 12      | IFQX2           | Complementary quadrature phase IF output downconverter 2 |
| 13      | IFQ2            | Quadrature phase IF output downconverter 2               |
| 14      | IFI2            | In phase IF output downconverter 2                       |
| 15      | IFIX2           | Complementary in phase IF output downconverter 2         |
| 16      | TEST PIN        | Test pin; DC coupled pin                                 |
| 17      | TEST PIN        | Test pin; DC coupled pin                                 |
| 18      | $\overline{CS}$ | Chip select input SPI (inverted)                         |
| 19      | CLK             | Clock input SPI block                                    |
| 20      | SI              | Data input SPI block                                     |
| 21      | VEE             | Ground   |
| 22      | TX              | Transmit output  |
| 23      | TXX             | Complementary transmit output                            |
| 24      | VEE             | Ground   |
| 25      | ANA             | Analog output  |
| 26      | Q1              | Prescaler output 1.5GHz                                  |
| 27      | Q2              | Prescaler output 23kHz                                   |
| 28      | IFIX1           | Complementary in phase IF output downconverter 1         |
| 29      | IFI1            | In phase IF output downconverter 1                       |
| 30      | IFQ1            | Quadrature phase IF output downconverter 1               |
| 31      | IFQX1           | Complementary quadrature phase IF output downconverter 1 |
| 32      | VEE             | Ground   |

### 3.3 SPI

1.) Three signals control the serial peripheral interface of the BGT24ATR12:

SI (Data); CLK (Clock);  $\overline{CS}$  (Chip select)

2.) The data bits SI (MSB first) are read in the shift with falling edge of the CLK signal.

Please make sure, that the data is present at least 10 ns before and at least 10 ns after the falling edge of the clock signal.

3.) The CLK and  $\overline{CS}$  signals are combined internally.

At least 20 ns before first rising edge of the first CLK signal  $\overline{CS}$  needs to be in "low" state.

While the Data is read,  $\overline{CS}$  has to remain in "low" state.

4.) When Data read in is finished, the shift register content will be written in the latch at the rising edge of the  $\overline{CS}$  signal. The time between the last falling edge of the CLK signal and the rising edge of the  $\overline{CS}$  must be at least 20 ns.

**Table 12 SPI Block Data Bit Description**

| Data Bit | Name       | Description (Logic High)  | Power ON State |
|----------|------------|---|----------------|
| 15       | GS         | LNA Gain reduction  | low            |
| 14       | –          | Not used  | low            |
| 13       | AMUX2      | Analog multiplexer control bit 2  | high           |
| 12       | DIS_PA     | Disable Power Amplifier   | high           |
| 11       | Test Bit   | Test bit, must be low otherwise malfunction   | low            |
| 10       | Test Bit   | Test bit, must be low otherwise malfunction   | low            |
| 9        | Test Bit   | Test bit, must be low otherwise malfunction   | low            |
| 8        | AMUX1      | Analog multiplexer control bit 1  | low            |
| 7        | AMUX0      | Analog multiplexer control bit 0  | low            |
| 6        | DIS_DIV64k | Disable 64k divider   | low            |
| 5        | DIS_DIV16  | Disable 16 divider  | low            |
| 4        | PC2_BUF    | High LO buffer output power, need to be low otherwise increased current consumption | low            |
| 3        | PC1_BUF    | High TX buffer output power   | low            |
| 2        | PC2_PA     | TX power reduction bit 2  | high           |
| 1        | PC1_PA     | TX power reduction bit 1  | high           |
| 0        | PC0_PA     | TX power reduction bit 0  | high           |

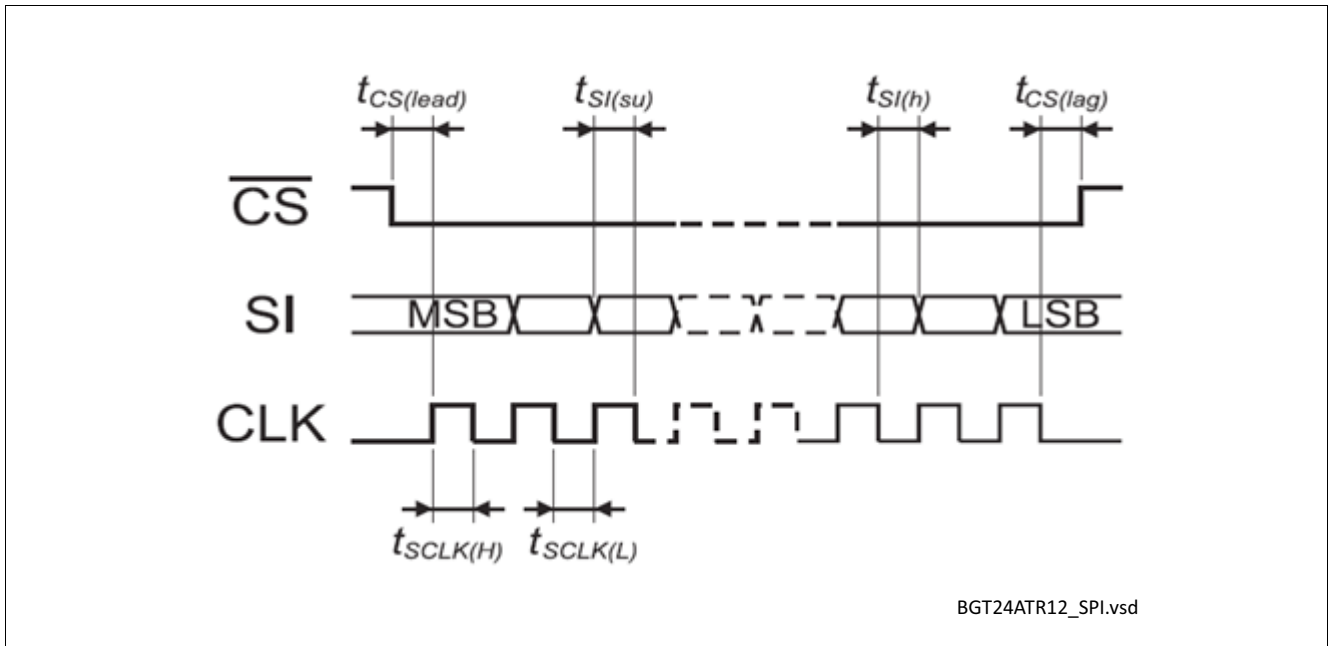


Figure 4 Timing Diagram of the SPI

Table 13 SPI Timing and Logic Levels

| Parameter                                     | Symbol         | Values |      |          | Unit    |
|---|----------------|--------|------|----------|---------|
|   |                | Min.   | Typ. | Max.     |         |
| Serial clock frequency                        | $f_{SCLK}$     | 0      | –    | 50       | MHz     |
| Serial clock high time                        | $t_{SCLK(H)}$  | 10     | –    | –        | ns      |
| Serial clock low time                         | $t_{SCLK(L)}$  | 10     | –    | –        | ns      |
| Chip select lead time                         | $t_{CS(lead)}$ | 20     | –    | –        | ns      |
| Chip select lag time                          | $t_{CS(lag)}$  | 20     | –    | –        | ns      |
| Data setup time                               | $t_{SI(su)}$   | 10     | –    | –        | ns      |
| Data hold time                                | $t_{SI(h)}$    | 10     | –    | –        | ns      |
| Low level (SI, CLK, $\overline{CS}$ )         | $V_{IN(L)}$    | 0      | –    | 0.8      | V       |
| High level (SI, CLK, $\overline{CS}$ )        | $V_{IN(H)}$    | 2.0    | –    | $V_{CC}$ | V       |
| Input capacitance (SI, CLK, $\overline{CS}$ ) | $C_{IN}$       | –      | –    | 2        | pF      |
| Input current (SI, CLK, $\overline{CS}$ )     | $I_{IN}$       | -150   | –    | 150      | $\mu A$ |

Table 14 Truth Table AMUX

| Output signal ANA | AMUX2 | AMUX1 | AMUX0 |
|-------------------|-------|-------|-------|
| $V_{OUT,TX}$      | low   | low   | low   |
| $V_{REF,TX}$      | low   | low   | high  |
| $V_{OUT,LO}$      | low   | high  | low   |
| $V_{REF,LO}$      | low   | high  | high  |
| $V_{TEMP}$        | high  | low   | low   |
| Test_Signal1      | high  | low   | high  |

**Table 14 Truth Table AMUX (cont'd)**

| <b>Output signal ANA</b> | <b>AMUX2</b> | <b>AMUX1</b> | <b>AMUX0</b> |
|--------------------------|--------------|--------------|--------------|
| Test_Signal2             | high         | high         | low          |
| Test_Signal2             | high         | high         | high         |

### 3.4 Application Board

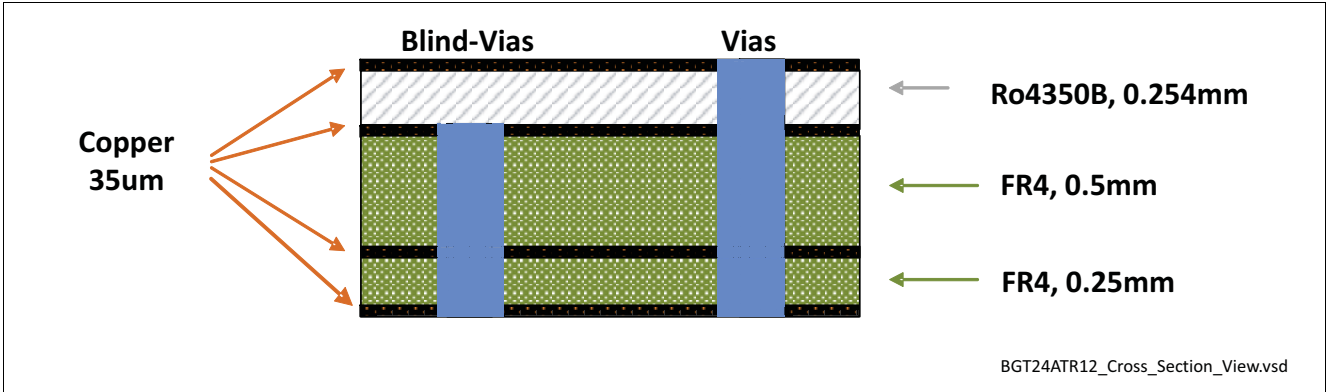


Figure 5 Cross-Section View of Application Board

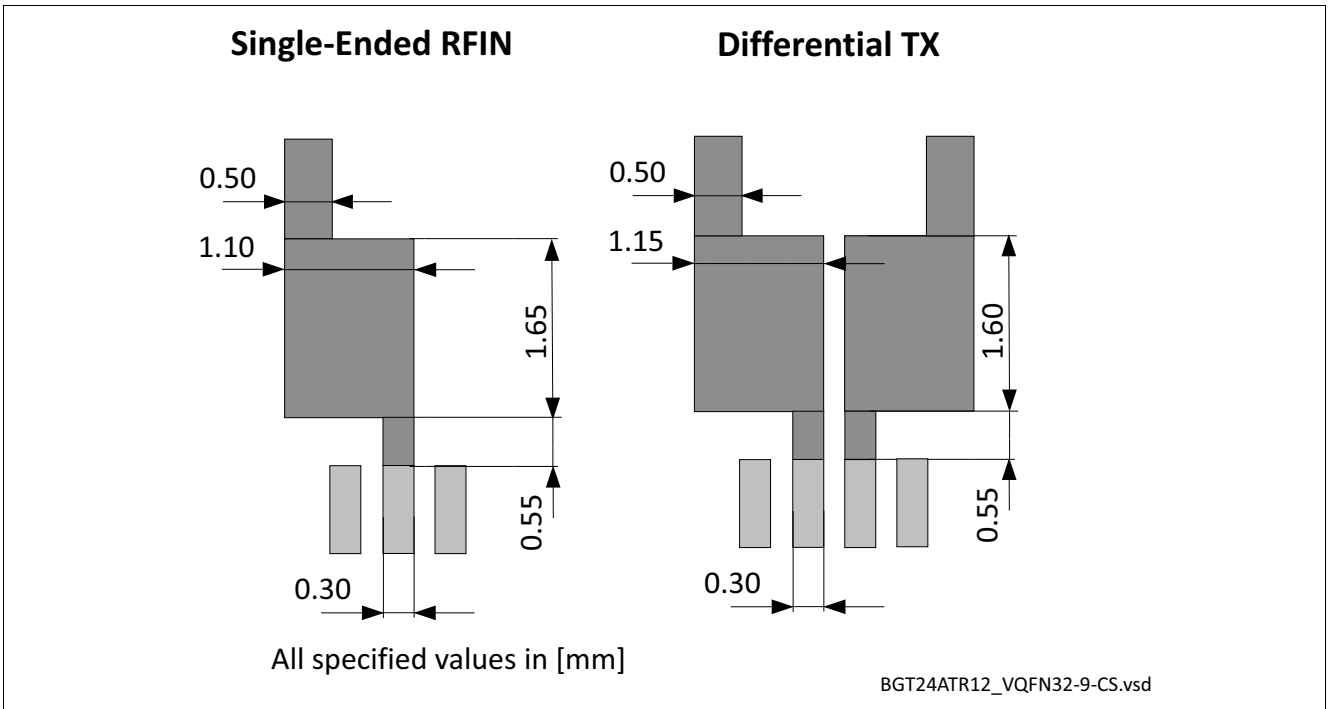
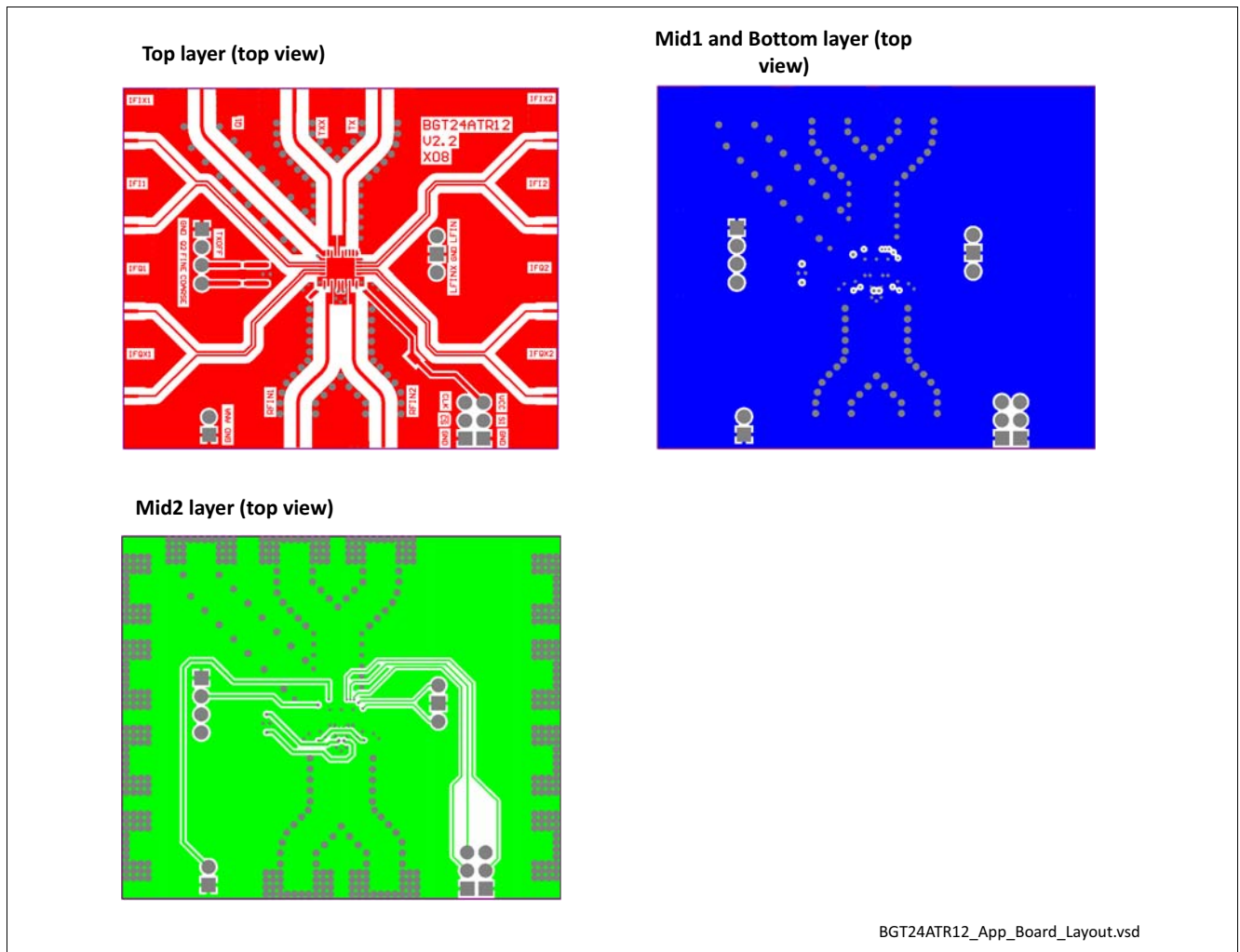


Figure 6 Detail of Compensation Structure (valid for appl. board mat. Ro4350B, 0.254mm acc. to Fig. 5)



**Figure 7 Application Board Layout**

*Note: In order to achieve the same performance as given in this datasheet please follow the suggested PCB-layout. The compensation structure is critical for RF performance. Via holes as recommended on one of next pages (not shown above).*

### 3.5 Equivalent Circuit Diagram of MMIC Interfaces

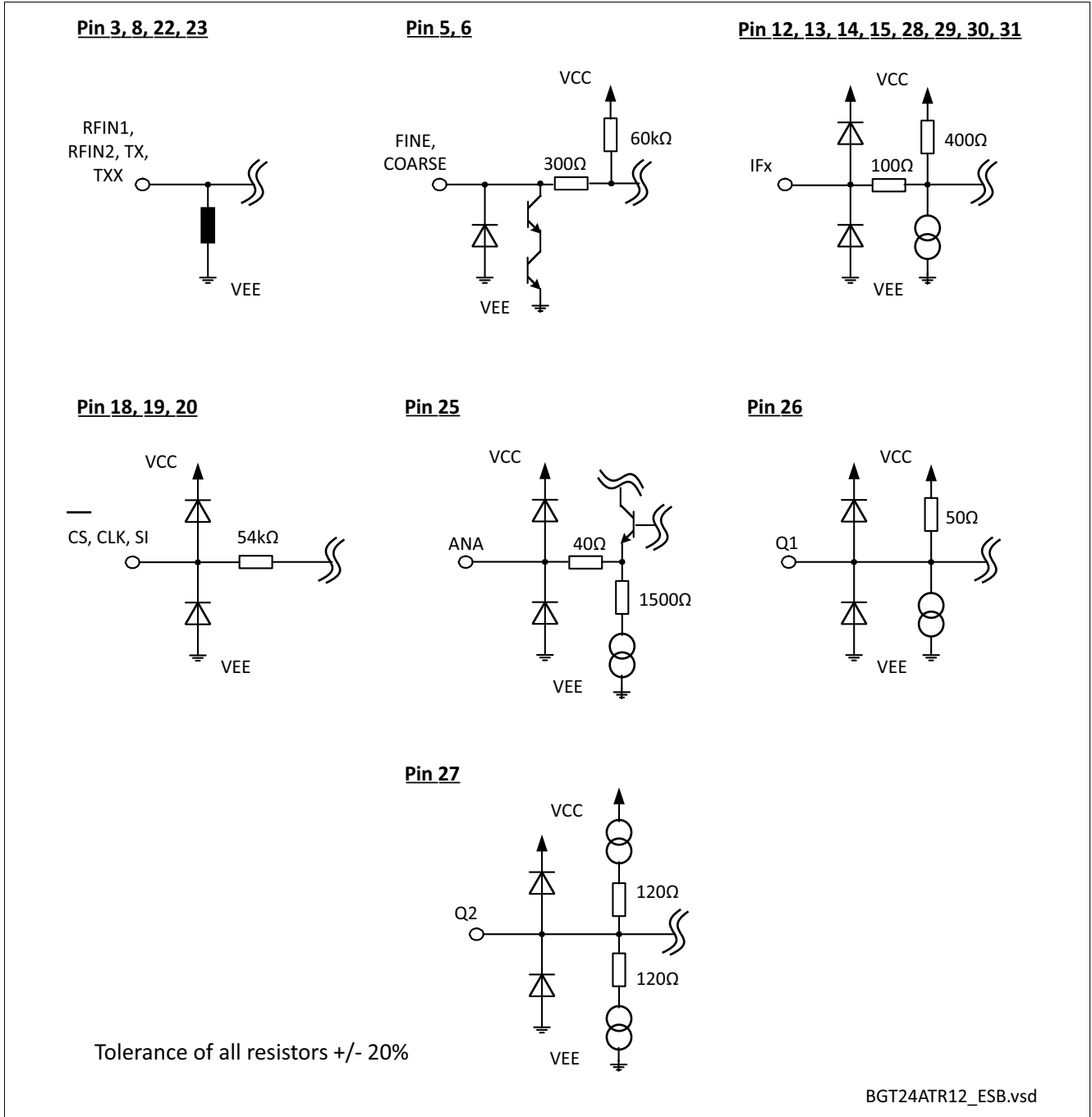


Figure 8 Equivalent Circuit Diagram of MMIC Interfaces



## 4 Physical Characteristics

### 4.1 Package Footprint

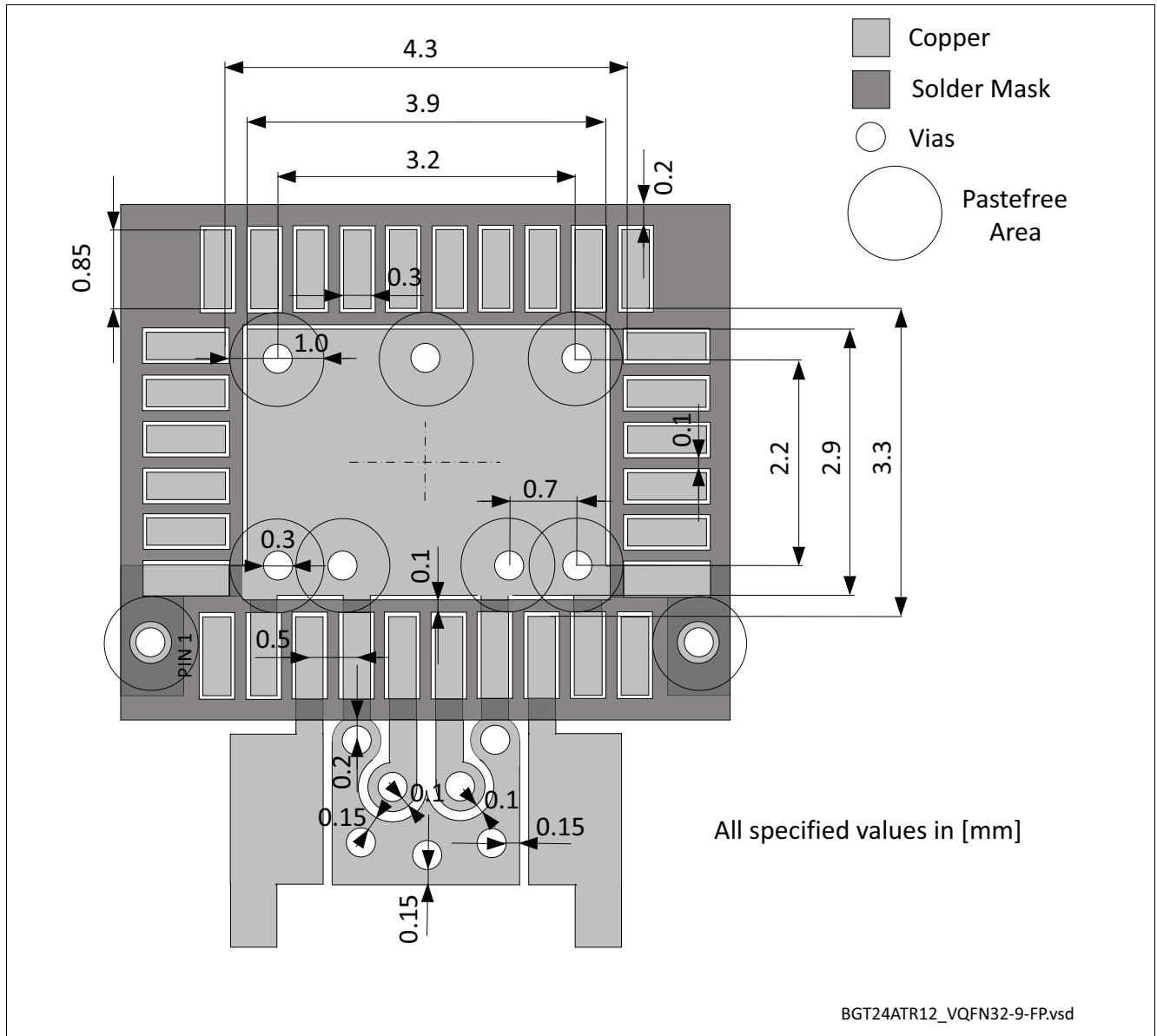


Figure 9 Recommended Footprint and Stencil Layout for the VQFN32-9 Package

## 4.2 Reflow Profile

Soldering process qualified during qualification with "Preconditioning MSL-3: 30°C. 60%r.h., 192h, according to JEDEC JSTD20".

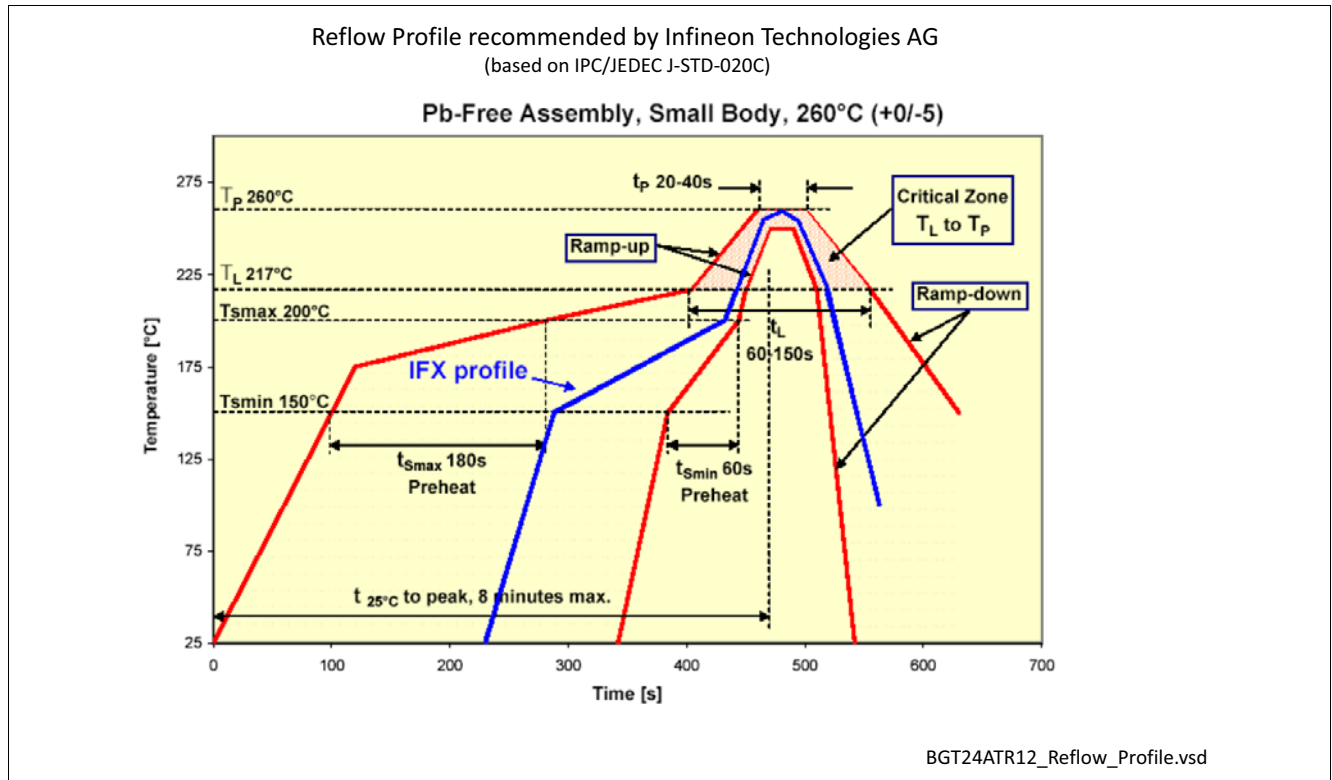


Figure 10 Reflow Profile for BGT24ATR12 (VQFN32-9)

4.3 Package Dimensions

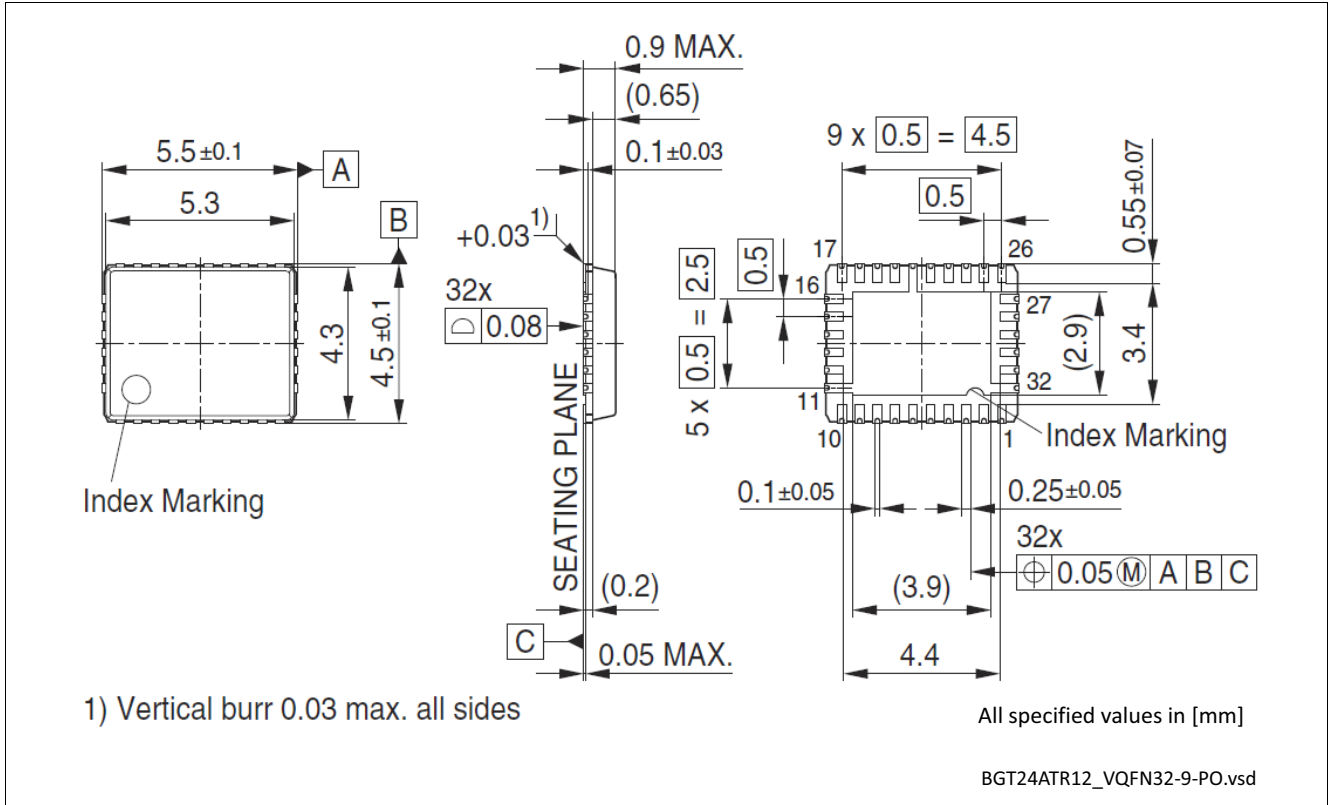


Figure 11 Package Outline (Top, Side and Bottom View)

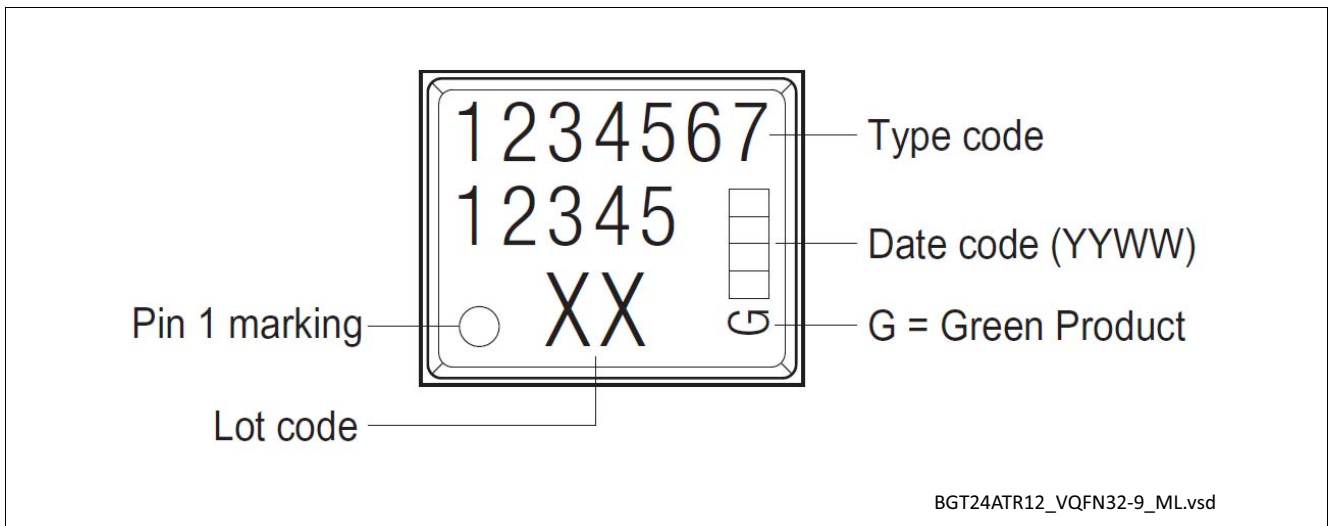
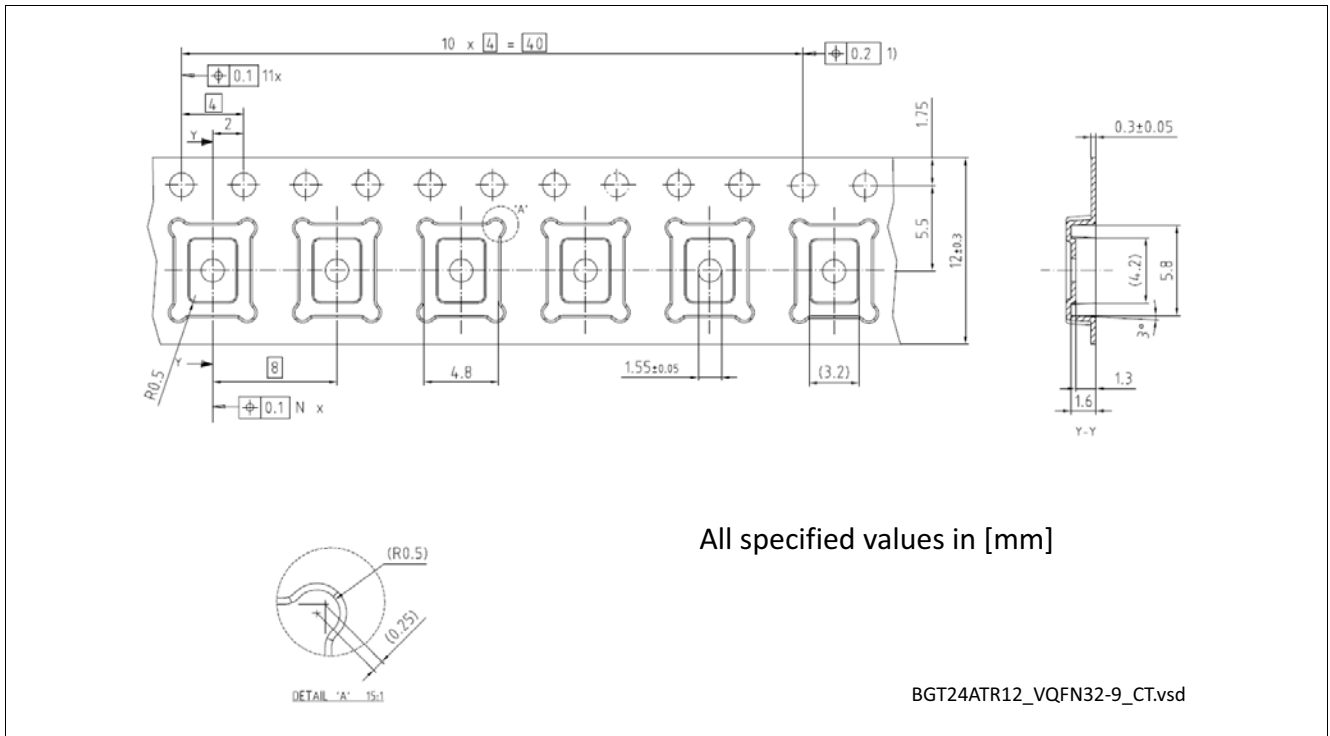


Figure 12 Marking Layout VQFN32-9



**Figure 13** Tape of VQFN32-9

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