AN-EVAL ICE3AR1080VJZ

34 W 12 V SMPS Evaluation Board with ICE3AR1080VJZ

Application Note

About this document

Scope and purpose

This document is an engineering report that describes universal input 34 W 12 V off-line flyback converter power supply using Infineon CoolSET™ F3R80 family, ICE3AR1080VJZ. The converter is operated in Discontinuous Conduction Mode, 100 kHz fixed frequency, very low standby power and various mode of protections for a high reliable system. This evaluation board is designed to evaluate the performance of ICE3AR1080VJZ in ease of use.

Intended audience

This document is intended for users of the ICE3AR1080VJZ who wish to design low cost and high reliable systems of off-line SMPS for enclosed adapter or open frame auxiliary power supply of white goods, PC, server, DVD, TV, Set-top box, etc.

Table of Contents

1 Abstract

This document is an engineering report of a universal input 34 W 12 V off-line flyback converter power supply utilizing F3R80 CoolSET™ ICE3AR1080VJZ. The application evaluation board is operated in Discontinuous Conduction Mode (DCM) and is running at 100 kHz switching frequency. It has a single output voltage with secondary side control regulation. It is especially suitable for small power supply such as DVD player, set-top box, game console, charger and auxiliary power of white goods, server, PC and high power system, etc. The ICE3AR1080VJZ is the latest version of the CoolSET™. Besides having the basic features of the F3R CoolSET™ such as Active Burst Mode, propagation delay compensation, soft gate drive, auto restart protection for major fault (V_{CC} over voltage, V_{CC} under voltage, adjustable input OVP, over temperature, over-load, open loop and short opto-coupler), it also has the BiCMOS technology design, selectable entry and exit burst mode level, adjustable AC line input over voltage protection feature, built-in soft start time, built-in and extendable blanking time and frequency jitter feature, etc. The particular features are the best-in-class low standby power and the good EMI performance.

2 Evaluation board

This document contains the list of features, the power supply specification, schematic, bill of material and the transformer construction documentation. Typical operating characteristics such as performance curve and scope waveforms are showed at the rear of the report.

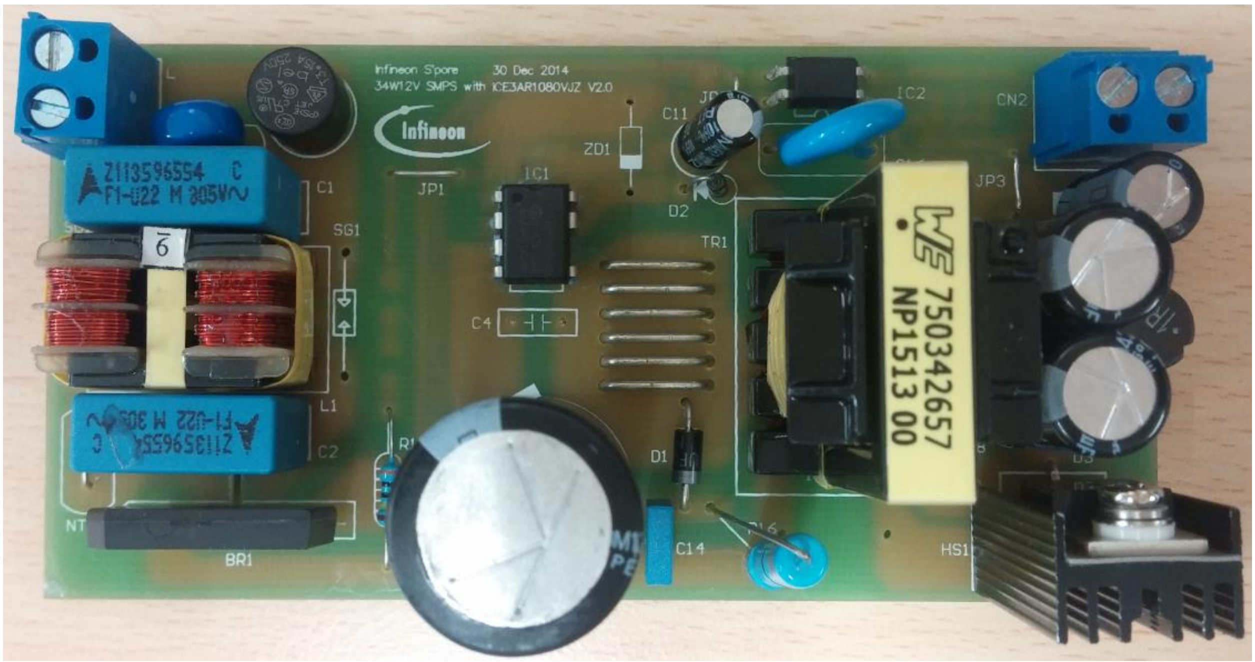


Figure 1 EVAL ICE3AR1080VJZ

3 Specifications of evaluation board

Table 1 Specifications of EVAL ICE3AR1080VJZ

Input voltage	85 V_{AC} ~ 265 V_{AC}
Input frequency	50 ~ 60 Hz
Output voltage	12 V
Output current	2.83 A
Output power	34 W
Steady state output ripple voltage (±1% of norminal output voltage)	$V_{ripple\_P\_P}$ < 50 mV
Dynamic load response undershoot and overshoot (±3% of norminal output voltage)	$V_{ripple\_P\_P}$ < 610 mV
Active mode four point average efficiency (25%,50%,75% and 100%load) Active mode at 10% load efficiency	> 85% at 115 V_{AC} and 230 V_{AC} > 70%
No-load power consumption (EU CoC Version 5, Tier 2)	< 75 mW
Maximum input power(Peak Power) for universal input range (< ±5% of average maximum input power)	< ±5% of average maximum input power

4 Features of ICE3AR1080VJZ

Table 2 Features of ICE3AR1080VJZ

800 V avalanche rugged CoolMOS™ with startup cell
Active Burst Mode for lowest standby power
Selectable entry and exit burst mode level
100 kHz internally fixed switching frequency with jittering feature
Auto restart protection for over load, open Loop, V_{CC} under voltage and over voltage and over temperature
Over temperature protection with 50 °C hysteresis
Built-in 10 ms soft start
Built-in 20 ms and extendable blanking time for short duration peak power
Propagation delay compensation for both maximum load and burst mode
Adjustable input OVP
Overall tolerance of current limiting < ±5%
BiCMOS technology for low power consumption and wide V_{CC} voltage range
Soft gate drive with 50 Ω turn-on resistor

5 Circuit description

5.1 Introduction

The EVAL ICE3AR1080VJZ evaluation board is a low cost off-line flyback switch mode power supply (SMPS) using the ICE3AR1080VJZ integrated power IC from the CoolSET™-F3R80 family. The circuit shown in Figure 2 details a 12 V, 34 W power supply that operates from an AC line input voltage range of 85 V_{AC} to 265 V_{AC} and line input OVP detect/reset voltage is 300/282 V_{AC}, suitable for applications in enclosed adapter or open frame auxiliary power supply for different system such as white goods, PC, server, DVD, LED TV, Set-top box, etc.

5.2 Line input

The AC line input side comprises the input fuse F1 as over-current protection. The choke L1, X-capacitors C1, C2 and Y-capacitor C16 act as EMI suppressors. Optional spark gap device SG1, SG2 and varistor VAR can absorb high voltage stress during lightning surge test. After the bridge rectifier BR1 and the input bulk capacitor C3, a voltage of 90 to 424 V_{DC} is present which depends on input line voltage.

5.3 Line input over voltage protection

The AC line input OVP mode is detected by sensing the voltage level at BV pin through the resistors divider from the bulk capacitor. Once the voltage level at BV pin hits above 1.98V, the controller stops switching and enters into input OVP mode. When the BV voltage drops to 1.91V and the Vcc hits 17V, the input OVP mode is released.

5.4 Start up

Since there is a built-in startup cell in the ICE3AR1080VJZ, no external start up resistor is required. The startup cell is connecting the drain pin of the IC. Once the voltage is built up at the Drain pin of the ICE3AR1080VJZ, the startup cell will charge up the V_{CC} capacitor C11 and C7. When the V_{CC} voltage exceeds the UVLO at 17 V, the IC starts up. Then the V_{CC} voltage is bootstrapped by the auxiliary winding to sustain the operation.

5.5 Operation mode

During operation, the V_{CC} pin is supplied via a separate transformer winding with associated rectification D2 and buffering C11 and C7.In order not to exceed the maximum voltage at V_{CC} pin due to poor coupling of transformer winding, an external zener diode ZD1 can be added.

5.6 Soft start

The soft start is a built-in function and is set at 10 ms.

5.7 RCD clamper circuit

While turns off the CoolMOS™, the clamper circuit C14, R16 and D1 absorbs the current caused by transformer leakage inductance once the voltage exceeds clamp capacitor voltage. Finally drain to source voltage of CoolMOS™ is lower than maximum break down voltage ($V_{(BR)DSS}$ = 800 V) of CoolMOS™.

5.8 Peak current control of primary current

The CoolMOS™ drain source current is sensed via external shunt resistors R1 and R2 which determine the tolerance of the current limit control. Since ICE3AR1080VJZ is a current mode controller, it would have a cycle-by-cycle primary current and feedback voltage control which can make sure the maximum power of the converter is controlled in every switching cycle. Besides, the patented propagation delay compensation is implemented to ensure the maximum input power can be controlled in an even tighter manner. The evaluation board shows approximately ± 4.1% of average maximum input power (refer to Figure 11).

5.9 Output stage

On the secondary side the power is coupled out by a schottky diode D3. The capacitors C8 and C9 provide energy buffering following with the LC filter L2 and C10 to reduce the output voltage ripple considerably. Storage capacitors C8, C9 and C10 are selected to have a very small internal resistance (ESR) to minimize the output voltage ripple.

6 Circuit diagram

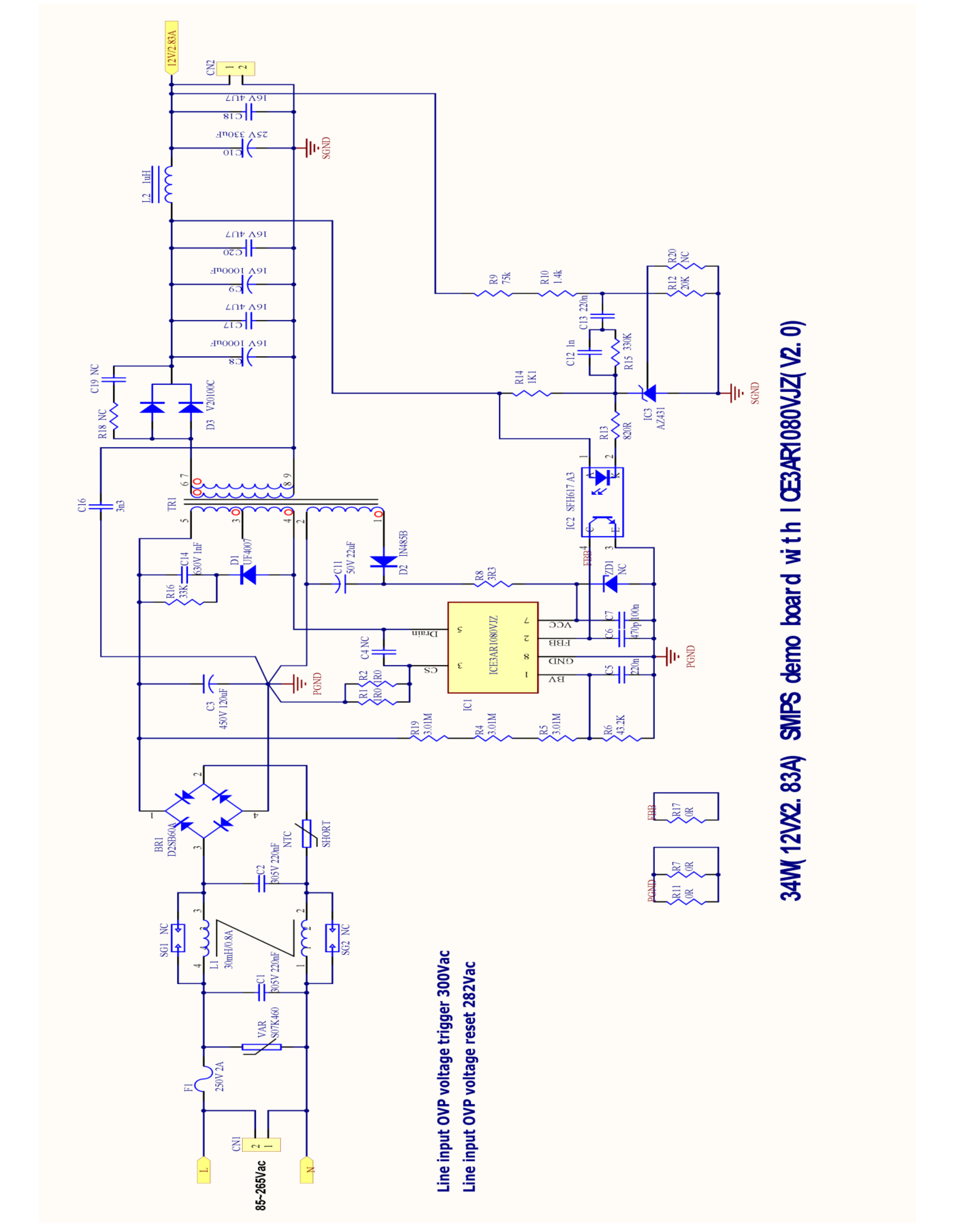


Figure 2 Schematic of EVAL ICE3AR1080VJZ

Note: *In order to get the optimized performance of the CoolSET™, the grounding of the PCB layout must be connected very carefully. From the circuit diagram above, it indicates that the grounding for the CoolSET™ can be split into several groups; signal ground, V_{CC} ground, Current sense resistor ground and EMI return ground. All the split grounds should be connected to the bulk capacitor ground separately.*

Signal ground includes all small signal grounds connecting to the CoolSET™ GND pin such as filter capacitor ground C7, C6, C5 and opto-coupler ground.

V_{CC} ground includes the V_{CC} capacitor ground C11 and the auxiliary winding ground, pin 2 of the power transformer.

Current Sense resistor ground includes current sense resistor R1 and R2.

EMI return ground includes Y capacitor C16.

7 PCB layout

7.1 Top side

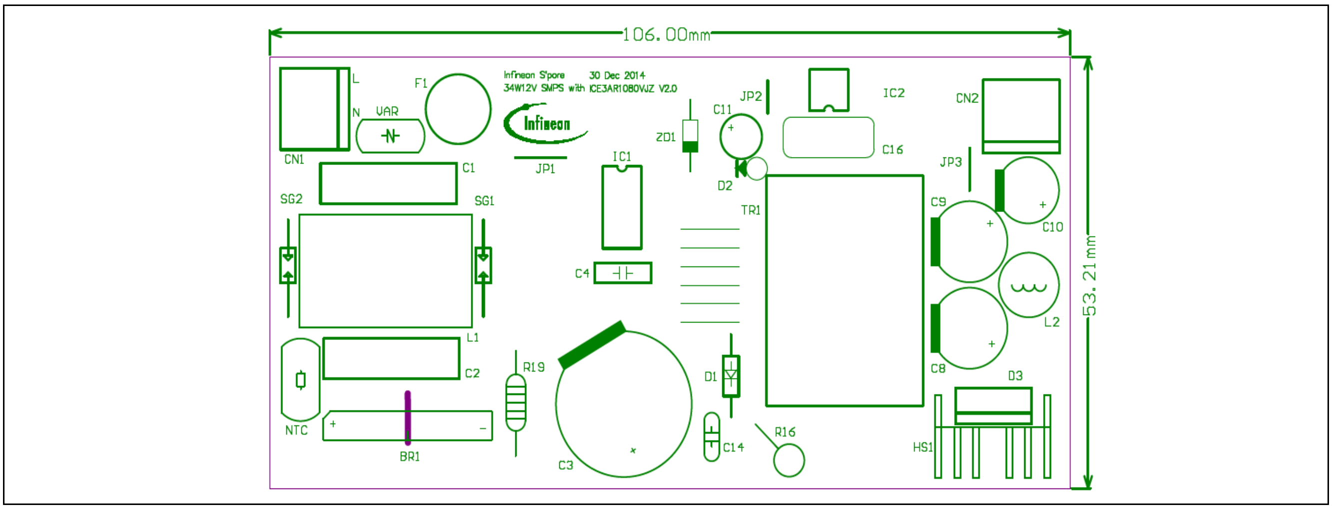


Figure 3 Top side component legend

7.2 Bottom side

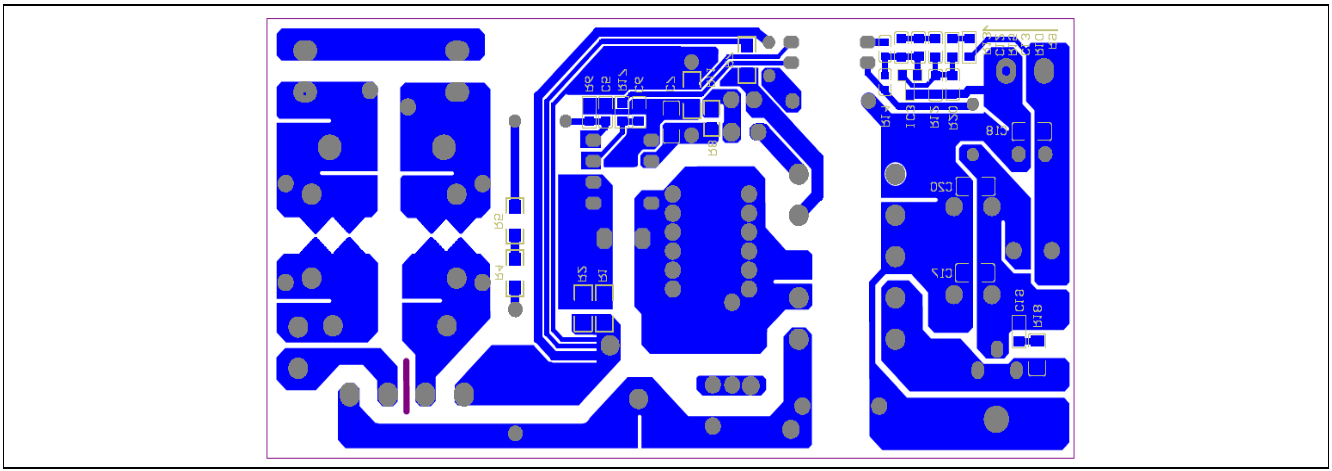


Figure 4 Bottom side copper and component legend

8 Bill of material (BOM)

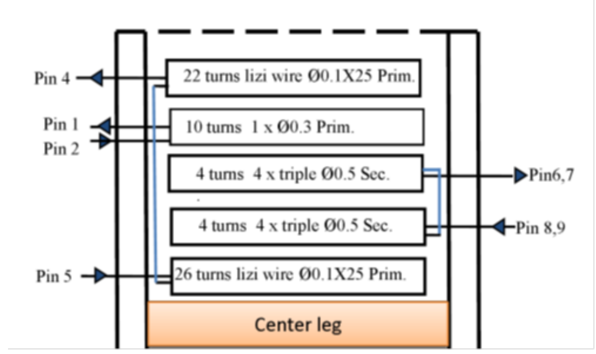
Table 3 Bill of materials

No.	Designator	Component Description	Footprint	Part Number	Manufacturer	Quantity
1	CN1,CN2	12V Test point	Connector	691101710002	Wurth Electronics	2
2	BR1	600V/2A	Bridge（2S）	D2SB60A	SHINDENGEN	1
3	C1,C2	MKT/220nF/305V	L*W*H:12.5*7*18-P15mm	B32922C3224M	EPCOS	2
4	C10	16V/330u	Φ*H :8*11.5-P3.5mm	16YXF330MEFC10x20	RUBYCON	1
5	C11	22uF/50V	Φ*H:5*11-P2.5mm	50PX22MEFC5X11	RUBYCON	1
6	C14	1N/630V	W*L*H: 7.3*12.5*6.5-P5mm	B32529C8102K000	EPCOS	1
7	C16	Y1/3.3nF/400Vac	L*W*H:9*5*10-P10mm			1
8	C17,C18,C20	16V/4U7	1206		MURATA	3
9	C3	120uF/450V	Φ*H:18*31.5-P7.5.5mm	450CXW120MEFC18X31	RUBYCON	1
10	C5	50V/220N	0805			1
11	C6	50V/470pF	0805			1
12	C7	50V/100N	0805			1
13	C12	50V /1nF	0805			1
14	C8,C9	16V/1000uF	Φ*H :10*20-P5mm	16ZL1000MEFC10X20	RUBYCON	2
15	R1	1.0R	1206			1
16	R2	1.0R	1206			1
17	C13	50V/220N	0805			1
18	R10	1K4	0805			1
19	R12	20K	0805			2
20	R17	0R	0805			1
21	R7 ,R11	0R	1206			2
22	R13	820R	0805			1
23	R14	1K1	0805			1
24	R15	330K	0805			1
25	R16	33K/2W	DIP-2W			1
26	R19	3M	R-1/4W-P15(0.8)			1
27	R4,R5	3.01M	1206			2
28	R6	43.2K	0805			1
29	R8	3R3	0805			1
30	R9	75K	0805			1
31	D1	1000V/1A	DO-41	UF4007		1
32	D2	200V/0.2A	DO-35	IN485B		1
33	F1	250Vac/2A	Φ*H：8.5*7.5-P5mm			1
34	IC1	ICE3AR1080VJZ	PG-DIP7	ICE3AR1080VJZ	INFINEON	1
35	IC2	SFH617-3	DIP-4	SFH617 A3		1
36	IC3	TL431	SOT-23	TL431		1
37	L1	30mH/0.8A		750342718	Wurth Electronics	1
38	JP1	Jumper	DIP-P6.5mm			1
39	JP2	Jumper	DIP-P4mm			1
40	JP3	Jumper	DIP-P6mm			1

41	NTC	Jumper	DIP-P5mm			1
42	L2	1uH/5A	Φ*H：7.8*9-P5mm	744772010	Wurth Electronics	1
43	VAR	VR /S07K460	W*L*H: 9*5.7*11.5-P5mm	B72207S461K101	Epcos	1
44	TR1	250uH(48:8:10)	DIP10(EF25)	750342657	Wurth Electronics	1
45	D3	100V/20A	TO-220AB	V20100C		1
46	HS1					1

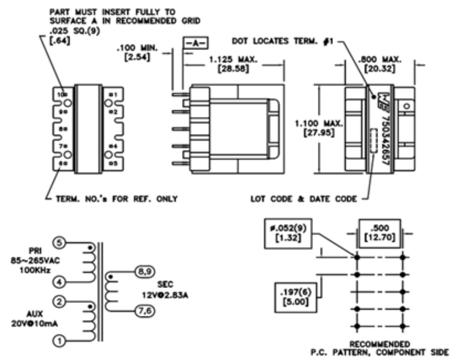
9 Transformer construction

Core and material: EE25/13/7(EF25), TP4A (TDG)
Bobbin: 070-4846(10-Pins, TH-T, Vertical version)
Primary Inductance, L_P=250 µH (±5%), measured between pin 4 and pin 5
Manufacturer and part number: Wurth Electronics Midcom (750342657)



Start	End	No.of Turns	Wire size	Layers
5		26	Lizi wire Ø0.1 mmX25	1/2 Primary
8,9		4	4 x triple Ø0.5 mm	½ Secondary
	6,7	4	4 x triple Ø0.5 mm	½ Secondary
2	1	10	1 x Ø0.3 mm	Aux primary
	4	22	Lizi wire Ø0.1 mmX25	1/2 Primary

CUSTOMER TERMINAL	RoHS	LEAD(Pb)–FREE
Sn96%, Ag4%	Yes	Yes



ELECTRICAL SPECIFICATIONS @ 25°C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	5–4	@20°C	0.198 ohms max.
D.C. RESISTANCE	2–1	@20°C	0.153 ohms max.
D.C. RESISTANCE	6–8	@20°C,tie(6+7,8+9)	0.020 ohms max.
INDUCTANCE	4–5	50kHz, 100mVAC, Ls	250uH ±10%
LEAKAGE INDUCTANCE	4–5	tie(2+1, 6+7+9+8), 100kHz, 100mVAC, Ls	3.7uH typ, 5.5uH max.
DIELECTRIC	5–6	tie(4+1, 9+8), 3750VAC, 1 second	3000VAC, 1 minute
DIELECTRIC	5–1	1800VAC, 1 second	1500VAC, 1 minute
TURNS RATIO		(5–4):(8–6), tie(6+7,8+9)	6:1, ±2%
TURNS RATIO		(5–4):(2–1)	4.8:1, ±2%

GENERAL SPECIFICATIONS:
OPERATING TEMPERATURE RANGE: –40°C to +125°C including temp rise.

Wire insulation & RoHS status not affected by wire color.
Wire insulation color may vary depending on availability.

REV.	DATE	Packaging Specifications	Tolerances unless otherwise specified	DRAWING TITLE	PART NO.
00	10/14	Method: Tray PKG–0734 www.we–online.com/midcom SEE REVISION SHEET FOR REVISION LEVEL	Angles: ±1° Decimals: ±.005 [.13] Fractions: ±1/64 Footprint: ±.001 [.03] This drawing is dual dimensioned. Dimensions in brackets are in millimeters.	TRANSFORMER eiSos p/n: 750342657	750342657 SPECIFICATION SHEET 1 OF 1

Figure 5 Transformer structure

10 Test results

10.1 Efficiency, regulation and output ripple

Table 4 Efficiency, regulation and output ripple

V_{in} (V_{AC})	P_{in} (W)	V_{out} (V_{DC})	I_{out} (A)	$V_{out\_ripple\_pk\_pk}$ (mV)	P_{out} (W)	Efficiency (η) (%)	Average η (%)	OLP P_{in} (W)	OLP I_{out} (A)
85	0.0390	12.13	0.00	35.8				52.9	3.71
	4.2700	12.13	0.28	11.5	3.43	80.42			
	10.0080	12.13	0.71	14.1	8.58	85.71	85.32		
	19.9500	12.13	1.41	21.1	17.15	85.99			
	30.1440	12.13	2.12	23.7	25.73	85.35			
	40.7520	12.12	2.83	38	34.32	84.22			
115	0.0460	12.13	0.00	37.8				54.19	3.82
	4.2810	12.13	0.28	11.5	3.43	80.21			
	10.0050	12.13	0.71	16.6	8.57	85.62	86.49		
	19.7040	12.13	1.41	21.1	17.15	87.06			
	29.6230	12.13	2.12	24.6	25.73	86.86			
	39.7080	12.12	2.83	27.5	34.32	86.43			
230	0.0630	12.14	0.00	42.9				56.35	4.04
	4.7000	12.13	0.28	12.2	3.43	73.06			
	10.5000	12.13	0.71	15.7	8.57	81.59	85.57		
	19.9700	12.13	1.41	19.2	17.15	85.90			
	29.5080	12.13	2.12	24.6	25.73	87.21			
	39.1830	12.12	2.83	25.6	34.32	87.59			
265	0.0690	12.14	0.00	46.1				57.42	4.11
	4.8640	12.13	0.28	12.2	3.43	70.60			
	10.6750	12.13	0.71	16.6	8.57	80.25	84.51		
	20.2380	12.13	1.41	18.6	17.15	84.76			
	29.8520	12.13	2.12	24.3	25.73	86.20			
	39.5120	12.12	2.83	30	34.31	86.83			

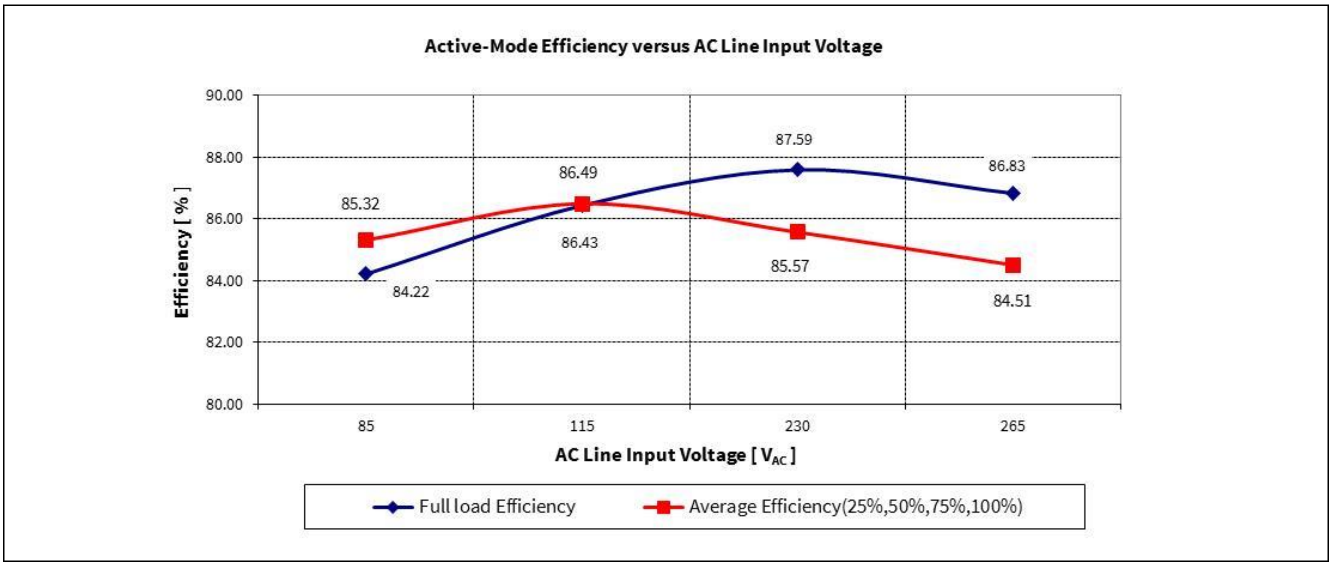


Figure 6 Efficiency vs AC line input voltage

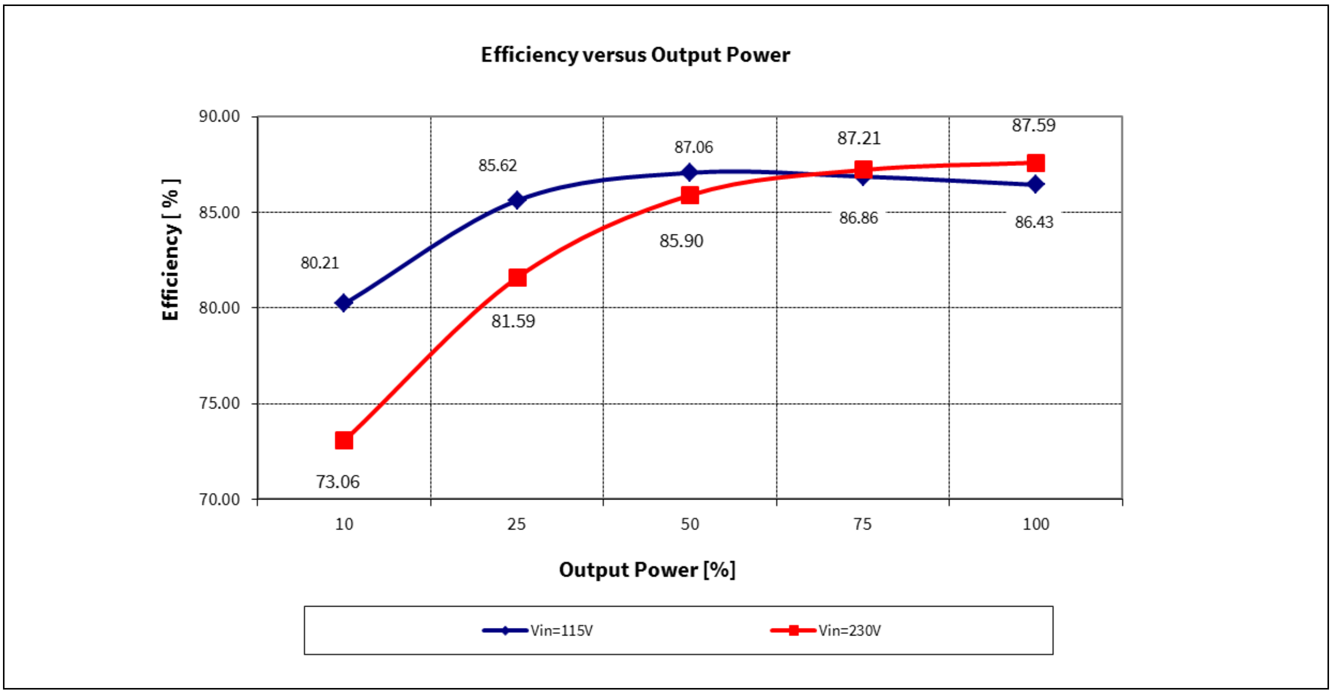


Figure 7 Efficiency vs output power @ 115 V_{AC} and 230 V_{AC} line

10.2 Standby power

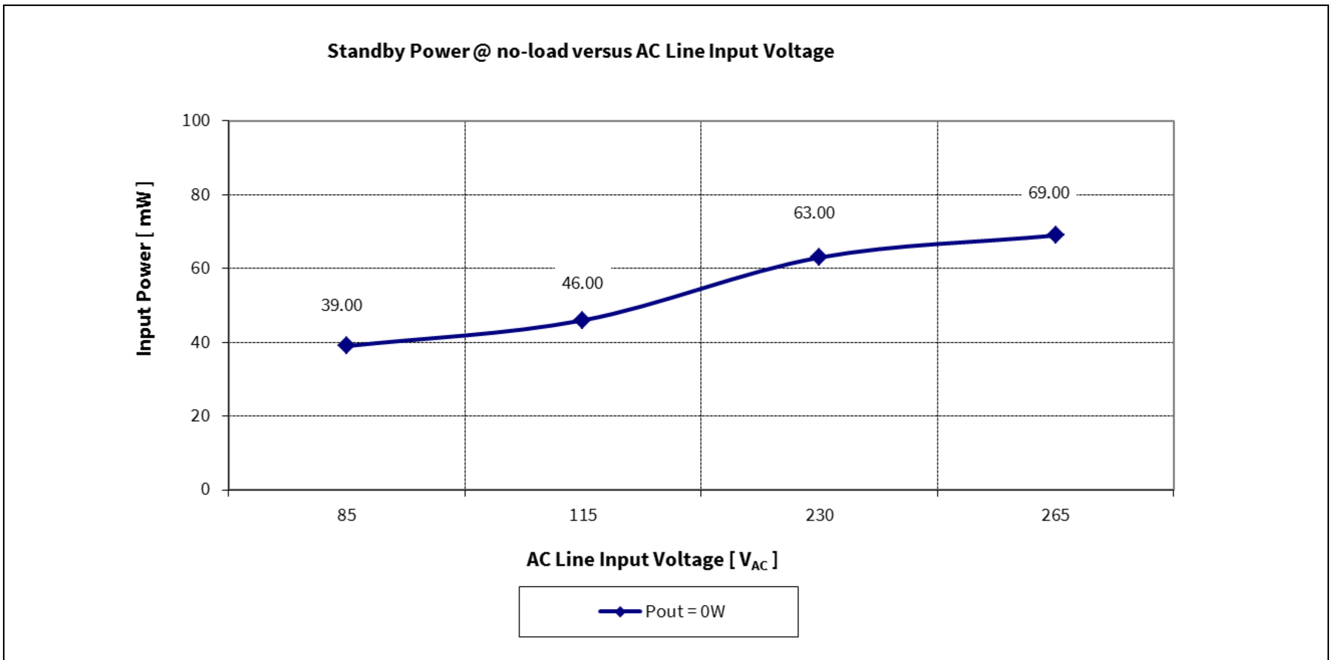


Figure 8 Standby power @ no load vs AC line input voltage (measured by Yokogawa WT210 power meter - integration mode)

10.3 Line regulation

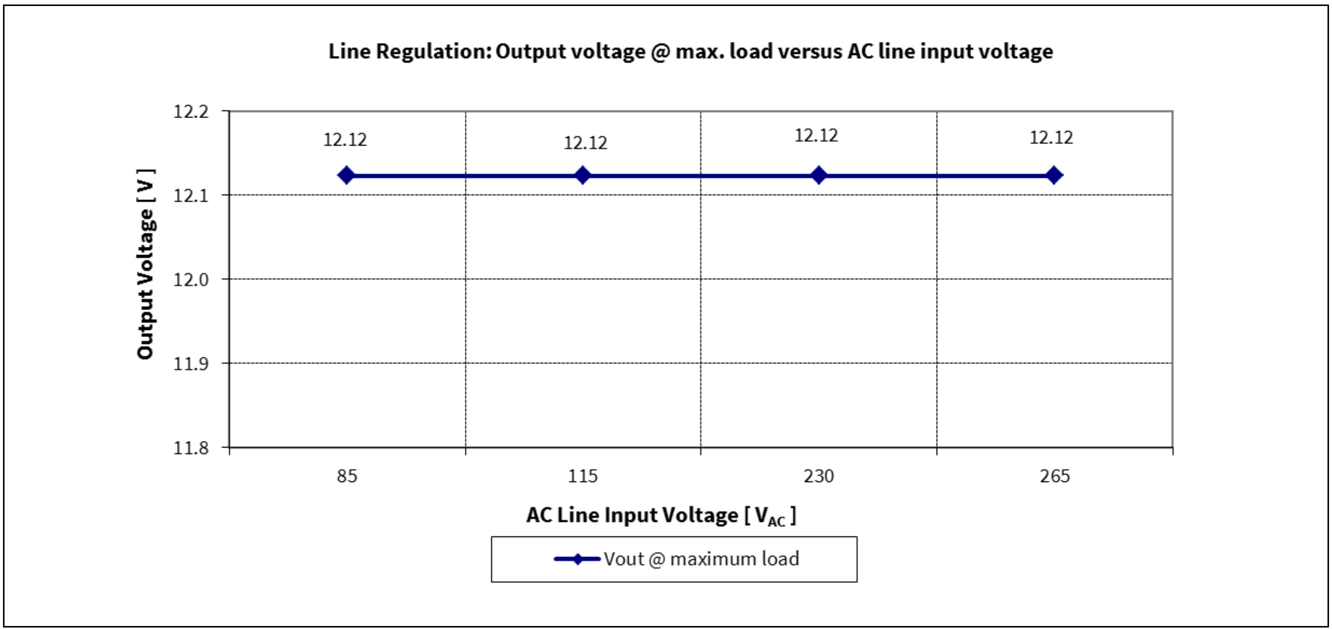


Figure 9 Line regulation V_{out} @ full load vs AC line input voltage

10.4 Load regulation

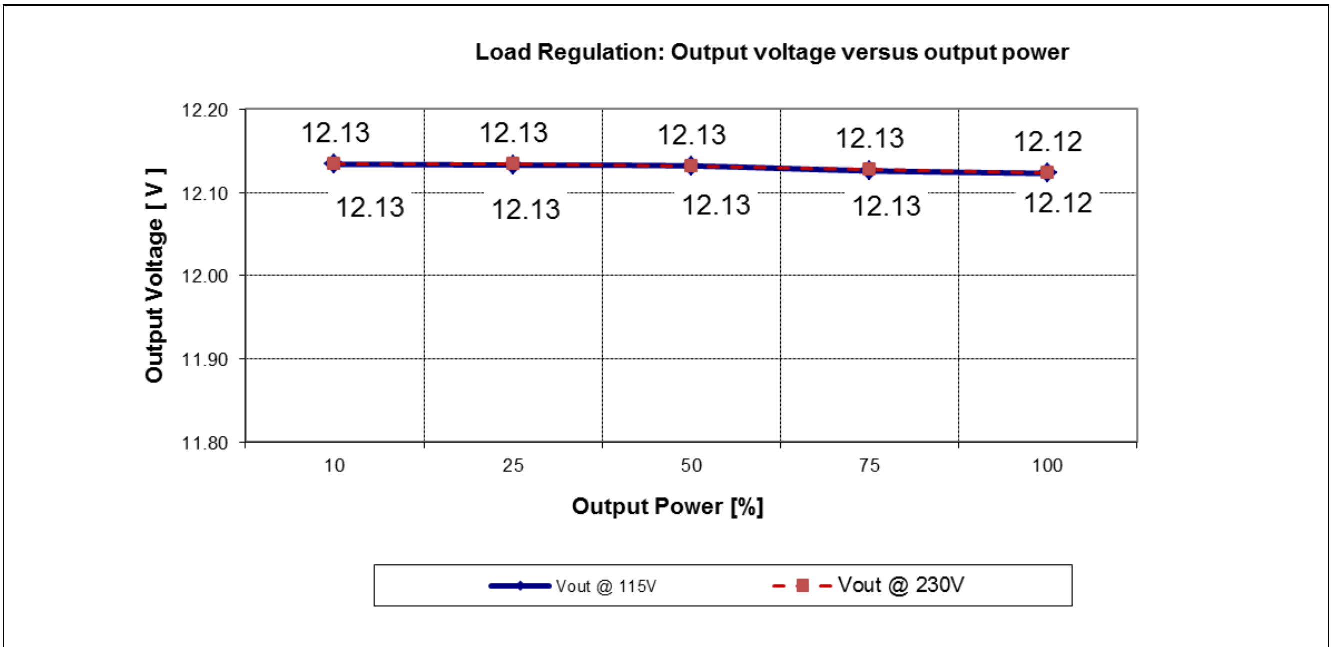


Figure 10 Load regulation V_{out} vs output power

10.5 Maximum power

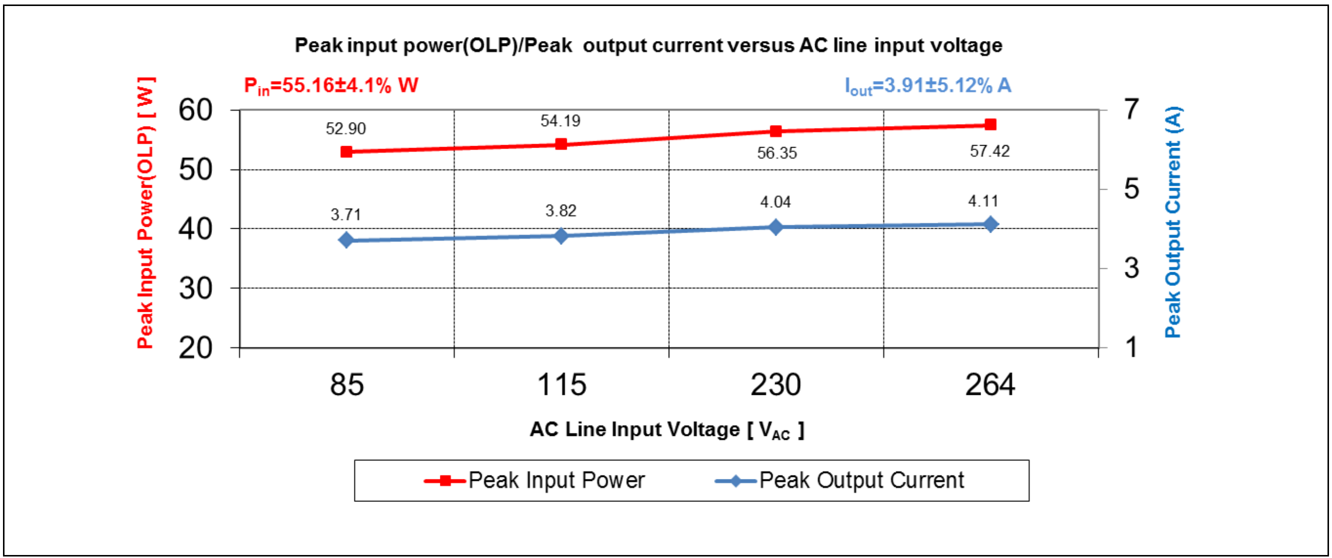


Figure 11 Maximum input power (before over-load protection) vs AC line input voltage

10.6 ESD immunity (EN61000-4-2)

Pass [level 3 (±6 kV) for contact discharge].

Pass [special level (±12 kV) for contact discharge by adding SG1 and SG2 (RLS302-301M)].

10.7 Surge immunity (EN61000-4-5)

Pass [Installation class 3, 2 kV (line to earth) and 1 kV (line to line)].

Pass [Installation class 4, 4 kV (line to earth) and 2 kV (line to line) by adding SG1 and SG2 (RLS302-301M)].

10.8 Conducted emissions (EN55022 class B)

The conducted EMI was measured by certified external lab and followed the test standard of EN55022 (CISPR 22) class B. The evaluation board was set up at maximum load (34 W) with input voltage of 115 V_{AC} and 230 V_{AC}.

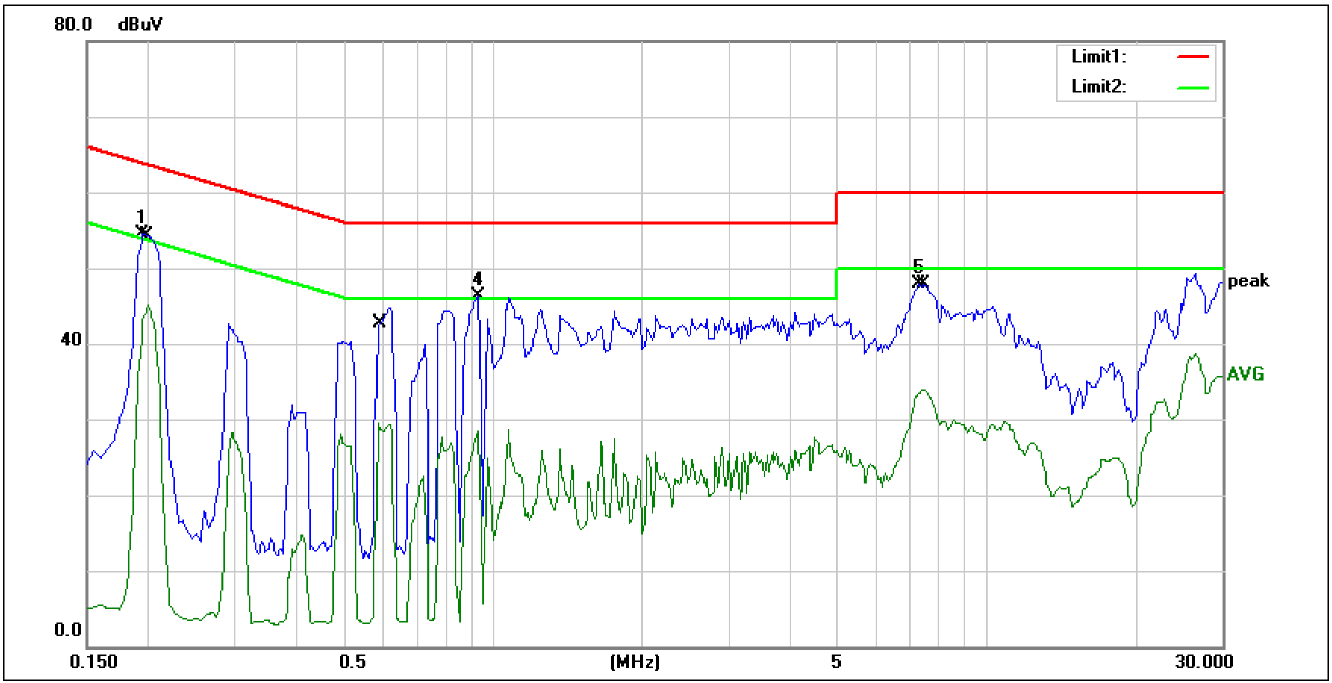


Figure 12 Conducted emissions(Line) at 115 V_{AC} and maximum Load

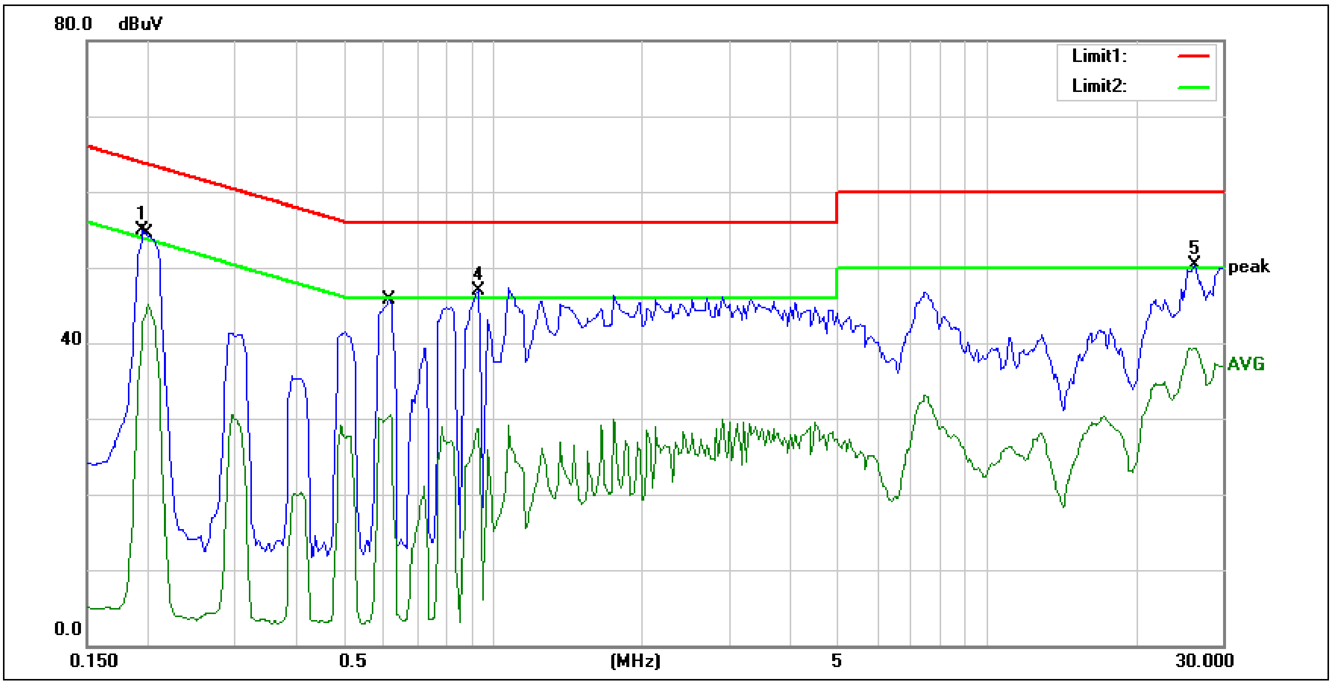


Figure 13 Conducted emissions(Neutral) at 115 V_{AC} and maximum Load

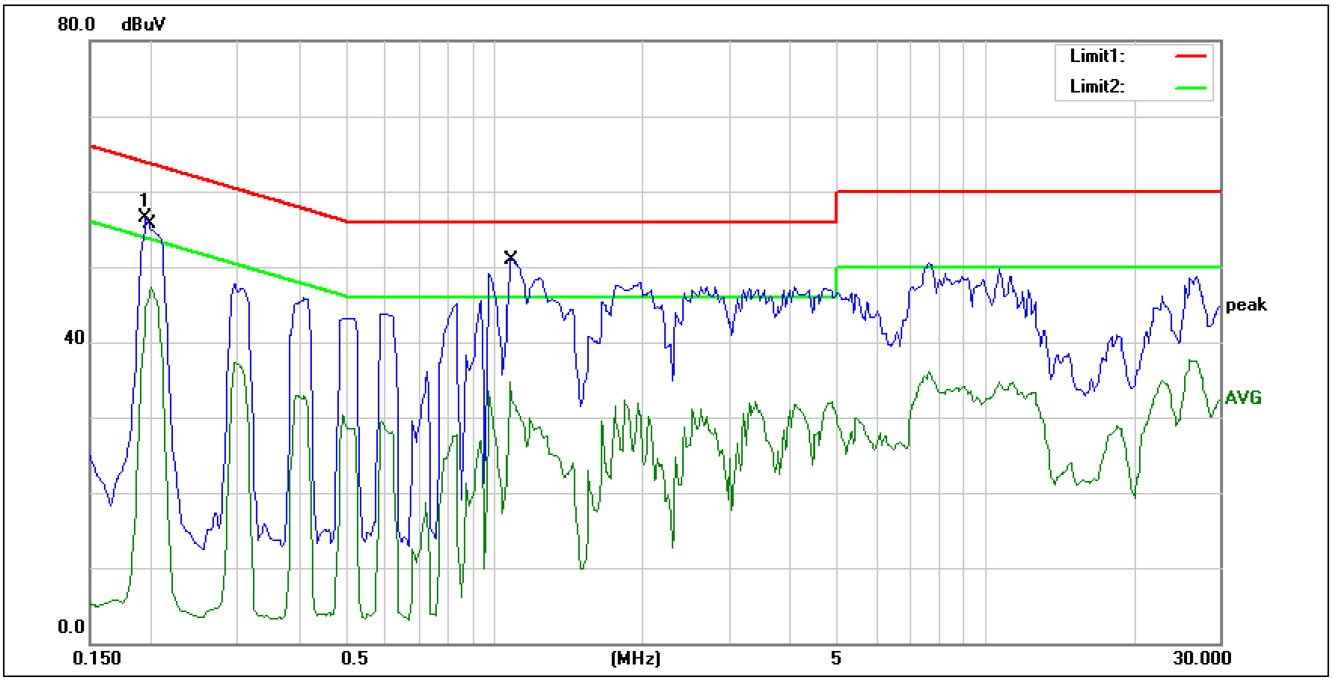


Figure 14 Conducted emissions(line) at 230 V_{AC} and maximum Load

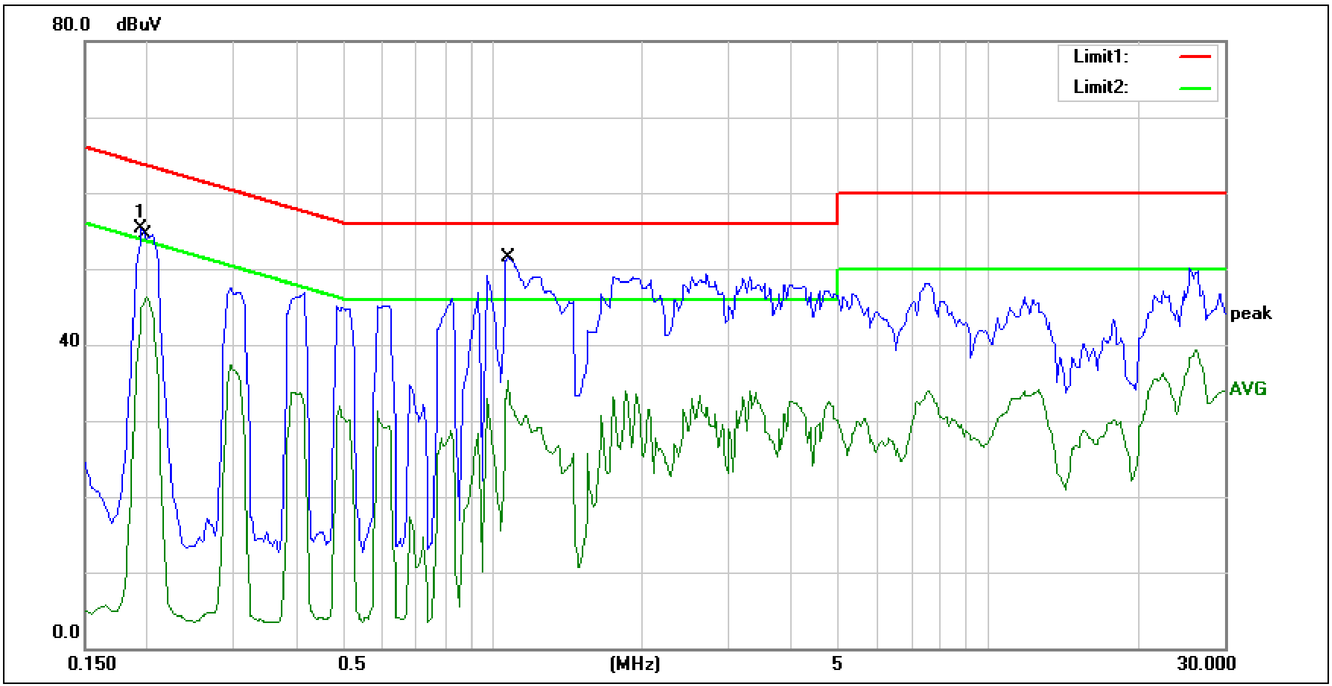


Figure 15 Conducted emissions(Neutral) at 230 V_{AC} and maximum Load

Pass conducted EMI EN55022 (CISPR 22) class B with > 6 dB margin for QP.

10.9 Thermal measurement

The thermal test of open frame evaluation board was done using an infrared thermography camera (TVS-500EX) at ambient temperature 25 °C. The measurements were taken after two hours running at full load (34 W).

Table 5 Hottest temperature of evaluation board

No.	Designator	Temperature @ 85 V_{AC} and FL(°C)	Temperature @ 265 V_{AC} and FL(°C)
1	IC1 (ICE3AR1080VJZ)	88.3	81.9
2	BR1	56.2	37.4
3	L1	73.6	37.2
4	TR1	55.4	62
5	D3	59.1	68.4
6	R16	47.3	45.2
7	Ambient	25	25

85 V_{AC} full load and 25 °C ambient

PCB top side

PCB bottom side

265 V_{AC} full load and 25 °C ambient

PCB top side

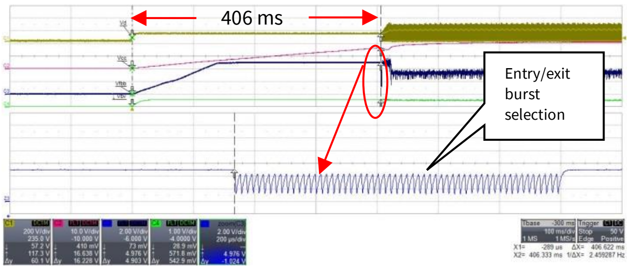
PCB bottom side

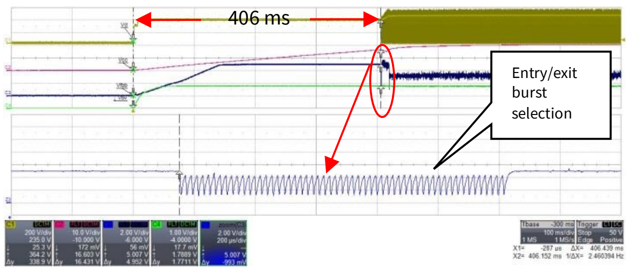
Figure 16 Infrared thermal image of EVAL ICE3AR1080VJZ

11 Waveforms and scope plots

All waveforms and scope plots were recorded with a LeCroy 6050 oscilloscope.

11.1 Startup at low/high AC line input voltage with maximum load

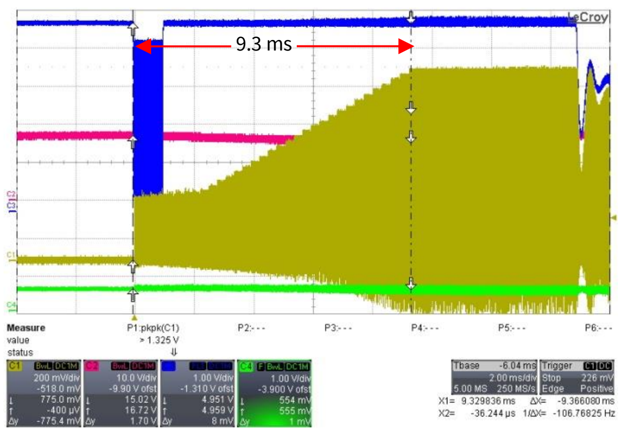




Channel 1; C1(Yellow) : Drain voltage (V_{Drain}) Channel 2; C2(Red): Supply voltage (V_{CC}) Channel 3; C3(Blue) : Feedback voltage (V_{FBB}) Channel 4; C4(Green) :BV voltage (V_{BV})	Channel 1; C1(Yellow) : Drain voltage (V_{Drain}) Channel 2; C2(Red): Supply voltage (V_{CC}) Channel 3; C3(Blue) : Feedback voltage (V_{FBB}) Channel 4; C4(Green) :BV voltage (V_{BV})
Startup time @ 85 V_{AC} & max. load = 406 ms	Startup time @ 265 V_{AC} & max. load = 406 ms

Figure 17 Startup

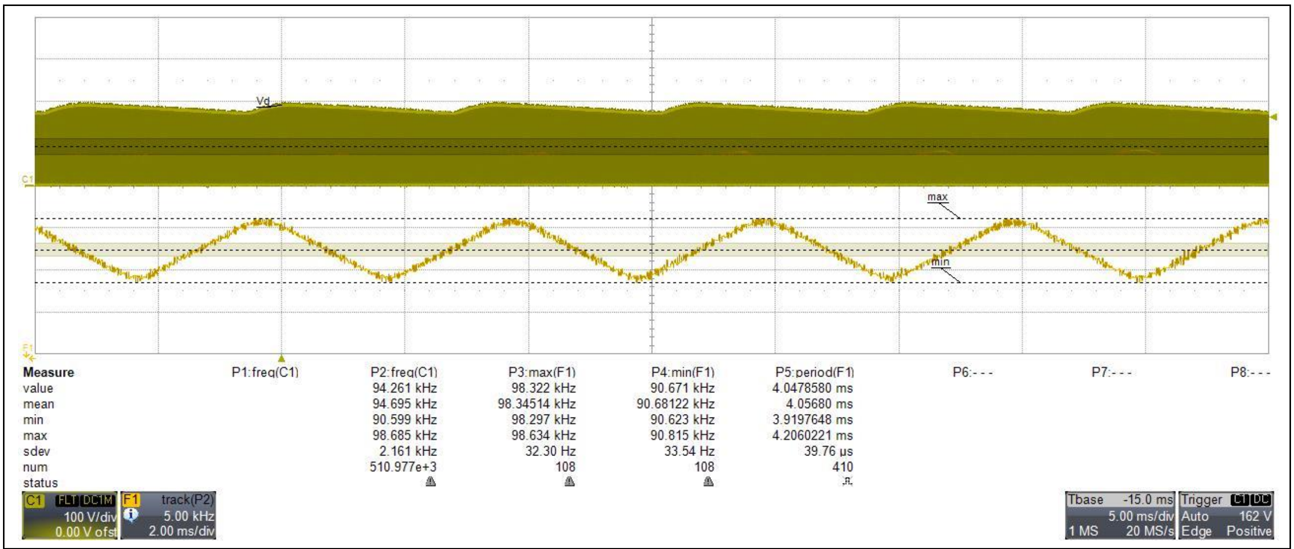
11.2 Soft start



Channel 1; C1 : Current sense voltage (V_{CS}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FBB}) Channel 4; C4 : Zero crossing voltage (V_{BV})
Soft Star time @ 85 V_{AC} & max. load = 9.3 ms

Figure 18 Soft start

11.3 Frequency jittering



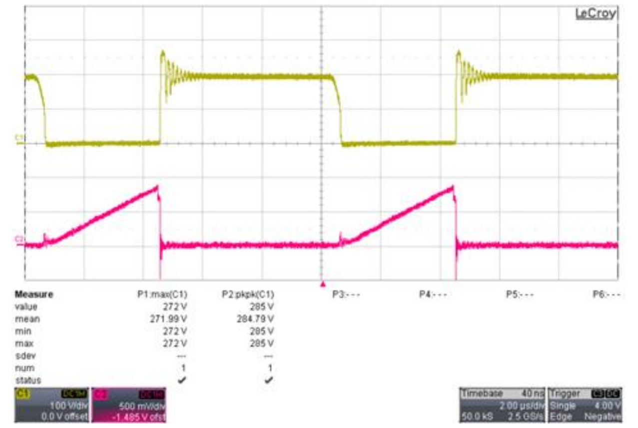
Channel 1; C1(Yellow) : Drain voltage (V_{Drain})

Channel F1 : Frequency track of C1

Frequency jittering from 90 kHz ~ 98 kHz, Jitter period is set at 4 ms internally

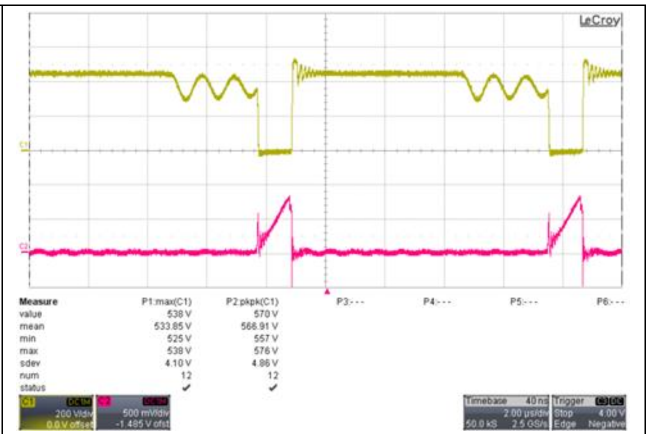
Figure 19 Frequency jittering @ 85 V_{AC} and max. load

11.4 Drain and current sense voltage at maximum load



Channel 1; C1 : Drain-source voltage (V_{DS})
Channel 2; C2 : Current sense voltage (V_{CS})

V_{Drain_peak} @ 85 V_{AC} = 285 V



Channel 1; C1 : Drain-source voltage (V_{DS})
Channel 2; C2 : Current sense voltage (V_{CS})

V_{Drain_peak} @ 265 V_{AC} = 570 V

Figure 20 Drain and current sense voltage at max. load

11.5 Load transient response (Dynamic load from 10% to 100%)

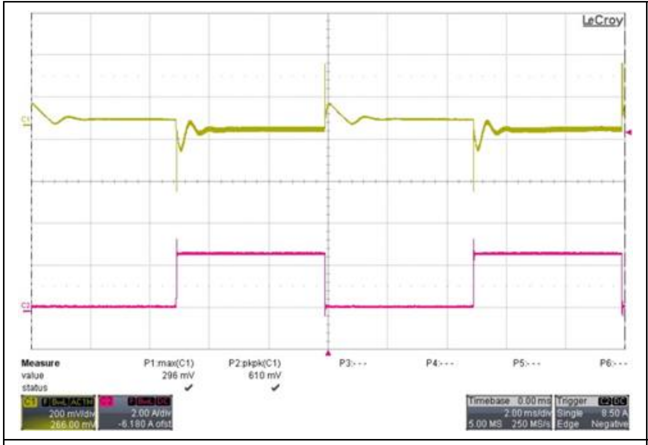
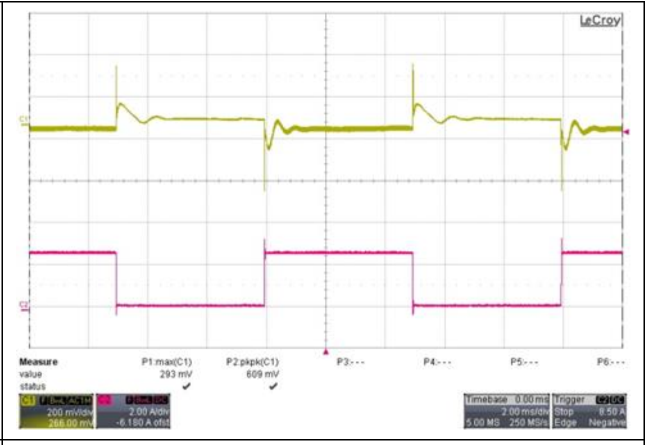
	
Channel 1; C1 : Output ripple voltage (V_{out}) Channel 2; C2 : Output current (I_{out})	Channel 1; C1 : Output ripple voltage (V_{out}) Channel 2; C2 : Output current (I_{out})
$V_{ripple\_pk\_pk}$ @ 85 V_{AC} =610 mV (Load change from10% to 100%, 100 Hz,0.4 A/µS slew rate) Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	$V_{ripple\_pk\_pk}$ @ 265 V_{AC} =609 mV (Load change from10% to 100%, 100 Hz,0.4A/µS slew rate) Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 21 Load transient response

11.6 Output ripple voltage at maximum load

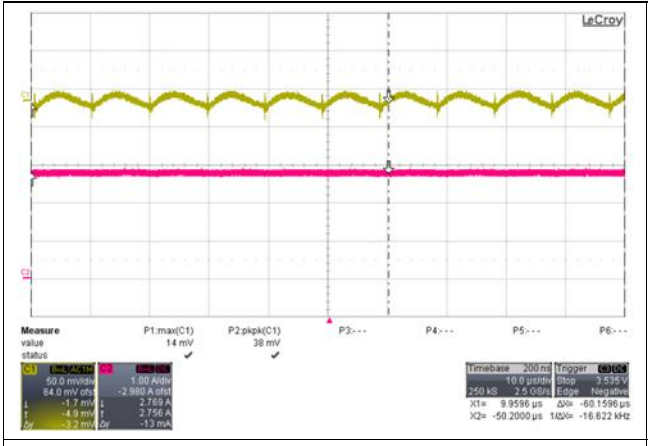
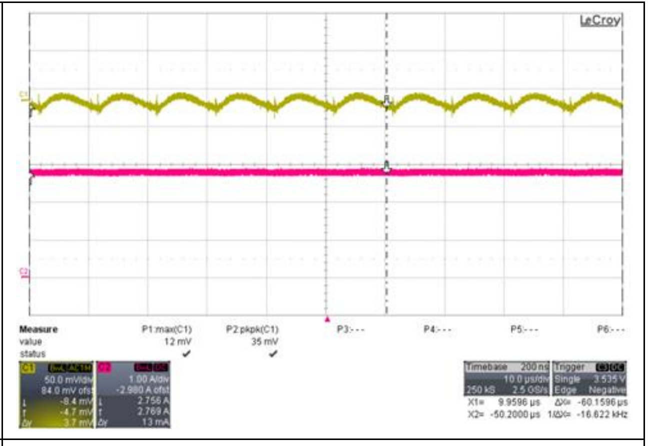
	
Channel 1; C1 : Output ripple voltage (V_{out}) Channel 2; C2 : Output current (I_{out})	Channel 1; C1 : Output ripple voltage (V_{out}) Channel 2; C2 : Output current (I_{out})
$V_{ripple\_pk\_pk}$ @ 85 V_{AC} 38 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	$V_{ripple\_pk\_pk}$ @ 265 V_{AC} = 35 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 22 AC output ripple at max. load

11.7 Output ripple voltage during burst mode at 1 W load

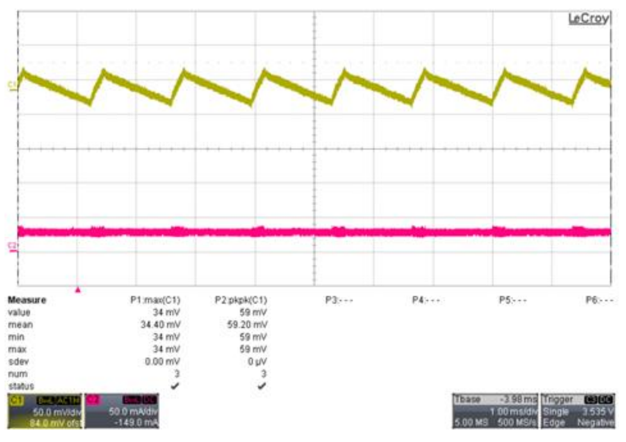
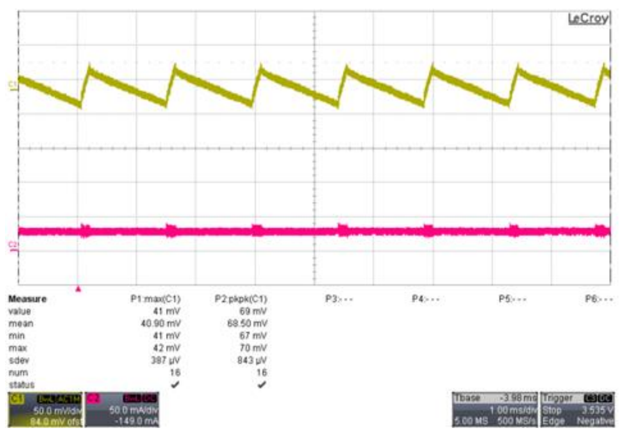
	
Channel 1; C1 : Output ripple voltage (V_{out}) Channel 2; C2 : Output current (I_{out})	Channel 1; C1 : Output ripple voltage (V_{out}) Channel 2; C2 : Output current (I_{out})
$V_{ripple\_pk\_pk}$ @ 85 V_{AC} = 59 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	$V_{ripple\_pk\_pk}$ @ 265 V_{AC} = 70 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 23 AC output ripple at 1 W load

11.8 Active Burst mode operation

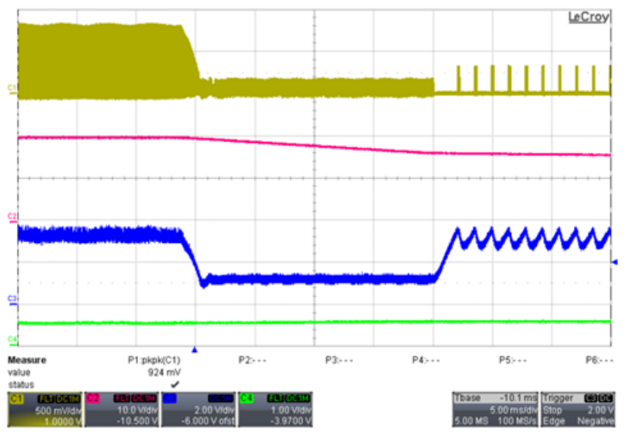
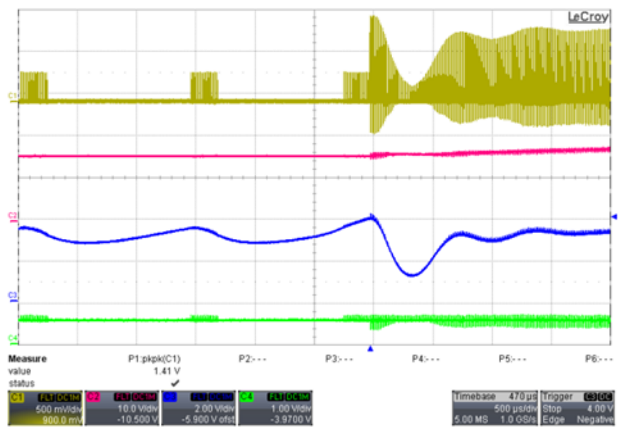
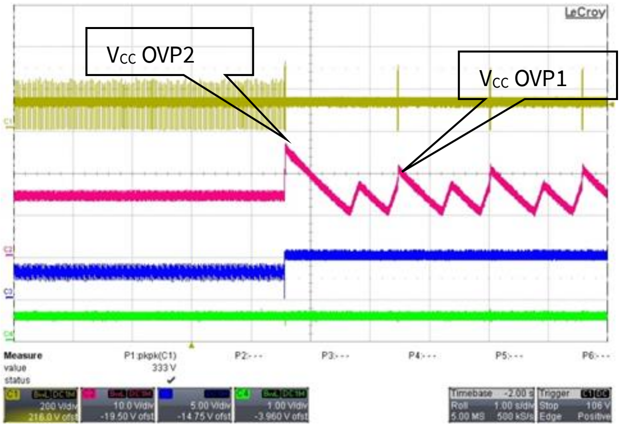
	
Channel 1; C1 : Current sense voltage (V_{CS}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FBB}) Channel 4; C4 :BV voltage (V_{BV})	Channel 1; C1 : Current sense voltage (V_{CS}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FBB}) Channel 4; C4 :BV voltage (V_{BV})
Condition to enter burst: V_{FB}<1.27 V and last for 20 ms (load change form full load to 1 W load)	Condition to leave burst: V_{FB}>4.5 V (load change form 1 W load to full load)

Figure 24 Active burst mode at 85 V_{AC}

11.9 V_{CC} over voltage protection (Odd skip auto restart mode)



Channel 1; C1 : Drain voltage (V_{Drain})

Channel 2; C2 : Supply voltage (V_{CC})

Channel 3; C3 : Feedback voltage (V_{FBB})

Channel 4; C4 : BV voltage (V_{BV})

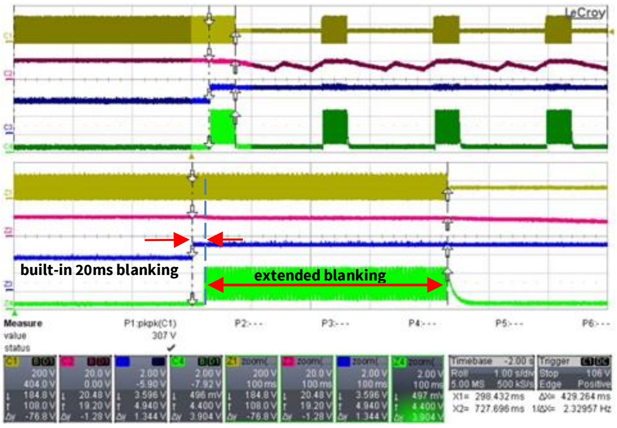
Condition: V_{CC}>25.5 V

V_{CC}>20.5 V and V_{FB}>4.5 V and during soft start

(Short the diode of optocoupler(Pin 1 and 2 of IC2) during system operating at no load)

Figure 25 V_{CC} overvoltage protection at 85 V_{AC}

11.10 Over load protection (Odd skip Auto restart mode)



Channel 1; C1(Yellow) : Drain voltage (V_{Drain})

Channel 2; C2(Red): Supply voltage (V_{CC})

Channel 3; C3(Blue) : Feedback voltage (V_{FBB})

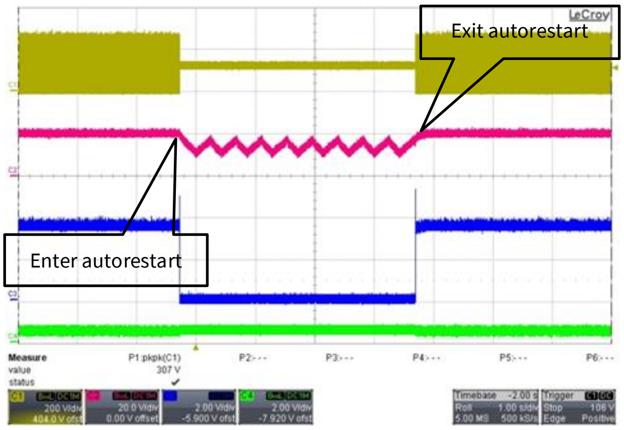
Channel 4; C4(Green) :BV voltage (V_{BV})

Condition: V_{FB}>4.5 V and last for 20 ms andV_{BV}>4.5 V

(output load change from 2.83 A to 4 A)

Figure 26 Over load protection with built-in+extended blanking time at 85 V_{AC}

11.11 V_{CC} under voltage/Short optocoupler protection (Normal auto restart mode)



Channel 1; C1(Yellow) : Drain voltage (V_{Drain})

Channel 2; C2(Red): Supply voltage (V_{CC})

Channel 3; C3(Blue) : Feedback voltage (V_{FBB})

Channel 4; C4(Green) :BV voltage (V_{BV})

Condition: V_{CC}<10.5 V

(short the transistor of optocoupler(Pin 3 and 4 of IC2) during system operating @ full load and release)

Figure 27 V_{CC} under voltage/short optocoupler protection at 85 V_{AC}

11.12 AC Line input OVP mode

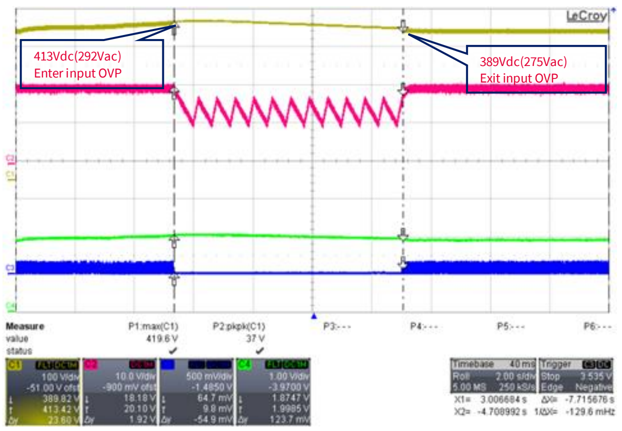
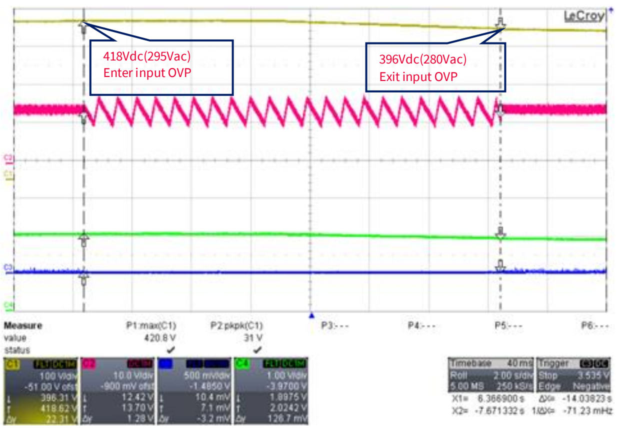
	
Channel 1; C1(Yellow) : Bulk voltage(V_{bulk}) Channel 2; C2(Red) : Supply voltage (V_{CC}) Channel 3; C3(Blue : Current sense voltage (V_{CS}) Channel 4; C4 (Green): BV voltage (V_{BV})	Channel 1; C1(Yellow) : Bulk voltage(V_{bulk}) Channel 2; C2(Red) : Supply voltage (V_{CC}) Channel 3; C3(Blue : Current sense voltage (V_{CS}) Channel 4; C4 (Green): BV voltage (V_{BV})
Max. load condition: V_{BV}>1.98 V and last for 400 µs (OVP detect) V_{BV}<1.91 V and last for 5µs (OVP reset) (gradually increase AC line voltage until OVP detect and decrease AC line until OVP reset)	No load condition: V_{BV}>1.98 V and last for 400 µs (OVP detect) V_{BV}<1.91 V and last for 5 µs (OVP reset) (gradually increase AC line voltage until OVP detect and decrease AC line until OVP reset)

Figure 28 Input OVP

12 References

[1] Infineon Technologies, Datasheet "CoolSET™-F3R80 ICE3AR1080VJZ Off-Line SMPS Current Mode Controller with integrated 800V CoolMOS™and Startup cell(input OVP and Frequency Jitter) in DIP-7"

[2] Infineon Technologies, AN-PS0044-CoolSET F3R80 DIP-7 brownout/input OVP and frequency jitter version design guide-V1.5

Revision History

Major changes since the last revision

Page or Reference	Description of change
--	First Release

Trademarks of Infineon Technologies AG

AURIX™, C166™, CanPAK™, CIPOS™, CIPURSE™, CoolMOS™, CoolSET™, CORECONTROL™, CROSSAVE™, DAVE™, DI-POL™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPIM™, EconoPACK™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, I²RF™, ISOFACE™, IsoPACK™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OptiMOS™, ORIGA™, POWERCODE™, PRIMARION™, PrimePACK™, PrimeSTACK™, PRO-SIL™, PROFET™, RASIC™, ReverSave™, SatRIC™, SIEGET™, SINDRION™, SIPMOS™, SmartLEWIS™, SOLID FLASH™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™.

Other Trademarks

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, KEIL™, PRIMECELL™, REALVIEW™, THUMB™, µVision™ of ARM Limited, UK. AUTOSAR™ is licensed by AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-iq™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOS™ of Epcos AG. FLEXGO™ of Microsoft Corporation. FlexRay™ is licensed by FlexRay Consortium. HYPERTERMINAL™ of Hilgraeve Incorporated. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ Openwave Systems Inc. RED HAT™ Red Hat, Inc. RFMD™ RF Micro Devices, Inc. SIRIUS™ of Sirius Satellite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex Limited.

Last Trademarks Update 2011-11-11

www.infineon.com

Edition 2015-05-12

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference

ANEVAL_201503_PL21_016

Legal Disclaimer

THE INFORMATION GIVEN IN THIS APPLICATION NOTE (INCLUDING BUT NOT LIMITED TO CONTENTS OF REFERENCED WEBSITES) IS GIVEN AS A HINT FOR THE IMPLEMENTATION OF THE INFINEON TECHNOLOGIES COMPONENT ONLY AND SHALL NOT BE REGARDED AS ANY DESCRIPTION OR WARRANTY OF A CERTAIN FUNCTIONALITY, CONDITION OR QUALITY OF THE INFINEON TECHNOLOGIES COMPONENT. THE RECIPIENT OF THIS APPLICATION NOTE MUST VERIFY ANY FUNCTION DESCRIBED HEREIN IN THE REAL APPLICATION. INFINEON TECHNOLOGIES HEREBY DISCLAIMS ANY AND ALL WARRANTIES AND LIABILITIES OF ANY KIND (INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS OF ANY THIRD PARTY) WITH RESPECT TO ANY AND ALL INFORMATION GIVEN IN THIS APPLICATION NOTE.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office. Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.