

SiC

Silicon Carbide Diode

5th Generation thinQ!TM

650V SiC Schottky Diode

IDK12G65C5

Final Data Sheet

Rev. 2.1, 2017-08-11

Power Management & Multimarket

5th Generation thinQ!™ SiC Schottky Diode

IDK12G65C5

1 Description

ThinQ!™ Generation 5 represents Infineon leading edge technology for the SiC Schottky Barrier diodes. The Infineon proprietary diffusion soldering process, already introduced with G3 is now combined with a new, more compact design and thin-wafer technology. The result is a new family of products showing improved efficiency over all load conditions, resulting from both the improved thermal characteristics and a lower figure of merit ($Q_C \times V_f$).

The new thinQ!™ Generation 5 has been designed to complement our 650V CoolMOS™ families: this ensures meeting the most stringent application requirements in this voltage range.

Features

- Revolutionary semiconductor material - Silicon Carbide
- Benchmark switching behavior
- No reverse recovery/ No forward recovery
- Temperature independent switching behavior
- High surge current capability
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target applications
- Breakdown voltage tested at 27 mA²⁾
- Optimized for high temperature operation

Benefits

- System efficiency improvement over Si diodes
- System cost / size savings due to reduced cooling requirements
- Enabling higher frequency / increased power density solutions
- Higher system reliability due to lower operating temperatures
- Reduced EMI

Applications

- Switch mode power supply
- Power factor correction
- Solar inverter
- Uninterruptible power supply

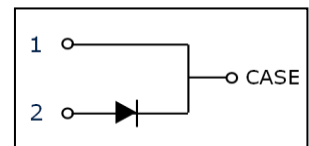
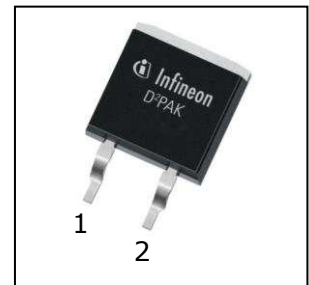


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DC}	650	V
$Q_C (V_R = 400 \text{ V})$	18	nC
$E_C (V_R = 400 \text{ V})$	4.3	μJ
$I_F (T_C < 140^\circ\text{C})$	12	A

Table 2 Pin Definition

Pin 1	Pin 2	Pin 3
C	A	n.a.

Type / ordering Code	Package	Marking	Related links
IDK12G65C5	PG-TO263-2	D1265C5	www.infineon.com/sic

1) J-STD20 and JESD22

2) All devices tested under avalanche conditions for a time period of 10 ms

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2 Maximum ratings

Table 3 Maximum ratings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Continuous forward current	I_F	–	–	12	A	$T_C < 140^\circ\text{C}$, $D = 1$
Surge non-repetitive forward current, sine halfwave	$I_{F,SM}$	–	–	97		$T_C = 25^\circ\text{C}$, $t_p = 10\text{ ms}$
		–	–	83		$T_C = 150^\circ\text{C}$, $t_p = 10\text{ ms}$
Non-repetitive peak forward current	$I_{F,max}$	–	–	505		$T_C = 25^\circ\text{C}$, $t_p = 10\text{ }\mu\text{s}$
i^2t value	$\int i^2 dt$	–	–	47	A ² s	$T_C = 25^\circ\text{C}$, $t_p = 10\text{ ms}$
		–	–	35		$T_C = 150^\circ\text{C}$, $t_p = 10\text{ ms}$
Repetitive peak reverse voltage	V_{RRM}	–	–	650	V	$T_j = 25^\circ\text{C}$
Diode dv/dt ruggedness	dv/dt	–	–	100	V/ns	$V_R = 0..480\text{ V}$
Power dissipation	P_{tot}	–	–	104	W	$T_C = 25^\circ\text{C}$
Operating and storage temperature	$T_j; T_{stg}$	-55	–	175	$^\circ\text{C}$	–

3 Thermal characteristics

Table 4 Thermal characteristics TO-263-2

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	–	0.9	1.5	K/W	–
Thermal resistance, junction-ambient ¹⁾	R_{thJA}	–	–	62		SMD version, device on PCB, minimal footprint
		–	35	–		SMD version, device on PCB, 6 cm ² cooling area

1) Device on 40 mm * 40 mm * 1.5 mm one layer epoxy PCB FR4 with 6 cm² copper area (thickness 70 μm) for cathode connection, PCB is vertical without air stream cooling.

4 Electrical characteristics

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
DC blocking voltage	V_{DC}	650	–	–	V	$I_R = 0.19 \text{ mA}, T_j = 25^\circ\text{C}$
Diode forward voltage	V_F	–	1.5	1.8		$I_F = 12 \text{ A}, T_j = 25^\circ\text{C}$
		–	1.8	2.2		$I_F = 12 \text{ A}, T_j = 150^\circ\text{C}$
Reverse current	I_R	–	0.65	190	μA	$V_R = 650 \text{ V}, T_j = 25^\circ\text{C}$
		–	0.16	68		$V_R = 600 \text{ V}, T_j = 25^\circ\text{C}$
		–	2.4	1350		$V_R = 650 \text{ V}, T_j = 150^\circ\text{C}$

Table 6 AC characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Total capacitive charge	Q_c	–	18	–	nC	$V_R = 400 \text{ V}, di/dt = 200 \text{ A}/\mu\text{s}$ $I_F \leq I_{F,MAX}, T_j = 150^\circ\text{C}$.
Total Capacitance	C	–	360	–	pF	$V_R = 1 \text{ V}, f = 1 \text{ MHz}$
		–	48	–		$V_R = 300 \text{ V}, f = 1 \text{ MHz}$
		–	47	–		$V_R = 600 \text{ V}, f = 1 \text{ MHz}$

5 Electrical characteristics diagrams

Table 7

Power dissipation	Diode forward current
$P_{tot} = f(T_C); R_{thJC,max}$	$I_F = f(T_C); T_j \leq 175^\circ\text{C}; R_{thJC,max};$ Parameter: $D =$ duty cycle

Table 8

Typical forward characteristics	Typical forward characteristics in surge current
$I_F = f(V_F); t_p = 200 \mu\text{s};$ parameter: T_j	$I_F = f(V_F); t_p = 200 \mu\text{s};$ parameter: T_j

Table 9

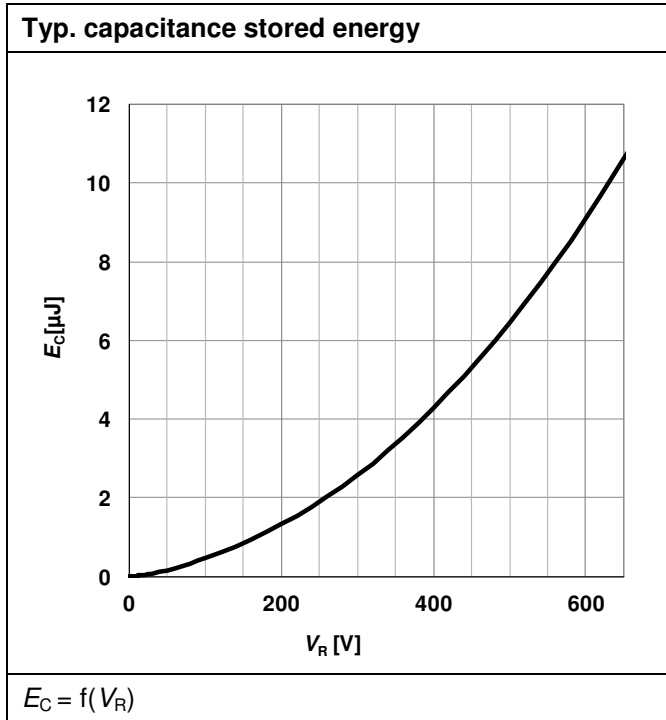
Typ. capacitance charge vs. current slope ¹⁾	Typ. reverse current vs. reverse voltage
$Q_C = f(di_F/dt); T_j = 150^\circ\text{C}; V_R = 400\text{ V}; I_F \leq I_{F,max}$	$I_R = f(V_R); \text{parameter: } T_j$

1) Only capacitive charge, guaranteed by design.

Table 10

Max. transient thermal impedance	Typ. capacitance vs. reverse voltage
$Z_{th,jc} = f(t_p); \text{parameter: } D = t_p/T;$	$C = f(V_R); T_j = 25^\circ\text{C}; f = 1\text{ MHz}$

Table 11



6 Simplified forward characteristics model

Table 12

Equivalent forward current curve	Mathematical Equation
	$V_F = V_{TH} + R_{DIFF} \cdot I_F$ $V_{TH}(T_j) = -0.001 \cdot T_j + 1.04 \text{ [V]}$ $R_{DIFF}(T_j) = 1.07 \cdot 10^{-6} \cdot T_j^2 + 1.07 \cdot 10^{-4} \cdot T_j + 0.039 \text{ [\Omega]}$
$V_F = f(I_F)$	$T_j \text{ [}^\circ\text{C]}; -55^\circ\text{C} < T_j < 175^\circ\text{C}; I_F < 24 \text{ A}$

7 Package outlines

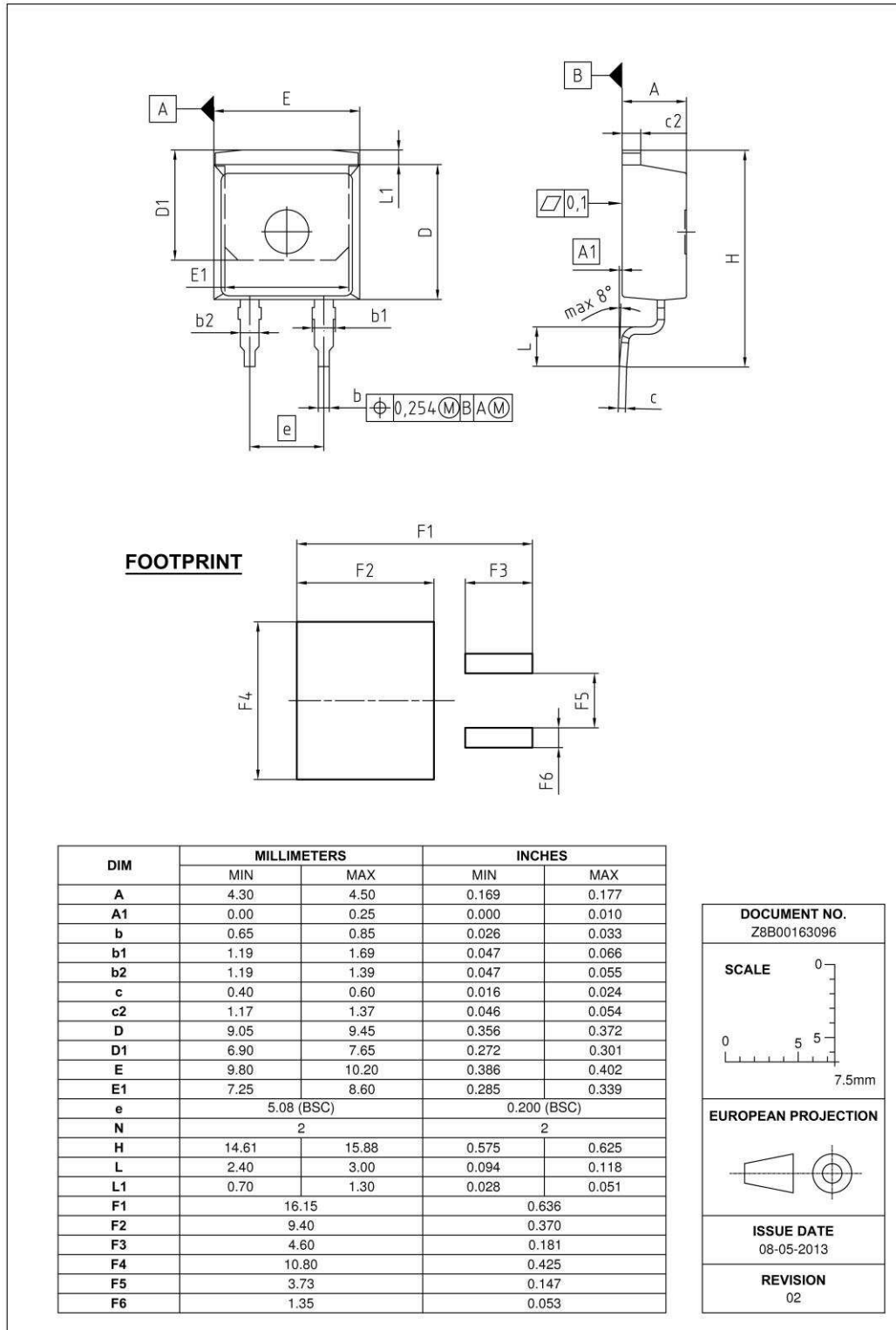


Figure 1 Outlines TO-263-2, dimensions in mm/inch

5th Generation thinQ!™ SiC Schottky Diode

IDK12G65C5

Revision History

IDK12G65C5

Revision: 2017-09-06, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.1	2017-09-06	Updated IR,max values in table 5

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