TLE8242-2

8 Channel Fixed Frequency Constant Current Control With Current Profile Detection

Automotive Power

Never stop thinking

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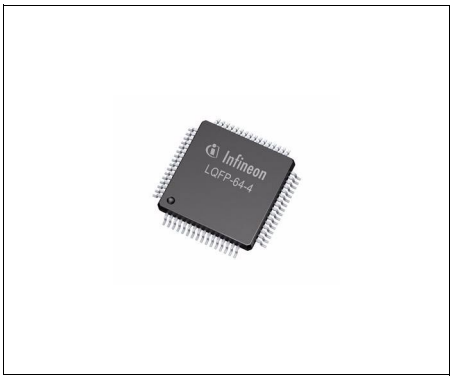
8 Channel Fixed Frequency Constant Current Control With Current Profile Detection **TLE8242-2**

AEC Qualified RoHS

1 Overview



PG-LQFP-64

1.1 Features

- Low side constant current control pre-driver integrated circuit
- Eight independent channels
- Output current programmable with 11 bit resolution
  - Current range = 0 to 1.2A (typ) with a 0.2 Ω sense resistor
  - Resolution = 0.78125 mA/bit (typ) with a 0.2 Ω sense resistor
  - +/- 2% full scale error over temperature when autozero is used
- Programmable PWM frequency via SPI from approximately 10 Hz to 4 kHz (typ)
- Programmable KP and KI coefficients for the PI controller for each channel
- Programmable superimposed dither
  - Dither programmed by setting a dither step size and the number of PWM periods in each dither period
  - Programmed via the SPI interface
  - The dither for each channel can be programmed independently
- Programmable synchronization of the PWM control signals
  - Phase delay time set via the SPI interface
  - Synchronization initiated via signal at the PHASE_SYNC input pin
  - Channels within one device and between multiple devices can be synchronized
- Each channel can be configured to for constant current control or for direct PWM control via SPI
- In Direct PWM mode, a current profile detection function is engaged
  - Verifies solenoid armature movement
  - Profile characteristics programmed via SPI
  - Pass / Fail Status can be read via SPI
- Interface and Control
  - 32 Bit SPI (Serial Peripheral Interface) - Slave only
  - ENABLE pin to disable all channels or freeze all channels
  - Active low RESET_B pin resets internal registers to their default state and disables all channels
  - Open drain FAULT pin can be programmed to transition low when various faults are detected
  - 5.0V and 3.3V logic compatible I/O
- Protection
  - Over current shutdown - monitored at POSx pin
  - Programmable over current threshold
  - Programmable over current delay time
  - Programmable over current retry time
  - Battery pin (BAT) overvoltage shutdown

Type	Package	Marking
TLE8242-2	PG-LQFP-64	TLE8242-2L

- Diagnostics
  - Over current
  - Open load in on state
  - Open load in off state
  - Short to ground
  - Test complete bit - indicates that fault detection test has completed
- Control loop monitor capabilities
  - The average current measurement over the last completed dither cycle for a selected channel can be accessed via SPI
  - The minimum and maximum current measurements over the last completed dither cycle for a selected channel can be accessed via SPI. This data can be used to measure the achieved dither amplitude
  - The duty cycle of each channel can be accessed via SPI
  - The auto zero values used to cancel the offsets of the input amplifiers can be accessed via SPI
- Required External Components:
  - N-Channel Logic level (5V) MOSFET transistor with typical Ron ≤ 100 mΩ (e.g. SPD15N06S2L-64)
  - Recirculation diode (ultrafast)
  - Sense resistor (0.2Ω for 1.2A average output current range)
- Green Product (RoHS compliant)
- AEC Qualified

1.2 Applications

- Variable Force Solenoids (e.g. automatic transmission solenoids)
- Other constant current solenoids
  - Idle Air Control
  - Exhaust Gas Recirculation
  - Vapor Management Valve
  - Suspension Control

1.3 General Description

The TLE8242G IC is an eight channel low-side constant current control predriver IC. Each channel can be configured to function either in direct PWM mode or in constant current mode by setting the appropriate CM bit in SPI message #1.

1.3.1 Direct PWM Mode Operation

For Direct PWM operation, the POSx and NEGx pins must be connected to the circuit in either of the configurations shown in **Figure 1**. If the sense resistor is included, the load current can be monitored by the microcontroller via a SPI command. The open load in on state fault detection feature is disabled in direct PWM mode.

Note: An external flyback clamp is required in this configuration otherwise the IC may be damaged.

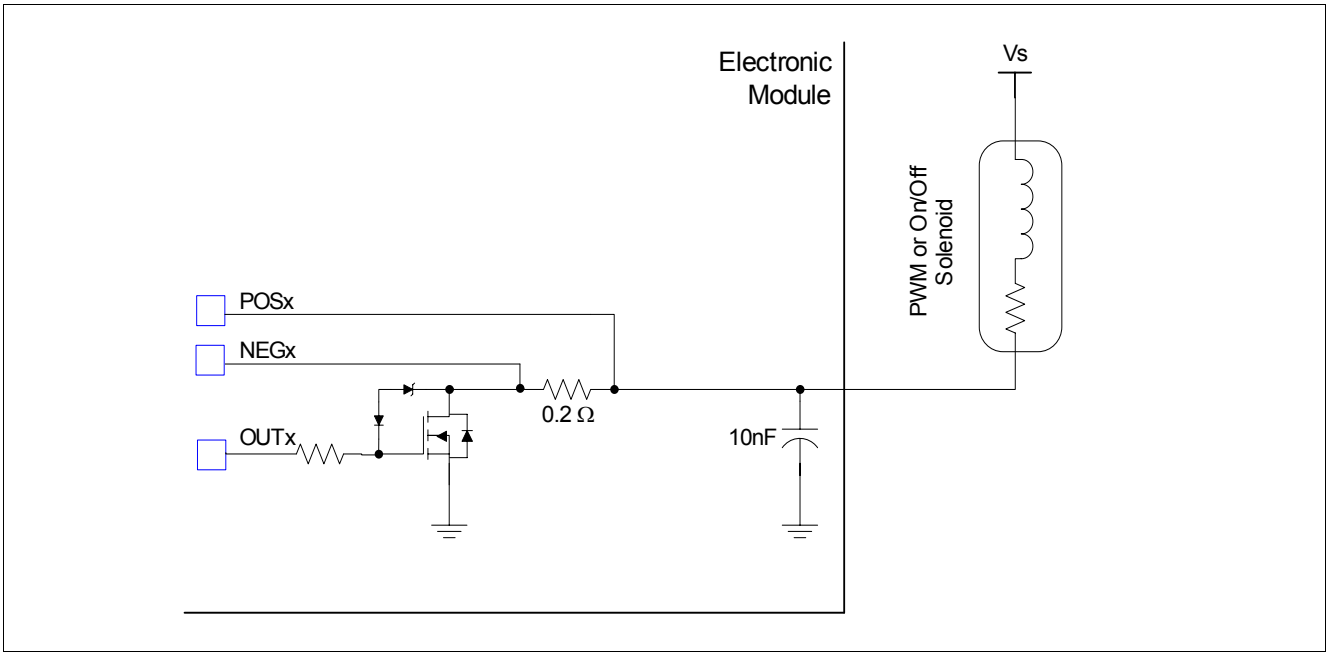


Figure 1 External Circuit Diagram for Direct PWM Mode Operation

1.3.2 Constant Current Mode Operation

During constant current operation, the POSx and NEGx pins must be connected to the circuit in the configuration shown in **Figure 2**.

Note: An external recirculation diode is required in this configuration otherwise the IC may be damaged.

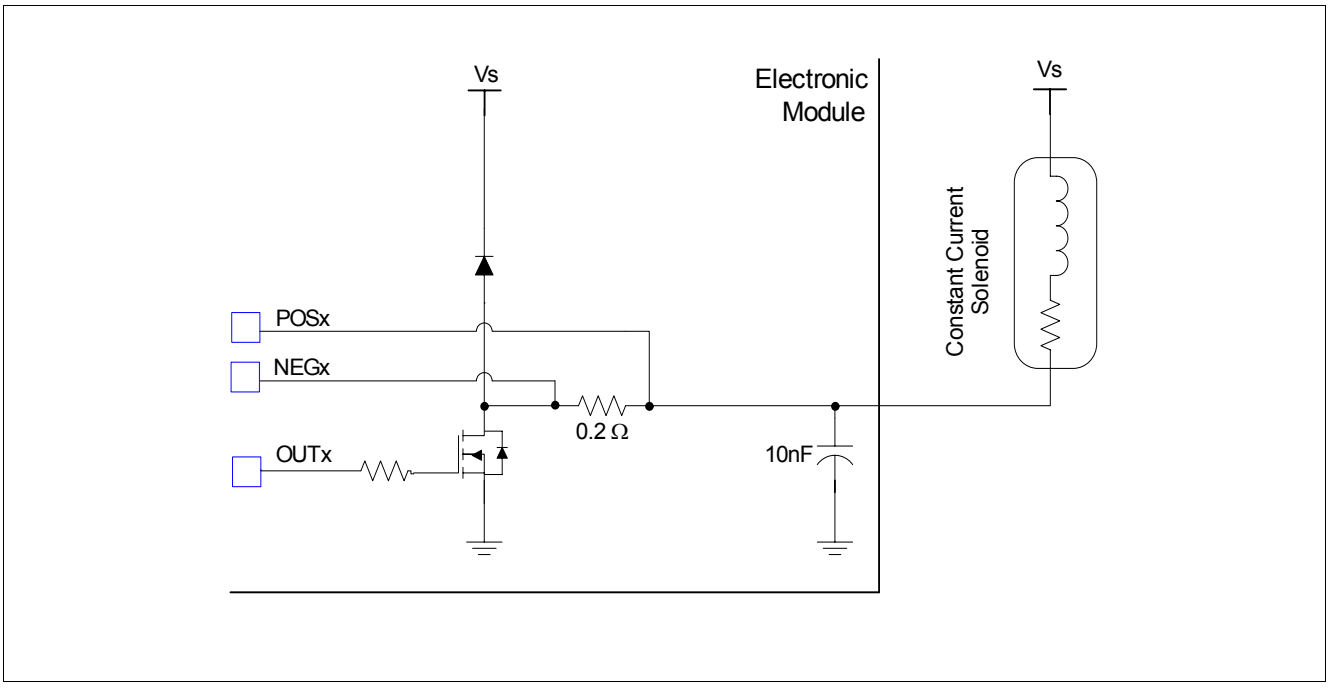


Figure 2 External Circuit Diagram for Constant Current Mode Operation

During constant current operation, the PWM control signal driven at the OUTx pin is controlled by the control loop shown in **Figure 3**. The PWM Frequency is programmed via the SPI message # 8. In this message the main period

divider, N, can be set to any value between 79 and 2^{14} -1 and the divider M can be set to 32, 64, or 128. In direct PWM mode, the value M can also be set to 512. The equation for calculating the PWM frequency is:

$$F_{PWM} = \frac{F_{CLK}}{M * N}$$

In constant current mode, the value of M is the number of A/D samples within one PWM period. Setting the SAM bit in SPI Message #8 to a “1” will cause the ADC samples immediately following a change in the state of the OUTx pin to be discarded. If the SAM bit is set to ‘0’, all M A/D samples are used in the average calculation.

The 11 bit Current Set Point is programmed via the SPI message #10. The equation for calculating the current setpoint is:

$$\text{CurrentSetpoint[mA]} = \frac{\text{setpoint(11bit)}}{2^{11}} * \frac{320[\text{mV}]}{R_{SENSE}[\text{ohm}]}$$

The Proportional coefficient (KP) and the Integral coefficient (KI) of the control loop are programmed in SPI message #9. The KP and KI values should be set to values that result in the desired transient response of the control loop. The duty cycle of the OUTx pin can be calculated from the difference equations:

$$DutyCycle(k) = KP * \frac{Rsense\ [Ohm]}{0.04 * M * N} * error(k-1)[A] + INT(k)$$

$$INT(k) = KI * \frac{Rsense\ [Ohm]}{0.04 * M * N} * error(k-1)[A] + INT(k-1)$$

where error is the difference between the commanded average current and measured average current in units of Amps.

where k indicates the integer number of PWM periods that have elapsed since current regulation was initiated.

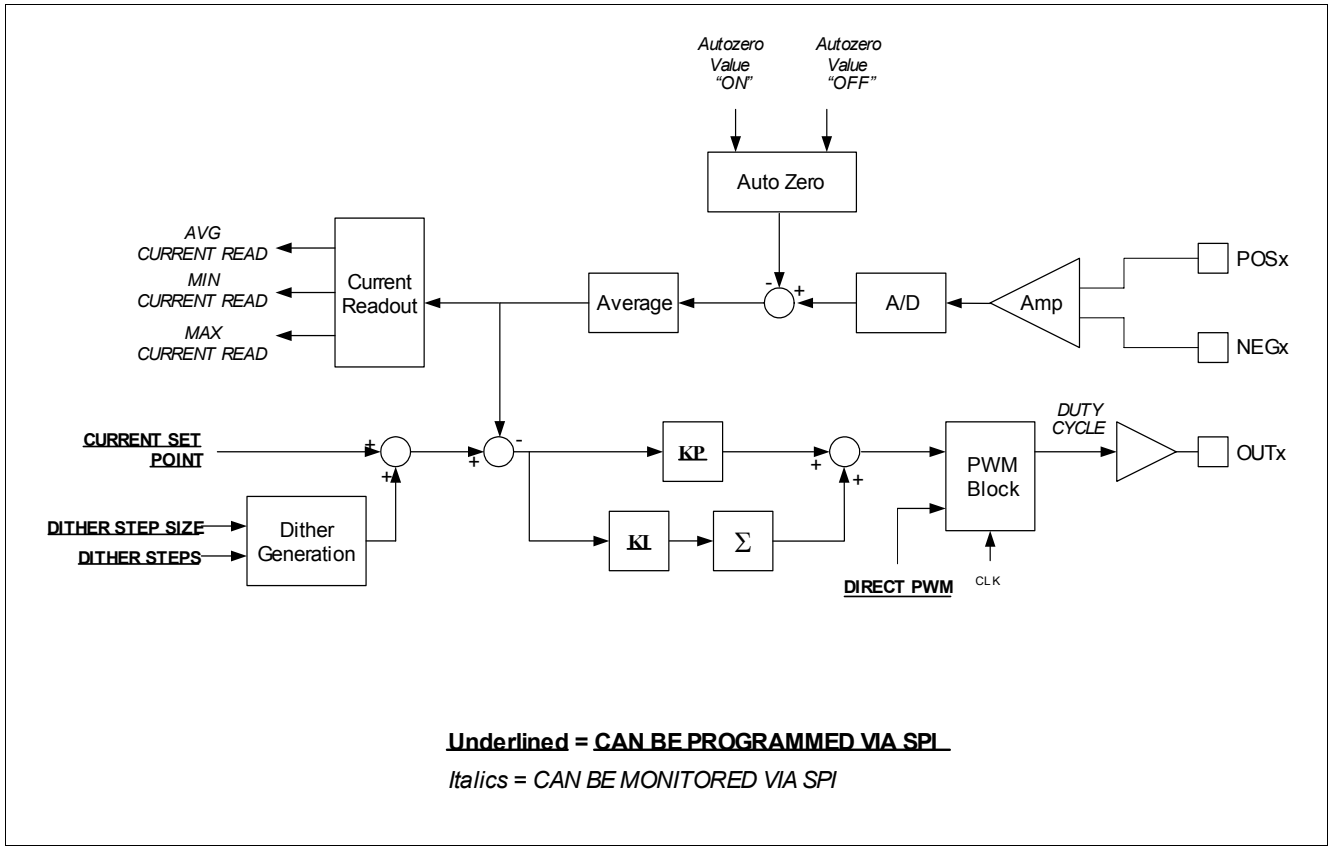


Figure 3 Control Loop - Simplified Diagram

Table 1 describes the effect on the integrator of the PI controller of several events.

Table 1 Control Loop Integrator Control

Condition	Action to Integrator
Reset Active	Cleared
V5D undervoltage	Cleared
V5Ax undervoltage	Cleared
ENABLE pin low (SPI message #10 bit EN = 0)	Cleared
ENABLE pin low (SPI message #10 bit EN = 1)	Remains Operational
VBAT overvoltage	Held at current value
Short to BAT	Cleared
Phase_Sync Transition	Remains Operational Integrator value for first PWM cycle = value from end of last complete PWM cycle.
Average Current set to 0	Cleared
Control Mode set to Direct PWM	Cleared
Main Period Set (N, M) Changed	Remains Operational
KP, KI settings Changed	Remains Operational

Auto Zero

The TLE8242 includes an autozero feature for each channel. When the setpoint of a channel is set to 0 mA and the autozero is triggered by an SPI command, the offset of the amplifiers and analog to digital converters are measured. The time required for the autozero sequence is calculated according to the formula:

$$T_{AZ} = \frac{4 * M * N}{F_{CLK}}$$

The measured offsets can be read via SPI message #14. these offsets will be subtracted from the A/D converter output as shown in **Figure 3** when the current set point is greater than 0.

Dither

A triangular dither waveform can be superimposed on the current set point by setting the amplitude and frequency parameters of the dither waveform via SPI messages #10 and #11. See the SPI message section for details.

The first programmed value is the step size of the dither waveform which is the number of bits added or subtracted from the setpoint per PWM period. One LSb of the dither step size is 1/4th the magnitude of the nominal setpoint current value. The second programmed value is the number of steps in one quarter of the dither waveform.

When dither is enabled, a new average current set point will not be activated until the current dither cycle has completed. The dither cycle is completed on the positive zero crossing of the dither waveform. A new dither amplitude setting or a new dither frequency setting will also not be activated until the current dither cycle has completed. See **Figure 4**.

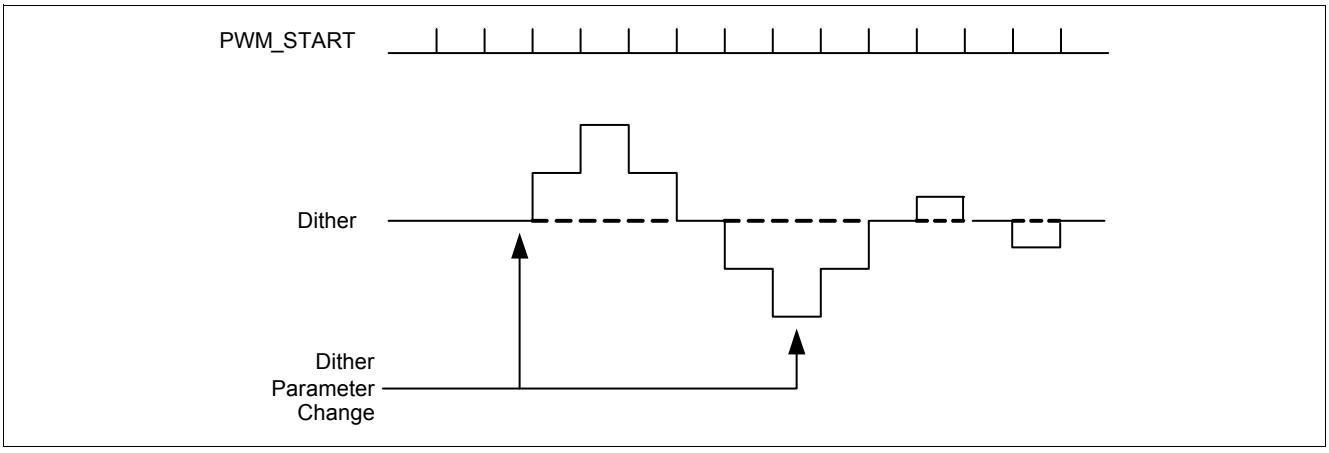


Figure 4 New Dither Values Programmed and the Resulting Waveform Timing

Note: The actual measured dither waveform is attenuated and phase shifted according to the frequency response of the control loop.

2 Block Diagram

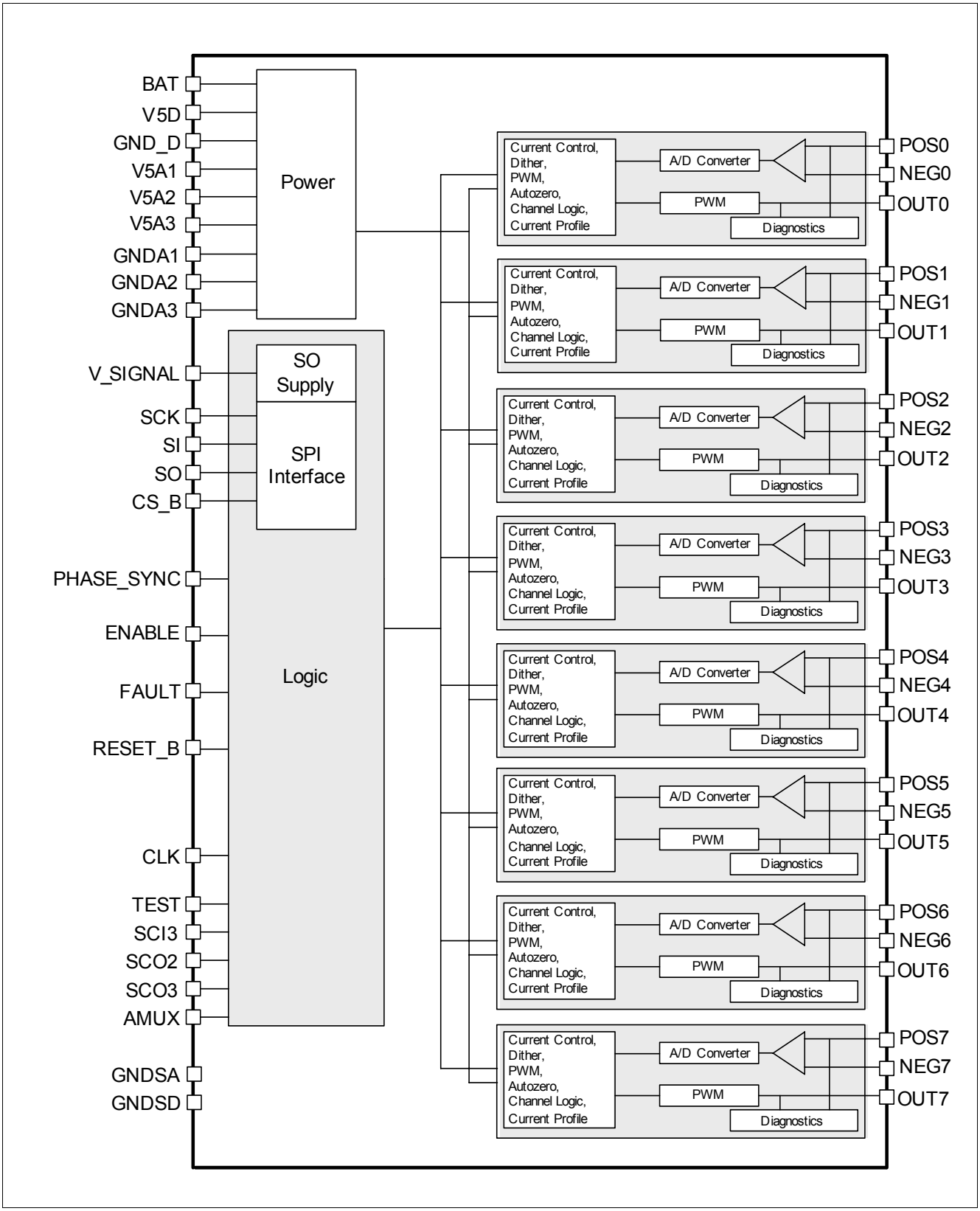


Figure 5 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

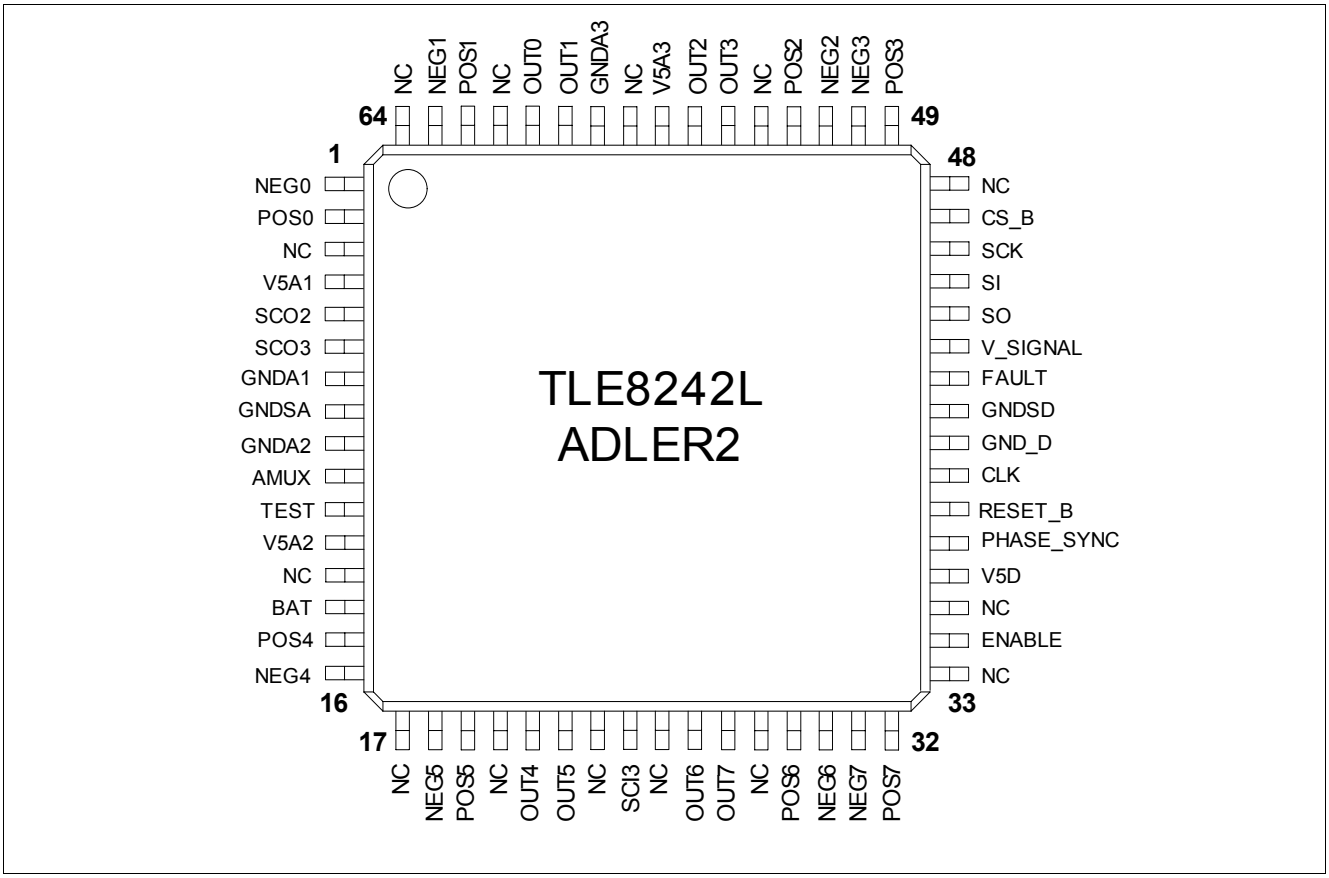


Figure 6 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	NEG0	**Channel #0 Negative sense pin;** Connect to the “FET” side of the external sense resistor
2	POS0	**Channel #0 Positive sense pin;** Connect to the “load” side of the external sense resistor
3	NC	**Not Connected;** do not connect to external supply, ground, or signal
4	V5A1	**Supply Voltage;** 5V input for analog circuits. An external capacitor is to be connected between this pin and GND_A near this pin
5	(T) SCO2	**Test Pin;** Used for IC test. Must be connected to GND_D for specified operation of the IC
6	(T) SCO3	**Test Pin;** Used for IC test. Must be connected to GND_D for specified operation of the IC
7	GND_A1	**Ground;** ground pin for analog circuits
8	GNDSA	**Ground;** ground pin for substrate connection near analog circuits

Pin	Symbol	Function
9	GND_A2	**Ground;** ground pin for analog circuits
10	(T) AMUX	**Test Pin;** Used for IC test. Must be connected to GND_D for specified operation of the IC
11	(T) TEST	**Test Pin;** Used for IC test. Must be connected to GND_D for specified operation of the IC
12	V5A2	**Supply Voltage;** 5V input for analog. An external capacitor is to be connected between this pin and GND_A near this pin
13	NC	**Not Connected;** do not connect to external supply, ground, or signal
14	BAT	**Battery Sense Input;** for over-voltage detection. Connect through a series resistor (e.g. 1 K ohm) to the solenoid supply voltage. A large electrolytic capacitor (e.g. 47uF) should be placed between the BAT supply and ground
15	POS4	**Channel #4 Positive sense pin**; Connect to the “load” side of the external sense resistor
16	NEG4	**Channel #4 Negative sense pin**; Connect to the “FET” side of the external sense resistor
17	NC	**Not Connected;** do not connect to external supply, ground, or signal
18	NEG5	**Channel #5 Negative sense pin**; Connect to the “FET” side of the external sense resistor
19	POS5	**Channel #5 Positive sense pin;** Connect to the “load” side of the external sense resistor
20	NC	**Not Connected;** do not connect to external supply, ground, or signal
21	OUT4	**Gate driver output for channel #4;** Connect to the gate of the external MOSFET
22	OUT5	**Gate driver output for channel #5;** Connect to the gate of the external MOSFET
23	NC	**Not Connected;** do not connect to external supply, ground, or signal
24	(T) SCI3	**Test Pin;** Used for IC test. Must be connected to GND_D for specified operation of the IC
25	NC	**Not Connected;** do not connect to external supply, ground, or signal
26	OUT6	**Gate driver output for channel #6**; Connect to the gate of the external MOSFET
27	OUT7	**Gate driver output for channel #7;** Connect to the gate of the external MOSFET
28	NC	**Not Connected;** do not connect to external supply, ground, or signal
29	POS6	**Channel #6 Positive sense pin;** Connect to the “load” side of the external sense resistor
30	NEG6	**Channel #6 Negative sense pin;** Connect to the “FET” side of the external sense resistor
31	NEG7	**Channel #7 Negative sense pin**; Connect to the “FET” side of the external sense resistor
32	POS7	**Channel #7 Positive sense pin**; Connect to the “load” side of the external sense resistor
33	NC	**Not Connected;** do not connect to external supply, ground, or signal

Pin	Symbol	Function
34	ENABLE	**ENABLE logic input;** When this input pin is low all channels are turned off (zero current) or remain in their last state, depending on how the channel is programmed to respond
35	NC	**Not Connected;** do not connect to external supply, ground, or signal
36	V5D	**Supply Voltage;** 5V input for digital circuits. An external capacitor is to be connected between this pin and GND_D near this pin
37	PHASE_SYNC	**Phase Synchronization Input:** Used to synchronize the rising edges of the PWM signal on the OUTx pins for each channel
38	RESET_B	**Reset Input;** When this input pin is low all channels are turned off and all internal registers are reset to the default state. The part must be held in reset by an external source until all supplies are stable and within tolerance
39	CLK	**CLOCK;** Main clock input for the chip. A clock input of 20 MHz to 40 MHz is required
40	GND_D	**Ground;** ground pin for digital circuits
41	GNDSD	**Ground;** ground pin for substrate connection near digital circuits
42	FAULT	**Fault Output Pin;** Open drain output pin is pulled low when a fault condition is detected. Certain faults can be masked via SPI
43	V_SIGNAL	**Supply Voltage;** Supply pin for the SPI SO output and the pull-up current sources of the digital inputs CS_B and RESET_B. An external capacitor must be connected between this pin and GND_D near this pin
44	SO	**SPI Serial Data Out**
45	SI	**SPI Serial Data In**
46	SCK	**SPI Serial Clock Input**
47	CS_B	**SPI Chip Select Bar;** active low signal
48	NC	**Not Connected;** do not connect to external supply, ground, or signal
49	POS3	**Channel #3 Positive sense pin**; Connect to the “load” side of the external sense resistor
50	NEG3	**Channel #3 Negative sense pin**; Connect to the “FET” side of the external sense resistor
51	NEG2	**Channel #2 Negative sense pin**; Connect to the “FET” side of the external sense resistor
52	POS2	**Channel #2 Positive sense pin**; Connect to the “load” side of the external sense resistor
53	NC	**Not Connected;** do not connect to external supply, ground, or signal
54	OUT3	**Gate driver output for channel #3**; Connect to the gate of the external MOSFET
55	OUT2	**Gate driver output for channel #2;** Connect to the gate of the external MOSFET
56	V5A3	**Supply Voltage;**5V input for analog. An external capacitor is to be connected between this pin and GND_A near this pin.
57	NC	**Not Connected;** do not connect to external supply, ground, or signal
58	GND_A3	**Ground;** ground pin for analog circuits
59	OUT1	**Gate driver output for channel #1**; Connect to the gate of the external MOSFET

Pin	Symbol	Function
60	OUT0	**Gate driver output for channel #0;** Connect to the gate of the external MOSFET
61	NC	**Not Connected;** do not connect to external supply, ground, or signal
62	POS1	**Channel #1 Positive sense pin;** Connect to the “load” side of the external sense resistor
63	NEG1	**Channel #1 Negative sense pin**; Connect to the “FET” side of the external sense resistor
64	NC	**Not Connected;** do not connect to external supply, ground, or signal

4 General Product Characteristics

4.1 Maximum Ratings

Absolute Maximum Ratings [1]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Battery Input (VBAT)	V_{BAT}	-13	50	V	–
4.1.2	Supply Voltage (logic)	V_{5D}, V_{5A1} V_{5A2}, V_{5A3} V_{signal}	-0.3	6.0	V	–
4.1.3	POSx, NEGx	V_{pos}, V_{neg}	-0.3	50	V	–
4.1.4	POSx-NEGx	V_{pos}-V_{neg}	-0.2	13	V	–
4.1.5	OUTx	V_{out}	-0.3	min(V_{5D}+ 0.3; 6)	V	–
4.1.6	RESET_B, SI, SCK, CS_B, CLK, TEST, PHASE_SYNC, ENABLE	V_{io}	-0.3	min(V_{5D}+ 0.3; 6)	V	–
4.1.7	SO, FAULT	V_{io}	-0.3	min(V_{signal} + 0.3; 6)	V	–
4.1.8	Maximum difference between V5D and V5Ax pins		-500	500	mV	–
Currents						
4.1.9	Input Clamp Current ENABLE, PHASE_SYNC, RESET_B, SI, SCK, CS_B, CLK	I_{CLAMP}	5	–5	mA	[2]
Temperatures						
4.1.10	Storage Temperature	T_{stg}	-65	150	°C	–
4.1.11	Junction Temperature	T_j	-40	150	°C	–
ESD Susceptibility						
4.1.12	HBM		-2	2	kV	[3]
4.1.13	CDM all pins		-500	500	V	[4]
4.1.14	CDM corner pins		-750	750	V	[4]

1) Not subject to production test, specified by design.
2) Current needs to be limited only when maximum voltages are exceeded
3) ESD Susceptibility HBM according to EIA/JESD 22-A 114B
4) ESD Susceptibility CDM according to EIA/JESD22-C101

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply Voltage Range for Normal Operation - VBAT	V_{BAT}	5.5	42	V	–
4.2.2	Supply Voltage Range for Normal Operation - V5D, V5A1, V5A2, V5A3	V_{V5D} V_{V5A1}, V_{V5A2}, V_{V5A3}	4.75	5.25	V	–
4.2.3	Supply Voltage Range for Normal Operation -V_SIGNAL	V_{V_SIGNAL}	3.0	5.25	V	–
4.2.4	Clock Frequency	f_{CLK}	20	40	MHz	
4.2.5	PWM Frequency for Normal Operation	f_{PWM}	10	4000	Hz	
4.2.6	Extended PWM Frequency Range	f_{PWM}	10	8000	Hz	Parameter deviations possible
4.2.7	Common Mode Voltage Range for Normal Operation - POSx, NEGx pins.	V_{pos} , V_{neg}	0	30	V	–
4.2.8	Extended Common Mode Voltage Range for Operation - POSx, NEGx pins.	V_{pos} , V_{neg}	0	42	V	Parameter deviations possible

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Ambient[1)]	R_{thJA}	–	38	–	K/W	[2)]

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2, -7 at natural convection on FR4 2s2p board; The Product (chip + Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm, 2 x 35 µm Cu).

5 Functional Description and Electrical Characteristics

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

5.1 Supply and Reference

The device includes a power-on reset circuit. This feature will disable the channels and reset the internal registers to their default values when the voltage on V5A1, V5A2, V5A3, and/or V5D are below their respective reset thresholds.

The V5D pin and GND_D pin are the supply and ground pins for the digital circuit blocks. The current through these pins contain high frequency components. Decoupling with ceramic capacitors and careful PCB layout are required to obtain good EMC performance.

The V5A1, V5A2, V5A3 pins and GND_A pin are the supply and ground pins for the analog circuit blocks.

The V_SIGNAL pin supplies the SPI output pin (SO) and is the source voltage for the pull up currents on the CS_B and RESET_B pins. V_SIGNAL should be connected to the I/O supply of the microcontroller (3.3V or 5.0V).

The BAT pin is an input pin used to detect over voltage faults. This pin is not a power supply input. A series resistor should be connected between this pin and the solenoid supply voltage for transient protection.

Electrical Characteristics:

V5D = 4.75V to 5.25V, Vbat = 5.5V to 42V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.1	Undervoltage reset (internally generated) V5A1, V5A2, and V5A3	V_{V5A1}, V_{V5A2}, V_{V5A3}	3.5	–	4.5	V	Internal reset occurs if V5A1 V5A2, or V5A3 is below the undervoltage limit
5.1.2	Undervoltage reset (internally generated) V5D	V_{V5D}	1.0	–	4.5	V	Internal reset occurs if V5D is under the undervoltage limit
5.1.3	V5D supply current	I_{V5D}	–	–	75 40	mA mA	f_{CLK}=40MHz f_{CLK}=20MHz
5.1.4	V5A1 supply current	I_{V5A1}	–	–	20	mA	
5.1.5	V5A2 supply current	I_{V5A2}	–	–	20	mA	
5.1.6	V5A3 supply current	I_{V5A3}	–	–	5	mA	
5.1.7	V_SIGNAL supply current	I_{V_SIGNAL}	–	–	300	µA	V_{SIGNAL}=5.25V SO = Hi-Z state
5.1.8	VBAT current	I_{VBAT}	–	–	80	µA	full operating range
5.1.9	VBAT current - unpowered	I_{VBAT}	–	–	5	µA	V5D=V5Ax=0V, BAT=14V

5.2 Input / Output

All digital inputs are compatible with 3.3 V and 5 V I/O logic levels. The supply voltage for the SPI output SO is the V_SIGNAL pin. All digital inputs are pulled to a known state by a weak internal current source or current sink when not connected. However, unused digital input pins should be connected to ground or to V_SIGNAL (according to the desired functionality) by an external connection or resistor. All input pin weak internal current sources are supplied by the V_SIGNAL pin.

The RESET_B pin is an active low input pin. When this pin is low, all channels are off, and all internal registers are reset to their default states. The device must be held in reset by an external source until all the power supplies have stabilized. The IC contains an internal power on and undervoltage reset which becomes active when V5D, V5A1, V5A2, or V5A3 fall below the undervoltage reset thresholds.

The ENABLE pin is an active high input pin which must be held high for normal operation of the device. When this pin is held low all channels are either turned off or will remain in the last state, depending on how the enable behavior of the channel is programmed via SPI Message #10. The default condition is that all channels are turned off when the ENABLE pin is low.

The CLK pin is the main clock input for the device. The input thresholds are compatible with 3.3 V and 5.0 V logic levels. No synchronization is required between the clock signal connected to the CLK pin and the SPI clock signal (SCK). All internal clock signals of the TLE8242 (PWM signals, A/D sampling, diagnostics, etc.) are generated from the this clock input. Also, this clock is required for the device to accept and respond to SPI messages.

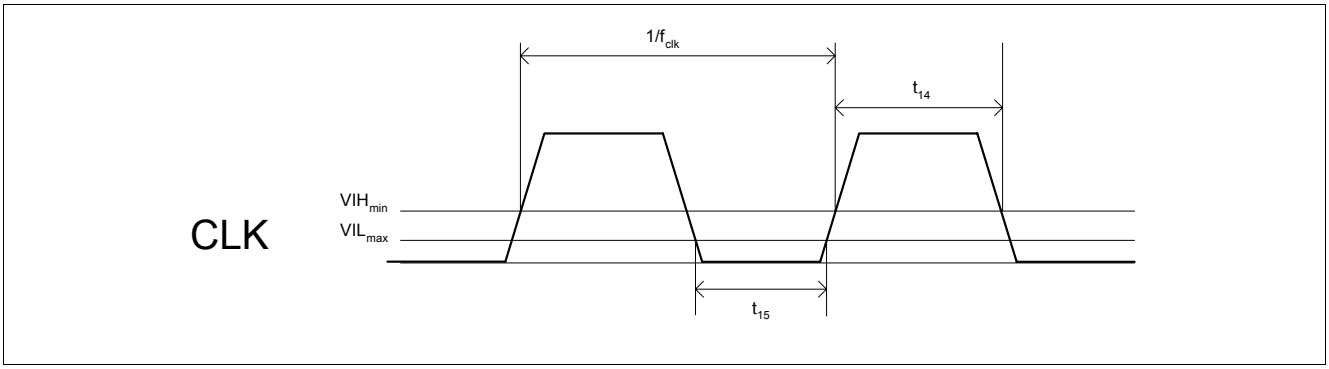


Figure 7 CLK Timing Diagram

The PHASE_SYNC pin is an input pin that can be used by the microcontroller to synchronize the PWM control signals of multiple channels. The desired phase delay between the rising edge of the signal applied to the PHASE_SYNC pin and the rising edge of the PWM signal of each channel can be programmed independently via SPI message #6. The equation for calculating the offset is:

$$T_{offset} = \frac{PhaseSynchOffset}{32 * F_{PWM}}$$

Each time a pulse is received on the PHASE_SYNC pin, the IC will latch a bit which is reported via the response to SPI message #19. (See SPI interface section for bit/message location.) This latch is cleared when the message is read.

Note: The PWM periods are restarted when a rising edge is detected on the PHASE_SYNC pin. A periodic pulse train on this pin will disturb the current regulation.

Note: After exiting the reset state, a pulse is needed on the PHASE_SYNC pin in order to synchronize the PWM periods of the channels

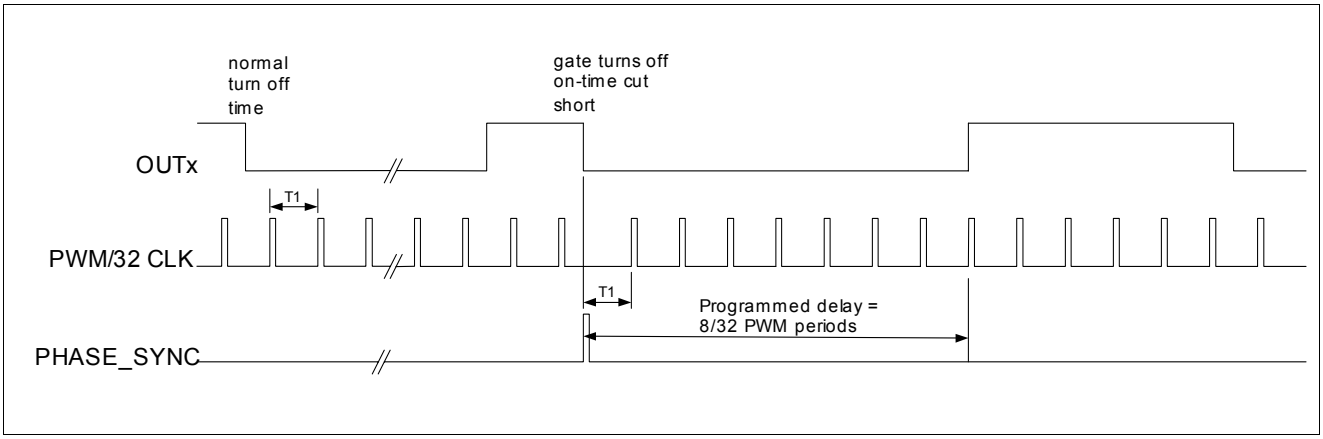


Figure 8 Phase Synchronization Diagram

The TEST, SCI3, SCO2, SCO3, and AMUX pins are used during IC level test. These pins should be connected directly to ground for normal device operation.

The FAULT pin is an open drain output pin. This pin will be pulled low by the device when an unmasked fault has been detected. The fault masks are programmed via SPI message #1.

Electrical Characteristics:

V5D = 4.75V to 5.25V, Vbat = 5.5V to 42V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.1	Logic input low voltage	V_{ILMAX}	–	–	0.8	V	
5.2.2	Logic input high voltage	V_{IHMIN}	2.0	–	–	V	
5.2.3	Logic output low voltage	V_{OLMAX}	–	–	0.2	V	I_L=200µA
5.2.4	Logic output high voltage	V_{OHMIN}	0.8*V_ SIGNAL	–	–	V	I_L=-200µA
5.2.5	Pull down digital input (SI, CLK, SCK, PHASE_SYNC, ENABLE)	I_{pd}	10	–	50	µA	V_{in}=V_SIGNAL
5.2.6	Pull up digital input (CS_B, RESET_B)	I_{pu}	-50	–	-10	µA	V_{in}=0V (Current drain from V_SIGNAL)
5.2.7	Fault pin voltage	$V_{fault.low}$	–	–	0.4	V	Active state; I_{fault}=2mA
5.2.8	Fault pin current	$I_{fault,max}$	2.0	–		mA	Active state; V_{fault}=0.4V
5.2.9	CLK high time (rise 2.0V to fall 2.0V)	t_{14}	8	–	–	ns	
5.2.10	CLK low time (fall 0.8V to rise 0.8V)	t_{15}	8	–	–	ns	

5.3 Diagnostics

The TLE8242 includes both on-state and off-state diagnostics. On-state diagnostics are active when the OUTx pin is driven high and off-state diagnostics are active when the OUTx pin is driven low. A detected fault can be used to activate the open drain FAULT pin on the IC. This pin can be used to interrupt the microcontroller when a fault is detected. Certain faults can be prevented from activating the FAULT pin by setting the fault mask register in SPI message #1.

Once a fault is detected it is latched into the respective fault register. The microcontroller can access the fault registers by SPI messages #4, #5, and #19.

If the RESET_B line transitions high-to-low, a RB_L bit is latched into the Generic Flag Bits register. This register is cleared after it is read from the SPI, and the RB_L bit will not be set again until the next high-to-low transition occurs on the RESET_B pin.

If the ENABLE pin voltage is low, the EN_L bit is latched in the Generic Flag Bits register. The ENL bit is cleared when the ENABLE pin returns to a high state and the Generic Flag Bits register is accessed by SPI message #19.

The diagnostic delay timers for the on-state and off-state diagnostic functions are derived from the master clock signal applied to the pin CLK using a programmable predivider. This predivider is programmable by the DIAG_TMR bits in SPI message #1.

Table 2 Timebase for Diagnostics

DIAG_TMR1	DIAG_TMR0	Pre-divider	nfault min ... max	Tested Timer and Fault Detection Timer Period.	
				f_{CLK}=20 MHz	f_{CLK}=40 MHz
0	0	128	10 ... 11	64 µsec	32 µsec
0	1	192	10 ... 11	96 µsec	48 µsec
1	0	128	2 ... 3	12.8 µsec	6.4 µsec
1	1	256	10 ... 11	128 µsec	64 µsec

$$t_{DIAG\_PERIOD} = \frac{n_{fault} * predivider}{F_{CLK}}$$

Three unique fault types are detected using 4 different fault bits

The fault bit is set to a “1“ if the fault is detected.

Table 3 Diagnostic Flags / Bits

Fault Type	Abr.	Gate is ON	Gate is OFF
Short to Ground Fault	SG	OL-ON-F reported (=0 in ON/OFF mode)	Bit SG-F
Short to Battery Fault	SB	Bit SB-F	
Open Load Fault	OL	BIT OL-ON-F (=0 in ON/OFF mode)	Bit OL-OFF-F

Note: In order to differentiate between a Short to Ground Failure and an Open Load Failure, the channel must be turned off (setpoint = 0ma).

Tested Diagnostic Bits

The tested bits allow the distinction between a a case when a fault bit is not set because the fault is not detected, and the case when a fault bit is not set because the diagnostic test has not completed. For instance, the calculated duty cycle is too low to complete the short to battery test.

Two fault tested bits are defined:

The tested bit is set to 1 when the fault test has completed successfully.

Table 4 Diagnostics Tested Bits / Flags

Tested Type	OUTx High	OUTx Low
Short to Ground and Open load OFF tested		Bit OFF-T
Short to Battery tested	Bit SB-T	

Each fault type can be described by the two bits: FAULT and TESTED.

Table 5 FAULT vs. TESTED Bits Matrix and Interpretation

FAULT	TESTED	Interpretation by microcontroller
0	0	This fault type has not been tested
0	1	No Fault - The fault type has been tested and no fault is present
1	0	This combination cannot occur
1	1	Fault - This particular fault type has occurred

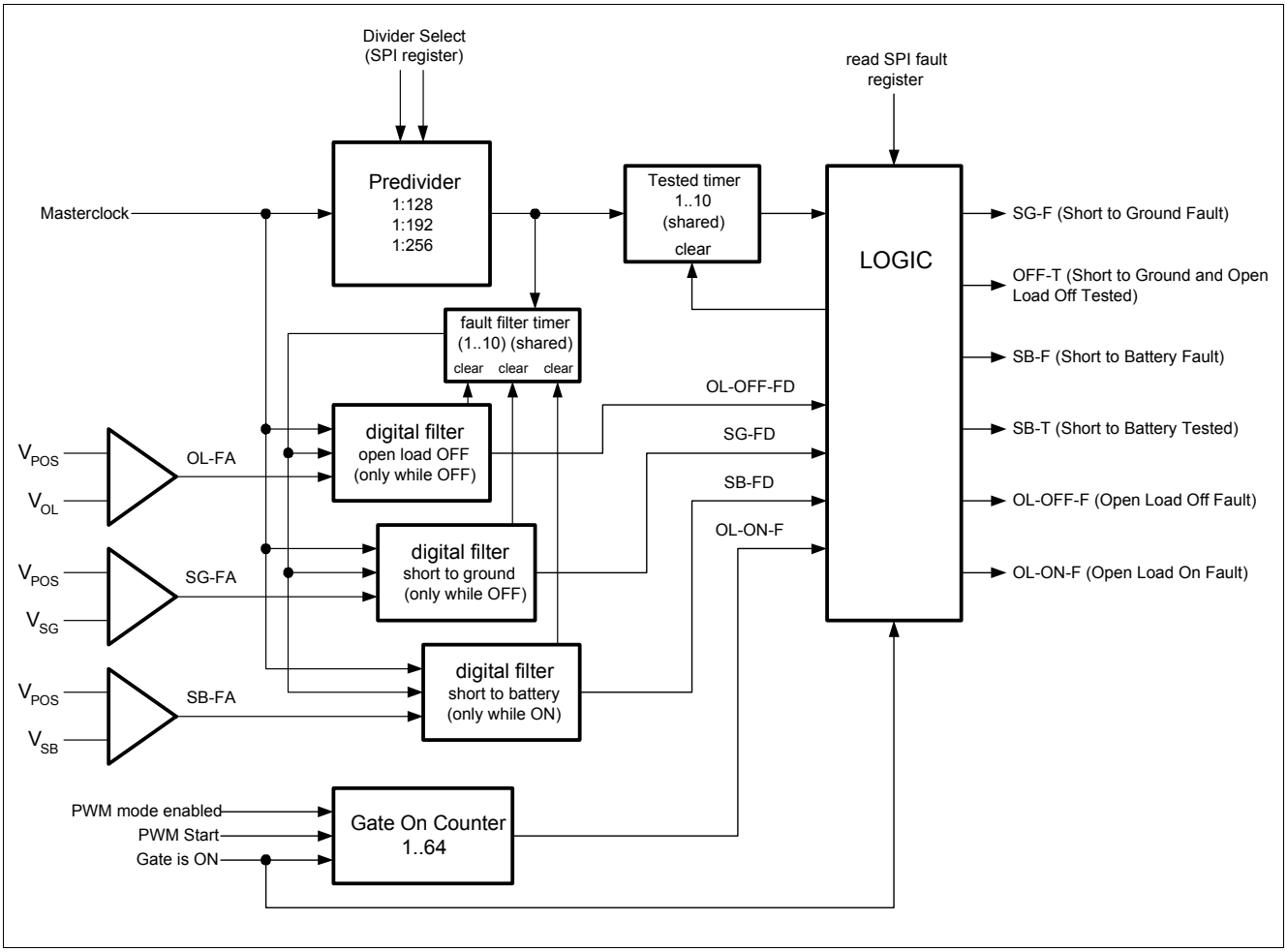


Figure 9 Diagnostic Block Diagram

5.3.1 On-State Diagnostics

When the OUTx pin transitions high, the fault timers are cleared to 0 and the tested timer starts. If the tested timer expires, the Bit SB-T (in the SPI registers #4 and #5) is set to 1. If the OUTx pin transitions low, the tested timer is cleared and then used for the off-state diagnostics.

If the analog SB fault signal (SB-FA) changes to 1, the fault filter timer starts. If the fault filter timer expires, the digitally filtered SB fault signal (SB-FD) is set to one. If SB-FA changes to 0, SB-FD changes immediately to 0 and the filter timer is cleared to 0.

A SB-FD=1 and SB-T=1 switches off the OUTx signal and the SB-F bit in the FAULT register will be set. The OUTx pin remains in the off state until the fault retry PWM period counter expires.

If the SPI message #3 or #4 is read, then the SB-F bit and the SB-FT bit in this register are cleared. Also, the tested timer is cleared to 0.

The Short to Battery (SB) detection functions in both direct PWM and constant current mode. The SG-FD and OL-OFF-FD signals are held to 0 while the OUTx pin is high.

If the TLE8242 IC is in direct PWM mode, Open Load ON detection is disabled (OL-ON-F = 0).

If the TLE8242 IC is not in direct PWM mode and the OUTx pin is high for 64 PWM periods, then the open load fault ON mode fault is detected, and the OL-ON-F bit in the diagnostic register is set. This bit will be cleared when SPI message #3 or #4 is read. If the OUTx pin remains in a high state, then the open load - on fault condition is detected again after another 64 PWM cycles.

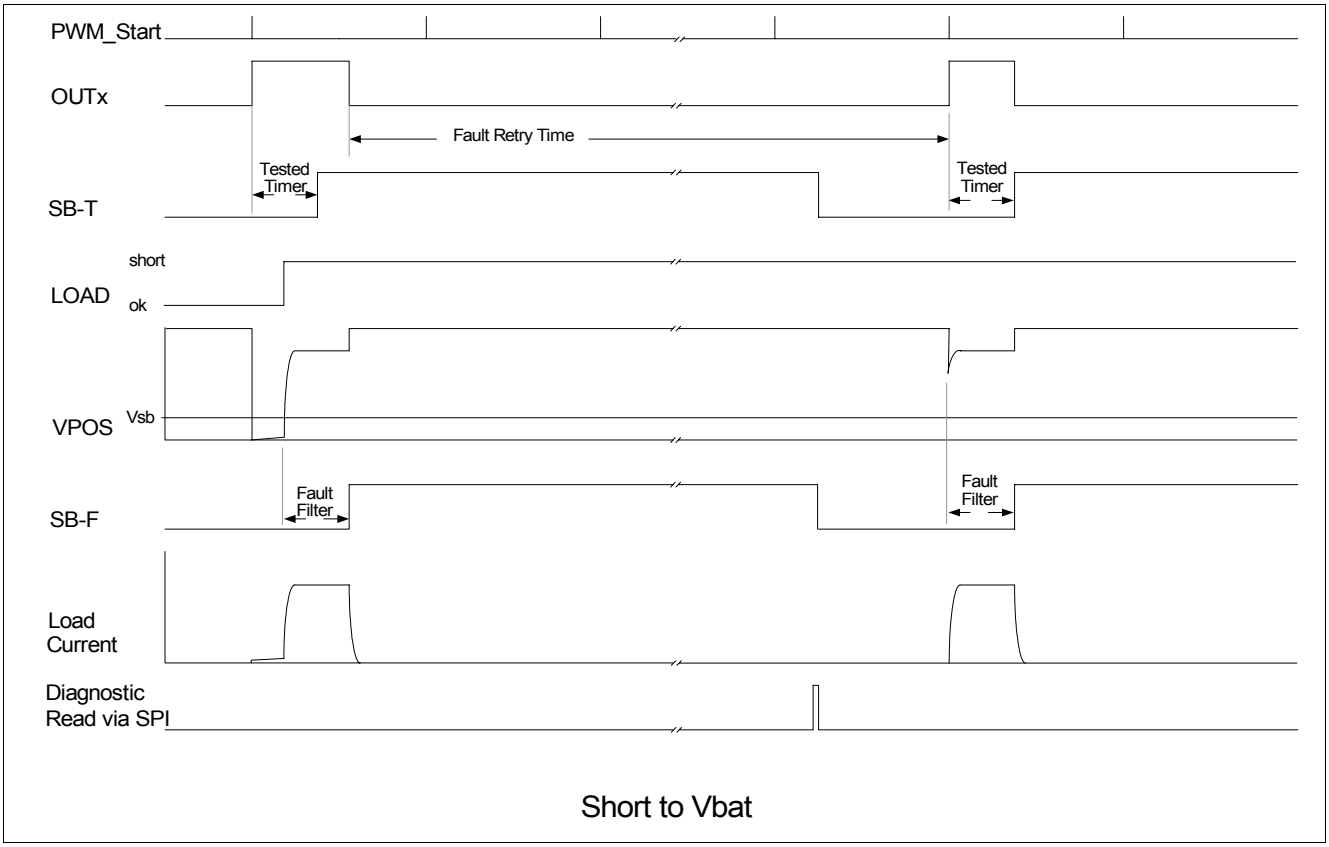


Figure 10 On-State Diagnostic Timing - Short to Vbat

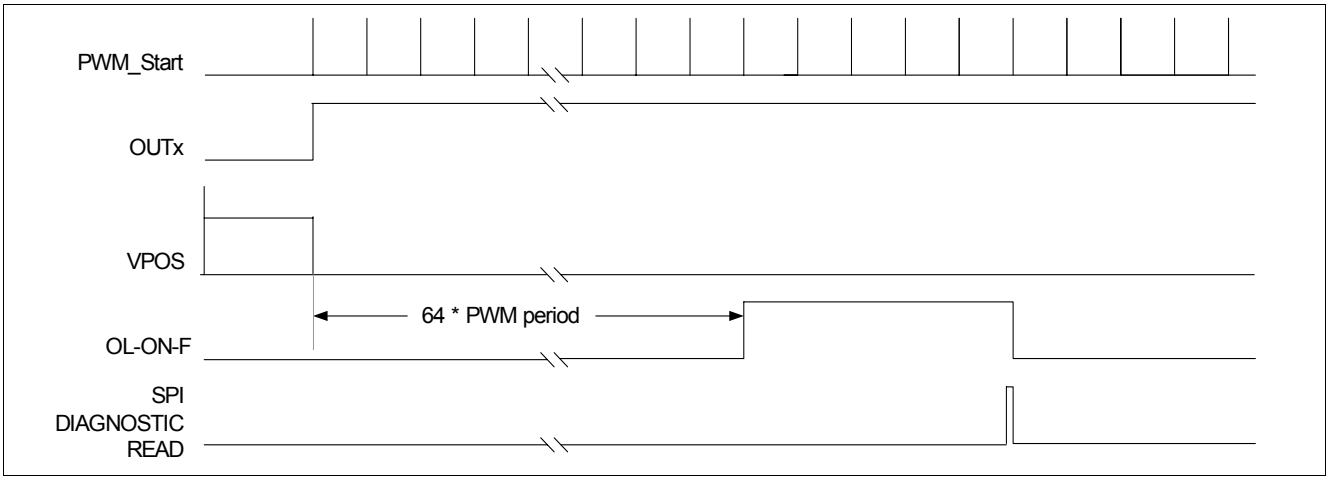


Figure 11 Open - On

5.3.2 Off-State Diagnostics

The off-state diagnostics function in both constant current mode and in direct PWM mode.

When the OUTx pin transitions low, the fault timers are cleared to 0 and the tested timer starts to count up. If the tested timer expires, the Bit OFF-T in the Diagnostic register is set. If a SPI diagnostic register read occurs, the tested timer is cleared to 0 and starts again to count up. If the OUTx pin transitions high, the tested-timer is cleared to zero and then used for on-state diagnostics.

If the analog OL fault signal (OL-FA) changes to 1, the fault filter timer starts to count up. If the fault filter timer expires, the digitally filtered OL fault signal (OL-ON-FD) is set to one.

If OL-FA changes to 0, OL-FD changes immediately to 0 and the fault filter timer is cleared to 0.

If the analog SG fault signal (SG-FA) changes to 1, the fault filter timer is cleared to 0 and starts to count up. If the fault filter timer expires, the digitally filtered SG fault signal (SG-FD) is set to one. If SG-FA changes to 0, SG-FD changes immediately to 0 and the fault filter timer is cleared to 0.

If SG-FD = 1 and the tested timer is expired then the SG-F bit in the FAULT register is set and the OL-OFF-F bit in the FAULT register remains unchanged (independently from OL-OFF-FD).

If SG-FD = 0 and OL-OFF-FD = 1 then the OL-F Bit in the FAULT register is set.

If a SPI fault read occurs, the OFF-T Bit, the SG-F Bit and the OL-F Bit in the SPI registers are cleared to zero (and the timers are cleared to 0).

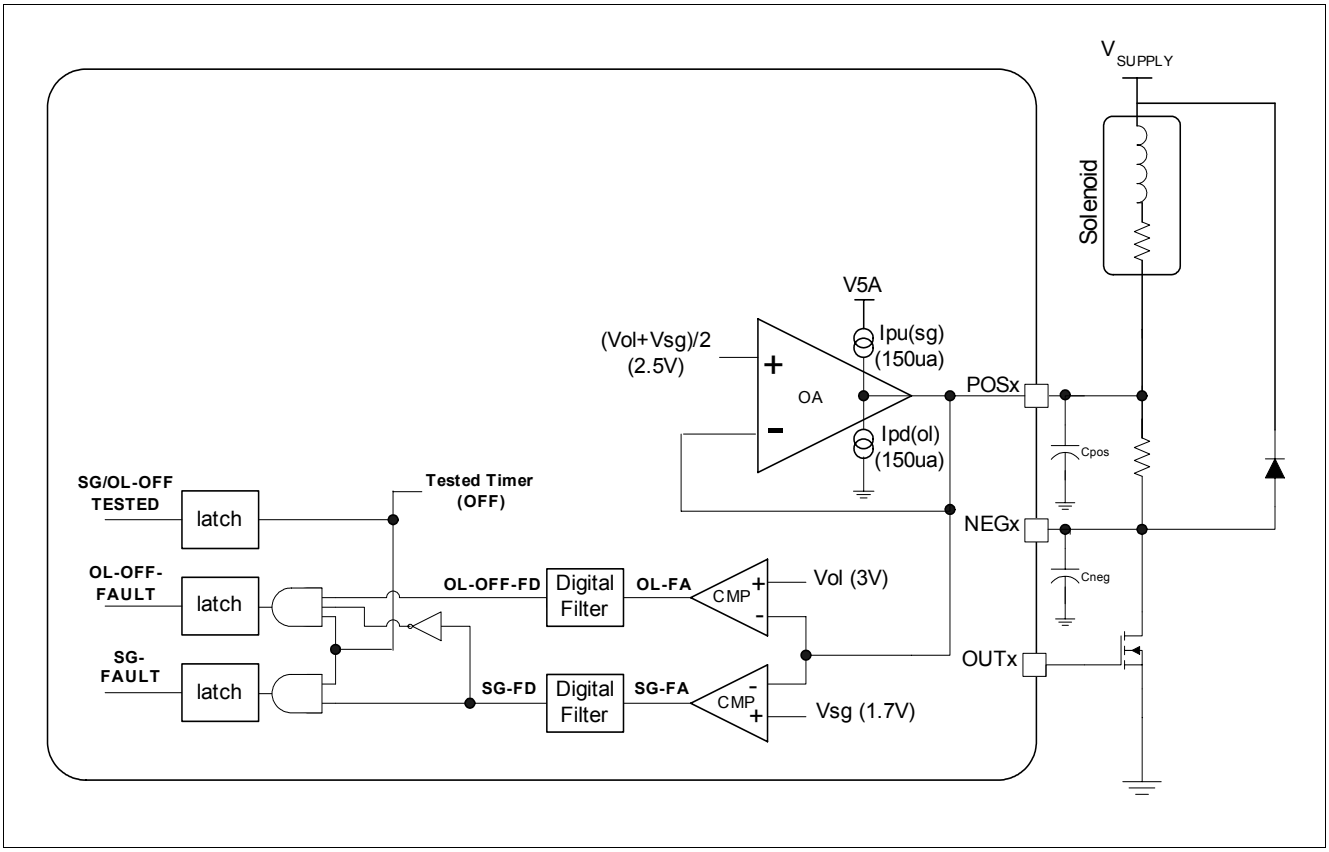


Figure 12 Off-State Diagnostics

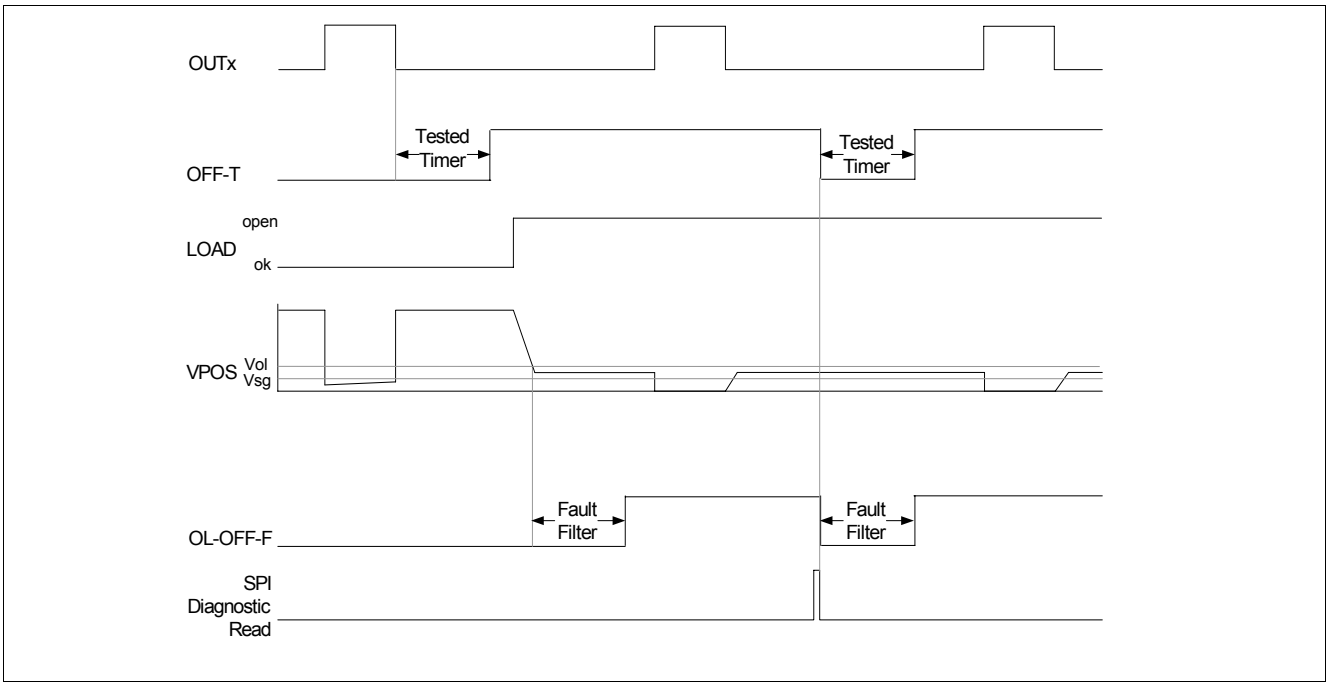


Figure 13 Off-State Diagnostics Timing Diagram - open

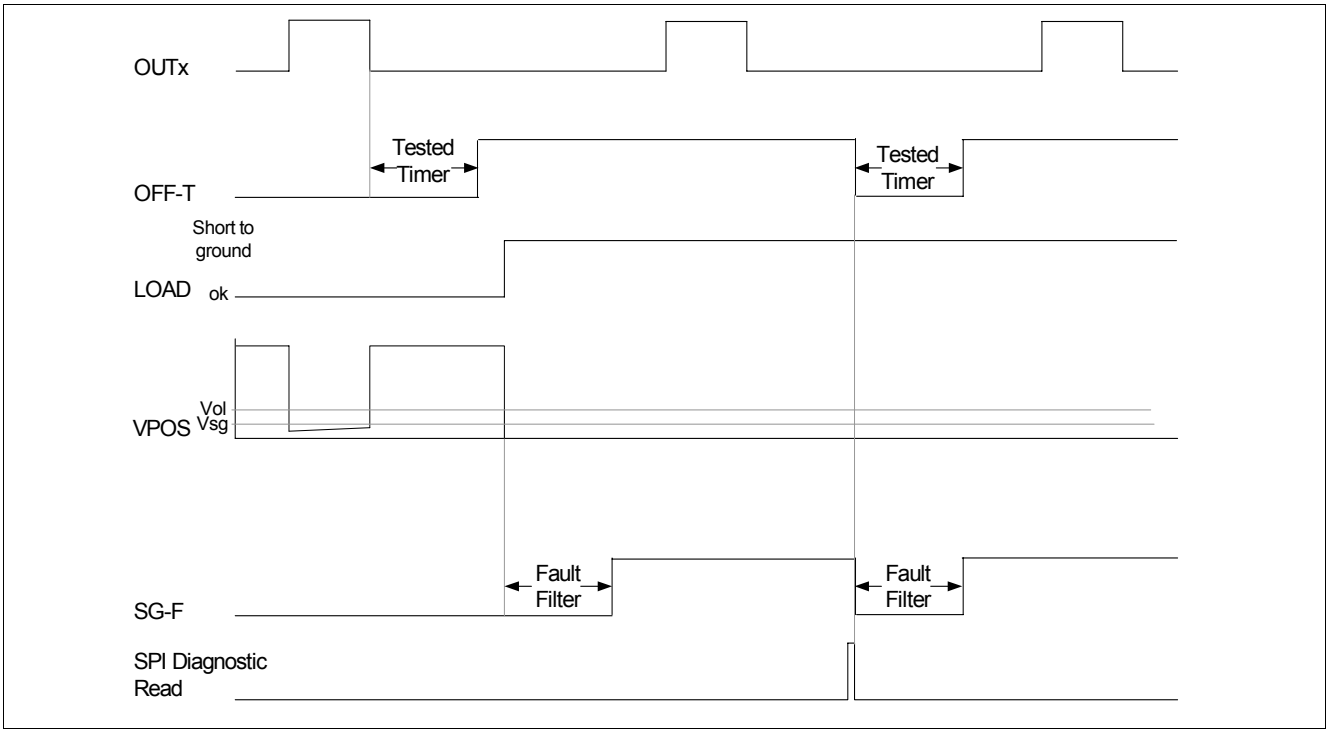


Figure 14 Off-State Diagnostics Timing Diagram - short to ground

Over Voltage Shutdown and Diagnostics

If the voltage at the BAT pin is above $VBAT_{OV}$, the output drivers set all OUTx pins to low, and a diagnostic bit is set (SPI Message #19 bit OV). During over voltage condition the integrator of the steady state current control is halted (actual value of the duty cycle is not changed during over voltage). All other functions operate normally (e.g. ADC, Dithering, Auto zero, Filters, …).

Electrical Characteristics:

V5D = 4.75V to 5.25V, Vbat = 5.5V to 42V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.1	Over voltage shutdown	V_{BATOV}	42	–	–	V	Rising voltage on BAT
5.3.2	Open load detection voltage	$V_{POS(OL)}$	V5A-2.5	–	V5A-1.5	V	
5.3.3	POS pin OL pull down current	$I_{PD(OL)}$	90	150	225	µA	V5A=5V, V_{POS}=V_{NEG}=V5A
5.3.4	Short to GND detection voltage	$V_{POS(SHG)}$	V5A-3.8	–	V5A-2.8	V	
5.3.5	POS pin SG pull-up current	$I_{PU(SHG)}$	-280	-150	-90	µA	V5A=5V, V_{POS}=V_{NEG}=0V
5.3.6	NEG bias current - Low common mode	$I_{NEG(L)}$	-40	–	10	µA	V5A=5V, V_{POS}=V_{NEG}=0V
5.3.7	NEG bias current - High common mode	$I_{NEG(H)}$	0	–	60	µA	V5A=5V, V_{POS}=V_{NEG}=V5A

Functional Description and Electrical Characteristics

V5D = 4.75V to 5.25V, Vbat = 5.5V to 42V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.8	POS Fault Threshold Voltage	V_{FLT}	0.6	0.7	0.8	V	POS voltage required to trigger a short to battery fault: config bits = 00
5.3.9	POS Fault Threshold Voltage	V_{FLT}	0.8	0.9	1.0	V	POS voltage required to trigger a short to battery fault: config bits = 01
5.3.10	POS Fault Threshold Voltage	V_{FLT}	1.0	1.1	1.2	V	POS voltage required to trigger a short to battery fault: config bits = 10
5.3.11	POS Fault Threshold Voltage	V_{FLT}	1.2	1.3	1.4	V	POS voltage required to trigger a short to battery fault: config bits = 11
5.3.12	Fault Filter Timer	n_{fault}	10		11	clock cycles	DIAG_TMR = 00, 01 and 11
5.3.13	Fault Filter Timer	n_{fault}	2		3	clock cycles	DIAG_TMR = 10
5.3.14	Fault Filter Time	T_{ff}	$\frac{n_{fault} \cdot predivider}{f_{CLK}}$				Clock Divider (SPI Message 7) 00, 10- Predivider 128 01 - Predivider 192 11 - Predivider 256
5.3.15	Tested Timer Time	T_{tt}	$\frac{n_{fault} \cdot predivider}{f_{CLK}}$				Clock Divider (SPI Message 7) 00, 10 - Predivider 128 01 - Predivider 192 11 - Predivider 256

5.4 Output Driver

The OUTx pins of the device are connected to the gates of the external MOSFET transistors. The OUTx pin driver circuits charge and discharge the MOSFET gate capacitance with a constant current source and sink. The supply for the current source is the V5D pin. Internal resistors to ground are included on the OUTx pins so that the external MOSFET is held in the off state when power is not applied to the device.

An external resistor is typically placed between the OUTx pin and the gate of the external MOSFET in order to set the MOSFET turn-on and turn-off times. The value of the resistor must be chosen such that the turn-on and turn-off times of the MOSFET are no longer than 1/(Fpwm*32).

Electrical Characteristics:

V5D = 4.75V to 5.25V, Vbat = 5.5V to 42V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.4.1	Passive Gate Pull Down Resistance	R_{PD}	50	–	200	kΩ	Internal pull down resistor present at each OUTx pin
5.4.2	OUTx source current	I_{O_SRC}	-30	–	-15	mA	V_{OUT} = V5D-2V
5.4.3	OUTx sink current	I_{O_SNK}	15	–	30	mA	V_{OUT} = 2V

5.5 Current Control

Electrical Characteristics:

V5D = 4.75V to 5.25V, Vbat = 5.5V to 42V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.5.1	Offset Error Output from Average block in **Figure 3**. 1 count = 320/Rsense * 2^{-13} mA		0	–	120	counts	Autozero disabled.Vpos-Vneg=0mV Vpos, Vneg ≤ 30V Dither disabled
5.5.2	Gain Error		-2	–	2	%	Autozero Enabled.Vpos-Vneg=300mV Vpos, Vneg ≤ 30V

5.6 Current Feedback Registers

The average current over each PWM cycle is measured resulting in a 13 bit value. The summation of the 13 bit values for all PWM periods in a dither period can be read by accessing SPI message #13. Also, the 11 MSb's of the minimum and maximum 13 bit values within a dither period can be read by accessing SPI message #12.

Average Current Over Dither Period

When the SPI message #13 is read or written, the 13 bit average current value for each PWM cycle within the dither period is summed beginning with the positive going zero crossing of the dither waveform. The resulting 20 bit value represents the average current over the dither cycle as shown in equation:

$$\text{Dither Current Feedback}\,[\text{mA}] = \frac{\text{Avg Dither Current}}{2^{15} * \text{Dither Steps}} * \frac{320\,[\text{mV}]}{\text{Rsense}\,[\text{Ohm}]}$$

If dither is disabled (Dither Steps = 0 or Dither Amplitude = 0), then the Average Current Feedback value will be updated every PWM period and will be the same as the 13 bit current feedback value used in the PI controller.

The SPI message #13 includes a VALID bit that indicates whether the average current measurement has completed since the last register access. When the register is accessed, the VALID bit is cleared. The VALID bit is set again when the summation is completed and new data has been stored in the register.

The summation process runs continuously on the last selected channel. So if the same channel is repeatedly selected, new data is always available within one dither period after the SPI register is accessed.

If the selected channel is different than the previously selected channel, the summation process does not begin until the beginning of the next dither period. So, new data may not be available until two dither cycles have completed.

The channel selection for the Average Dither Current Feedback Message message will also select the channel for the Minimum and Maximum Current Over Dither Period function.

Minimum and Maximum Current Over Dither Period

When the SPI message #12 is read or written, the 13 bit average current value for each PWM cycle within the dither period is monitored beginning with the positive going zero crossing of the dither waveform. The most significant 11 bits of the minimum and the maximum average current values are stored.

If dither is disabled (Dither Steps = 0 or Dither Amplitude = 0), then the Minimum and Maximum values will be updated every PWM period and will be the 11 Msb's of the 13 bit current feedback value used in the PI controller.

The SPI message #12 includes a VALID bit that indicates whether a dither period has completed since the last register access. When the register is accessed, the VALID bit is cleared. The VALID bit is set again when the dither period is completed and new data has been stored in the minimum and maximum registers.

The minimum and maximum detection process runs continuously on the last selected channel. So, if the same channel is repeatedly selected, new data is always available within one dither period after the SPI register is accessed.

If the selected channel is different than the previously selected channel, the detection process does not begin until the beginning of the next dither period. So, new data may not be available until two dither cycles have completed.

The channel selection for the Minimum and Maximum Current Over Dither Period message will also select the channel for the Average Dither Current Feedback function.

5.7 Direct PWM control

In Direct PWM control mode, the PI control loop is disabled. The integrator in the constant current control logic is cleared and held at 0 while direct PWM mode is active. The frequency and duty cycle of the OUTx pin signal is directly controlled via SPI messages.

5.7.1 Selecting the Frequency of Operation

The period of the PWM is programmed in whole numbers of clocks from the CLK input (as in constant current mode). The following formula is applied:

$$T_{PWM} = T_{CLK} * M * N$$

or

$$f_{PWM} = \frac{f_{CLK}}{M * N}$$

The value N is the divider programmed via the SPI interface. The IC will automatically limit the lower value of N to 79. If a value lower than 79 is programmed, the IC shall default N for that channel to 79 and return a value of 79 in the SPI response. The maximum value of N is 2^{14}-1 as it is programmed as a 14-bit number via SPI.

If a new value of N is programmed during operation, the new value of N will be returned on the next SPI message, and the new value of N will be used at the beginning of the next PWM cycle. The default value for N is 625.

The value of M is the number of A/D samples in one PWM period. M is programmed with the value 32, 64, 128, or 512 via an SPI message. The default value for M is 32. The PWM frequency multiplied by the value M is the analog to digital converter sample rate. This sample rate must be no greater than 128 KHz.

5.7.2 Selecting the Duty Cycle

The duty cycle of the PWM is also programmed in whole numbers of clocks from the CLK input. The following formula is applied:

$$T_{ON} = T_{CLK} * \text{PWM duty cycle} * \frac{M}{32}$$

PWM duty cycle is a 19 bit value programmed in SPI message # 15 “PWM duty cycle”.

or

$$\text{Duty Cycle}[\%] = \frac{\text{PWM duty cycle}}{32 * N} * 100\%$$

The maximum duty cycle is clipped to 100%

5.8 Current Profile Detection

The TLE8242 will detect current profiles due to the change in inductance caused by the opening/closing of solenoid valves. Examples of the types of waveforms seen in this instance are shown in **Figure 15** and **Figure 16**. Examples of waveforms that fail the Current Profile Detection test are shown in **Figure 17** and **Figure 18**.

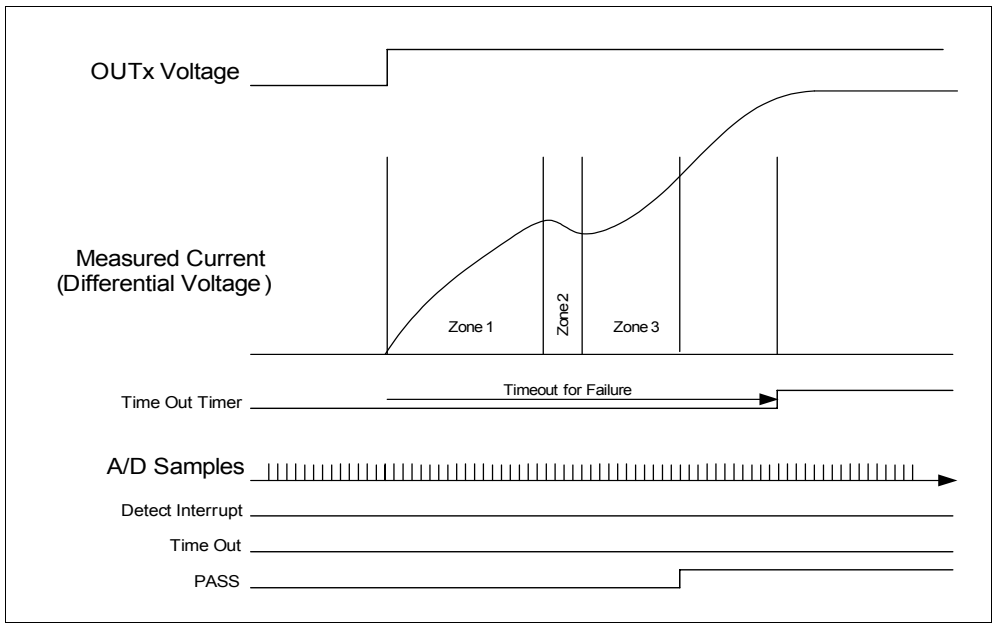


Figure 15 Current Profile Diagram - Waveform Showing Valve Movement

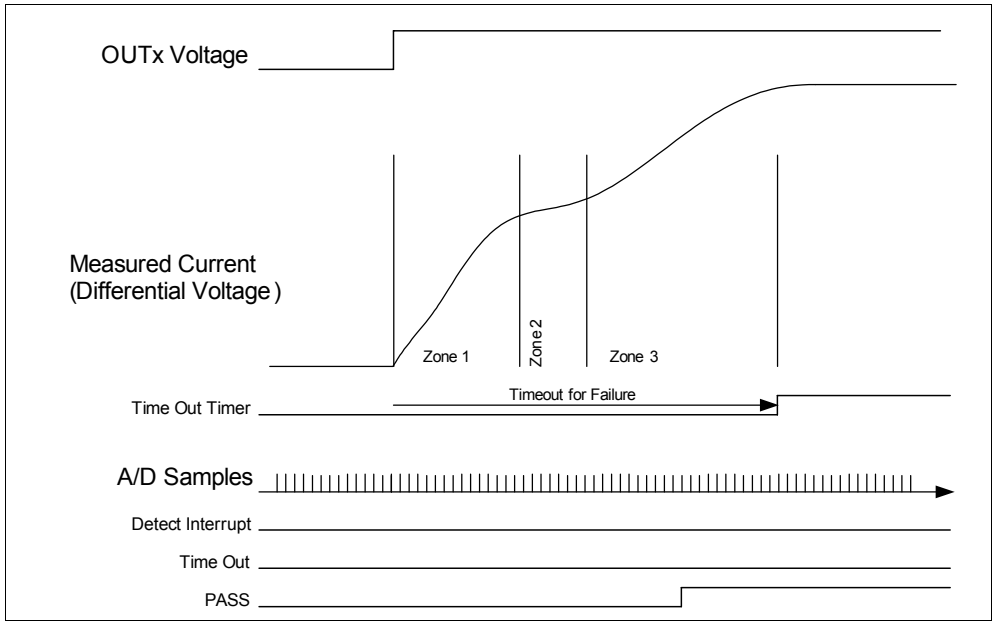


Figure 16 Current Profile Diagram - Waveform Showing Valve Movement with Non-Zero Threshold in Zone 2

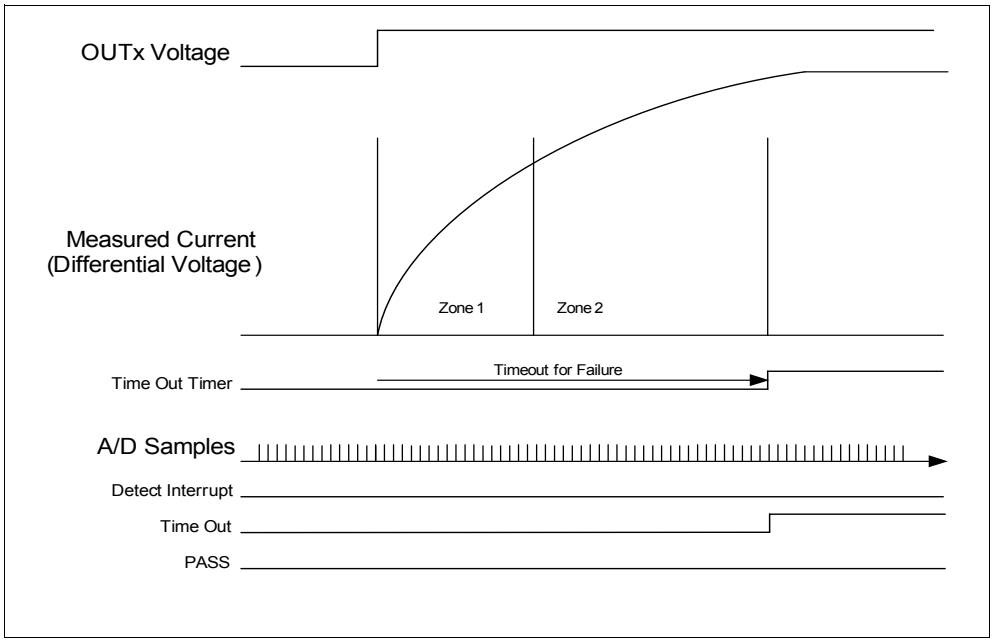


Figure 17 Current Profile Diagram - Time Out Failure

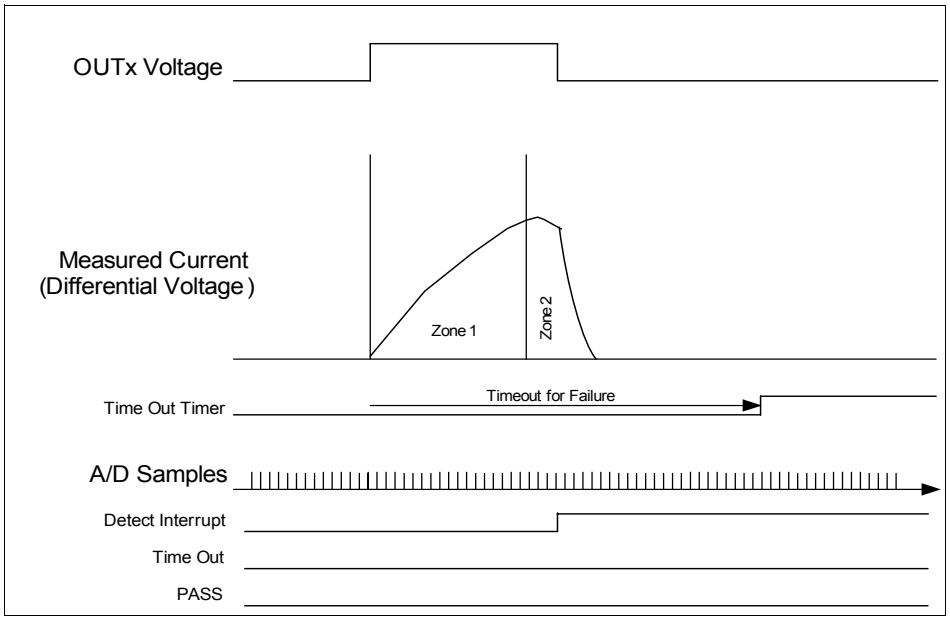


Figure 18 Current Profile Diagram - Detection Interrupted Failure

The Current Profile Detection feature is active only in Direct PWM mode. The method employed is to look for three specific "patterns" of the current in 3 zones. This detection method is generally used for on/off valves. The on/off control of the valve is achieved by selecting the PWM period desired and setting to a 0% or 100% duty cycle via SPI, however the detection may work within a single PWM on-time with a duty cycle less than 100% if the profile completes before the gate turns off.

The PWM period (N and M values) are critical as these values set the A/D sample rate used in the current profile detection. The full 10-bit result of the A/D converter is used for the CPD function. Using a 200 mOhm sense resistor, this translates into a resolution of 1.56 mA.

5.8.1 Zone 1

When the OUTx pin transitions from low-to-high, zone 1 of the logic is entered. The TLE8242 compares the difference between successive A/D samples and calculates the ADDIFF value. This value is compared with Threshold1 as follows:

- ADDIFF = A/D_{m+1} - A/D_m
- IF (ADDIFF > Threshold1) THEN count = count +1

When ADDIFF is greater than Threshold 1 for Count1 out of Count1 + 1 successive comparisons, zone 1 is passed and zone 2 is entered. Note that if one of the tests fails, the actual test performed on the next sample after the single failure is

- ADDIFF = A/D_{m+1} - A/D_{m-1}
- IF (ADDIFF > 2 * Threshold1) THEN count = count +1

This has the effect of filtering out a single noise spike in the A/D measurement.

5.8.2 Zone 2

In zone 2, the TLE8242 compares the difference between successive A/D samples and calculates the ADDIFF value. This value is compared with Threshold2 as follows:

- ADDIFF = A/D_{m+1} - A/D_m
- IF (ADDIFF <Threshold2) THEN count = count +1

When ADDIFF is less than Threshold2 for Count2 out of Count2 + 1 successive comparisons, zone 2 is passed and zone 3 is entered. When the thresold2 is set to 0, a negative difference in the A/D samples (negative slope) must be detected. Note that if one of the tests fails, the actual test performed on the next sample after the single failure is

- ADDIFF = A/D_{m+1} - A/D_{m-1}
- IF (ADDIFF <2 * Threshold2) THEN count = count +1

This has the effect of filtering out a single noise spike in the A/D measurement.

5.8.3 Zone 3

In zone 3, the TLE8242 sample rate for the CPD function can be altered from the sample rate used for zone 1 and zone 2. As in zone 1 and zone 2, the TLE8242 compares the difference between two A/D samples and calculates ADDIFF. The sample rate can be altered in zone 3 such that ADDIFF is calculated as shown in Table 5.This allows for more noise immunity and also allows the programming of a lower effective slope to be detected. When ADDIFF is greater than Threshold3 for Count3 output of Count3 + 1 successive comparisons, the test passes and zone 3 is completed. When zone 3 passes, the current profile is passed.

Table 6 Zone 3 Sample Rate Selection

SPI Bit Values	Samples Used	ADDIFF
00	successive A/D samples	A/D_m - A/D_{m-1}
01	every 2nd A/D sample	A/D_m - A/D_{m-2}
10	every 3rd A/D sample	A/D_m - A/D_{m-3}
11	every 4th A/D sample	A/D_m - A/D_{m-4}

Note that if one of the tests fails, the actual test performed on the next sample after the single failure is

- ADDIFF = A/D_m - A/D_{m-2*a} (a=1, 2, 3, 4 depending on the settings in Table 6)
- IF (ADDIFF > 2 * Threshold3) THEN count = count +1

This has the effect of filtering out a single noise spike in the A/D measurement.

5.8.4 Current Profile Time out & Detection Interrupted

If the Current Profile Time out value is achieved before the completion of the test, the current profile test has failed. If this failure occurred, the Current Profile Time out bit in the SPI message is set.

The Current Profile Time out value is programmable and should be set to a value less than the PWM period.

If the OUTx pin is turned off before the completion of the test as in **Figure 18**, the Detection Interrupted SPI Bit is set. Note that the OUTx pin must transition from high to low to set the Detection Interrupted fault bit. The Detection Interrupted fault bit is not set by the expiration of the PWM period if the duty cycle is set to >= 100%.

If the entire CPD test passes (all three zones are passed before the time out), the "Passed Since Last Read" SPI bit is set SPI message # 18.

Each channel of the Adler 2 is individually configurable for the current profile detection patterns.

The thresholds and counts for each zone must not be changed via SPI while a current profile detection sequence is active, otherwise an incorrect detection may occur.

5.9 Serial Peripheral Interface (SPI)

SPI messages for the TLE8242 IC are 32-bit values broken down into the following fields.

Bit 31: Read/Write Bit - 0 = Read 1 = Write

Bits 30-24: Message Identifier

Bits 23-0: Message Data

In cases where multiple channels require the same message structure, bits 24-25 of the Message Identifier represent the channel numbers. The structure follows the following pattern

Bit 31: Read/Write Bit - 0 = Read / 1 = Write

Bits 30-27: Message Identifier

Bits 26-24: Channel Number

Bits 23-0: Message Data

The message from the microcontroller must be sent MSB first. The data from the SO pin is sent MSB first. The TLE8242 will sample data from the SI pin on the rising edge of SCK and will shift data out of the SO pin on the rising edge of SCK.

All SPI messages must be exactly 32-bits long, otherwise the SPI message is discarded. The response to an invalid message (returned in the next SPI message) is the message with identifier 00000 (Manufacturer ID).

When the ENABLE pin is low, all SPI writes commands are executed as read commands.

When RESET_B pin is low, the SPI port is disabled. No SPI messages are received and no responses are sent. The SO pin remains in a high impedance state.

There is a one message delay in the response to each message (i.e. the response for message N will be returned during message N+1).

Read/Write operation is referenced from the SPI master. The TLE8242 IC is the slave device.

When bit 31 is = 0 to denote a read operation to the IC, the message data in bits 23-0 of the sent message are ignored, but will contain valid data in the response message.

All response data (either from a read or write operation) is the direct contents of the addressed internal register, and is not an echo of the data sent in the previous SPI message.

The response to the first SPI message after a reset is message #0 (IC Version / Manufacturer).

5.9.1 SPI Signal Description

Electrical Characteristics:

V5D = 4.75V to 5.25V, Vbat = 5.5V to 42V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified). Maximum capacitive load on the SO pin = 200 pF.

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.9.1	Lead Time	t_1	140	–	–	ns	CS_B falling (0.8V) to SCK rising (0.8V)
5.9.2	Lag Time	t_2	50	–	–	ns	SCK falling (0.8V) to CS_B rising (0.8V)
5.9.3	Dead time	t_3	450	–	–	ns	CS_B rise (2.0V) to CS_B fall (2.0V)
5.9.4	$1/F_{SCK}$ Period of SCK	t_4	100	–	–	ns	SCK rise to rise
5.9.5	SCK to CSB set up time	t_5	10	–	–	ns	SCK falling (0.8V) to CS_B fall (2.0V)
5.9.6	SCK high time	t_6	40	–	–	ns	SCK high time (rise 2.0V to fall 2.0V)
5.9.7	SCK low time	t_7	40	–	–	ns	SCK low time (fall 0.8V to rise 0.8V)
5.9.8	CSB to SCK hold time	t_8	10	–	–	ns	CS_B rise (2.0V) to SCK rise (0.8V)
5.9.9	SI setup time	t_9	20	–	–	ns	SI setup time to SCK rise (0.8V)
5.9.10	SI hold time	t_{10}	20	–	–	ns	SI hold time after SCK rise (2.0V)
5.9.11	SO enable	t_{11}	–	–	110	ns	CS_B fall (2.0V) to SO Bit0 valid
5.9.12	SO valid time	t_{12}	–	–	80	ns	SO data valid after SCK rise (2.0V)
5.9.13	SO disable time	t_{13}	–	–	110	ns	SO tristate after CS_B rise (2.0V)
5.9.14	Number of clock pulses while CS_B low		32	–	32	cycles	
5.9.15	SO rise time	T_{SO_RISE}	–	–	50	ns	(20% to 80%)
5.9.16	SO fall time	T_{SO_FALL}	–	–	50	ns	(80% to 20%)
5.9.17	Input pin capacitance. CS_B, SI, and SCK	C_{in}	–	–	20	pF	
5.9.18	SO pin capacitance	C_{so}	–	–	25	pF	Tristate

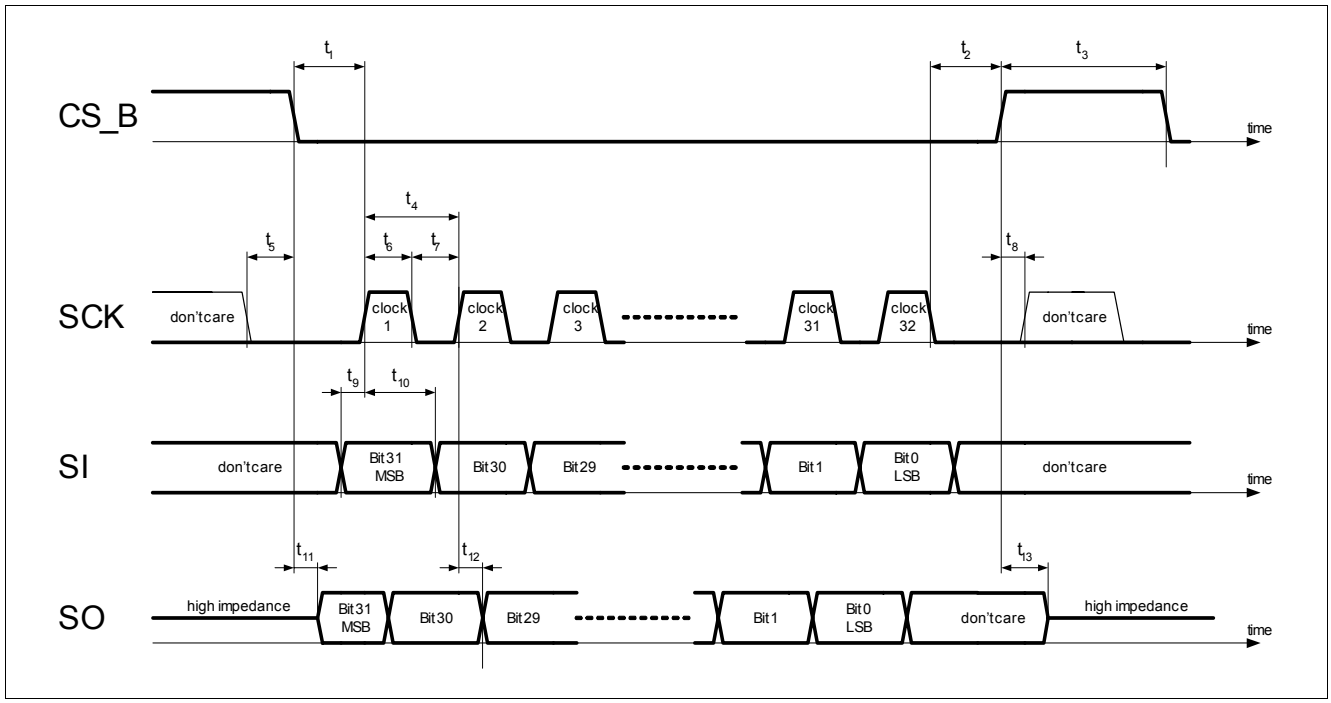


Figure 19 SPI Timing Diagram

5.9.2 SPI Message Structure

5.9.2.1 SPI Message #0 - IC Version / Manufacturer

Sent Values:
IC Version / Manufacturer

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	**MSG_ID**							**not used**							
	0	0	0	0	0	0	0								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
not used															

Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:24	ADDR	**Message Identifier** 000 0000 = IC Version / Manufacturer

Response:
IC Version / Manufacturer

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**MSG_ID**							**IC Manuf ID**							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Version Number								**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:24	ADDR	**Message Identifier** 000 0000 = IC Version / Manufacturer
IC Manuf ID	23:16	DATA	**IC Manufacturer ID Number** 1100 0001= Infineon Technologies
Version Number	15:8	DATA	**Version Number** 0000 0010 = B21

5.9.2.2 SPI Message #1 - Control Method and Fault Mask Configuration

Sent Values:
Control Method and Fault Mask Configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	**MSG_ID**							**CM0**	**CM1**	**CM2**	**CM3**	**CM4**	**CM5**	**CM6**	**CM7**
	0	0	0	0	0	0	1								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FM0	**FM1**	**FM2**	**FM3**	**FM4**	**FM5**	**FM6**	**FM7**	**FMR**	**FME**	**DIAG_TMR**		**unused**			
										msb	lsb				

Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:24	ADDR	**Message Identifier** 000 0001 = Control Method and Fault Mask Configuration

CMx	23:16	DATA	**Control Mode for Channel #x**
			0 = Current Control (RESET value)
			1 = Direct PWM

FMx	15:8	DATA	**Fault Mask for Channel #x**
			0 = faults don't trigger FAULT pin (RESET value)
			1 = fault triggers FAULT pin

FMR	7	DATA	**Fault Mask for RESET_B pin** 0 = RESET_B=Low doesn't trigger FAULT pin (RESET value) 1= RESET_B=Low does trigger FAULT pin
FME	6	DATA	**Fault Mast for ENABLE pin** 0 = ENABLE=Low doesn't trigger FAULT pin (RESET value) 1 = ENABLE=Low does trigger FAULT pin
DIAG_TMR	5:4	DATA	**Diagnostic Timer** 00 = divide by 128, nfault = 10 ... 11 (RESET value) 01 = divide by 192, nfault = 10 ... 11 10 = divide by 128, nfault = 2... 3 11 = divide by 256, nfault = 10 ... 11

Response:

Control Method and Fault Mask Configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**MSG_ID**							**CM0**	**CM1**	**CM2**	**CM3**	**CM4**	**CM5**	**CM6**	**CM7**
	0	0	0	0	0	0	1								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FM0	**FM1**	**FM2**	**FM3**	**FM4**	**FM5**	**FM6**	**FM7**	**FMR**	**FME**	**DIAG_TMR**		**0**	**0**	**0**	**0**
										msb	lsb				

Field	Bits	Type	Description
MSG_ID	30:24	ADDR	**Message Identifier** 000 0001 = Control Method and Fault Mask Configuration

CMx	23:16	DATA	**Control Mode of Channel #x**
			0 = Current Control (RESET value)
			1 = direct PWM

FMx	15:8	DATA	**Fault Mask of Channel #x**
			0 = faults don’t trigger FAULT pin (RESET value)
			1 = fault triggers FAULT pin

FMR	7	DATA	**Fault Mask for RESET_B pin** 0 = RESET_B=Low doesn’t trigger FAULT pin (RESET value) 1 = RESET_B=Low does trigger FAULT pin
FME	6	DATA	**Fault Mast for ENABLE pin** 0 = ENABLE=Low doesn’t trigger FAULT pin (RESET value) 1 = ENABLE=Low does trigger FAULT pin
DIAG_TMR	5:4	DATA	**Diagnostic Timer** 00 = divide by 128, nfault = 10 ... 11 (RESET value) 01 = divide by 192, nfault = 10 ... 11 10 = divide by 128, nfault = 2... 3 11 = divide by 256, nfault = 10 ... 11

5.9.2.3 SPI Message #2 - Diagnostic Configuration (channel 0-3)

Sent Values:
Diagnostic Configuration (channels 0-3)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	**MSG_ID**							**SB0**		**SB_RETRY0**				**SB1**	
	0	0	0	0	0	1	0	msb	lsb	msb			lsb	msb	lsb

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SB_RETRY1				**SB2**		**SB_RETRY2**				**SB3**		**SB_RETRY3**			
msb			lsb	msb	lsb	msb			lsb	msb	lsb	msb			lsb

Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:24	ADDR	**Message Identifier** 000 0010 = Diagnostic Configuration (channel 0-3)
SBx	23:22, 17:16, 11:10, 5:4	DATA	**Short To Battery Threshold** 00 = 0.7V 01 = 0.9V 10 = 1.1V 11 = 1.3V (RESET value)
SB_RETRYx	21:18, 15:12, 9:6, 3:0	DATA	**Short to Battery Retry Time** Retry after 16* xxxx periods (RESET Value = 1111b or 240 PWM periods)

Response Values:
Diagnostic Configuration (channels 0-3)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**MSG_ID**							**SB0**		**SB_RETRY0**				**SB1**	
	0	0	0	0	0	1	0	msb	lsb	msb			lsb	msb	lsb

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SB_RETRY1				**SB2**		**SB_RETRY2**				**SB3**		**SB_RETRY3**			
msb			lsb	msb	lsb	msb			lsb	msb	lsb	msb			lsb

Field	Bits	Type	Description
MSG_ID	30:24	ADDR	**Message Identifier** 000 0010 = Diagnostic Configuration (channel 0-3)

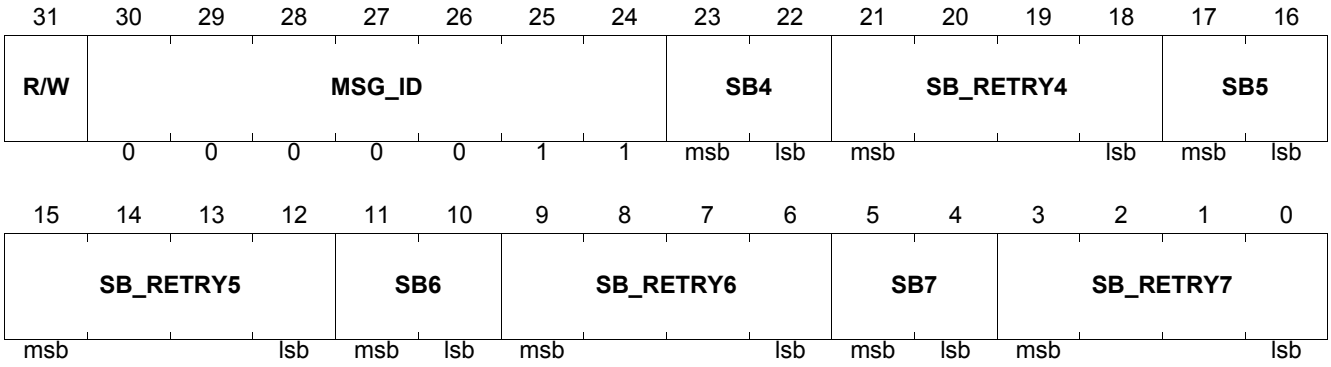
Field	Bits	Type	Description
SBx	23:22, 17:16, 11:10, 5:4	DATA	**Short To Battery Threshold** 00 = 0.7V 01 = 0.9V 10 = 1.1V 11 = 1.3V (RESET value)
SB_RETRYx	21:18, 15:12, 9:6, 3:0	DATA	**Short to Battery Retry Time** Retry after 16* xxxx periods (RESET Value = 1111b or 240 PWM periods)

$$\text{Retry Period} = \frac{16 * \text{SB\_Retry}_x}{f_{PWM}}$$

Equation: Short to Battery Retry Period (1)

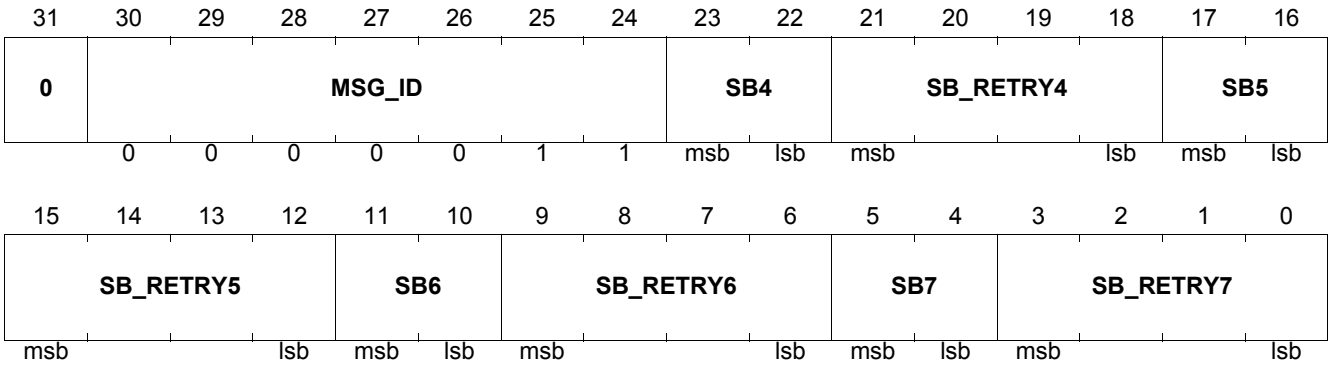
5.9.2.4 SPI Message #3 - Diagnostic Configuration (channel 4-7)

Sent Values:
Diagnostic Configuration (channels 4-7)



Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:24	ADDR	**Message Identifier** 000 0011 = Diagnostic Configuration (channel 4-7)
SBx	23:22, 17:16, 11:10, 5:4	DATA	**Short To Battery Threshold** 00 = 0.7V 01 = 0.9V 10 = 1.1V 11 = 1.3V (RESET value)
SB_RETRYx	21:18, 15:12, 9:6, 3:0	DATA	**Short to Battery Retry Time** Retry after 16 * xxxx periods (RESET Value = 1111b or 240 PWM periods)

Response Values:
Diagnostic Configuration (channels 4-7)



Field	Bits	Type	Description
MSG_ID	30:24	ADDR	**Message Identifier** 000 0011 = Diagnostic Configuration (channel 4-7)

Field	Bits	Type	Description
SBx	23:22, 17:16, 11:10, 5:4	DATA	**Short To Battery Threshold** 00 = 0.7V 01 = 0.9V 10 = 1.1V 11 = 1.3V (RESET value)
SB_RETRYx	21:18, 15:12, 9:6, 3:0	DATA	**Short to Battery Retry Time** Retry after 16* xxxx periods (RESET Value = 1111b or 240 PWM periods)

$$\text{Retry Period} = \frac{16 * \text{SB\_Retry}_x}{f_{PWM}}$$

Equation: Short to Battery Retry Period (2)

5.9.2.5 SPI Message #4 - Diagnostic Read (channel 0-3)

Sent Values:
Diagnostic Read (channels 0-3)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	MSG_ID							unused							
	0	0	0	0	1	0	0								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused															

Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write (interpreted as a read)
MSG_ID	30:24	ADDR	**Message Identifier** 000 0100 = Diagnostic Read (channel 0-3)

Response Values:
Diagnostic Read (channels 0-3)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	MSG_ID							SG0	OFF-TST0	SB0	SB-TST0	OL-OFF0	OL-ON0	SG1	OFF-TST1
	0	0	0	0	1	0	0								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SB1	SB-TST1	OL-OFF1	OL-ON1	SG2	OFF-TST2	SB2	SB-TST2	OL-OFF2	OL-ON2	SG3	OFF-TST3	SB3	SB-TST3	OL-OFF3	OL-ON3

Field	Bits	Type	Description
MSG_ID	30:24	ADDR	**Message Identifier** 000 0100 = Diagnostic Read (channel 0-3)
SGx	23, 17, 11, 5	DATA	**Short to Ground - Fault** (RESET value = 0)
OFF-TSTx	22, 16, 10, 4	DATA	**Short to Ground & Open Ld (Gate Off) - Tested** (RESET value = 0)
SBx	21, 15, 9, 3	DATA	**Short to Battery - Fault** (RESET value = 0)
SB-TSTx	20, 14, 8, 2	DATA	**Short to Battery - Tested** (RESET value = 0)
OL-OFFx	19, 13, 7, 1	DATA	**Open Load (Gate Off) - Fault** (RESET value = 0)
OL-ONx	18, 12, 6, 0	DATA	**Open Load (Gate On) - Fault** (RESET value = 0)

5.9.2.6 SPI Message #5 - Diagnostic Read (channel 4-7)

Sent Values:
Diagnostic Read (channels 4-7)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	**MSG_ID**							**unused**							
	0	0	0	0	1	0	1								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused															

Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write (interpreted as a read)
MSG_ID	30:24	ADDR	**Message Identifier** 000 0101 = Diagnostic Read (channel 4-7)

Response Values:
Diagnostic Read (channels 4-7)

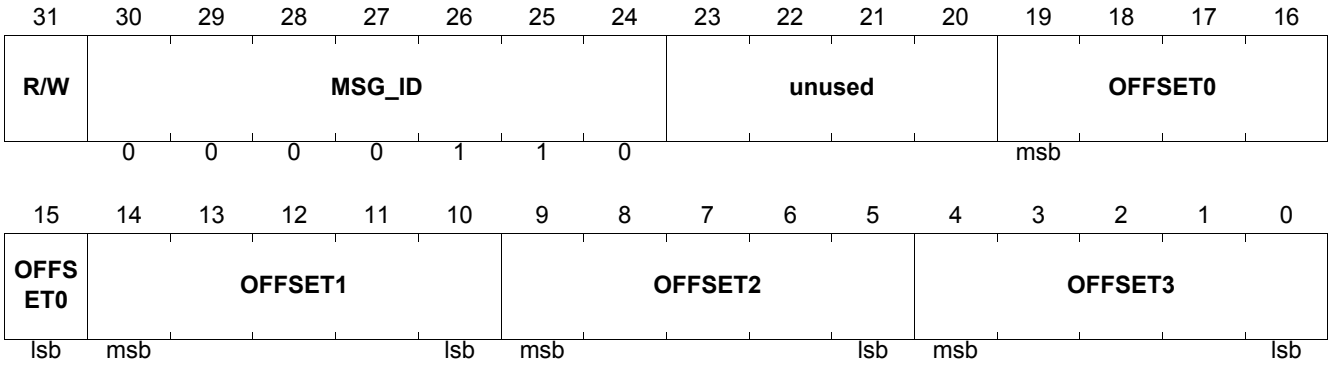
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**MSG_ID**							**SG4**	**OFF-TST4**	**SB4**	**SB-TST4**	**OL-OFF4**	**OL-ON4**	**SG5**	**OFF-TST5**
	0	0	0	0	1	0	1								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SB5	**SB-TST5**	**OL-OFF5**	**OL-ON5**	**SG6**	**OFF-TST6**	**SB6**	**SB-TST6**	**OL-OFF6**	**OL-ON6**	**SG7**	**OFF-TST7**	**SB7**	**SB-TST7**	**OL-OFF7**	**OL-ON7**

Field	Bits	Type	Description
MSG_ID	30:24	ADDR	**Message Identifier** 000 0101 = Diagnostic Read (channel 4-7)
SGx	23, 17, 11, 5	DATA	**Short to Ground - Fault** (RESET value = 0)
OFF-TSTx	22, 16, 10, 4	DATA	**Short to Ground & Open Load (Gate Off) - Tested** (RESET value = 0)
SBx	21, 15, 9, 3	DATA	**Short to Battery - Fault** (RESET value = 0)
SB-TSTx	20, 14, 8, 2	DATA	**Short to Battery - Tested** (RESET value = 0)
OL-OFFx	19, 13, 7, 1	DATA	**Open Load (Gate Off) - Fault** (RESET value = 0)
OL-ONx	18, 12, 6, 0	DATA	**Open Load (Gate On) - Fault** (RESET value = 0)

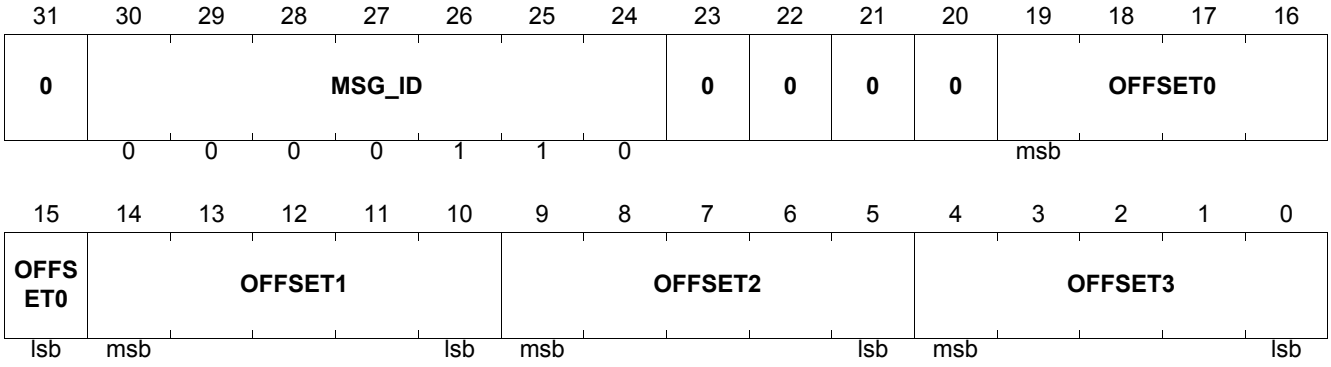
5.9.2.7 SPI Message #6 - PWM Offset (channel 0-3)

Sent Values:
PWM Offset (channels 0-3)



Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:24	ADDR	**Message Identifier** 000 0110 = PWM Offset (channel 0-3)
OFFSETx	19:15, 14:10, 9:5, 4:0	DATA	**Channelx Pulse Offset** 1/32 of PWM period set by N and M values (RESET Value = 0) note: after exiting reset, a pulse on the PHASE_SYNC pin is needed to synchronize the channels

Response Values:
PWM Offset (channels 0-3)



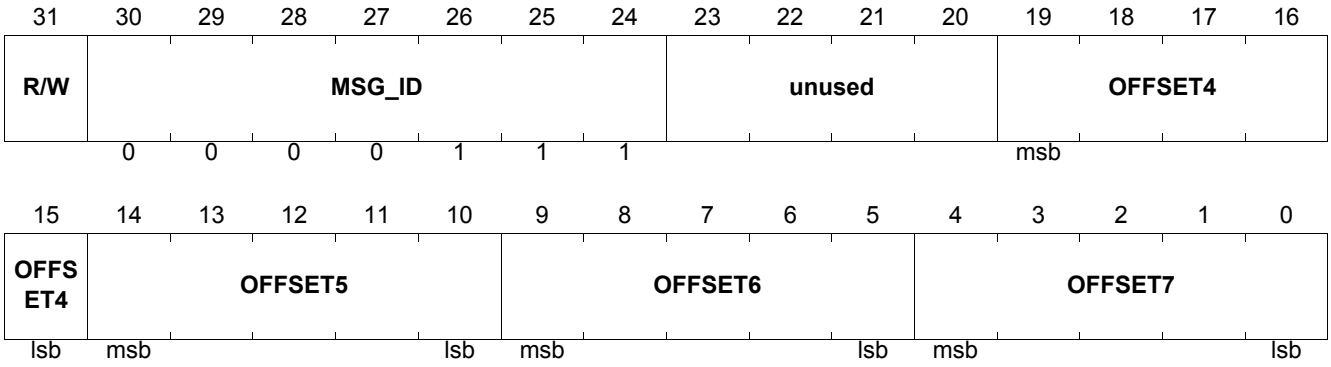
Field	Bits	Type	Description
MSG_ID	30:24	ADDR	**Message Identifier** 000 0110 = PWM Offset (channel 0-3)
OFFSETx	19:15, 14:10, 9:5, 4:0	DATA	**Channelx Pulse Offset** 1/32 of period set by N value (RESET Value = 0)

$$PhaseSynchOffset = \frac{OFFSET_x}{32 * f_{PWM}}$$

Equation: Phase Sync Offset (3)

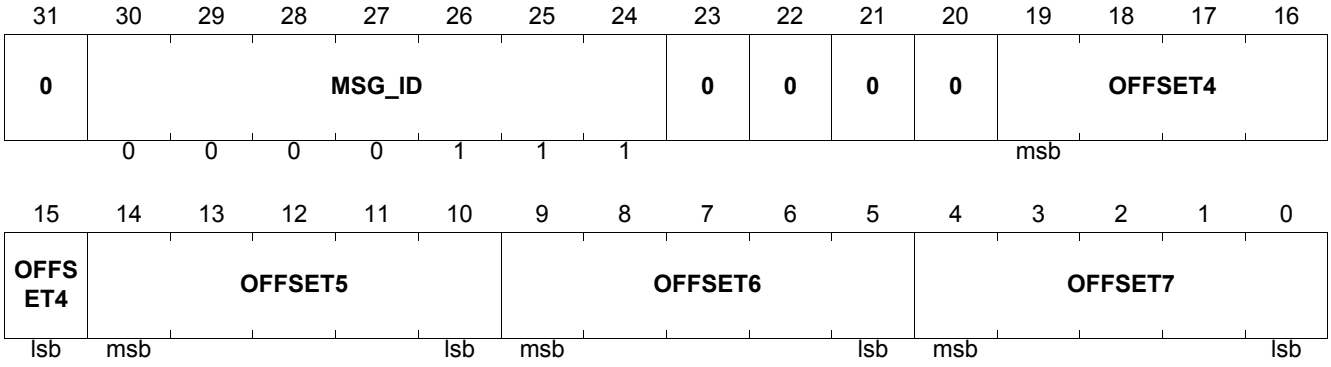
5.9.2.8 SPI Message #7 - PWM Offset (channel 4-7)

Sent Values:
PWM Offset (channels 4-7)



Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:24	ADDR	**Message Identifier** 000 0111 = PWM Offset (channel 4-7)
OFFSETx	19:15, 14:10, 9:5, 4:0	DATA	**Channelx Pulse Offset** 1/32 of period set by N value (RESET Value = 0) note: after exiting reset, a pulse on the PHASE_SYNC pin is needed to synchronize the channels

Response Values:
PWM Offset (channels 4-7)



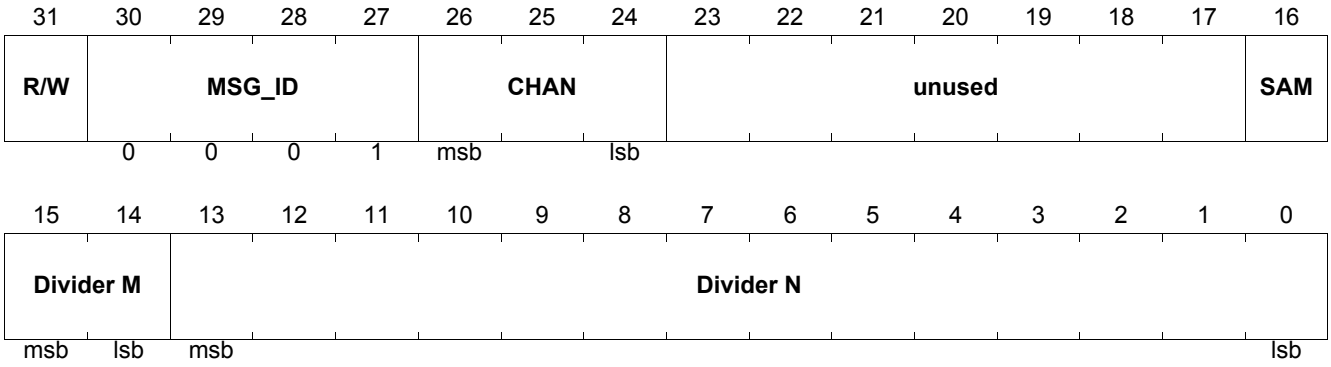
Field	Bits	Type	Description
MSG_ID	30:24	ADDR	**Message Identifier** 000 0111 = PWM Offset (channel 4-7)
OFFSETx	19:15, 14:10, 9:5, 4:0	DATA	**Channelx Pulse Offset** 1/32 of period set by N value (RESET Value = 0)

$$\text{Phase Synch Offset} = \frac{\text{OFFSET}_x}{32 * f_{PWM}}$$

Equation: Phase Sync Offset (4)

5.9.2.9 SPI Message #8 - Main Period Set

Sent Values:
Main Period Set



Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:27	ADDR	**Message Identifier** 0001 = Main Period Set
CHAN	26:24	ADDR	**Channel Number**
SAM	16	DATA	**Sample Summation Method** 0 = Use all values of samples (RESET Value) 1 = throw out first ADC samples after an OUTx pin transition and use previous sample twice in the average calculation
Divider M	15:14	DATA	**Divider M (Number of A/D samples per PWM period)** 00 = 32 (RESET Value) 01 = 64 10 = 128 11 = 512 (Direct PWM) = 128 (Current Control)
Divider N	13:0	DATA	**Divider N (Number of main CLK periods between A/D samples)** (RESET Value = 271_H or 625_D) $T_{PWM} = N*M*T_{CLK}$ & $T_{ADC} = N*T_{CLK}$

Response:
Main Period Set

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**MSG_ID**				**CHAN**			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SAM**
	0	0	0	1	msb		lsb								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Divider M		**Divider N**													
msb	lsb	msb													lsb

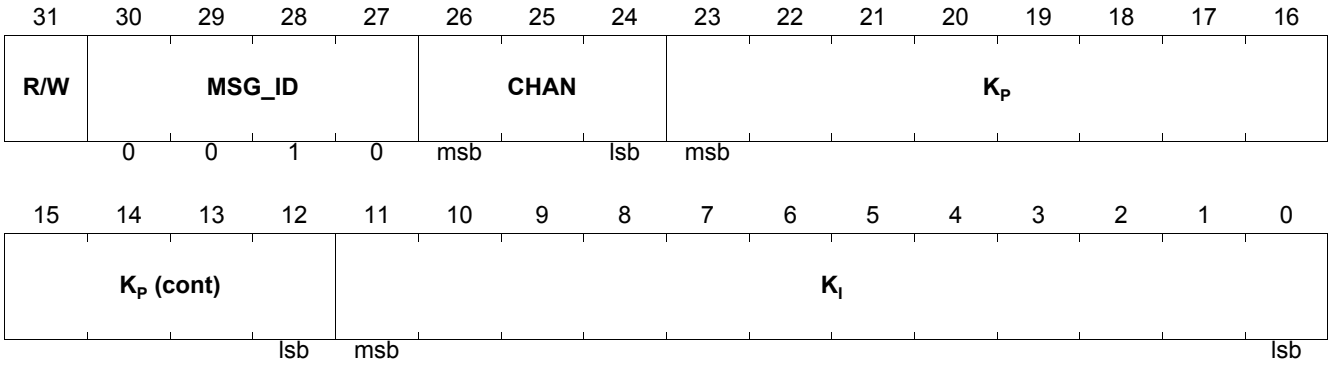
Field	Bits	Type	Description
MSG_ID	30:27	ADDR	**Message Identifier** 0001 = Main Period Set
CHAN	26:24	ADDR	**Channel Number**
SAM	16	DATA	**Sample Summation Method** 0 = Use all values of samples (RESET Value) 1 = throw out first ADC samples after an OUTx pin transition and use previous sample twice in the average calculation
Divider M	15:14	DATA	**Divider M (Number of A/D samples per PWM period)** 00 = 32 (RESET value) 01 = 64 10 = 128 11 = 512 (Direct PWM) = 128 (Current Control)
Divider N	13:0	DATA	**Divider N (Number of main CLK periods between A/D samples)** (RESET Value = 271_H or 625_D) $T_{PWM} = N*M*T_{CLK}$ & $T_{ADC} = N*T_{CLK}$

$$\text{PWM Period} = \frac{N * M}{f_{CLK}} \quad [\text{seconds}]$$

Equation: Main Period Setting (5)

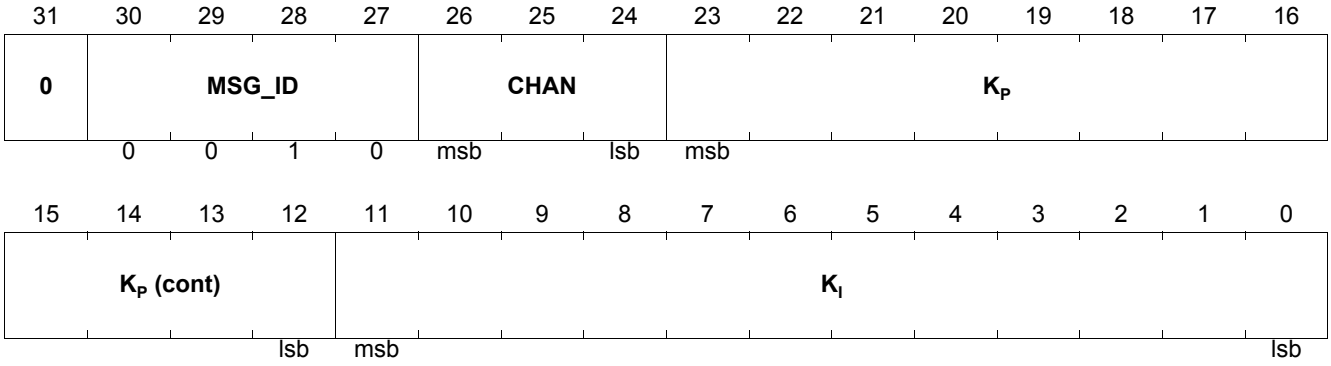
5.9.2.10 SPI Message #9 - Control Variable Set (K_P and K_I)

Sent Values:
Control Variable Set



Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:27	ADDR	**Message Identifier** 0010 =Control Variable Set
CHAN	26:24	ADDR	**Channel Number**
K_P	23:12		**Control Loop Proportional Coefficient** (RESET Value = 0)
K_I	11:0		**Control Loop Integral Coefficient** (RESET Value = 0)

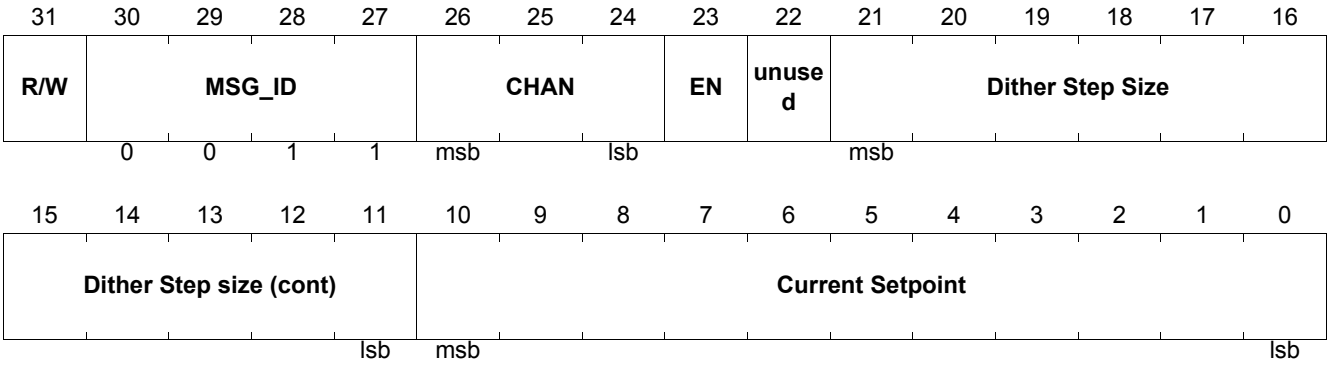
Response:
Control Variable Set



Field	Bits	Type	Description
MSG_ID	30:27	ADDR	**Message Identifier** 0010 =Control Variable Set
CHAN	26:24	ADDR	**Channel Number**
K_P	23:12	DATA	**Control Loop Proportional Coefficient** (RESET Value = 0)
K_I	11:0	DATA	**Control Loop Integral Coefficient** (RESET Value = 0)

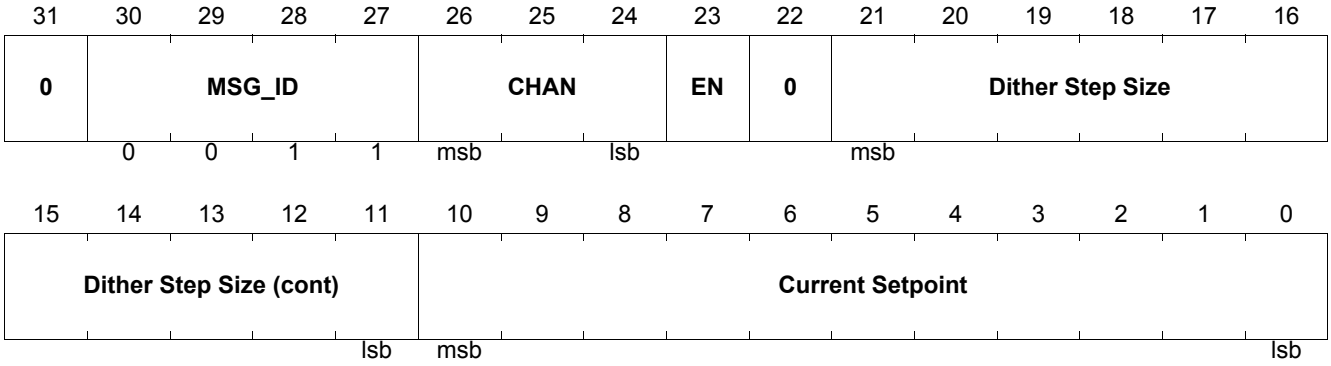
5.9.2.11 SPI Message #10 - Current and Dither Amplitude Set

Sent Values:
Current and Dither Amplitude Set



Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:27	ADDR	**Message Identifier** 0011 =Current and Dither Amplitude Set
CHAN	26:24	ADDR	**Channel Number**
EN	23	DATA	**Operation during ENABLE deactivation** 0 = disable (RESET Value) 1 = remain in operation at last setpoint including dither
Dither Step Size	21:11	DATA	**Dither Step Size (LSb's value is 2^{-2} of the current setpoint LSb)** (RESET Value = 0) Note: A value of 0 will disable the dither function
Current Setpoint	10:0	DATA	**Current Set Point** (RESET Value = 0)

Response:
Current and Dither Amplitude Set



Field	Bits	Type	Description
MSG_ID	30:27	ADDR	**Message Identifier** 0011 =Current and Dither Amplitude set
CHAN	26:24	ADDR	**Channel Number**
EN	23	DATA	**Operation during ENABLE deactivation** 0 = disable (RESET Value) 1 = remain in operation at last setpoint including dither
Dither Step Size	21:11	DATA	**Dither Step Size (LSb's value is 2^{-2} of the current setpoint LSb)** (RESET Value = 0) Note: A value of 0 will disable the dither function
Current Setpoint	10:0	DATA	**Current Set Point** (RESET Value = 0)

$$\text{Dither Amplitude}\,[\text{mA pp}] = \frac{2 * \text{Dither Stepsize} * \text{Dither Steps}}{2^{13}} * \frac{320[\text{mV}]}{\text{Rsense}\,[\text{Ohm}]}$$

Equation: Dither Amplitude Setting (6)

$$\text{Average Current Setting}\,[\text{mA}] = \frac{\text{Current Setpoint}}{2^{11}} * \frac{320[\text{mV}]}{\text{Rsense}[\text{Ohm}]}$$

Equation: Average Current Setting (7)

5.9.2.12 SPI Message #11 - Dither Period Set

Sent Values:
Dither Period Set

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	**MSG_ID**				**CHAN**			**unused**							
	0	1	0	0	msb		lsb								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused											**Number of Steps**				
											msb				lsb

Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:27	ADDR	**Message Identifier** 0100 =Dither Period Set
CHAN	26:24	ADDR	**Channel Number**
Number of Steps	4:0	DATA	**Number of Dither Steps in 1/4 waveform** (RESET Value = 0) Note: A value of 0 will disable the dither function

Response:
Dither Period Set

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**MSG_ID**				**CHAN**			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
	0	1	0	0	msb		lsb								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Number of Steps**				
											msb				lsb

Field	Bits	Type	Description
MSG_ID	30:27	ADDR	**Message Identifier** 0100 =Dither Period Set
CHAN	26:24	ADDR	**Channel Number**
Number of Steps	4:0	DATA	**Number of Dither Steps in 1/4 waveform** (RESET Value = 0) Note: A value of 0 will disable the dither function

$$\text{Dither Period} = \frac{4 * \text{Number of Steps}}{f_{PWM}}$$

Equation: Dither Period Setting (8)

5.9.2.13 SPI Message #12 - Max / Min Current Read

Sent Values:
Max / Min Current Read

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	MSG_ID				CHAN			unused							
	0	1	0	1	msb		lsb								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused															

Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:27	ADDR	**Message Identifier** 0101 =Max / Min Current Read
CHAN	26:24	ADDR	**Channel Number** Note: the channel selection for this message will also be the channel selected for the Average Current Read over Dither Period.

PEAK

Response:
Max / Min Current Read

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	MSG_ID				CHAN			0	VALID	MAX					
	0	1	0	1	msb		lsb			msb					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX (cont)					MIN										
				lsb	msb										lsb

Field	Bits	Type	Description
MSG_ID	30:27	ADDR	**Message Identifier** 0101 =Current Read
CHAN	26:24	ADDR	**Channel Number**
VALID	22	DATA	**VALID** Reset when the register is read or when the channel number is changed (RESET Value = 0) Set when a new data set is available.

Field	Bits	Type	Description
MAX	21:11	DATA	**The largest summation of "M" A/D samples (within one PWM period) during the previous dither cycle. The 11 most significant bits are reported.** Note: return value will be 0 until the first dither cycle is completed - (RESET Value = 0)
MIN	10:0	DATA	**The smallest summation of "M" A/D samples (within one PWM period) during the previous dither cycle. The 11 most significant bits are reported.** Note: return value will be 2047until the first dither cycle is completed - (RESET Value = 2047)

$$\text{Max Current Feedback}[\text{mA}] = \frac{\text{MAX}}{2^{11}} * \frac{320[\text{mV}]}{\text{Rsense}[\text{Ohm}]}$$

Equation: Maximum Dither Current Feedback (9)

$$\text{Min Current Feedback}[\text{mA}] = \frac{\text{MIN}}{2^{11}} * \frac{320[\text{mV}]}{\text{Rsense}[\text{Ohm}]}$$

Equation: Minimum Dither Current Feedback (10)

Note: When the selected channel is different than the previously selected channel (the last time this message was addressed), the new Min and Max data will be available after no more than two dither cycles. When the selected channel is the same as the previously selected channel, the new Min and Max data will be available in no more than one dither cycle.

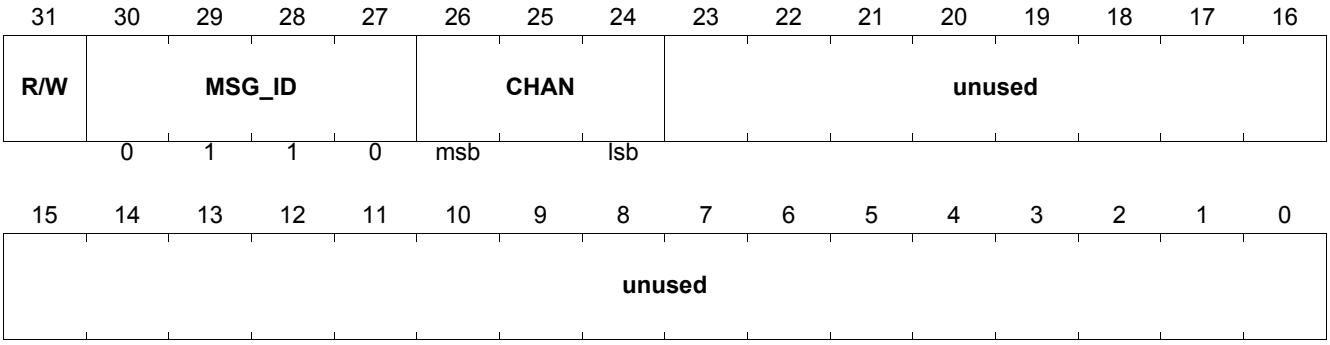
Note: When M=512 in Direct PWM mode, the following formula applies. The application software must ensure that the register has not overflowed.

$$\text{Min / Max Current Feedback}[\text{mA}] = \frac{\text{MIN or MAX}}{2^{13}} * \frac{320[\text{mV}]}{\text{Rsense}[\text{Ohm}]}$$

Equation: Min/Max Dither Current Feedback M=512 (11)

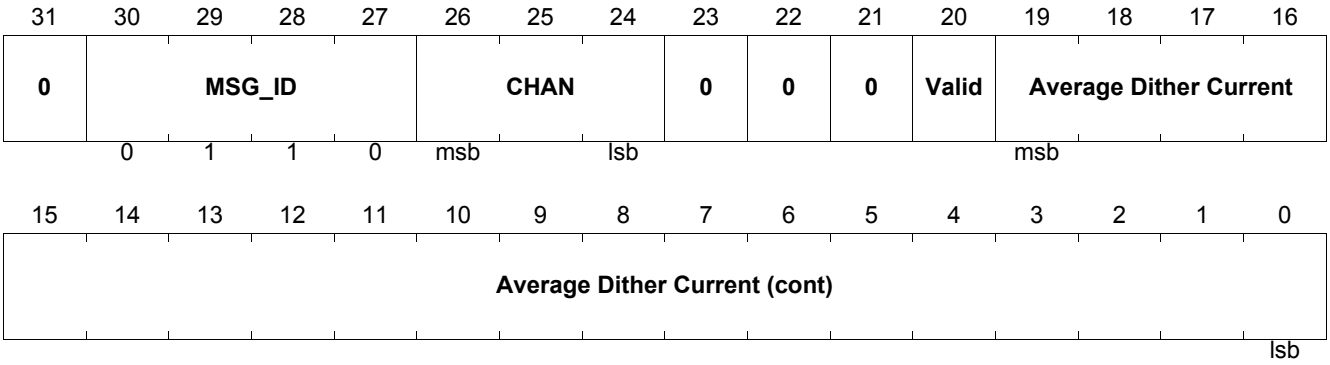
5.9.2.14 SPI Message #13 - Average Current Read Over Dither Period

Sent Values:
Average Dither Current Read



Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:27	ADDR	**Message Identifier** 0110 =Dither Current Read
CHAN	26:24	ADDR	**Channel Number**

Response:
Average Dither Current Read



Field	Bits	Type	Description
MSG_ID	30:27	ADDR	**Message Identifier** 0110 =Dither Current Read
CHAN	26:24	ADDR	**Channel Number** Note: the channel selection for this message will also be the channel selected for the Max / Min Current Read Command.
VALID	20	DATA	**VALID BIT** Reset when register is read or when channel number is changed. Set when new data is available. (RESET Value = 0)

Field	Bits	Type	Description
Average Dither Current	19:0	DATA	**20 bit summation of the total current over a dither period.** (RESET Value = 0)

$$\text{Dither Current Feedback}\,[\text{mA}] = \frac{\text{Avg Dither Current}}{2^{15} * \text{Dither Steps}} * \frac{320[\text{mV}]}{\text{Rsense}\,[\text{Ohm}]}$$

Equation: Average Dither Current Feedback with Dither enabled (12)

$$\text{Dither Current Feedback}\,[\text{mA}] = \frac{\text{Avg Dither Current}}{2^{13}} * \frac{320[\text{mV}]}{\text{Rsense}\,[\text{Ohm}]}$$

Equation: Average Dither Current Feedback with Dither disabled (13)

Note: When the selected channel is different than the previously selected channel (the last time this message was addressed), the new Average Dither Current data will be available after no more than two dither cycles. When the selected channel is the same as the previously selected channel, the new Average Dither Current data will be available in no more than one dither cycle.

Note: When M=512 in Direct PWM mode, the following formula applies. The application software must ensure that the register has not overflowed.

$$\text{Dither Current Feedback}\,[\text{mA}] = \frac{\text{Avg Dither Current}}{2^{17} * \text{Dither Steps}} * \frac{320[\text{mV}]}{\text{Rsense}\,[\text{Ohm}]}$$

Equation: Average Dither Current Feedback M=512 with dither enabled

(14)

$$\text{Dither Current Feedback}\,[\text{mA}] = \frac{\text{Avg Dither Current}}{2^{15}} * \frac{320[\text{mV}]}{\text{Rsense}\,[\text{Ohm}]}$$

Equation: Average Dither Current Feedback M=512 with dither disabled (15)

5.9.2.15 SPI Message #14 - Autozero Trigger / Read

Sent Values:
Autozero Trigger Read

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	**MSG_ID**				**CHAN**			**unused**							
	0	1	1	1	msb		lsb								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused															

Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:27	ADDR	**Message Identifier** 0111 =Autozero Trigger / Read
CHAN	26:24	ADDR	**Channel Number**

Response:
Autozero Trigger Read

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**MSG_ID**				**CHAN**			**0**	**0**	**0**	**0**	**0**	**0**	**AZon**	**AZoff**
	0	1	1	1	msb		lsb								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AZon value								**AZoff value**							
msb							lsb	msb							lsb

Field	Bits	Type	Description
MSG_ID	30:27	ADDR	**Message Identifier** 0111 =Autozero Trigger / Read
CHAN	26:24	ADDR	**Channel Number**
AZon	17	DATA	**Autozero - Gate on has occurred since last read** 0 = not occurred (RESET Value) 1 = has occurred
AZoff	16	DATA	**Autozero - Gate off has occurred since last read** 0 = not occurred (RESET Value) 1 = has occurred

Field	Bits	Type	Description
AZ on value	15:8	DATA	**Autozero value - Gate On**
AZ off value	7:0	DATA	**Autozero value - Gate Off**

When this register is written an Auto-Zero sequence is initiated for the selected channel, and the AZon and AZoff bits are reset. The AZon and AZoff bits are set after the autozero sequence has completed.

When this register is read, the Auto-Zero sequence is not initiated, but the AZon and AZoff bits are reset.

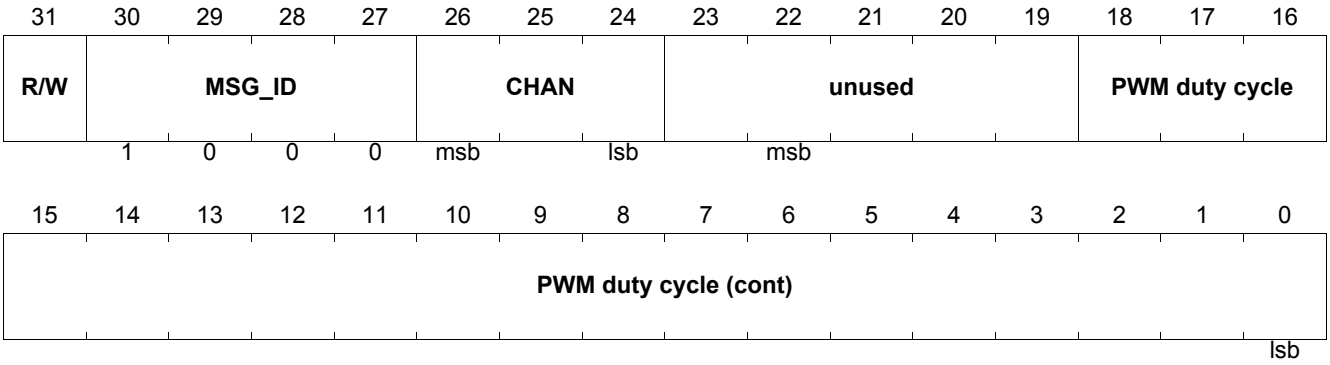
Note: When a channel transitions from on to off, the autozero sequence for that channel must not be initiated until the recirculation current has fully decayed to 0 mA. Otherwise, the calculated autozero values will be incorrect resulting in inaccurate current regulation when a non-zero setpoint is programmed.

$$\text{Autozero offset}\left[\text{mA}\right] = \frac{\text{AZ\_value}}{2^{11}} * \frac{320[\text{mV}]}{\text{Rsense}[\text{Ohm}]}$$

Equation: Auto-zero value (16)

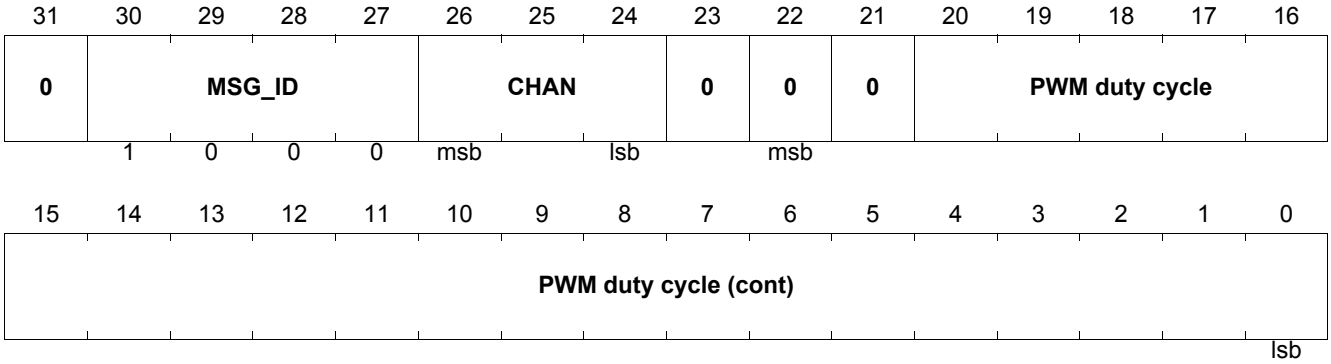
5.9.2.16 SPI Message #15 - PWM Duty Cycle

Sent Values:
PWM Duty Cycle



Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:27	ADDR	**Message Identifier** 1000 =PWM Duty Cycle
CHAN	26:24	ADDR	**Channel Number**
PWM duty cycle	18:0	DATA	**PWM duty cycle** This is used when Control Mode is set to “direct PWM”. See the “Control Method and Fault Mask Configuration” message. If this message is written when the Control Mode is set to “Current Control” the PWM data will be stored but not used until the control mode is switched to “Direct PWM”. (RESET Value = 0)

Response:
PWM Duty Cycle



Field	Bits	Type	Description
MSG_ID	30:27	ADDR	**Message Identifier** 1000 =PWM Duty Cycle
CHAN	26:24	ADDR	**Channel Number**
PWM duty cycle	20:0	DATA	**PWM duty cycle** This will report the duty cycle bits in the register. If the channel is set to “Current Control” the feedback will represent the value calculated by the PI controller. If the channel is set to “direct PWM” the feedback will represent the value in the register programmed by a SPI write with bits 11 and 12 always read as 0. See the “Control Method and Fault Mask Configuration” message. (RESET Value = 0)

$$\text{Duty Cycle}[\%] = \frac{\text{PWM duty cycle}}{N * M} * 100\%$$

Note: The Duty Cycle of 100% can be achieved. Although the above formula may result in duty cycle values greater than 100%, the actual duty cycle is of course limited to 100%.

Equation: PWM duty cycle readout for constant current mode operation (17)

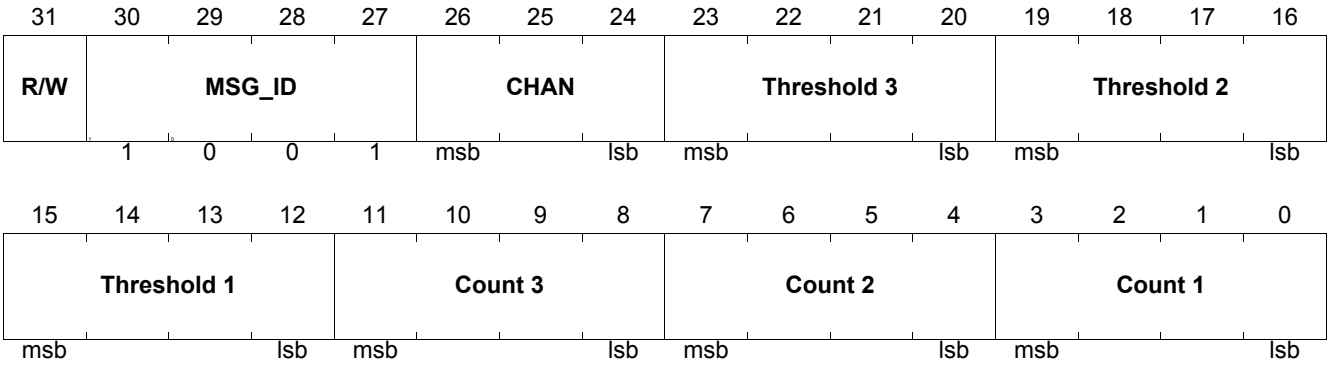
$$\text{Duty Cycle}[\%] = \frac{\text{PWM duty cycle}}{N * 32} * 100\%$$

Equation: PWM duty cycle readout for direct PWM mode operation (18)

Note: The Duty Cycle of 100% can be achieved. Although the above formula may result in duty cycle values greater than 100%, the actual duty cycle is of course limited to 100%.

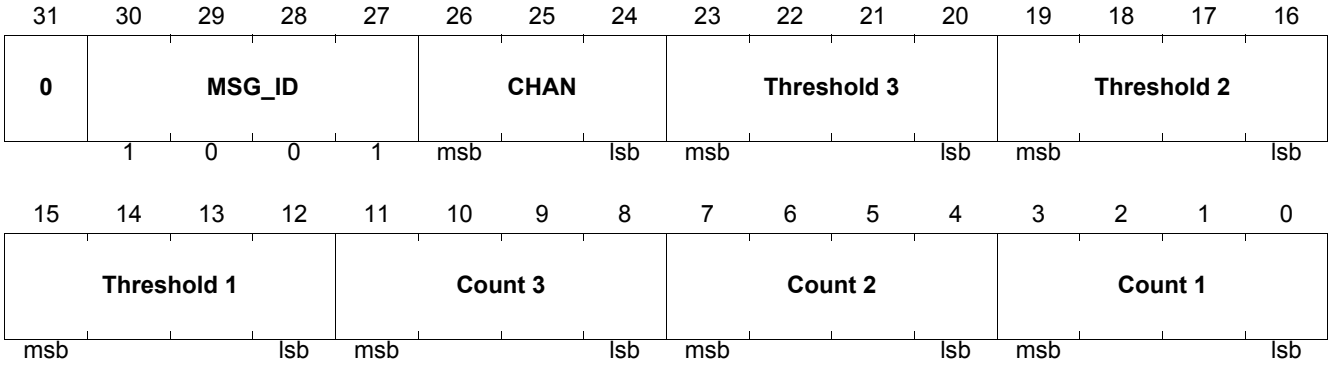
5.9.2.17 SPI Message #16 - Current Profile Detection Setup 1

Sent Values:
Current Profile Detection Setup 1



Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:27	ADDR	**Message Identifier** 1001 =Current Profile Setup 1
CHAN	26:24	ADDR	**Channel Number**
Threshold 3	23:20	DATA	**Threshold 3 (Zone 3)** (RESET Value = 0)
Threshold 2	19:16	DATA	**Threshold 2 (Zone 2)** (RESET Value = 0)
Threshold 1	15:12	DATA	**Threshold 1 (Zone 1)** (RESET Value = 0)
Count 3	11:8	DATA	**Count 3 (Zone 3)** (RESET Value = 0)
Count 2	7:4	DATA	**Count 2 (Zone 2** (RESET Value = 0)
Count 1	3:0	DATA	**Count 1 (Zone 1)** (RESET Value = 0)

Response:
Current Profile Detection Setup 1



Field	Bits	Type	Description
MSG_ID	30:27	ADDR	**Message Identifier** 1001 =Current Profile Setup 1
CHAN	26:24	ADDR	**Channel Number**
Threshold 3	23:20	DATA	**Threshold 3 (Zone 3)** (RESET Value = 0)
Threshold 2	19:16	DATA	**Threshold 2 (Zone 2)** (RESET Value = 0)
Threshold 1	15:12	DATA	**Threshold 1 (Zone 1)** (RESET Value = 0)
Count 3	11:8	DATA	**Count 3 (Zone 3)** (RESET Value = 0)
Count 2	7:4	DATA	**Count 2 (Zone 2)** (RESET Value = 0)
Count 1	3:0	DATA	**Count 1 (Zone 1)** (RESET Value = 0)

5.9.2.18 SPI Message #17 - Current Profile Detection Setup 2

Sent Values:
Current Profile Detection Setup 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	**MSG_ID**				**CHAN**			**unused**							
	1	0	1	0	msb		lsb								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused						**Time out**						**unused**		**ZONE 3 SET**	
						msb					lsb				

Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:27	ADDR	**Message Identifier** 1010 =Current Profile Setup 2
CHAN	26:24	ADDR	**Channel Number**
Time out	9:4	DATA	**Current Profile Time out** 1 lsb = 16 ADC sample periods (RESET Value = 0)
Zone 3 Set	1:0	DATA	**Zone 3 A/D setup** 00: ADDIFF=A/D_m - A/D_{m-1} 01: ADDIFF=A/D_m - A/D_{m-2} 10: ADDIFF=A/D_m - A/D_{m-3} 11: ADDIFF=A/D_m - A/D_{m-4}

Response:
Current Profile Detection Setup 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**MSG_ID**				**CHAN**			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
	1	0	1	0	msb		lsb								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**Time out**						**0**	**0**	**ZONE3 SET**	
						msb					lsb				

Field	Bits	Type	Description
MSG_ID	30:27	ADDR	**Message Identifier** 1010 =Current Profile Setup 2
CHAN	26:24	ADDR	**Channel Number**

Field	Bits	Type	Description
Time out	9:4	DATA	**Current Profile Time out** 1 lsb = 16 ADC sample periods (RESET Value = 0)
Zone 3 Set	1:0	DATA	**Zone 3 A/D setup** 00: ADDIFF=A/D_m - A/D_{m-1} 01: ADDIFF=A/D_m - A/D_{m-2} 10: ADDIFF=A/D_m - A/D_{m-3} 11: ADDIFF=A/D_m - A/D_{m-4}

5.9.2.19 SPI Message #18 - Current Profile Detection Feedback

Sent Values:
Current Profile Detection Feedback

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	**MSG_ID**				**CHAN**			**unused**							
	1	0	1	1	msb		lsb								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused															

Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:27	ADDR	**Message Identifier** 1011 =Current Profile Detection Feedback
CHAN	26:24	ADDR	**Channel Number**

Response:
Current Profile Detection Feedback

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**MSG_ID**				**CHAN**			**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
	1	0	1	1	msb		lsb								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Detect Intrpt**	**Time-out**	**PASS**

Field	Bits	Type	Description
MSG_ID	30:27	ADDR	**Message Identifier** 1011 =Current Profile Detection Feedback
CHAN	26:24	ADDR	**Channel Number**
Detection Interrupted	2	DATA	**Detect Interrupt Bit** (RESET Value = 0) Reset when this register is read. Set when the gate of the external FET is commanded off before the current profile detection sequence has completed.

Field	Bits	Type	Description
Time out	1	DATA	**Current Profile Timeout** (RESET Value = 0) Reset when this register is read. Set when the programmable time-out timer expires before the Current Profile Detection sequence has completed.
PASS	0	DATA	**Passed Since Last Read** (RESET Value = 0) Reset when this register is read. Set when the Current Profile Detection sequence has completed before the programmed time-out timer expired and before the gate is turned off.

Table 7 Interpretation of bits 2 to 0

Detect Interrupt Bit	Current Profile Timeout	Passed Since Last Read	Meaning
0	0	0	A current profile sequence has not completed since the last read of this register
X	X	1	At least one current profile sequence has completed successfully since the last read of this register
X	1	X	At least one time out failure has occurred since the last read of this register
1	X	X	At least one detect interrupt failure has occurred since the last read of this register.

5.9.2.20 SPI Message #19 - Read Generic Flag Bits

Sent Values:
Read Generic Flag Bits

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	**MSG_ID**				**unused**										
	1	1	1	1											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused															

Field	Bits	Type	Description
R/W	31		**Read / Write Bit** 0 = Read 1 = Write
MSG_ID	30:27	ADDR	**Message Identifier** 1111 = Read Generic Flag Bits

Response:
Read Generic Flag Bits

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**MSG_ID**				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
	1	1	1	1											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**OV**	**PS**	**EN_L**	**RB_L**

Field	Bits	Type	Description
MSG_ID	30:27	ADDR	**Message Identifier** 1111 = Read Generic Flag Bits
OV	3	DATA	**Overvoltage has occurred since last read** 0 = not occurred (RESET Value) 1 = has occurred
PS	2	DATA	**Phase Synch has occurred since last read** 0 = not occurred (RESET Value) 1 = has occurred
EN_L	1	DATA	**Enable Latch bit** (RESET Value = 1) Set to 0 when this register is read and ENABLE pin is High Set to 1 when the ENABLE pin is Low

Field	Bits	Type	Description
RB_L	0	DATA	**RESET_B Latch bit** (RESET Value = 1) Set to 0 when this register is read. Set to 1 when the a High to Low transition occurs on the RESET_B pin

6 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

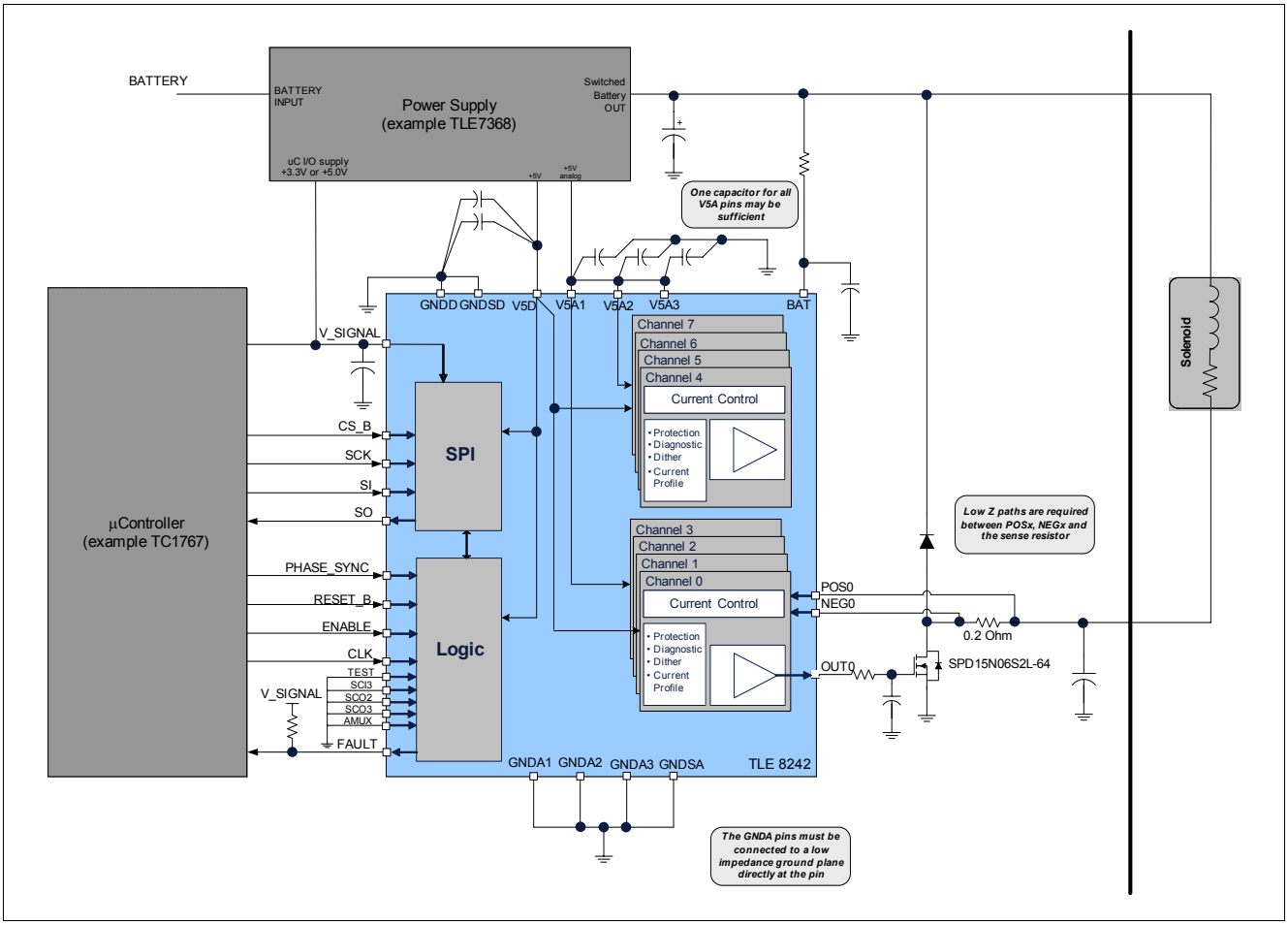


Figure 20 Application Diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

6.1 Further Application Information

- Please contact us to get the Pin FMEA
- For further information you may contact **http://www.infineon.com/**

7 Package Outlines

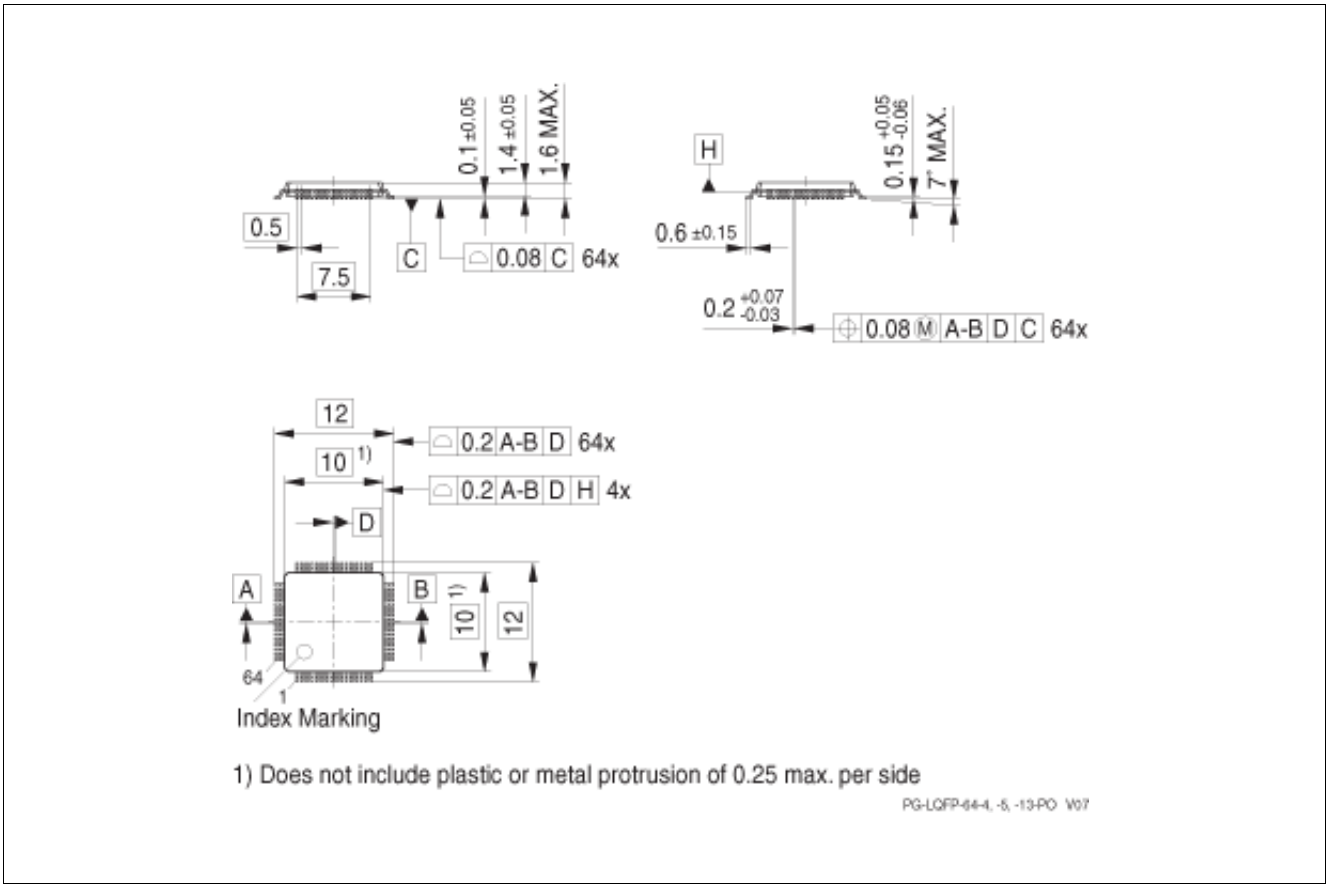


Figure 21 PG-LQFP-64

Green Product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

Dimensions in mm

8 Revision History

Revision	Date	Changes
1.0	2009-02-24	Page 6, Figures 1 and 2 : improved figure quality
		Page 7, improved description of SAM bit functionality
		Pages 24 to 26, Figures 10, 11, 13, and 14: improved figure quality
		Pages 51 and 52: improved description of SAM bit functionality
		Pages 72: corrected the name of the register in the MSG_ID descriptions
		Page 74, Figure 21 : updated the package outline drawing
1.0	2009-12-09	Changes from TLE8242L Rev 1.0 datasheet
1.0	2009-12-09	Section 1.3.2, equation for duty-cycle: revised equation to include the M variable. M is the # of ADC samples per PWM period. revised equation for calculating the duration of the autozero procedure
1.0	2009-12-09	Section 5.3, added new filter times to table 2
1.0	2009-12-09	Section 5.3.2, electrical table, parameters 5.3.12 through 5.3.15 revised with new filter times
1.0	2009-12-09	Section 5.9.2.1, revised IC version number
1.0	2009-12-09	Section 5.9.2.2, added new filter times.
1.0	2009-12-09	Section 5.9.2.14, added equations for current feedback value when dither is disabled
1.0	2009-12-09	Section 5.9.2.14, added equation for autozero offset value
1.0	2009-12-09	Section 5.9.2.7 and 5.9.2.8, added note that a pulse is needed on the phase_sync pin to synchronize the channels after exiting the reset state.
1.0	2009-12-09	Section 5.7.1, added maximum value of analog to digital converter sample rate
1.0	2009-12-09	Section 5.2, added note that a pulse is needed on the PHASE_SYNC pin in order to synchronize the PWM periods of the channels after exiting the reset state

Edition 2010-02-09

Published by
Infineon Technologies AG
81726 Munich, Germany

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