

MOSFET

OptiMOS™ 5 Linear FET, 150 V

Features

- Ideal for hot-swap and e-fuse applications
- Very low on-resistance $R_{DS(on)}$
- Wide safe operating area SOA
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target applications
- Halogen-free according to IEC61249-2-21



Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	150	V
$R_{DS(on),max}$	8.3	m Ω
I_D	105	A
I_{pulse} ($V_{DS}=56$ V, $t_p=10$ ms)	5.6	A



Type / Ordering Code	Package	Marking	Related Links
IPB083N15N5LF	PG-TO 263-3	083N15LF	-

¹⁾ J-STD20 and JESD22

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1 Maximum ratings

at $T_C=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	105 66 14	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$, $R_{thJA}=40\text{ K/W}^{(1)}$
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	-	-	420	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁽³⁾	E_{AS}	-	-	10	mJ	$I_D=25\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	179	W	$T_C=25\text{ °C}$
Operating and storage temperature	T_j , T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.45	0.7	K/W	-
Device on PCB, minimal footprint	R_{thJA}	-	-	62	K/W	-
Device on PCB, 6 cm ² cooling area ⁽¹⁾	R_{thJA}	-	-	40	K/W	-

⁽¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

⁽²⁾ See Diagram 3 for more detailed information

⁽³⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	3.3	4.1	4.9	V	$V_{DS}=V_{GS}$, $I_D=134\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	1 10	2 100	μA	$V_{DS}=120\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=120\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	2 -2	5 -5	μA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$ $V_{GS}=-10\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	6.9	8.3	$\text{m}\Omega$	$V_{GS}=10\text{ V}$, $I_D=100\text{ A}$
Gate resistance ¹⁾	R_G	-	28	42	Ω	-
Transconductance	g_{fs}	9	18	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=52\text{ A}$

Table 5 Dynamic characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	160	210	pF	$V_{GS}=0\text{ V}$, $V_{DS}=75\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	740	960	pF	$V_{GS}=0\text{ V}$, $V_{DS}=75\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	11	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=75\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	7	-	ns	$V_{DD}=75\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=52\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	46	-	ns	$V_{DD}=75\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=52\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	25	-	ns	$V_{DD}=75\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=52\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	6	-	ns	$V_{DD}=75\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=52\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	1.2	-	nC	$V_{DD}=75\text{ V}$, $I_D=52\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	31	-	nC	$V_{DD}=75\text{ V}$, $I_D=52\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	45	-	nC	$V_{DD}=75\text{ V}$, $I_D=52\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	6.6	-	V	$V_{DD}=75\text{ V}$, $I_D=52\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ¹⁾	Q_{oss}	-	111	148	nC	$V_{DD}=75\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	105	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	420	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.99	1.2	V	$V_{GS}=0\text{ V}, I_F=100\text{ A}, T_j=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	61	-	ns	$V_R=75\text{ V}, I_F=52\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	92	-	nC	$V_R=75\text{ V}, I_F=52\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

¹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

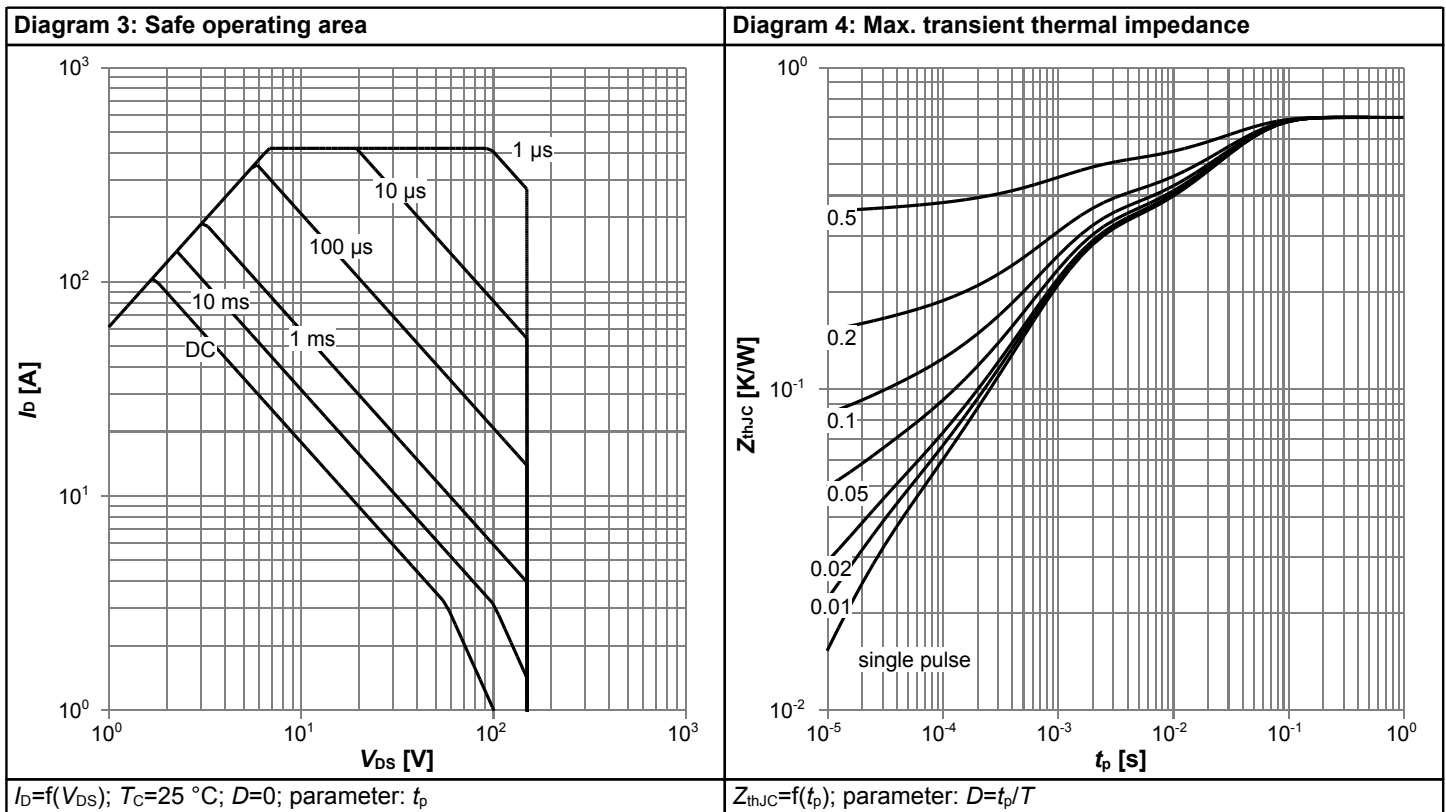
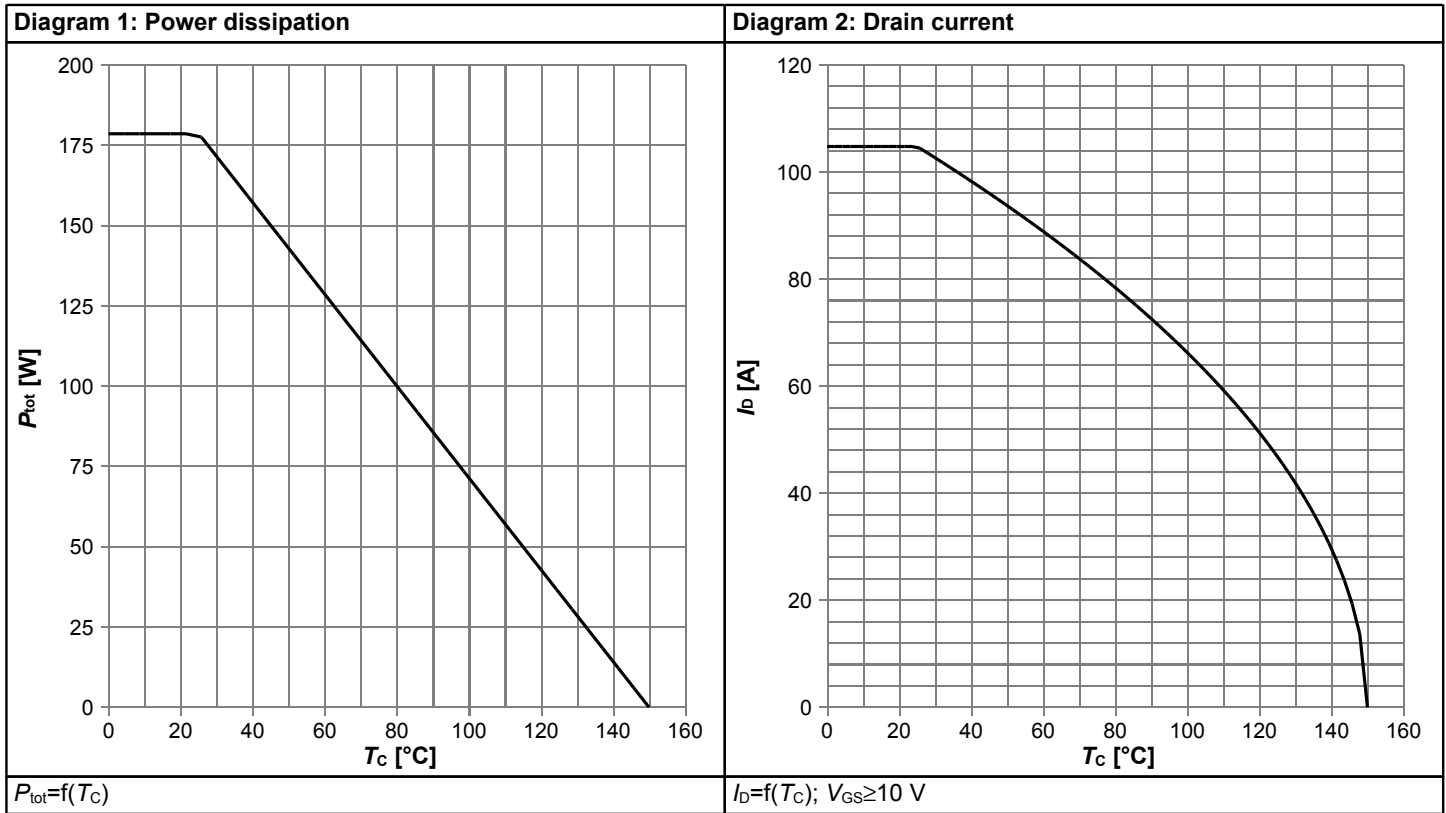
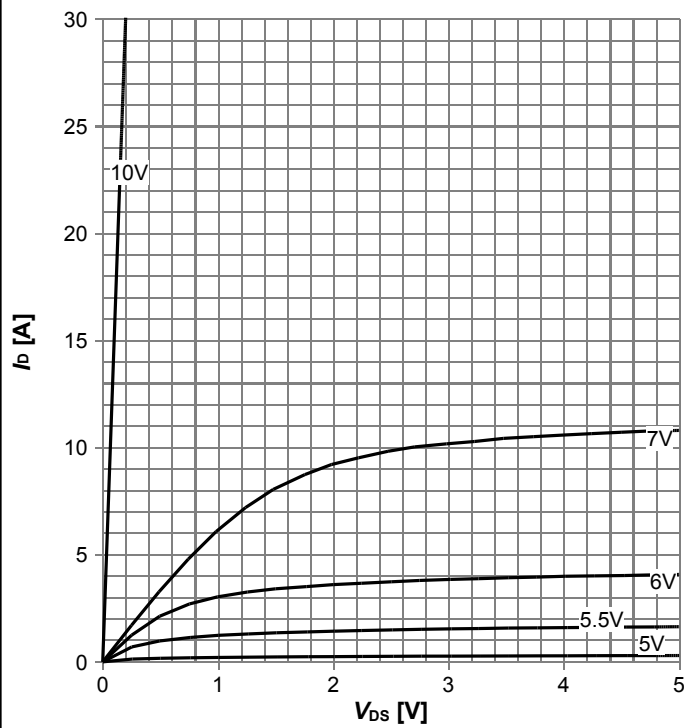
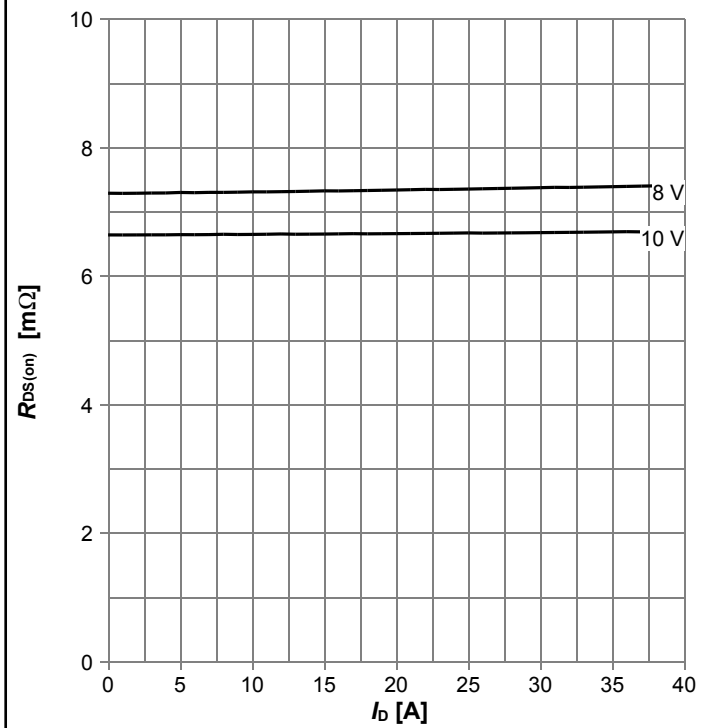


Diagram 5: Typ. output characteristics



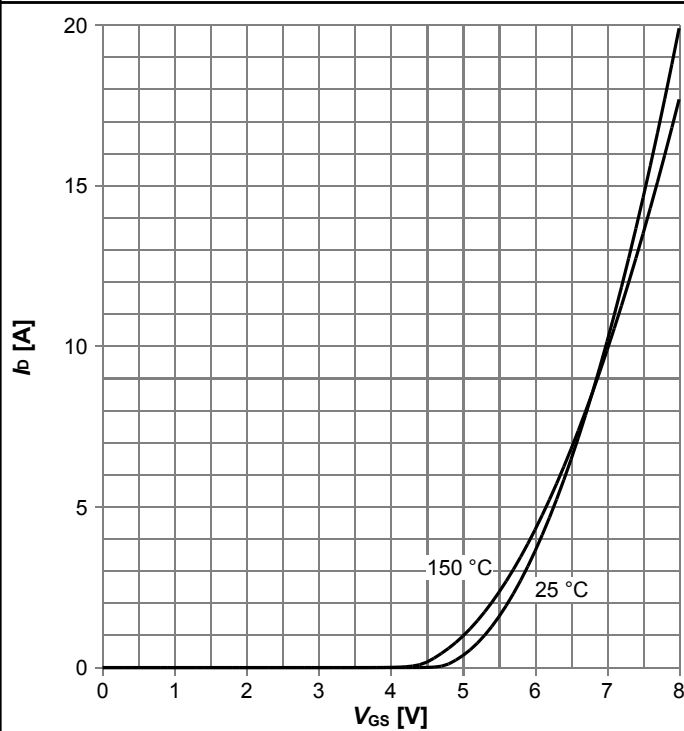
$I_D = f(V_{DS}), T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



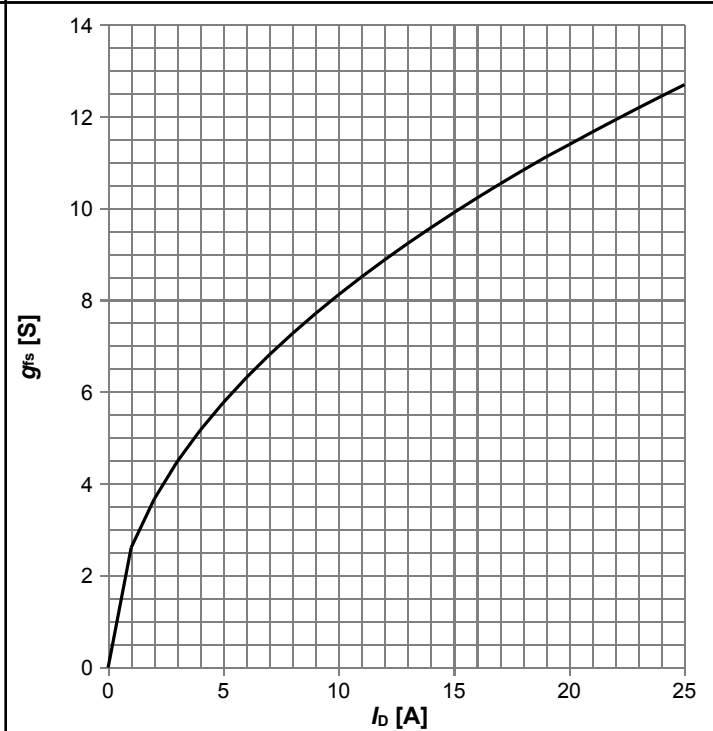
$R_{DS(on)} = f(I_D), T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



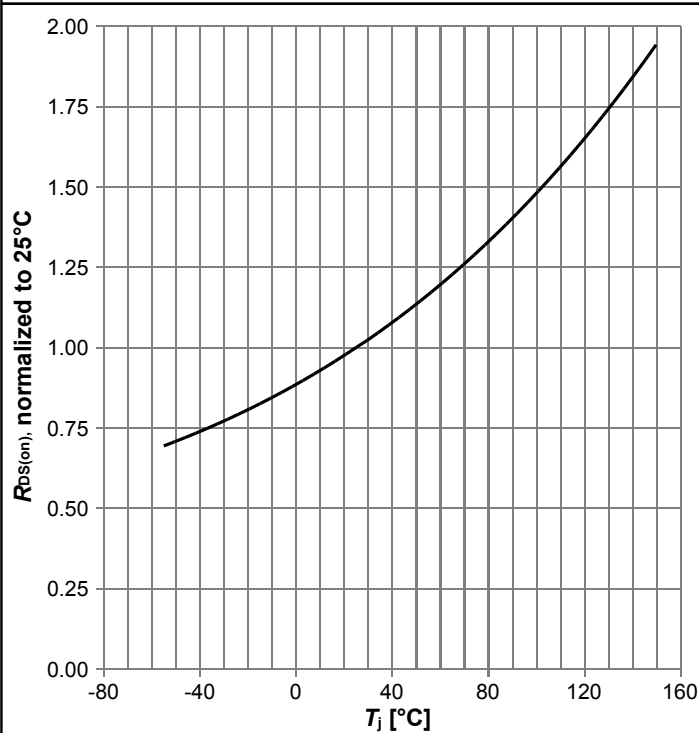
$I_D = f(V_{GS}), |V_{DS}| > 2 \cdot I_D / R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



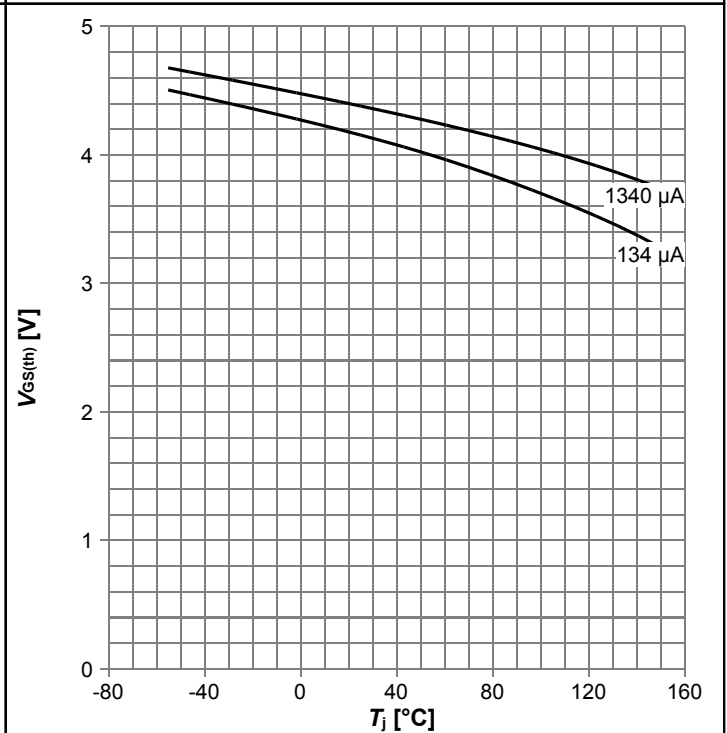
$g_{fs} = f(I_D), V_{DS} = 5\text{ V}, T_j = 25^\circ\text{C}$

Diagram 9: Normalized drain-source on-state resistance



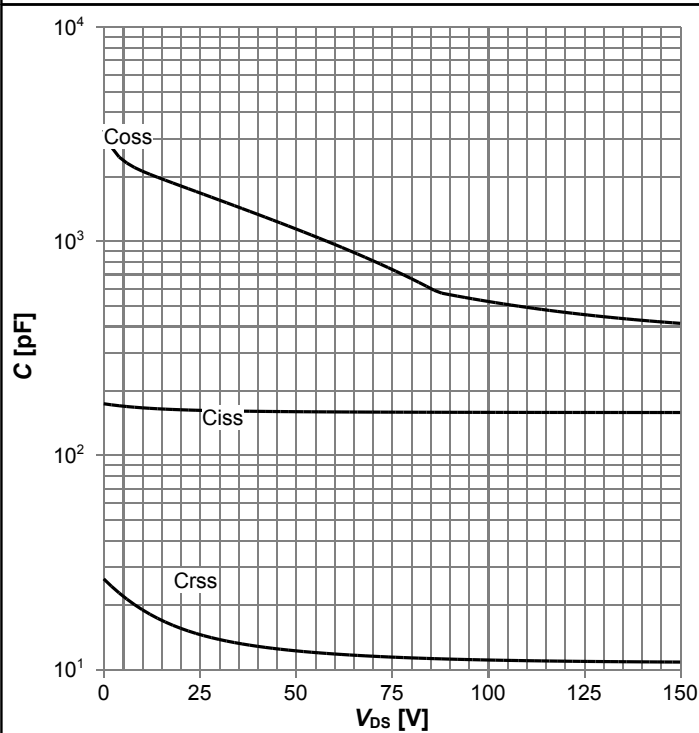
$R_{DS(on)}=f(T_j)$, $I_D=52$ A, $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



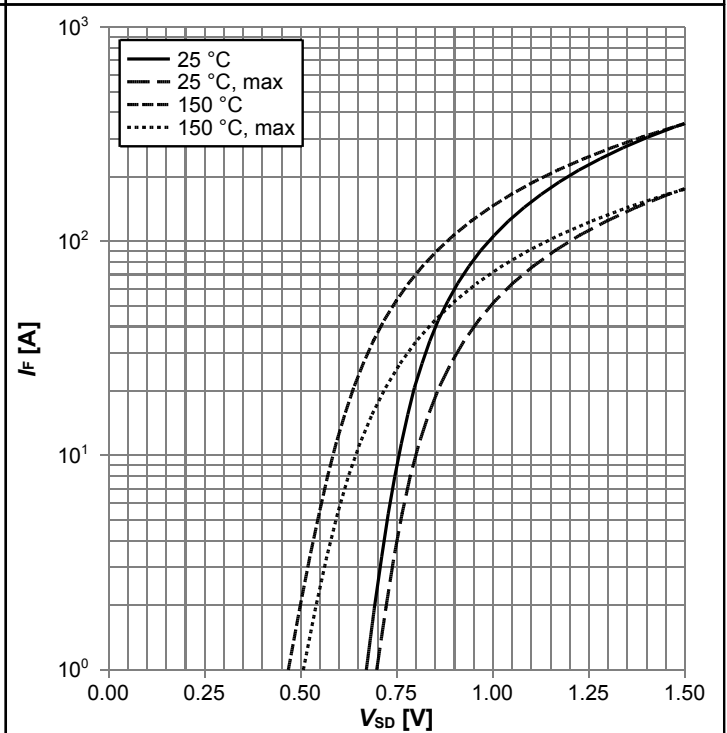
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



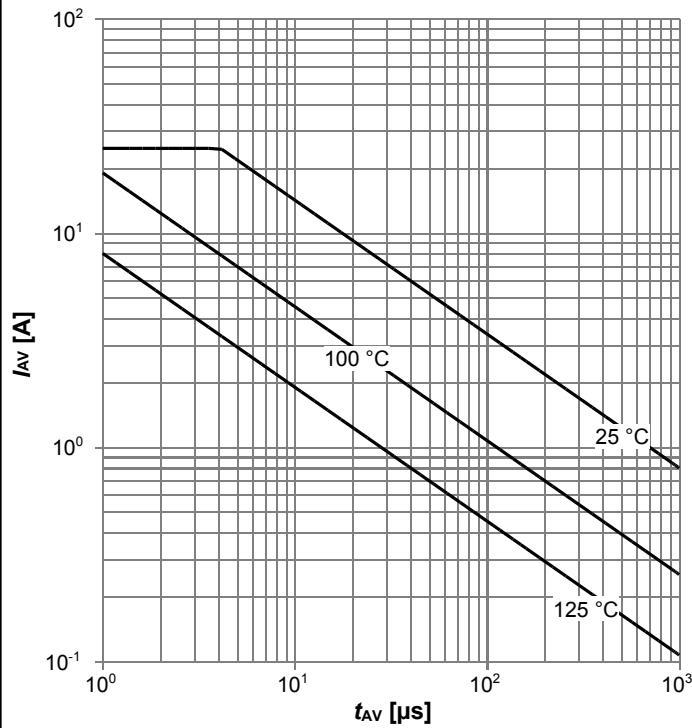
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode



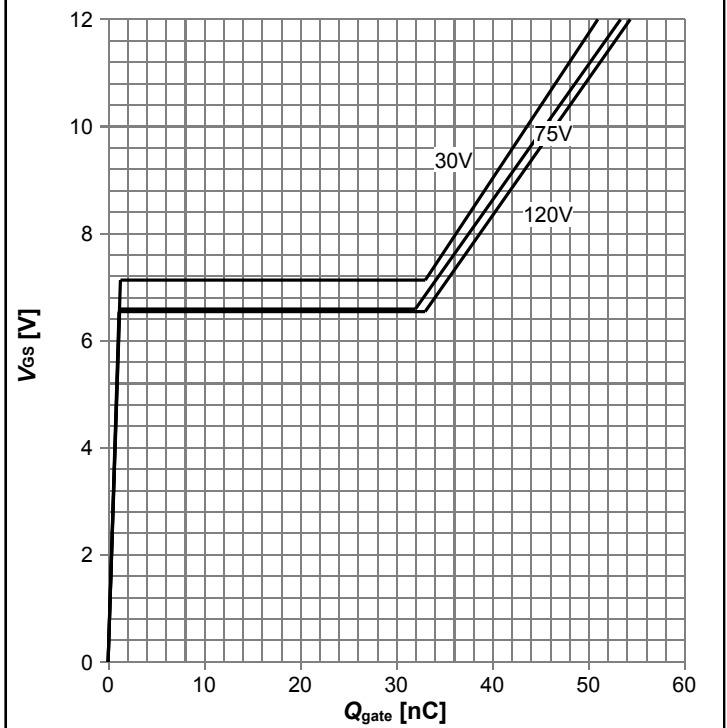
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



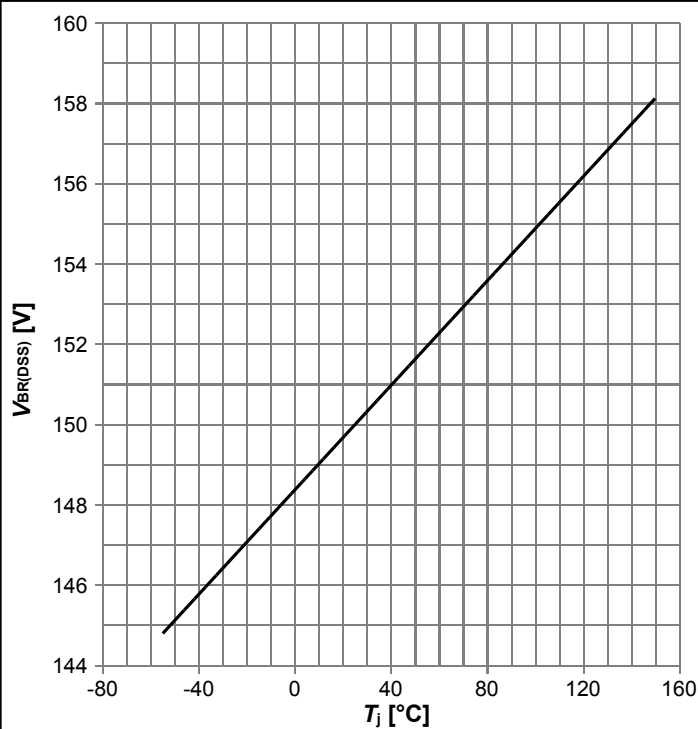
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



$V_{GS}=f(Q_{gate}); I_D=52 \text{ A}$ pulsed, resistive load; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Gate charge waveforms



5 Package Outlines



Figure 1 Outline PG-TO 263-3, dimensions in mm/inches

Revision History

IPB083N15N5LF

Revision: 2017-04-04, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2017-04-04	Release of final version

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