

# BGS18GA14

SP8T Diversity Antenna Switch with GPIO Interface

## Data Sheet

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Page	Subjects (major changes since last revision)
12	Carrier tape drawing updated

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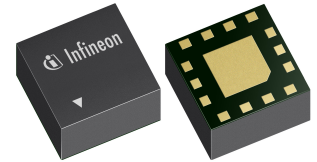
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# BGS18GA14

## 1 Features

- 8 high-linearity, interchangeable RX ports
- Low insertion loss
- Low harmonic generation
- High port-to-port-isolation
- Suitable for Edge / C2K / LTE / WCDMA Applications
- 0.1 to 3.8 GHz coverage
- No decoupling capacitors required if no DC applied on RF lines
- On chip control logic including ESD protection
- General Purpose Input-Output (GPIO) Interface
- Small form factor 2.0 mm x 2.0 mm
- No power supply blocking required
- High EMI robustness
- RoHS and WEEE compliant package



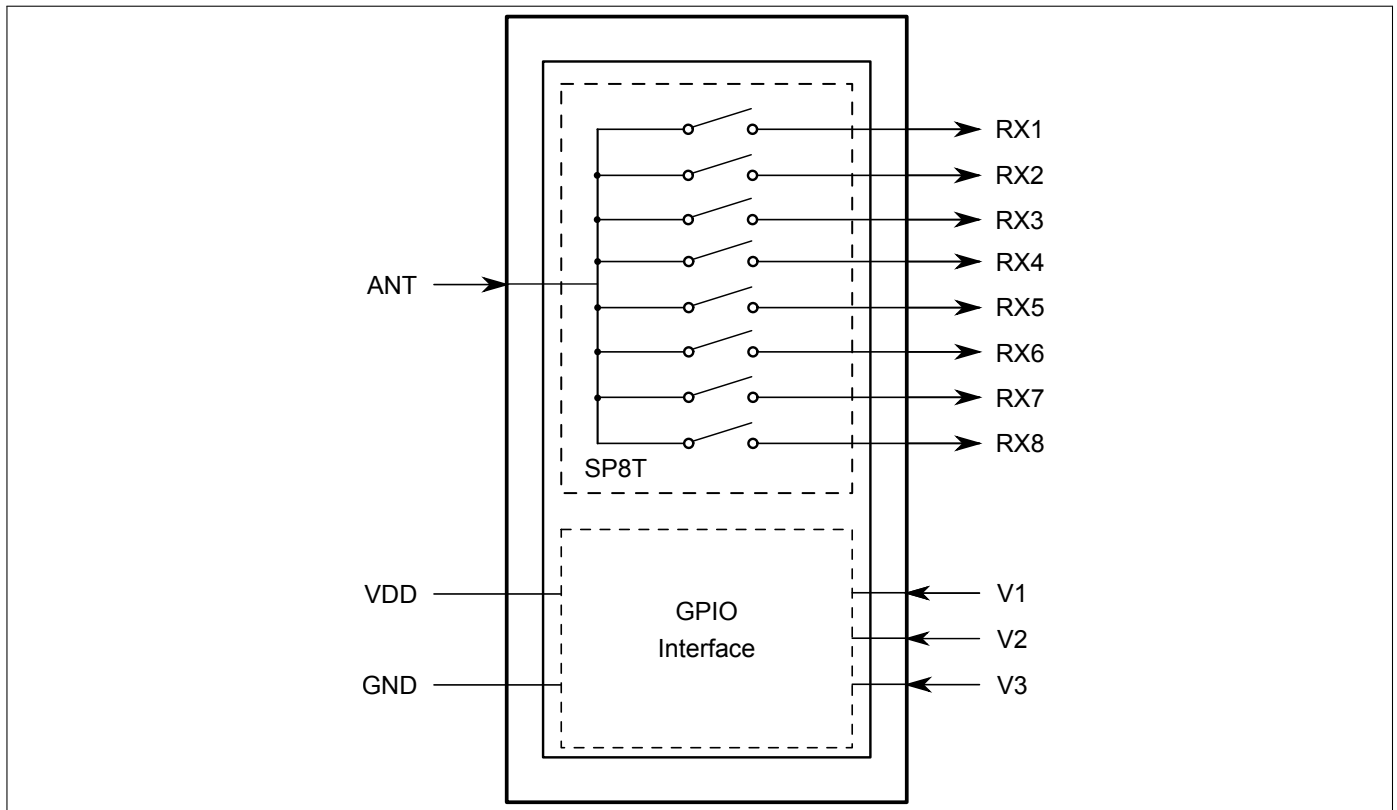
## 2 Product Description

The BGS18GA14 is a Single Pole Eight Throw (SP8T) Diversity Switch Module optimized for wireless applications up to 3.8 GHz. As part of a pin- and functional-compatible SP3T-SP8T product family it has been designed to meet the requirements of chipset reference designs. The module comes in a miniature ATSLP package and comprises of a high power CMOS SP8T switch with integrated GPIO interface. This RF switch is a perfect solution for multimode handsets based on LTE and WCDMA. The switch device configuration is shown in Fig. 1.

The switch is controlled via a GPIO interface. It features DC-free RF ports and unlike GaAs technology, external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally.

**Table 1: Ordering Information**

Type	Package	Marking
BGS18GA14	ATSLP-14	G8


**Figure 1:** BGS18GA14 block diagram

### 3 Maximum Ratings

**Table 2: Maximum Ratings, Table I** at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	$f$	0.1	–	–	GHz	<sup>1)</sup>
Supply voltage	$V_{dd}$	-0.5	–	3.6	V	–
Storage temperature range	$T_{STG}$	-55	–	150	$^\circ\text{C}$	–
Junction temperature	$T_j$	–	–	125	$^\circ\text{C}$	–
RF input power at all Rx ports	$P_{RF\_Rx}$	–	–	32	dBm	CW
ESD capability, CDM <sup>2)</sup>	$V_{ESDCDM}$	-500	–	+500	V	All pins
ESD capability, HBM <sup>3)</sup>	$V_{ESDHBM}$	-1	–	+1	kV	Digital, digital versus RF
		-1	–	+1	V	RF
ESD capability, system level <sup>4)</sup>	$V_{ESDANT}$	-8	–	+8	kV	ANT versus system GND, with 27 nH shunt inductor

<sup>1)</sup> There is also a DC connection between switched paths. The DC voltage at RF ports  $V_{RFDC}$  has to be 0V.

<sup>2)</sup> Field-Induced Charged-Device Model JESD22-C101. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.

<sup>3)</sup> Human Body Model ANSI/ESDA/JEDEC JS-001-2012 ( $R = 1.5\text{ k}\Omega$ ,  $C = 100\text{ pF}$ ).

<sup>4)</sup> IEC 61000-4-2 ( $R = 330\text{ }\Omega$ ,  $C = 150\text{ pF}$ ), contact discharge.

**Table 3: Maximum Ratings, Table II** at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction - soldering point	$R_{thJS}$	–	60	–	K/W	–
Maximum DC-voltage on RF-Ports and RF-Ground	$V_{RFDC}$	0	–	0	V	No DC voltages allowed on RF-Ports
GPIO control voltage levels	$V_{Ctrlx}$	-0.7	–	$V_{dd}+0.7$	V	–

## 4 Operation Ranges

**Table 4: Operation Ranges**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{dd}$	2.4	3.0	3.4	V	–
Supply current	$I_{dd}$	–	75	175	$\mu\text{A}$	–
GPIO control voltage high	$V_{Ctrl\_H}$	1.35	–	$V_{dd}$	V	–
GPIO control voltage low	$V_{Ctrl\_L}$	0	–	0.45	V	–
GPIO control input capacitance	$C_{Ctrl}$	–	–	2	pF	–
Ambient temperature	$T_A$	-30	25	85	$^\circ\text{C}$	–

**Table 5: RF Input Power**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rx ports ( $50\ \Omega$ )	$P_{RF\_Rx}$	–	–	28	dBm	–

## 5 RF Characteristics

**Table 6: RF Characteristics** at  $T_A = -30\text{ }^{\circ}\text{C} \dots 85\text{ }^{\circ}\text{C}$ ,  $P_{IN} = 0\text{ dBm}$ , Supply Voltage  $V_{dd} = 2.4\text{ V} \dots 3.4\text{ V}$ , unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
<b>Insertion Loss<sup>1)</sup></b>						
All Rx Ports	IL	–	0.27	0.35	dB	698–960 MHz
		–	0.42	0.56	dB	1428–1990 MHz
		–	0.48	0.58	dB	1920–2170 MHz
		–	0.56	0.62	dB	2170–2690 MHz
		–	0.69	0.75	dB	3400–3600 MHz
		–	0.74	0.80	dB	3600–3800 MHz
<b>Return Loss<sup>1)</sup></b>						
All Rx Ports	RL	20	24	–	dB	698–960 MHz
		14	19	–	dB	1428–1990 MHz
		13	17	–	dB	1920–2170 MHz
		12	15	–	dB	2170–2690 MHz
		11	12	–	dB	3400–3600 MHz
		10	11	–	dB	3600–3800 MHz
<b>Isolation<sup>1)</sup></b>						
All Rx Ports	ISO	32	50	–	dB	698–960 MHz
		26	41	–	dB	1428–1990 MHz
		24	39	–	dB	1920–2170 MHz
		22	37	–	dB	2170–2690 MHz
		19	33	–	dB	3400–3600 MHz
		19	32	–	dB	3600–3800 MHz
<b>Harmonic Generation (UMTS Band 1, Band 5)<sup>1)</sup></b>						
2 <sup>nd</sup> harmonic generation	$P_{H2}$	92	105	–	dBc	25 dBm, 50 $\Omega$ , CW mode
3 <sup>rd</sup> harmonic generation	$P_{H3}$	88	96	–	dBc	25 dBm, 50 $\Omega$ , CW mode
<b>Intermodulation Distortion (UMTS Band 1, Band 5)<sup>1)</sup></b>						
2 <sup>nd</sup> order intermodulation	IMD2 low	–	-105	-100	dBm	IMT, US Cell (see Tab. 7)
3 <sup>rd</sup> order intermodulation	IMD3	–	-110	-105	dBm	IMT, US Cell (see Tab. 8)
2 <sup>nd</sup> order intermodulation	IMD2 high	–	-115	-110	dBm	IMT, US Cell (see Tab. 7)
<b>Switching Time</b>						
RF Rise Time	$t_{RT}$	–	–	2	$\mu\text{s}$	10 % to 90 % RF signal
Switching Time	$t_{ST}$	–	2	4	$\mu\text{s}$	50 % Ctrl signal to 90 % RF signal
Power Up Settling Time	$t_{PUP}$	–	10	25	$\mu\text{s}$	After power down mode

<sup>1)</sup>On application board without any matching components.



**Table 7: IMD2 Testcases**

Band	CW tone 1 (MHz)	CW tone 1 (dBm)	CW tone 2 (MHz)	CW tone 2 (dBm)
IMT	1950	20	190 (IMD2 low)	-15
			4090 (IMD2 high)	
US Cell	835	20	45 (IMD2 low)	-15
			1715 (IMD2 high)	

**Table 8: IMD3 Testcases**

Band	CW tone 1 (MHz)	CW tone 1 (dBm)	CW tone 2 (MHz)	CW tone 2 (dBm)
IMT	1950	20	1760	-15
US Cell	835	20	790	-15

## 6 GPIO Specification

**Table 9: Modes of Operation (Truth Table)**

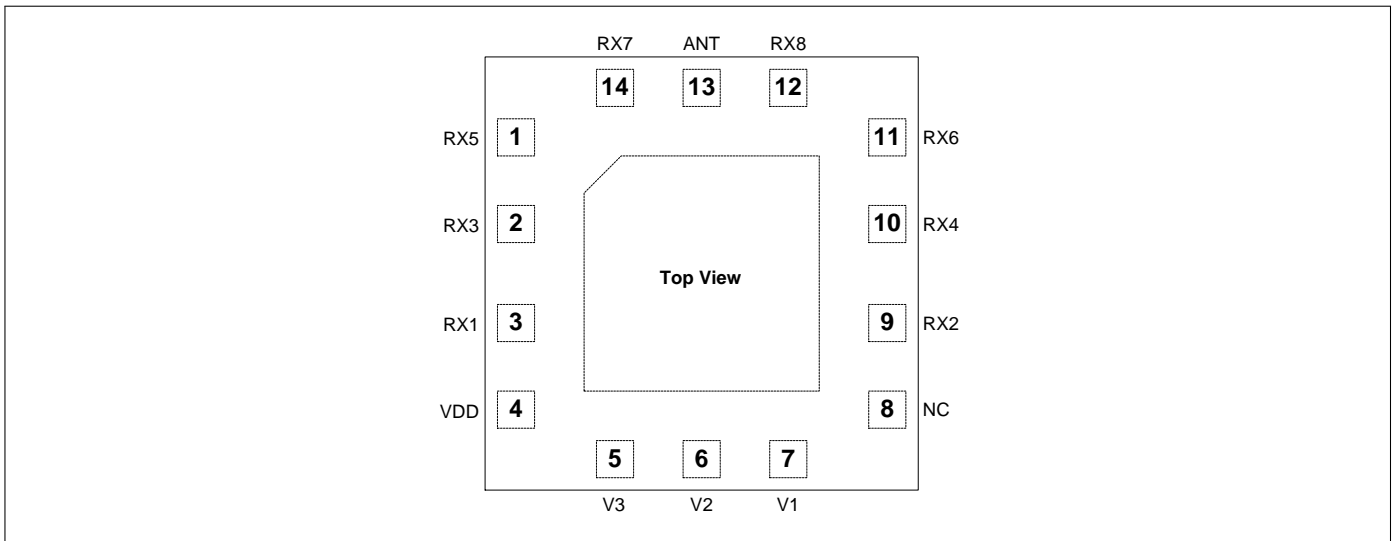
State	Mode	Control Inputs		
		V1	V2	V3
1	RX1-ANT	0	0	0
2	RX2-ANT	0	0	1
3	RX3-ANT	0	1	0
4	RX4-ANT	0	1	1
5	RX5-ANT	1	0	0
6	RX6-ANT	1	0	1
7	RX7-ANT	1	1	0
8	RX8-ANT	1	1	1

## 7 Package related information

The switch has a package size of 2000  $\mu\text{m}$  in x-dimension and 2000  $\mu\text{m}$  in y-dimension with a maximum deviation of  $\pm 50 \mu\text{m}$  in each dimension. Fig. 2 shows the footprint from top view. The definition of each pin can be found in Tab. 11. In addition a recommendation for the land pattern is displayed in Fig. 4 followed by information regarding laser marking (see Fig. 5).

**Table 10: Mechanical Data**

Parameter	Symbol	Value	Unit
Package X-Dimension	X	2000 $\pm$ 50	$\mu\text{m}$
Package Y-Dimension	Y	2000 $\pm$ 50	$\mu\text{m}$
Package Height	H	0.65 max	$\mu\text{m}$


**Figure 2:** Footprint, top view

**Table 11: Pin Definition**

No.	Name	Pin Type	Function
0	GND	GND	RF ground; die pad
1	RX5	I/O	RX port 5
2	RX3	I/O	RX port 3
3	RX1	I/O	RX port 1
4	VDD	PWR	$V_{DD}$ supply
5	V3	I	GPIO control pin
6	V2	I	GPIO control pin
7	V1	I	GPIO control pin
8	NC		Not connected
9	RX2	I/O	RX port 2
10	RX4	I/O	RX port 4
11	RX6	I/O	RX port 6
12	RX8	I/O	RX port 8
13	ANT	I/O	Antenna port
14	RX7	I/O	RX port 7



Figure 3: Package Outline Drawing

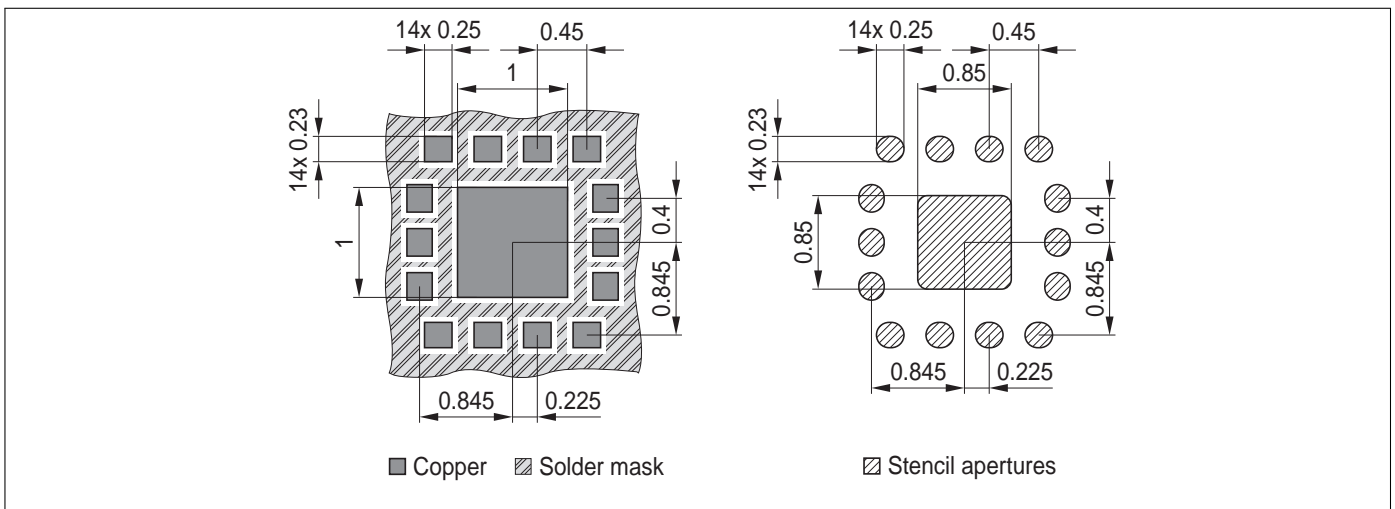
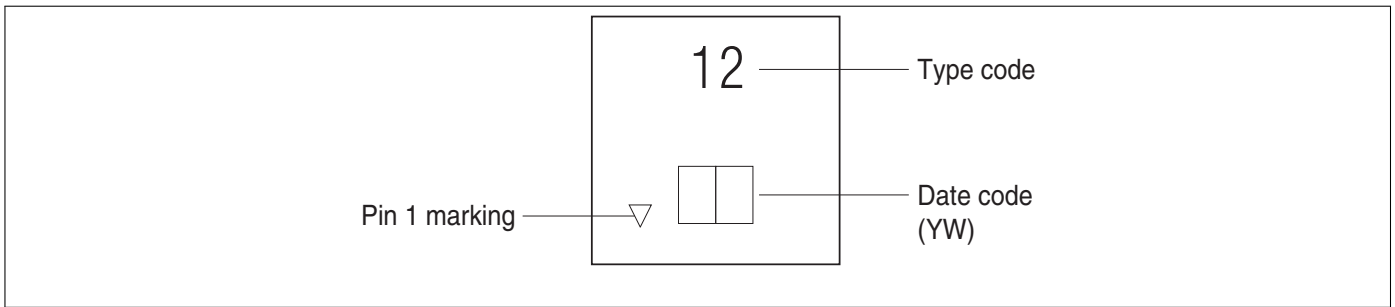
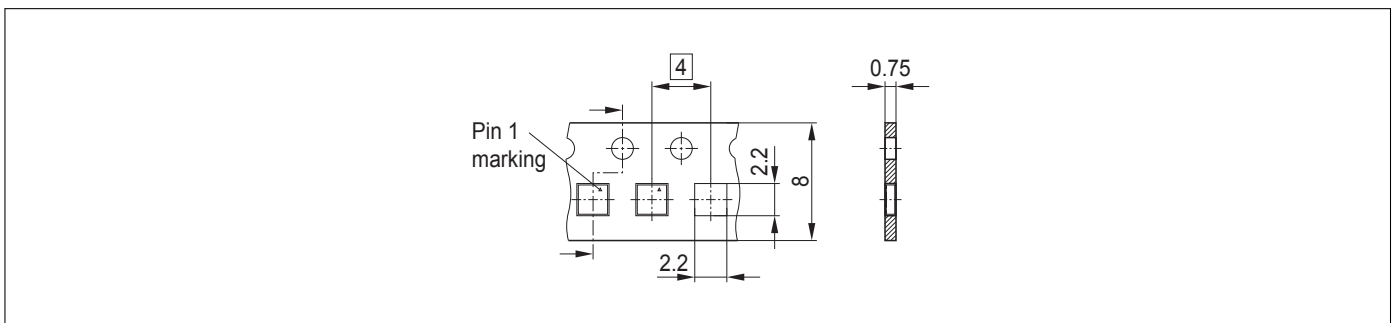


Figure 4: Land Pattern Drawing



**Figure 5:** Laser marking



**Figure 6:** Carrier Tape

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