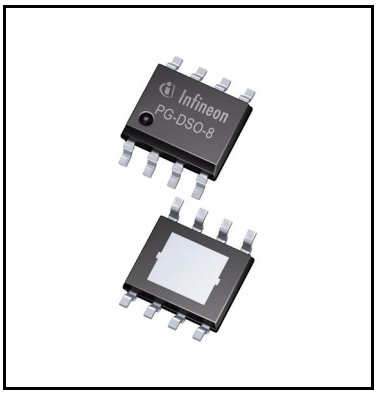
# OPTIREG™ Linear TLE4263-2ES

## 5 V low drop voltage regulator




## Features

- Output voltage tolerance ≤ ±2%
- 180 mA output current capability
- Low-drop voltage
- Very low standby current consumption
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Adjustable reset threshold
- Watchdog for monitoring microprocessor
- Power-on and undervoltage reset with programmable delay time
- Reset low down to $V_Q$ = 1V
- Wide temperature range
- Exposed pad package with excellent thermal behavior
- Suitable for use in automotive electronics
- Green Product (RoHS compliant)

## Potential applications

General automotive applications.

## Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

## Description

The OPTIREG™ Linear TLE4263-2ES is a monolithic integrated very low dropout voltage regulator in a SMD package PG-DSO-8 exposed pad, especially designed for automotive applications. An input voltage up to 45 V is regulated to an output voltage of 5.0 V. The component is able to drive loads up to 180 mA. The IC is short-circuit proof by the implemented current limitation and has an integrated overtemperature shutdown.

It additionally provides features like power-on and undervoltage reset with adjustable reset threshold, a watchdog circuit for monitoring a connected microcontroller and an inhibit input for enabling or disabling the component.

The reset output RO is set to “low” in case the output voltage falls below the reset switching threshold VQ,rt. This threshold can be decreased down to 3.5 V by an external resistor divider. The power-on reset delay time can be programmed by the external delay capacitor CD.

The watchdog circuit provides a monitoring function for microcontrollers: At missing pulses on the watchdog’s input W the reset output RO is set to “low”. The trigger time for the watchdog pulses can be set by the external capacitor CD.

The IC can be switched off by the inhibit input, reducing the current consumption to typically 0 mA.

| Type | Package | Marking |
|---|---|---|
| TLE4263-2ES | PG-DSO-8 exposed pad | 4263-2 |

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# 1 Block diagram

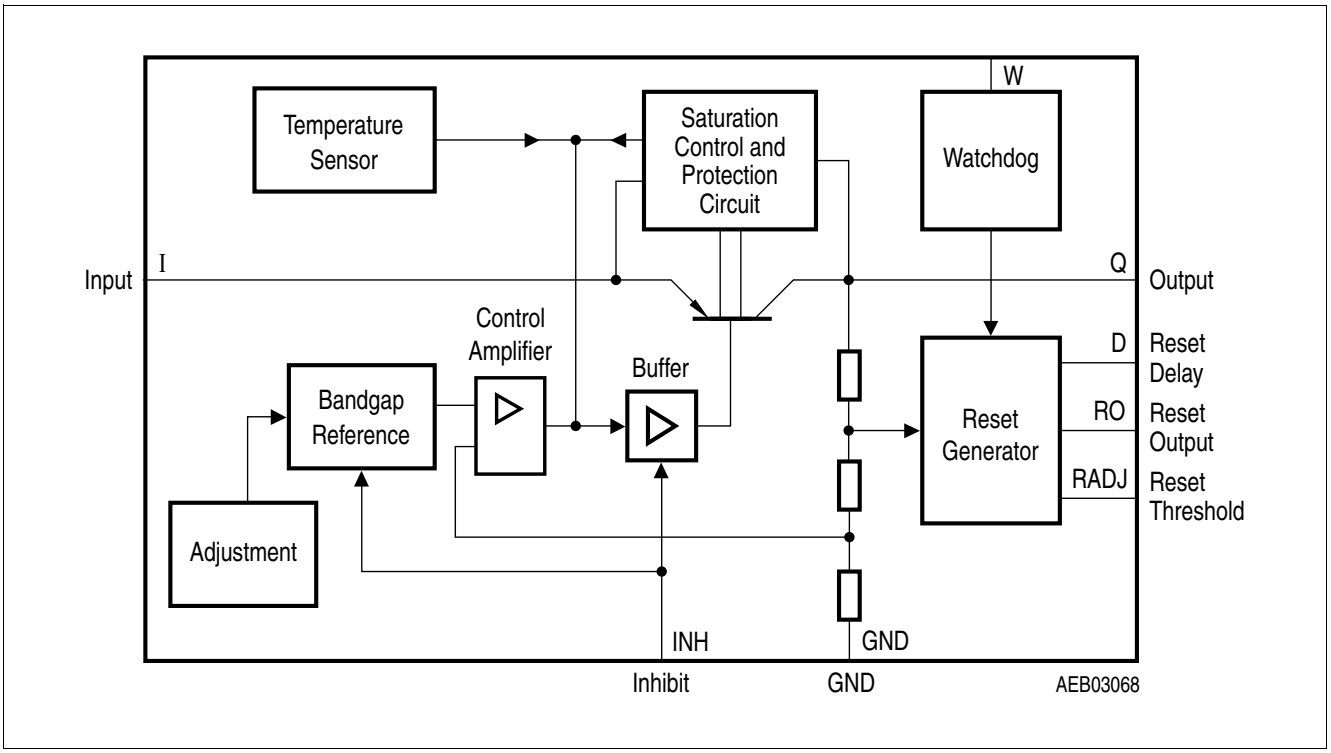



**Figure 1 Block diagram**

# 2 Pin configuration

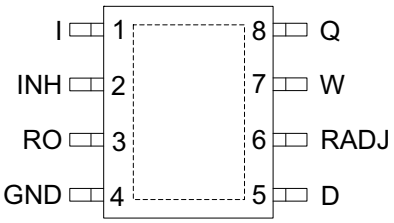



**Figure 2 Pin configuration** (top view)

**Table 1 Pin definition and functions**

| Pin | Symbol | Function |
|---|---|---|
| 1 | I | **Input**<br>for compensating line influences, a capacitor to GND close to the IC terminals is recommended |
| 2 | INH | **Inhibit**<br>enables/disables the device;<br>connect to I if the this function is not needed |
| 3 | RO | **Reset Output**<br>open-collector output connected to the output via an internal 30kΩ pull-up resistor;<br>leave open if the this function is not needed |
| 4 | GND | **Ground** |
| 5 | D | **Reset Delay Timing**<br>connect a ceramic capacitor to GND for adjusting the reset delay time / watchdog trigger time;<br>leave open if this function is not needed |
| 6 | RADJ | **Reset Threshold Adjust**<br>connect an external voltage divider to adjust the reset switching threshold;<br>connect to GND for using internal threshold |
| 7 | W | **Watchdog**<br>rising edge triggered input for monitoring a microcontroller;<br>connect to GND if this function is not needed |
| 8 | Q | **Output**<br>block to ground with a capacitor close to the IC terminals with a capacitance value $C \geq 22\ \mu F$, $ESR \leq 3\ \Omega$ |
| PAD | – | **Exposed Pad**<br>attach the exposed pad on package bottom to the heatsink area on circuit board;<br>connect to GND |

# 3 General product characteristics

## 3.1 Absolute maximum ratings

**Table 2 Absolute maximum ratings[1)]**

$T_j$ = -40°C to +150°C; all voltages with respect to ground (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Input I** | | | | | | | |
| Input voltage<br>Input current | $V_I$<br>$I_I$ | - 42<br>– | –<br>– | 45<br>– | V<br>– | –<br>Internally limited | P_3.1.1 |
| **Reset output RO** | | | | | | | |
| Input voltage<br>Input current | $V_{RO}$<br>$I_{RO}$ | - 0.3<br>– | –<br>– | 42<br>– | V<br>– | –<br>Internally limited | P_3.1.2 |
| **Reset threshold RADJ** | | | | | | | |
| Voltage | $V_{RADJ}$ | - 0.3 | – | 6 | V | – | P_3.1.3 |
| **Reset delay D** | | | | | | | |
| Voltage<br>Current | $V_D$<br>$I_D$ | - 0.3<br>– | –<br>– | 42<br>– | V<br>– | –<br>Internally limited | P_3.1.4 |
| **Output Q** | | | | | | | |
| Voltage<br>Current | $V_Q$<br>$I_Q$ | 0.30<br>– | –<br>– | 7.0<br>– | V<br>– | –<br>Internally limited | P_3.1.5 |
| **Inhibit INH** | | | | | | | |
| Input voltage<br>Input current | $V_{INH}$<br>$I_{INH}$ | -42<br>– | –<br>– | 45<br>– | V<br>– | –<br>Internally limited | P_3.1.6 |
| **Watchdog W** | | | | | | | |
| Voltage | $V_W$ | -0.3 | – | 6 | V | – | P_3.1.7 |
| **Ground GND** | | | | | | | |
| Current | $I_{GND}$ | -0.5 | – | – | A | – | P_3.1.8 |
| **Temperature** | | | | | | | |
| Junction temperature<br>Storage temperature | $T_j$<br>$T_{stg}$ | –<br>-50 | –<br>– | 150<br>150 | °C<br>°C | –<br>– | P_3.1.9 |
| **ESD susceptibility** | | | | | | | |
| Human body model (HBM) | Voltage | – | – | 2 | kV | 2) | P_3.1.10 |
| Charged device model (CBM) | Voltage | – | – | 1 | kV | 3) | P_3.1.11 |

1) Not subject to production test, specified by design.

2) ESD HBM test according JEDEC JESD22-A114

3) ESD CDM test according AEC/ESDA ESD-STM5 3.1-1999

**Notes**

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 3.2 Functional range

**Table 3 Functional range**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Input voltage | $V_I$ | 5.5 | – | 45 | V | 1) | P_3.2.1 |
| Junction temperature | $T_j$ | -40 | – | 150 | °C | – | P_3.2.2 |

1) Corresponds with characteristics of drop voltage, output current and power description (see diagrams).

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 3.3 Thermal resistance

**Table 4 Thermal resistance**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Junction to case | $R_{thJC}$ | – | 10 | – | K/W | 1) measured to exposed pad | P_3.3.1 |
| Junction to ambient | $R_{thJA}$ | – | 45 | – | K/W | 2) | P_3.3.2 |
| Junction to ambient | $R_{thJA}$ | – | 153 | – | K/W | footprint only 3) | P_3.3.3 |
| Junction to ambient | $R_{thJA}$ | – | 64 | – | K/W | 300 mm² heatsink area 2) | P_3.3.4 |
| Junction to ambient | $R_{thJA}$ | – | 55 | – | K/W | 600 mm² heatsink area 2) | P_3.3.5 |

1) Not subject to production test, specified by design

2) Specified $R_{thJA}$ value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified $R_{thJA}$ value is according to Jedec JESD 51-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 × 70 µm Cu).

# 4 Functional description

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The component also has a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity

In case the externally scaled down output voltage at the reset adjust input falls below 1.35 V, the external reset delay capacitor CD is discharged by the reset generator. When the voltage of the capacitor reaches the lower threshold VDRL, a reset signal occurs at the reset output and is held until the upper threshold VDU is exceeded. If the reset threshold input is connected to GND, reset is triggered at an output voltage of typically 4.65 V.

## 4.1 Choosing external components

The input capacitor $C_I$ is necessary for compensation of line influences. Using a resistor of approx. 1 Ω in series with $C_I$, the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor is necessary for the stability of the regulating circuit. Stability is ensured at values $C_Q \geq 22$ µF and an ESR of ≤ 3 Ω within the operating temperature range. For small tolerances of the reset delay the spread of the capacitance of the delay capacitor and its temperature coefficient should be noted.

## 4.2 Electrical characteristics

**Table 5 Electrical characteristics**

$V_I$ = 13.5 V; $V_{INH}$ > 3.6 V $T_j$ = -40°C to +150°C ; (unless specified otherwise)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Normal Operation** | | | | | | | |
| Output voltage | $V_Q$ | 4.90 | 5.00 | 5.10 | V | 5 mA ≤ $I_Q$ ≤ 150 mA; 6 V ≤ $V_I$ ≤ 28 V | P_4.2.1 |
| Output voltage | $V_Q$ | 4.90 | 5.00 | 5.10 | V | 6 V ≤ $V_I$ ≤ 32 V; $I_Q$ = 100 mA; $T_j$ = 100°C | P_4.2.2 |
| Output current limitation | $I_{Q,max}$ | 180 | 250 | 400 | mA | $V_Q$ = 4.8V | P_4.2.3 |
| Current consumption; $I_q = I_I - I_Q$ | $I_q$ | – | 0 | 10 | µA | $V_{INH}$ = 0 V; $T_J$ ≤ 115°C | P_4.2.4 |
| Current consumption; $I_q = I_I - I_Q$ | $I_q$ | – | 0.90 | 1.30 | mA | $I_Q$ = 0 mA | P_4.2.5 |
| Current consumption; $I_q = I_I - I_Q$ | $I_q$ | – | 10 | 18 | mA | $I_Q$ = 150 mA | P_4.2.6 |
| Current consumption; $I_q = I_I - I_Q$ | $I_q$ | – | 15 | 24 | mA | $I_Q$ = 150 mA; $V_I$ = 4.5 V | P_4.2.7 |
| Dropout voltage | $V_{dr}$ | – | 0.35 | 0.50 | V | $I_Q$ = 150 mA [1)] | P_4.2.8 |
| Load regulation | $\Delta V_{Q,lo}$ | – | – | 25 | mV | $I_Q$ = 5 mA to 150 mA | P_4.2.9 |

**Table 5 Electrical characteristics** (cont'd)

$V_I$ = 13.5 V; $V_{INH}$ > 3.6 V $T_j$ = -40°C to +150°C ; (unless specified otherwise)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Line regulation | $\Delta V_{Q,li}$ | – | 3 | 25 | mV | $V_I$ = 6 V to 28 V; $I_Q$ = 150 mA | P_4.2.10 |
| Power supply ripple rejection | *PSRR* | – | 54 | – | dB | [2] $f_r$ = 100 Hz; $V_r$ = 0.5 Vpp | P_4.2.11 |
| **Reset Generator** | | | | | | | |
| Switching threshold | $V_{Q,rt}$ | 4.5 | 4.65 | 4.8 | V | $V_{RADJ}$ = 0 V | P_4.2.12 |
| Reset adjust threshold | $V_{RADJ,th}$ | 1.26 | 1.36 | 1.44 | V | 3.5V ≤ $V_Q$ < 5 V | P_4.2.13 |
| Reset low voltage | $V_{RO,l}$ | – | 0.10 | 0.40 | V | $I_{RO}$ = 1 mA | P_4.2.14 |
| Saturation voltage | $V_{D,sat}$ | – | 50 | 110 | mV | $V_Q$ < $V_{RAD,th}$ | P_4.2.15 |
| Upper timing threshold | $V_{DU}$ | 1.40 | 1.70 | 2.20 | V | – | P_4.2.16 |
| Lower reset timing threshold | $V_{DRL}$ | 0.20 | 0.35 | 0.59 | V | – | P_4.2.17 |
| Charge current | $I_{D,ch}$ | 40 | 60 | 88 | µA | – | P_4.2.18 |
| Reset delay time | $t_{rd}$ | 1.3 | 2.8 | 4.1 | ms | $C_D$ = 100 nF | P_4.2.19 |
| Reset reaction time | $t_{rr}$ | 0.5 | 1.2 | 4.0 | µs | $C_D$ = 100 nF | P_4.2.20 |
| **Watchdog** | | | | | | | |
| Discharge current | $I_{D,wd}$ | 4.40 | 6.25 | 9.40 | µA | $V_D$ = 1.0 V | P_4.2.22 |
| Upper timing threshold | $V_{DU}$ | 1.40 | 1.70 | 2.20 | V | – | P_4.2.24 |
| Lower timing threshold | $V_{DWL}$ | 0.20 | 0.35 | 0.55 | V | – | P_4.2.25 |
| Watchdog trigger time | $T_{WI,tr}$ | 16 | 22.5 | 27 | ms | $C_D$ = 100 nF $V_Q$ > $V_{Q,RT}$ | P_4.2.26 |
| Watchdog output low time | $T_{WD,L}$ | 1.0 | 2.10 | 3.50 | ms | $C_D$ = 100 nF $V_Q$ > $V_{Q,RT}$ | P_4.2.27 |
| Watchdog period $T_{WI,p}$ = $T_{WD,L}$ + $T_{WI,tr}$ | $T_{WD,p}$ | 17 | 24.6 | 30.5 | ms | $C_D$ = 100 nF $V_Q$ > $V_{Q,RT}$ | P_4.2.28 |
| **Inhibit** | | | | | | | |
| Switching voltage | $V_{INH,ON}$ | 3.6 | – | – | V | IC turned on | P_4.2.29 |
| Turn-OFF voltage | $V_{INH,OFF}$ | – | – | 0.8 | V | IC turned off | P_4.2.30 |
| Input current | $I_{INH}$ | 5 | 10 | 27 | µA | $V_{INH}$ = 5 V | P_4.2.31 |

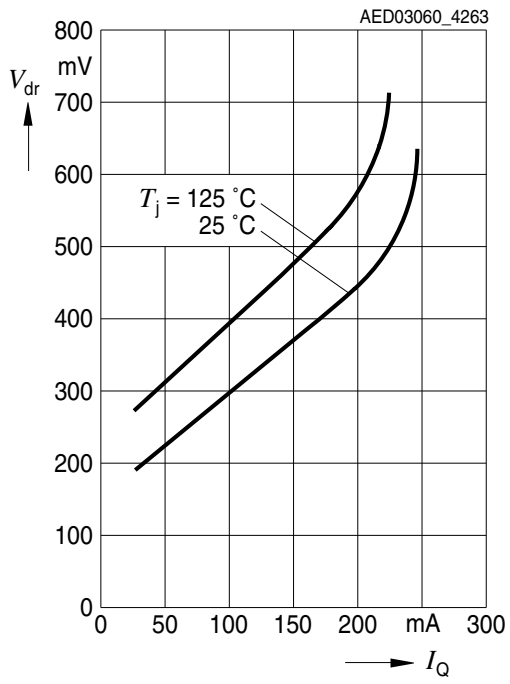
1) Drop voltage = $V_i$ - $V_Q$ (measured when the output voltage has dropped 100 mV from the nominal value obtained at 6 V input).

2) Not subject to production test, specified by design.

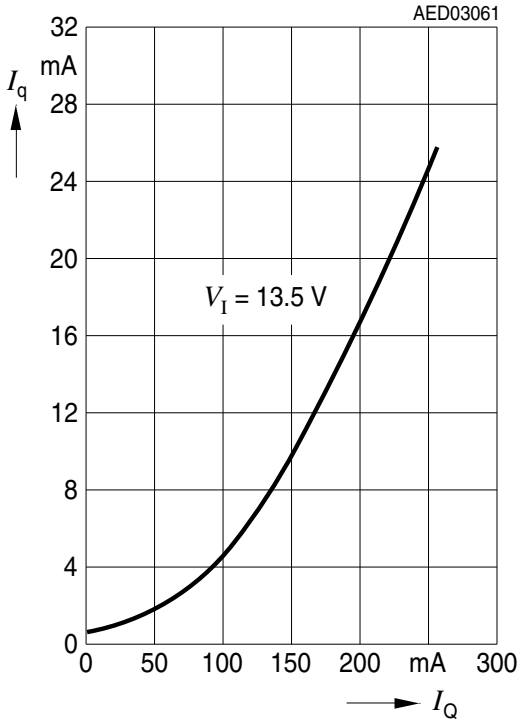
*Note: The reset output is "low" within the range $V_Q$ = 1 V to $V_{Q,rt}$.*

## 4.3 Typical performance characteristics

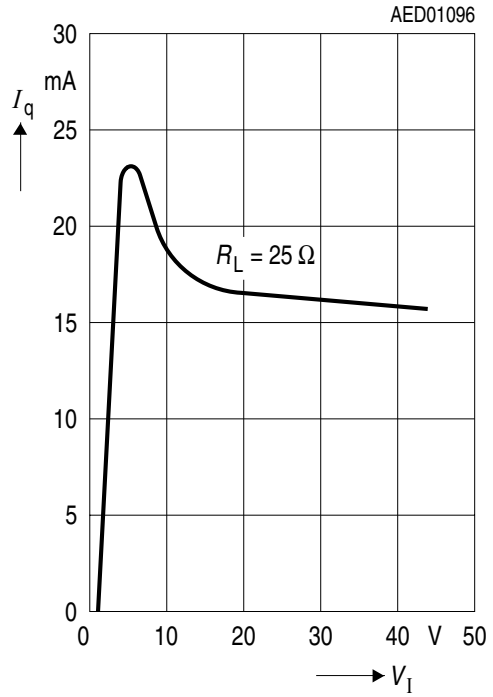
**Drop voltage $V_{DR}$ versus output current $I_Q$**



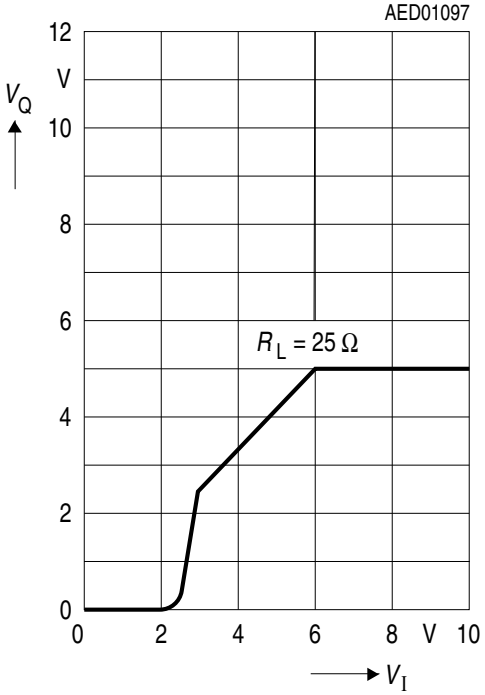

**Current consumption $I_q$ versus output current $I_Q$**



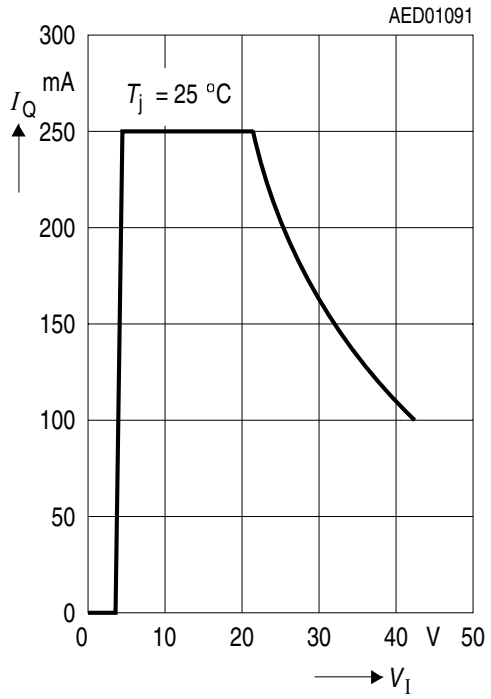

**Current consumption $I_q$ versus input voltage $V_I$**



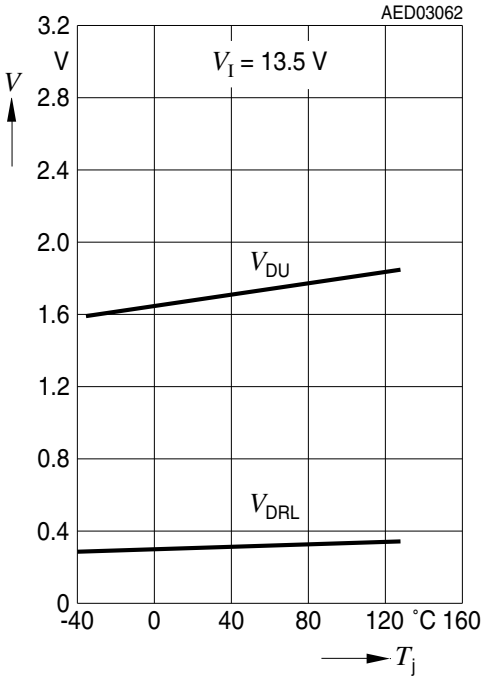

**Output voltage $V_Q$ versus input voltage $V_I$**



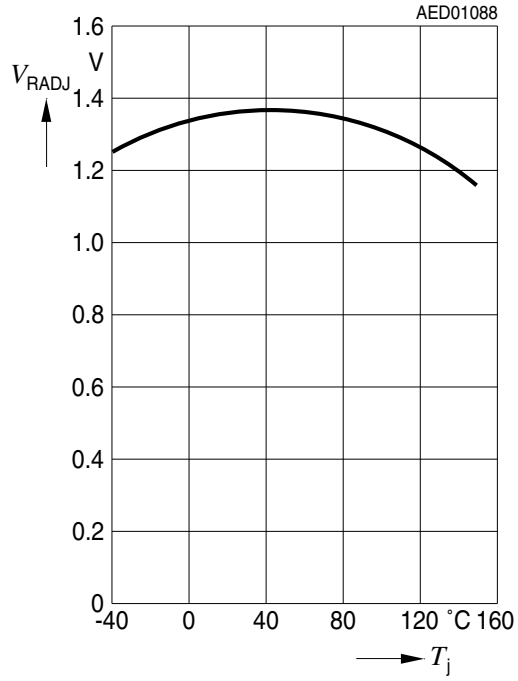
### Output current $I_Q$ versus input voltage $V_I$



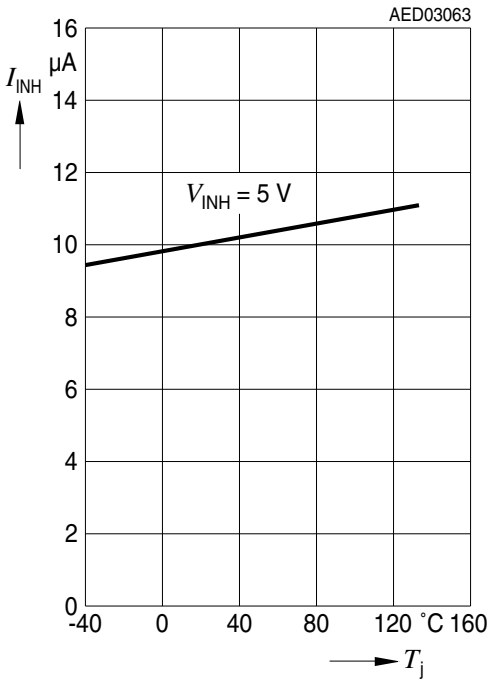

### Timing threshold voltage $V_{DU}$ and $V_{DRL}$ versus junction temperature $T_J$



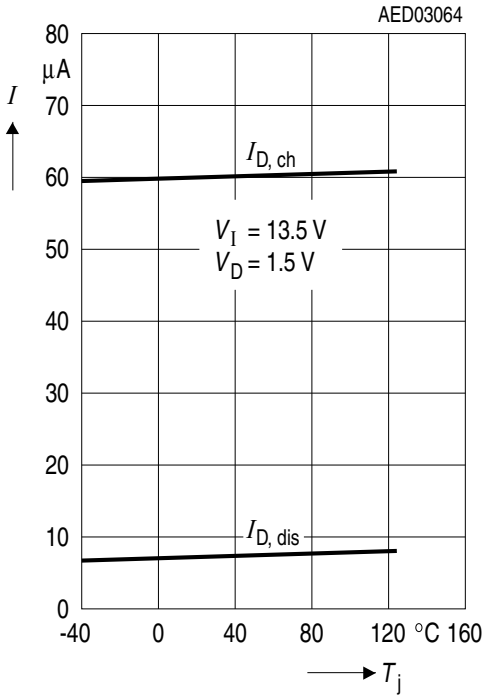

### Reset switching threshold $V_{RADJ}$ versus junction temperature $T_J$



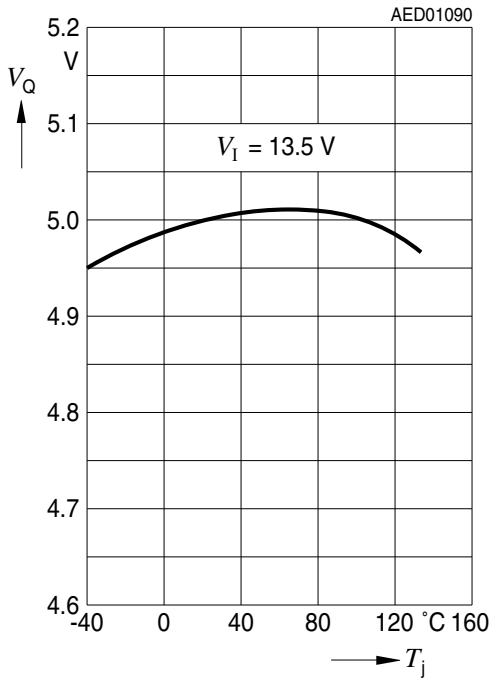

### Current consumption of inhibit $I_{INH}$ versus junction temperature $T_J$



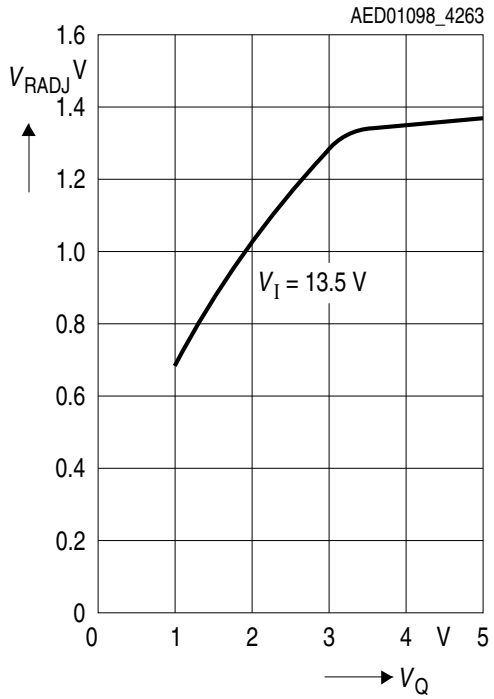
### Charge current and discharge current $I_{D,ch}$ ; $I_{D,dis}$ versus junction temperature $T_J$



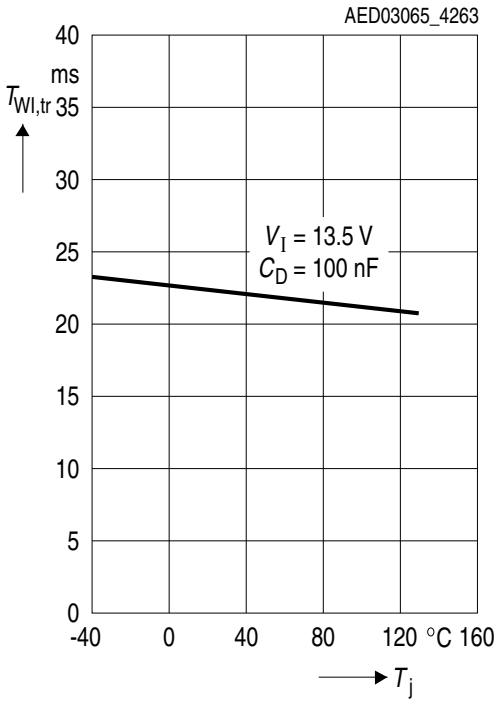

### Output voltage $V_Q$ versus junction temperature $T_J$



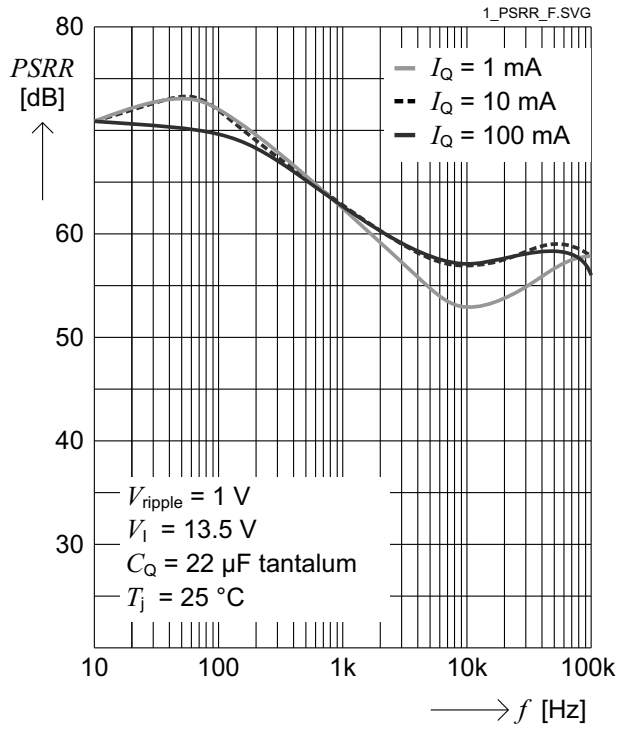
### Undervoltage reset adjust threshold $V_{RADJ}$ versus output voltage $V_Q$



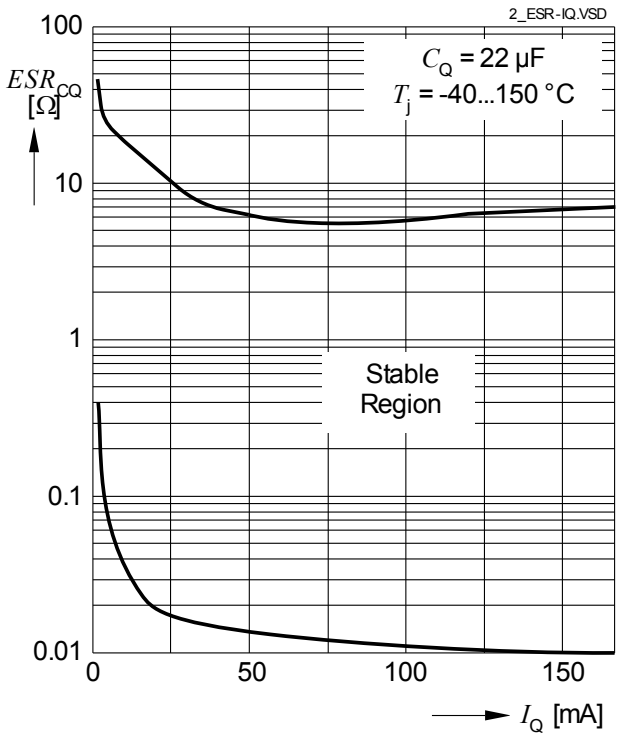

### Pulse time $T_{WI,tr}$ versus junction temperature $T_J$




### Power supply ripple rejection *PSRR* versus ripple frequency $f_r$




### Output capacitor series resistor *ESR* $C_Q$ versus output current $I_Q$



# 5 Application information

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality condition or quality of the device.*

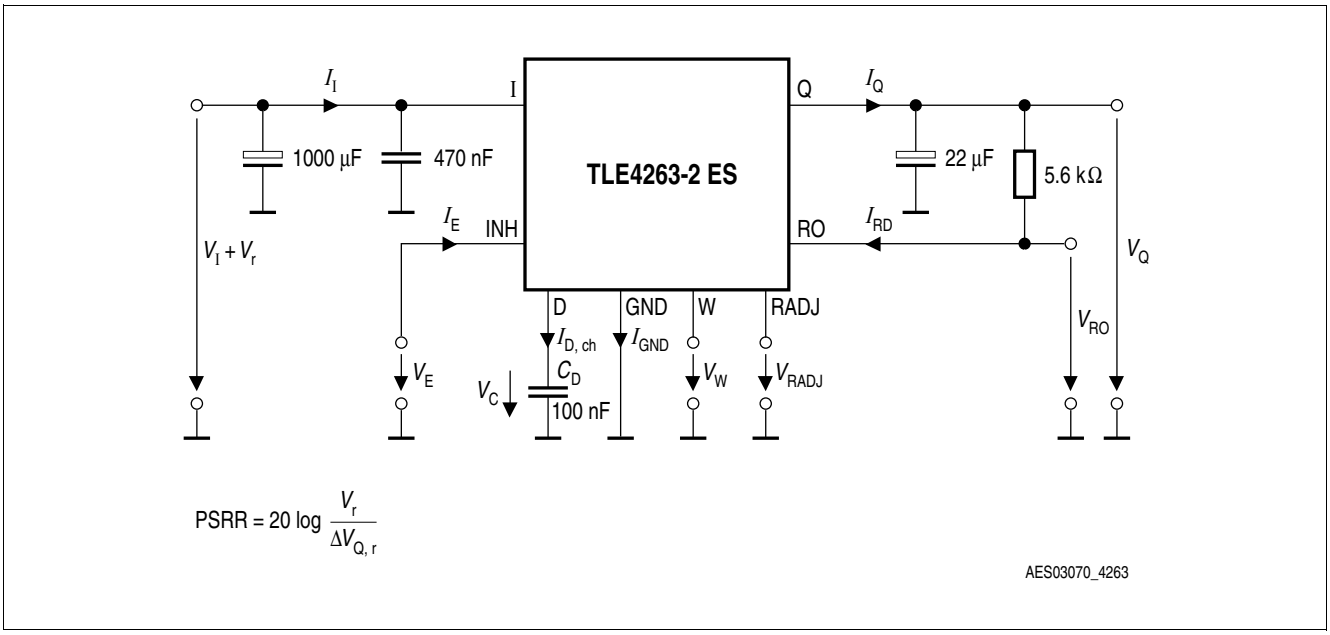



**Figure 3 Application circuit**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

## 5.1 Reset

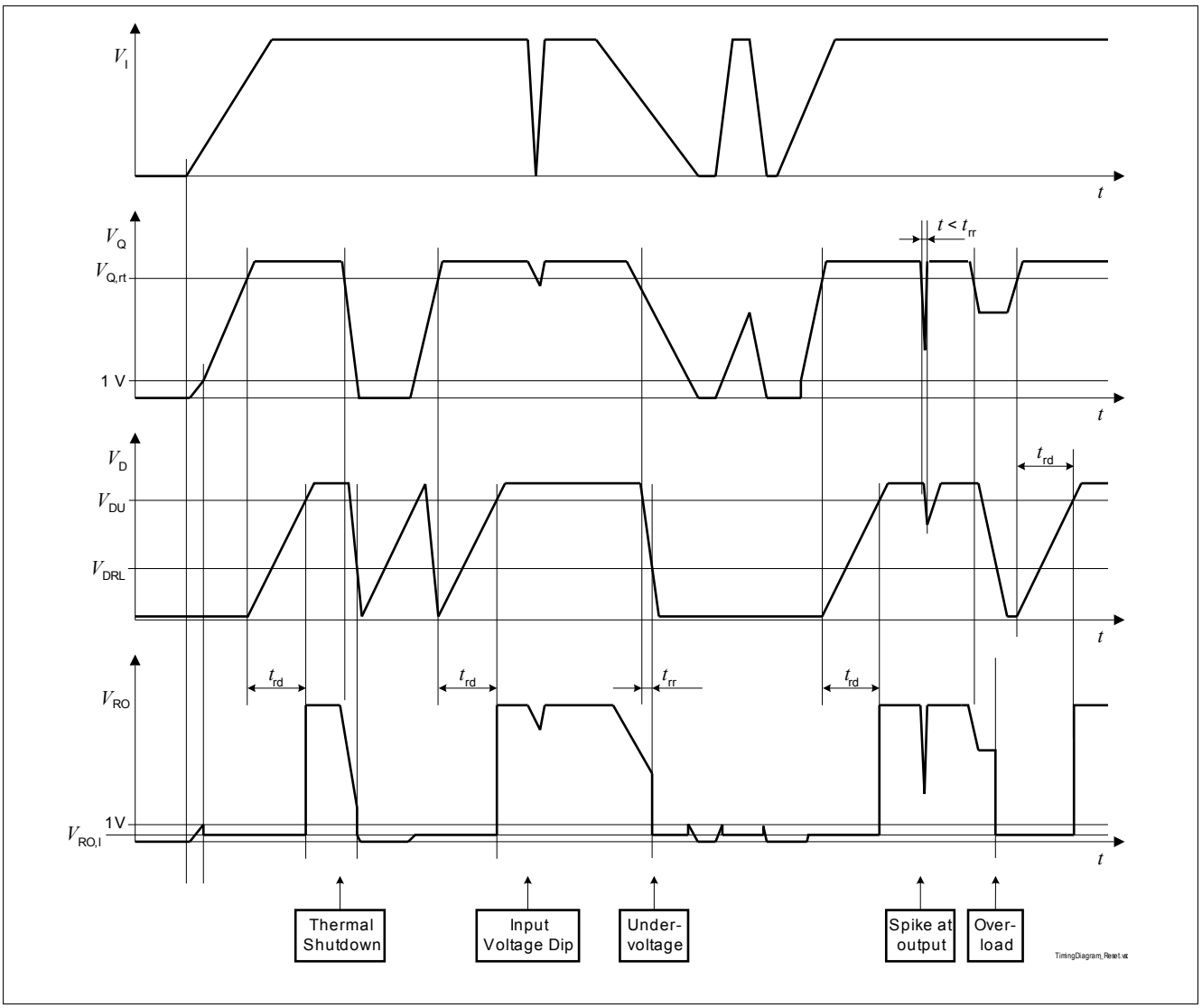



**Figure 4 Reset timing diagram**

## 5.2 Power-on reset delay time

If the application needs a power-on reset delay time $t_{rd}$ different from the value given in **"Reset Generator" on Page 9**, the delay capacitor's value can be derived from these specified values and the desired power-on delay time:

$$C_D = \frac{t_{rd,new}}{t_{rd}} \times 100nF \quad (5.1)$$

with:

- $C_D$: capacitance of the delay capacitor to be chosen
- $t_{rd,new}$: desired power-on reset delay time
- $t_{rd}$: power-on reset delay time specified in this datasheet

For a precise calculation also take the delay capacitor's tolerance into consideration.

## 5.3 Reset adjust function

The undervoltage reset switching threshold can be adjusted according to the application's needs by connecting an external voltage divider ($R_{ADJ1}$, $R_{ADJ2}$) at pin RADJ. For selecting the default threshold connect pin RADJ to GND.

When dimensioning the voltage divider, take into consideration that there will be an additional current constantly flowing through the resistors.

With a voltage divider connected, the reset switching threshold $V_{RT,new}$ is calculated as follows:

$$V_{RT,\,new} = \frac{R_{ADJ,\,1} + R_{ADJ,\,2}}{R_{ADJ,\,2}} \times V_{RADJ,\,th} \tag{5.2}$$

with

- $V_{RT,new}$: the desired new reset switching threshold
- $R_{ADJ1}$, $R_{ADJ2}$: resistors of the external voltage divider
- $V_{RADJ,th}$: reset adjust switching threshold given in *"Reset Generator" on Page 9*

## 5.4 Watchdog

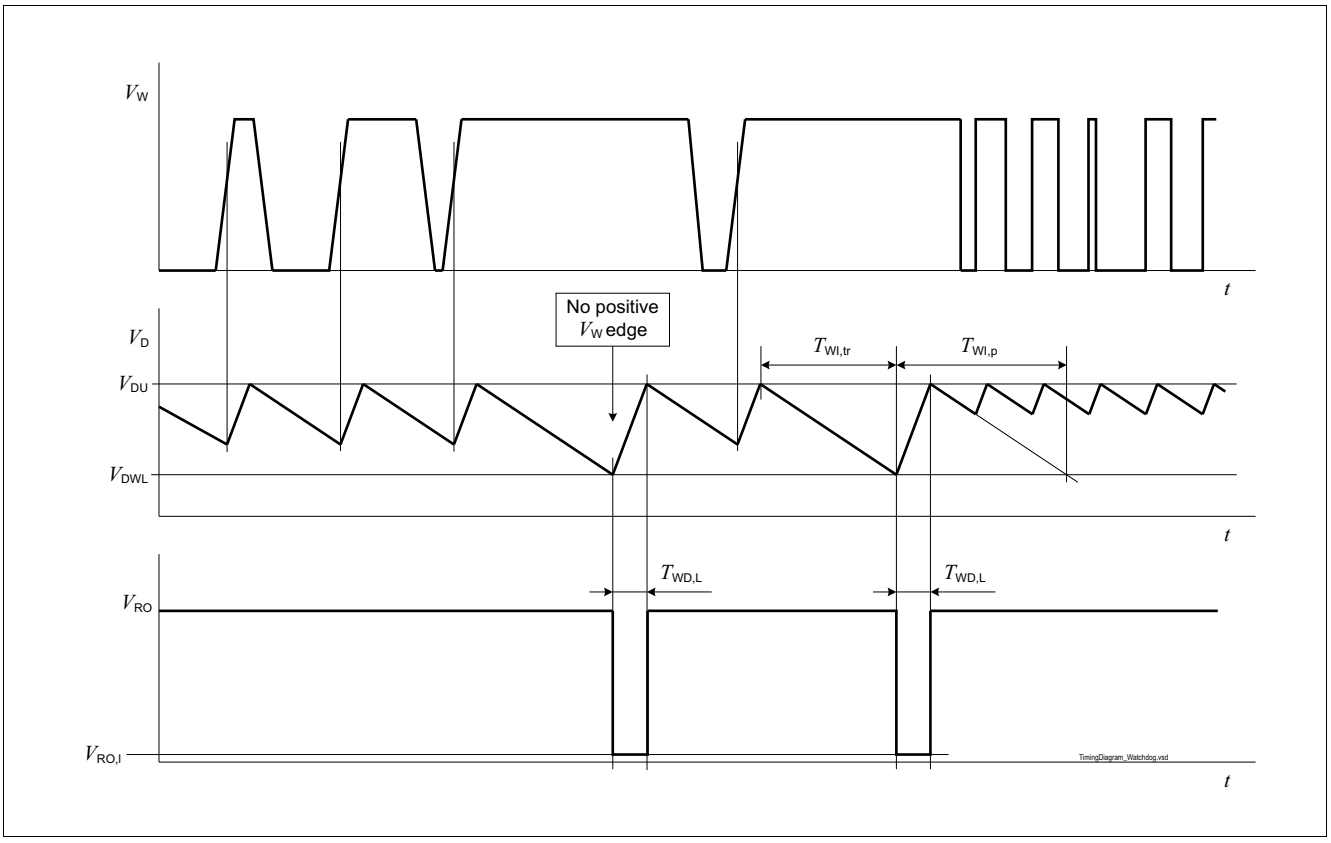



**Figure 5 Timing of the watchdog function reset**

## Application information

### Watchdog timing

The period of the watchdog pulses has to be smaller than the minimum watchdog trigger time which is set by the external reset delay capacitor $C_D$. Use the following formula for dimensioning $C_D$:

$$C_D = \frac{T_{WI,tr,new}}{T_{WI,tr}} \times 100\ nF \quad (5.3)$$

with

- $C_D$: capacitance of the delay capacitor to be chosen
- $T_{WI,tr,new}$: desired watchdog trigger time
- $T_{WI,tr}$: watchdog trigger time specified in this data sheet

# 6 Package information

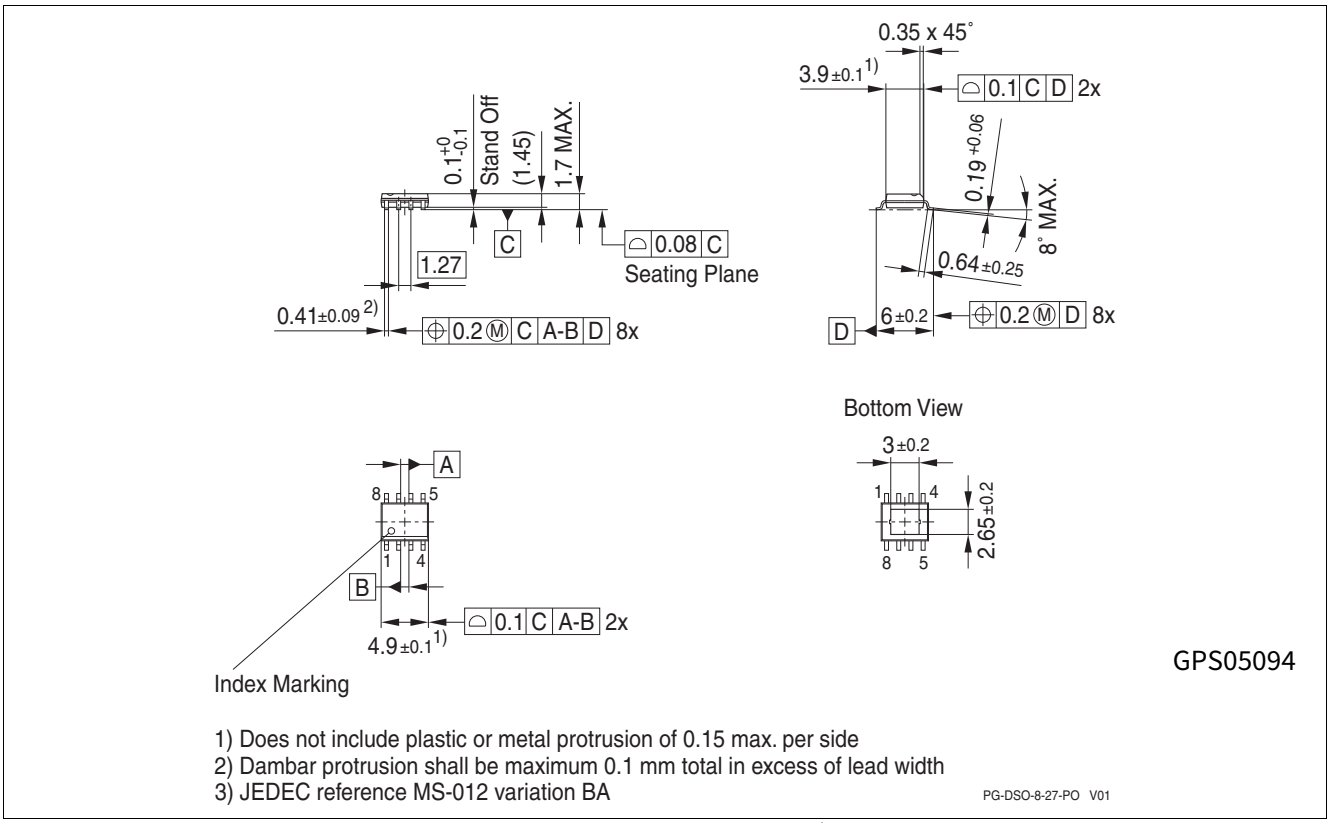



**Figure 6 PG-DSO-8 exposed pad (Plastic Dual Small Outline)[1)]**

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

### Further information on packages

**https://www.infineon.com/packages**

1) Dimension in mm

# 7 Revision history

| Revision | Date | Changes |
|---|---|---|
| 1.11 | 2019-10-21 | Editorial changes |
| 1.1 | 2019-03-27 | Updated layout and structure<br>Editorial changes |
| 1.0 | 2008-04-21 | Initial datasheet |

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**Edition 2019-10-21**
**Published by**
**Infineon Technologies AG**
**81726 Munich, Germany**



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**Document reference**
**Z8F52231382**

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