Angle Sensor

GMR-Based Angular Sensor
for Rotor-Position Sensing

TLE5012

TLE5012-E0318
TLE5012-E0742

Data Sheet

V 1.0, 2010-11
Final

Sensors

Edition 2010-11

Published by
Infineon Technologies AG
81726 Munich, Germany

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TLE5012 GMR-Based Angular Sensor

Revision History: 2010-11, V 1.0

Previous Version: -

Page	Major changes since last revision
general	correction of typing errors

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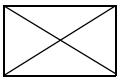
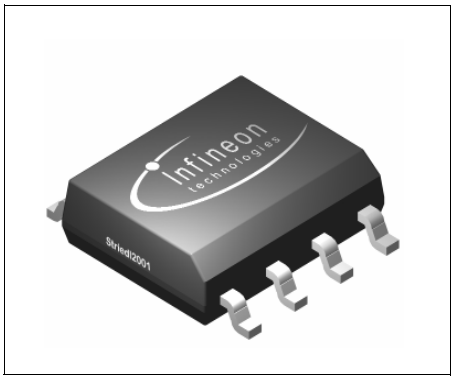


Table of Contents

List of Figures

List of Tables

1 Product Description



1.1 Overview

The TLE5012 is a 360° angle sensor that detects the orientation of a magnetic field by measuring sine and cosine angle components with monolithic integrated Giant Magneto Resistance (iGMR) elements.

Highly precise angle values are maintained at various temperatures throughout the device's lifetime using an internal autocalibration algorithm.

Data communications are accomplished with a bi-directional Synchronous Serial (SSC)-Interface that is Serial Peripheral Interface (SPI)-compatible.

The absolute angle value and other values are transmitted via SSC or via a Pulse-Width Modulation (PWM) protocol. The sine and cosine raw values can also be read out. These raw signals are digitally processed internally to calculate the angle orientation of the magnetic field (magnet).

The TLE5012 is a precalibrated sensor. The calibration parameters are stored in laser fuses. At start-up, the values of the fuses are written into flip-flops, where these values can be changed by the application-specific parameters. The TLE5012-E0318 and TLE5012-E0742 are especially configured in a Hall-Switch emulation mode for motors with three or seven pole pairs.

Online diagnostic functions are provided to ensure reliable operation.

Product Type	Marking	Ordering Code	Package
TLE5012	5012	SP000477068	PG-DSO-8
TLE5012-E0318	5012E03	SP000611246	PG-DSO-8
TLE5012-E0742	5012E07	SP000611250	PG-DSO-8

1.2 Features

- GMR-based principle
- Integrated magnetic field sensing for angle measurement
- Fully calibrated 0 - 360° angle measurement with revolution counter and angle speed measurement
- Two separate highly accurate single-bit SD-ADCs
- 15-bit representation of absolute angle value on the output (resolution of 0.01°)
- 16-bit representation of sine/cosine values on the interface
- Max. 1.0° angle error over lifetime and temperature with activated auto-calibration
- Bi-directional SSC Interface up to 8 Mbit/s
- Supports Safety Integrity Level (SIL) with diagnostic functions and status information
- Interfaces: SSC, PWM, Incremental Interface (IIF), Hall-Switch Mode (HSM)
- 0.25-µm CMOS technology
- Automotive qualified: -40°C to 150°C (junction temperature)
- ESD > 4 kV (HBM)
- RoHS-compliant (Pb-free package)

1.3 Typical Applications

The TLE5012 GMR-Based Angular Sensor is designed for angular position sensing in automotive applications, such as:

- Electrical commutated motor (e.g. used in Electric Power Steering (EPS))
- Rotary switch
- Steering angle
- General angular sensing

2 Functional Description

2.1 General

The GMR sensor uses vertical integration. This means that the GMR-sensitive areas are integrated above the logic portion of the TLE5012 device. These GMR elements change their resistance depending on the direction of the magnetic field.

Four individual GMR elements are connected to one Wheatstone sensor bridge. These GMR elements sense one of two components of the applied magnetic field:

- X component, V_x (cosine) or the
- Y component, V_y (sine)

The advantage of a full-bridge structure is that the amplitude of the GMR signal is doubled and temperature effects cancel out each other.

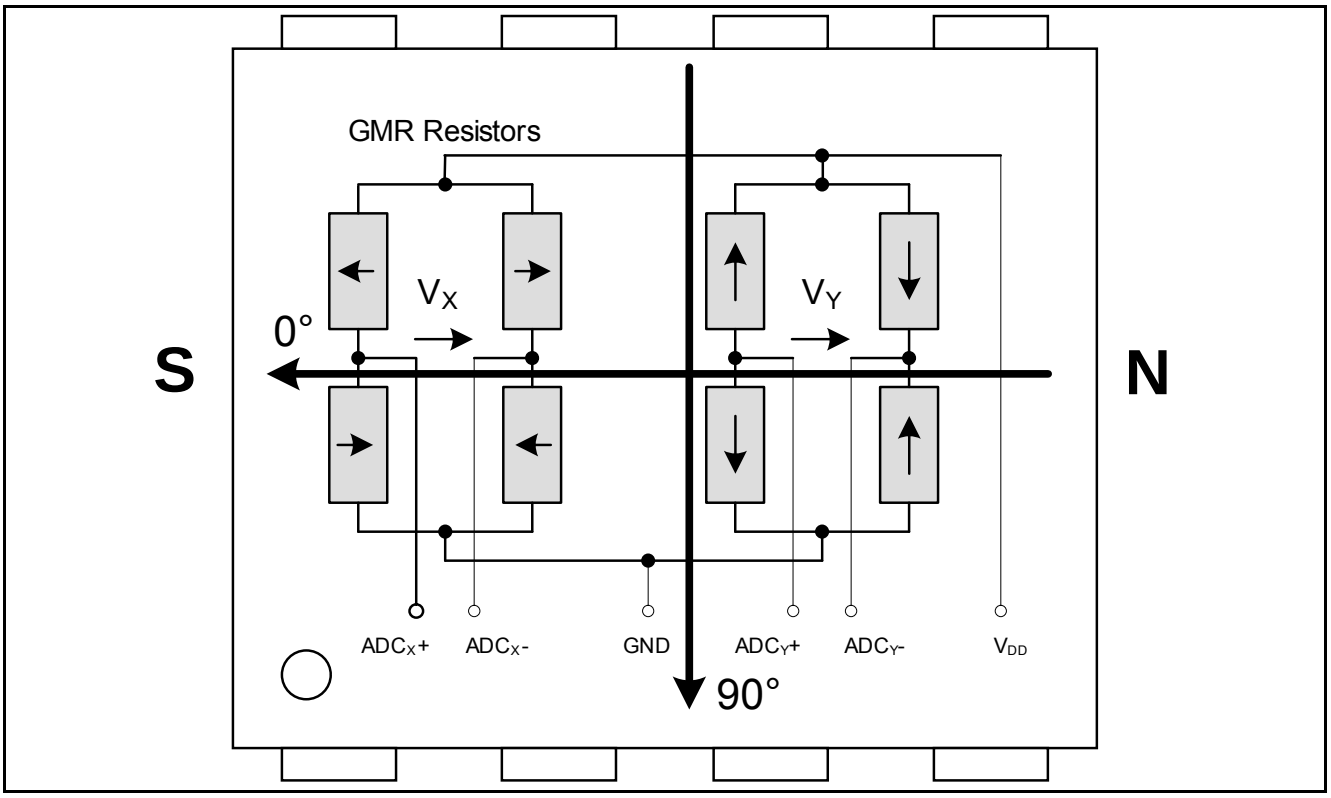


Figure 1 Sensitive bridges of the GMR sensor

*Note: In **Figure 1**, the arrows in the resistors represent the magnetic direction which is fixed in the Reference Layer. If the external magnetic field is parallel to the direction of the Reference Layer, the resistance is minimal. If they are anti-parallel, resistance is maximal.*

The output signal of each bridge is only unambiguous over 180° between two maxima. Therefore two bridges are oriented orthogonally to each other to measure 360°.

With the trigonometric function ARCTAN, the true 360° angle value can be calculated, based on the relationship of X and Y signals.

Because only the relative values influence the result, the absolute magnitude of the two signals is of minor importance. Therefore, it is possible to compensate for most external influences on the amplitudes.

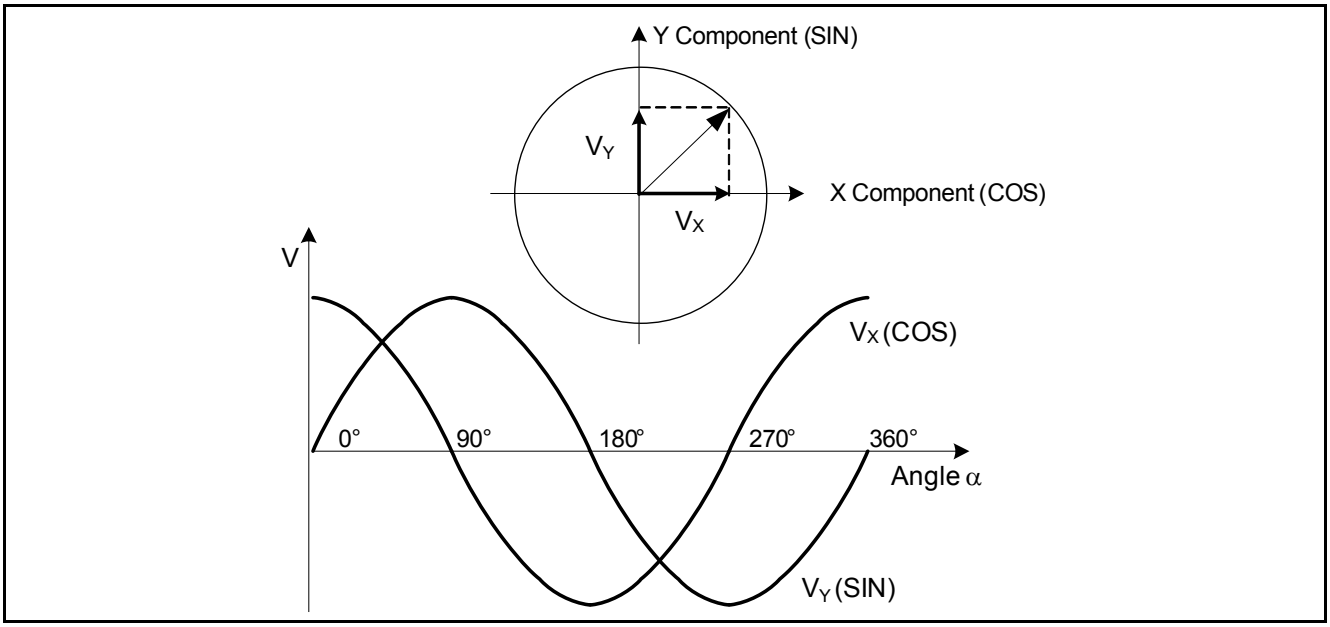


Figure 2 Theoretical output of the GMR sensor bridges

2.2 Pin Configuration

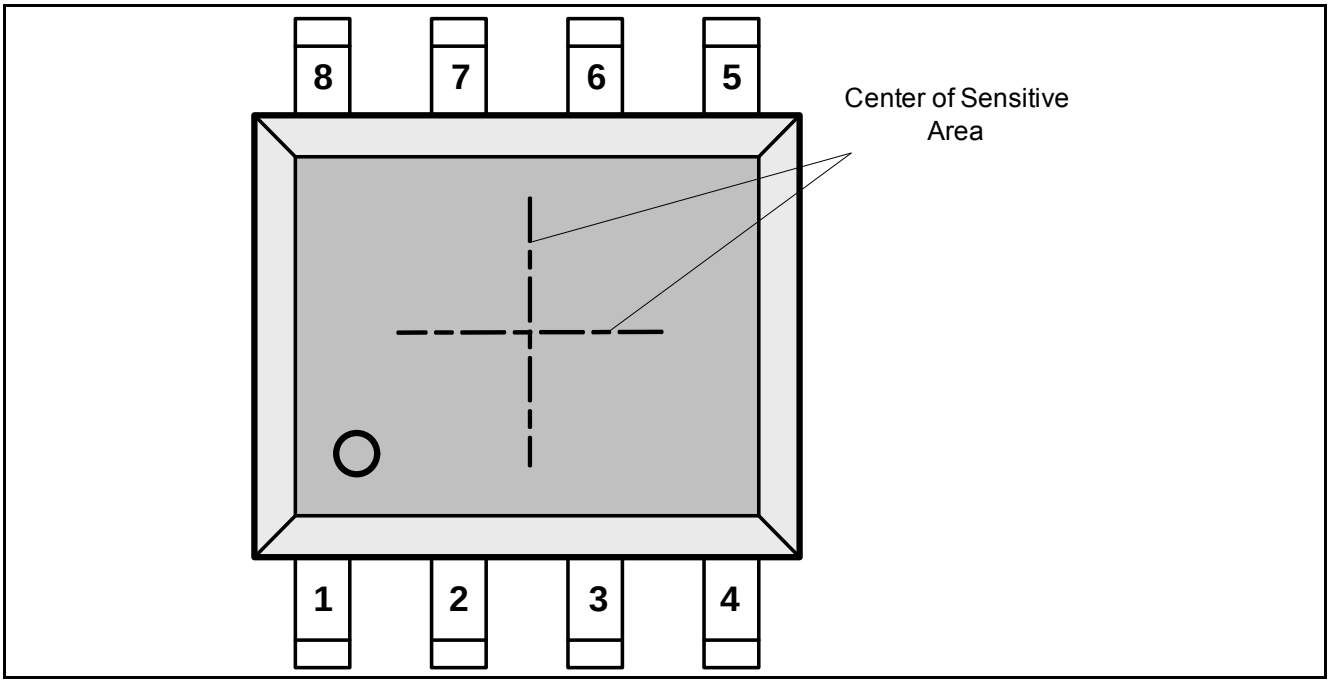


Figure 3 Pin configuration (top view)

2.3 Pin Description

Table 1 Pin description

Pin No.	Symbol	In/Out	Function
1	CLK	I	External Clock (selection of interface)[1)]
2	SCK	I	SSC Clock
3	CSQ	I	SSC Chip Select
4	DATA (DATA / IIF_Index / HS3)	I/O	Interface DATA: SSC DATA; IIF Index; Hall Switch signal 3 [2)]
5	IFA (IIF_A / HS1 / PWM)	O	Interface A: IIF phase A; Hall Switch signal 1; PWM [2)]
6	V_{DD}	-	Supply voltage
7	GND	-	Ground
8	IFB (IIF_B / HS2)	O	Interface B: IIF phase B; Hall Switch signal 2 [2)]

1) Connected to V_{DD} --> Incremental Interface is used; connected to GND--> Interface in IF_MD is used; sampling within Power-On Time; interface change within operation via SSC IF possible

2) Depends on external circuit of CLK and IF_MD setting

2.4 Block Diagram

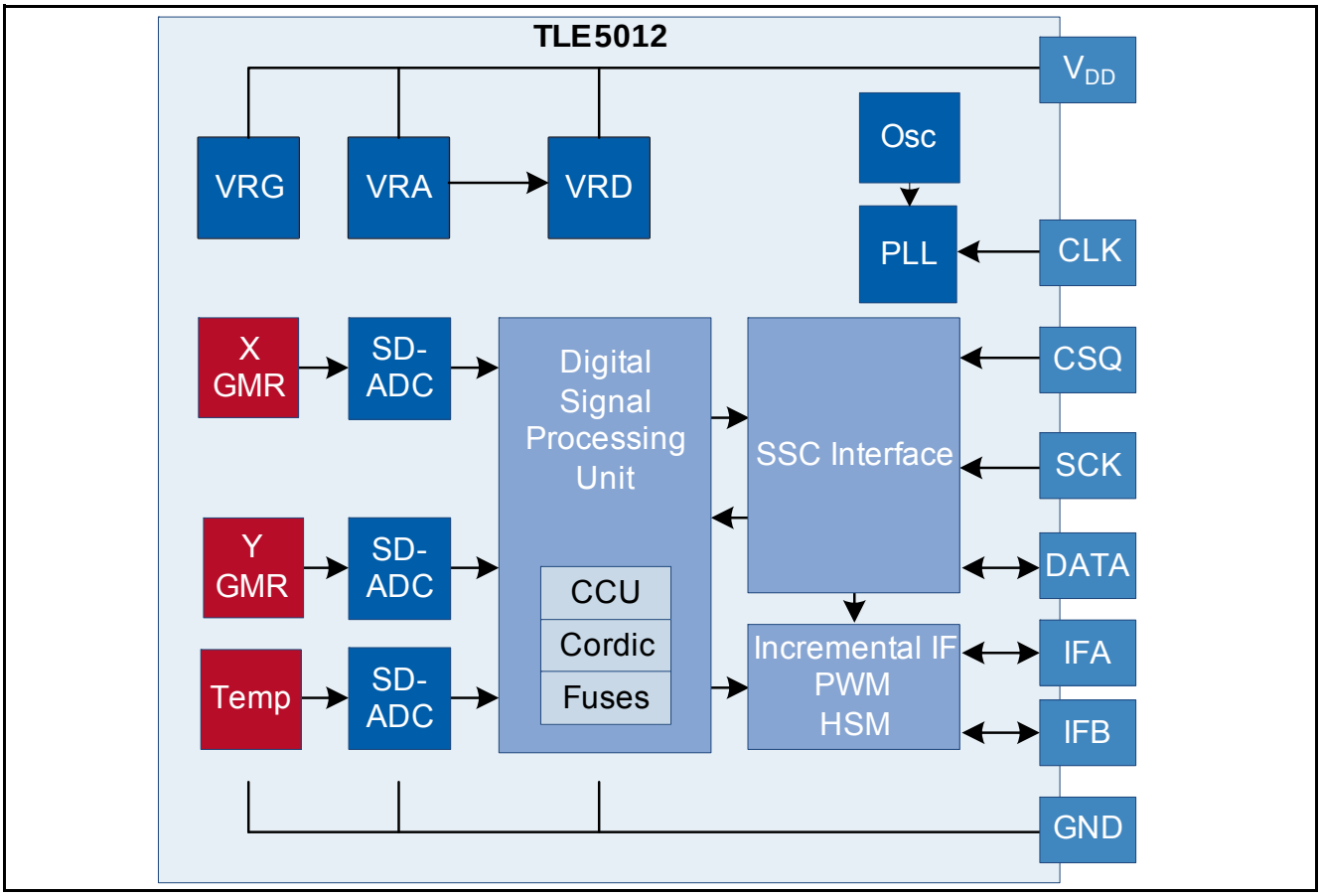


Figure 4 TLE5012 block diagram

2.5 Functional Block Description

2.5.1 Internal Power Supply

The internal stages of the TLE5012 have different voltage regulators.

- GMR Voltage Regulator VRG
- Analog Voltage Regulator VRA
- Digital Voltage Regulator VRD (derived from VRA)

These regulators are directly connected to the supply voltage V_{DD}.

2.5.2 Oscillator and PLL

The internal frequency oscillator feeds the Phase-Locked Loop (PLL). Therefore the external CLocK (CLK) can also be used.

2.5.3 SD-ADCs

The SD-ADCs transform the analog GMR voltages and temperature voltage into the digital domain.

2.5.4 Digital Signal Processing Unit

The Digital Signal Processing Unit (DSPU) contains the:

- **C**apture **C**ompare **U**nit (**CCU**), which is used to generate the PWM signal
- **CO**ordinate **R**otation **DI**gital **C**omputer (**CORDIC**), which contains the trigonometric function for angle calculation
- Fuses, which contain the calibration parameters

2.5.5 Interfaces

Different Interfaces can be selected:

- SSC Interface
- PWM
- Incremental Interface
- Hall Switch Mode

2.5.6 Safety Features

The TLE5012 offers a multiplicity of safety features to support Safety Integrity Level (SIL). Sensors with this performance are identified by the following logo:

Figure 5 PRO-SIL™ Logo

Safety features are:

- Test vectors switchable to ADC input
- Inversion or combination of filter input streams
- Data transmission check via 8-bit Cyclic Redundancy Check (CRC)
- Self-test routines
- Two independent active interfaces possible
- Overvoltage and undervoltage detection

Disclaimer

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The PRO-SIL™ Trademark designates Infineon products which contain SIL Supporting Features.

SIL Supporting Features are intended to support the overall System Design to reach the desired SIL (according to IEC61508) or A-SIL (according to ISO26262) level for the high efficiency Safety System.

SIL respectively A-SIL certification for such a system has to be reached on system level by the System Responsible at an accredited Certification Authority.

SIL stands for Safety Integrity Level (according to IEC 61508)

A-SIL stands for Automotive-Safety Integrity Level (according to ISO 26262)

3 Specifications

3.1 Application Circuit

The application circuits shown in **Figure 6**, **Figure 7**, **Figure 8** and **Figure 9** show the various communication possibilities of the TLE5012.

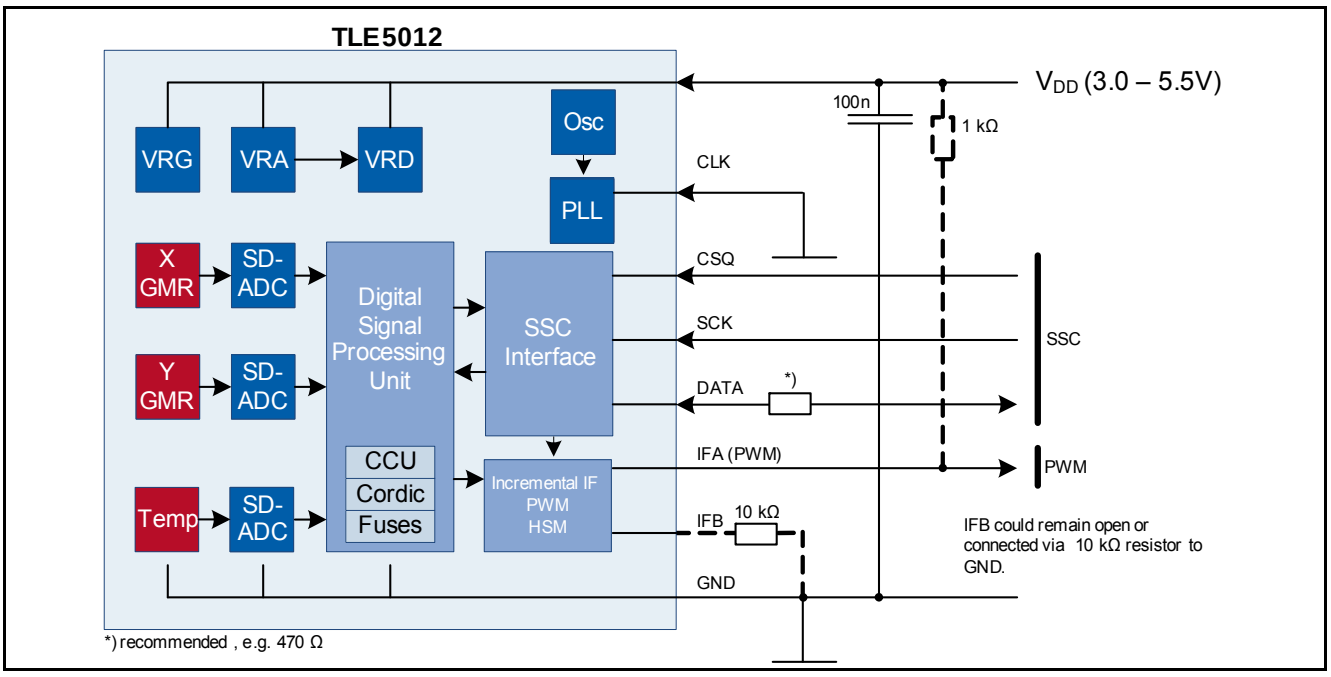


Figure 6 Application circuit for TLE5012 with SSC and PWM Interface (using internal CLK)

Figure 6 shows a basic block diagram of the TLE5012 with PWM Interface. This interface is selectable by connecting CLK to GND. In addition to the PWM, the SSC Interface could be used. Within the SSC Interface, the PWM Mode is selectable between push-pull and open drain.

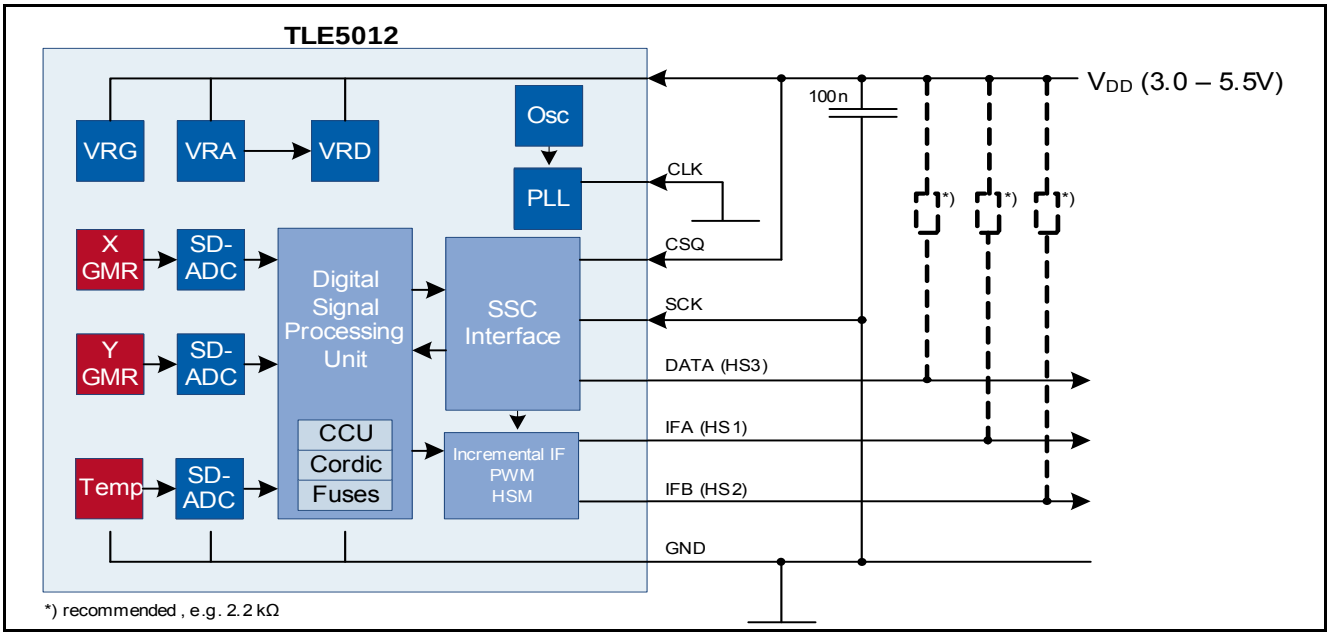


Figure 7 Application circuit for TLE5012 with HS Mode (using internal CLK)

Figure 7 shows a basic block-diagram of the TLE5012 in the Hall Switch Mode. This interface is selectable by connecting CLK to GND and CSQ to V_{DD}. In addition to the HSM, the SSC Interface can be used by pulling CSQ to GND. Within the SSC Interface, the HSM is selectable between push-pull and open drain.

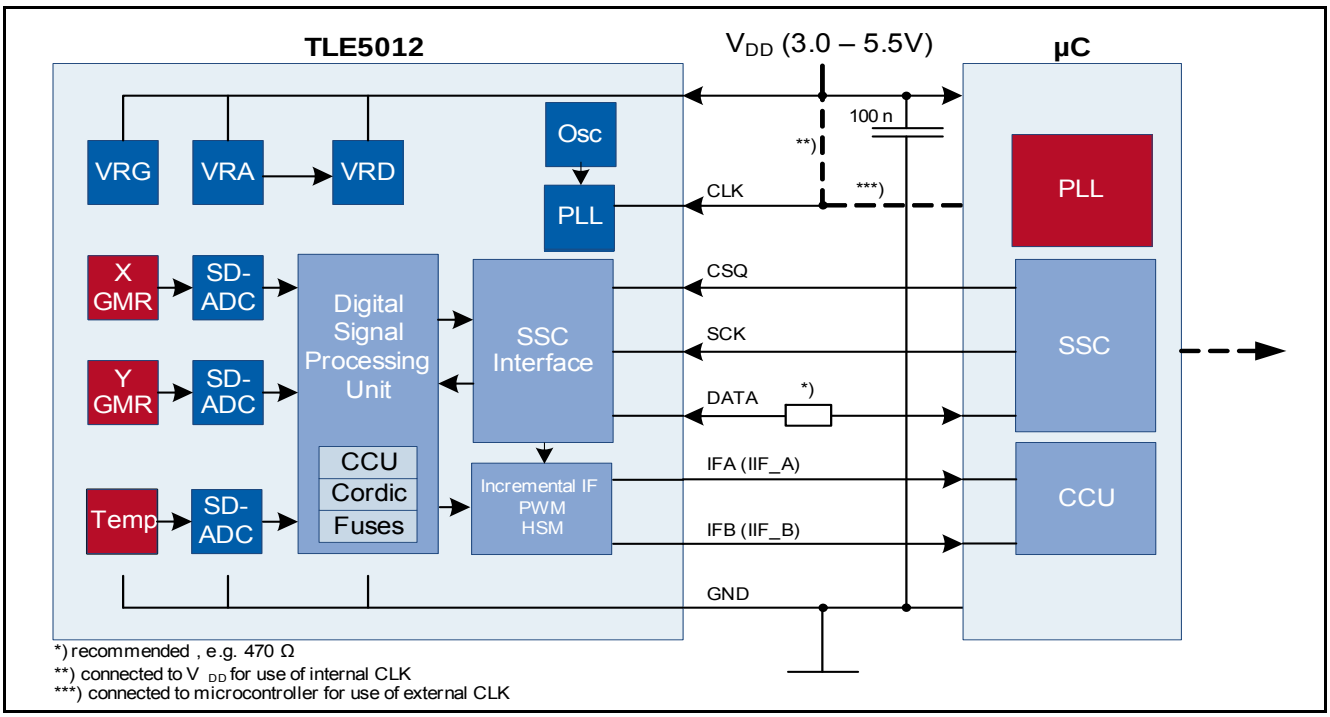


Figure 8 Application circuit for TLE5012 with SSC Interface and IIF (using external CLK)

Figure 8 shows a basic block diagram of an angle sensor system using a TLE5012 and a microcontroller for rotor-positioning applications. The interface configuration depicted is needed for high-speed applications such as electrical commutated motor drives. It is possible to connect the TLE5012 to a microcontroller via the Incremental Interface, and for safety reasons also via the SSC Interface.

The TLE5012 Exxxx can be configured with PWM only (**Figure 9**). This is not possible with the Standard TLE5012 type.[1)]

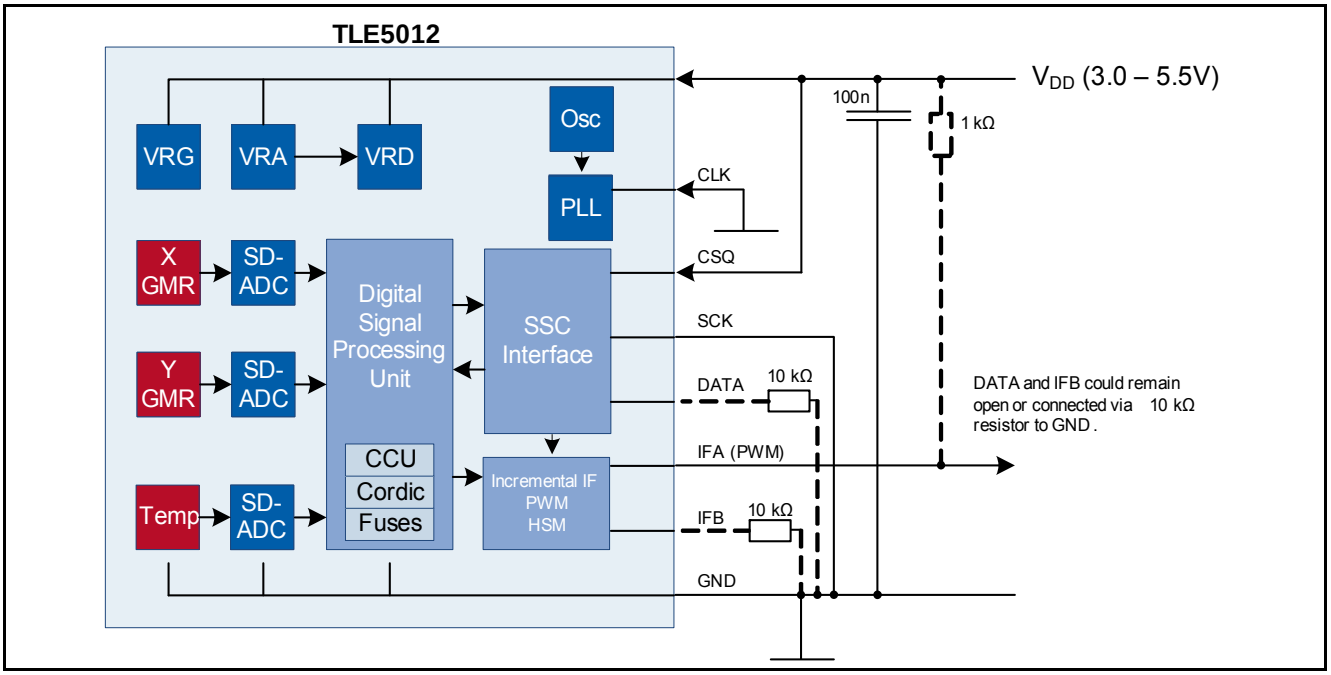


Figure 9 Application circuit for TLE5012 with only PWM Interface (using internal CLK)

1) For more information, please contact Infineon

3.2 Absolute Maximum Ratings

Table 2 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage on V_{DD} pin with respect to ground (V_{SS})	V_{DD}	-0.5	-	6.5	V	Max. 40 h/lifetime
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	-	6.5	V	Additionally V_{DD} + 0.5 V may not be exceeded
Junction temperature	T_J	-40	-	150	°C	
		-	-	150	°C	For 1000 h not additive
Magnetic field induction	B	-	-	|125|	mT	Max. 5 min @ T_A = 25°C
		-	-	|100|	mT	Max. 5 h @ T_A = 25°C
Storage temperature	T_{ST}	-40	-	150	°C	Without magnetic field

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the device.

3.3 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLE5012. All parameters specified in the following sections refer to these operating conditions, unless otherwise noted. **Table 3** is valid for -40°C < T_J < 150°C unless otherwise noted.

Table 3 Operating range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	3.0	5.0	5.5	V	1)
Output current (DATA-Pad)	I_Q	-	-	-25	mA	PAD_DRV =’0x’, sink current2)3)
		-	-	-5	mA	PAD_DRV =’10’, sink current2)3)
		-	-	-0.4	mA	PAD_DRV =’11’, sink current2)3)
Output current (IFA / IFB-Pad)	I_Q	-	-	-15	mA	PAD_DRV =’0x’, sink current2)3)
		-	-	-5	mA	PAD_DRV =’1x’, sink current2)3)
Input voltage	V_{IN}	-0.3	-	5.5	V	V_{DD} + 0.3 V may not be exceeded

Table 3 Operating range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Magnetic induction at T_A = 25°C 4)5)	B_{XY}	30	-	50	mT	-40°C < T_J < 150°C
	B_{XY}	30	-	60	mT	-40°C < T_J < 100°C
	B_{XY}	30	-	70	mT	-40°C < T_J < 85°C
Expanded magnetic induction at T_A = 25°C 4)5)	B_{XY}	25	-	30	mT	Additional angle error of 0.1° 6)
Angle range	Ang	0	-	360	°	

1) Directly blocked with 100-nF ceramic capacitor
2) Max. current to GND over open-drain output
3) At V_{DD} = 5V
4) Values refer to an homogenous magnetic field (B_{XY}) without vertical magnetic induction (B_Z = 0mT)
5) See **Figure 10**
6) 0 h

The field strength of a magnet can be selected within the colored area in **Figure 10**. By limitation of the junction temperature, a higher magnetic field can be applied. In case of a maximum temperature T_J=100°C a magnet with up to 60mT at T_A=25°C is allowed.

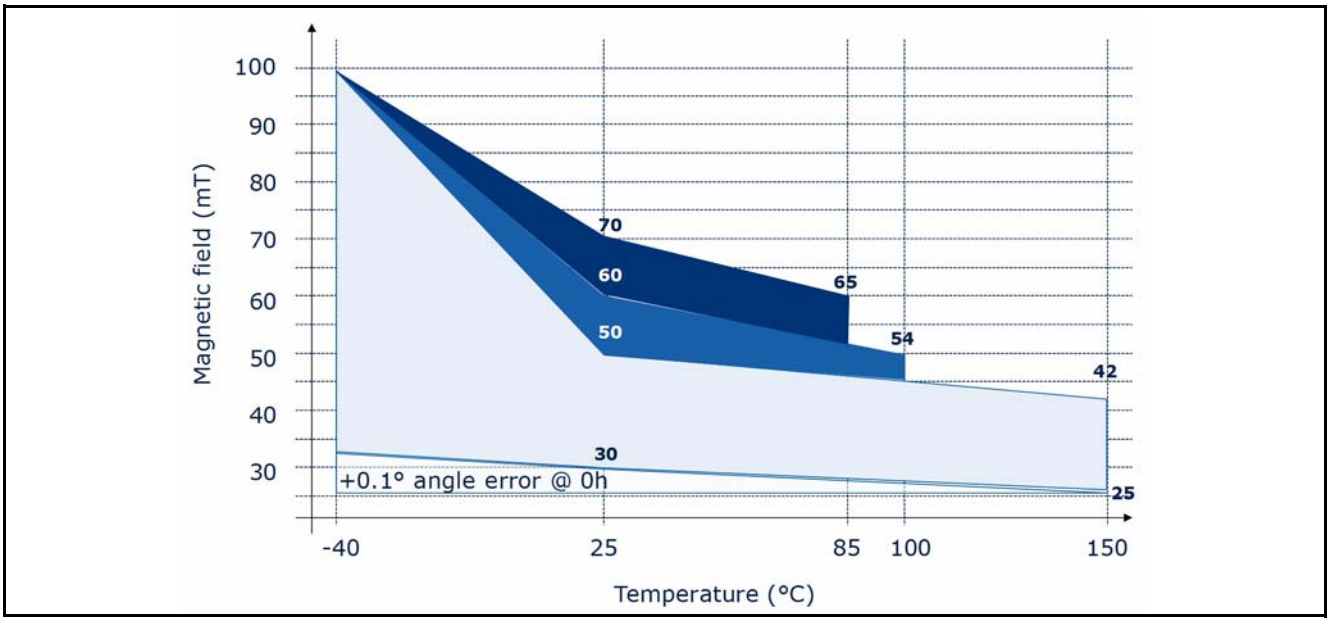


Figure 10 Magnet performance (ambient temperature)

*Note: The thermal resistances listed in **Table 29 "Package parameters" on Page 61** must be used to calculate the corresponding ambient temperature.*

Calculation of the Junction Temperature

The total power dissipation P_{TOT} of the chip increases its temperature above the ambient temperature.

The power multiplied by the total thermal resistance R_{thJA} (Junction to Ambient) leads to the final junction temperature. R_{thJA} is the sum of the addition of the values of the two components Junction to Case and Case to Ambient.

$$R_{thJA} = R_{thJC} + R_{thCA} \quad (1)$$

$$T_J = T_A + \Delta T$$

$$\Delta T = R_{thJA} \times P_{TOT} = R_{thJA} \times (V_{DD} \times I_{DD} + V_{OUT} \times I_{OUT}) \quad (I_{DD}, I_{OUT} > 0, \text{ if direction is into IC})$$

Example (assuming no load on V_{out}):

$$V_{DD} = 5V \quad (2)$$

$$I_{DD} = 14mA$$

$$\Delta T = 150\left[\frac{K}{W}\right] \times (5[V] \times 0.014[A] + 0[VA]) = 10.5K$$

For molded sensors, the calculation with R_{thJC} is more appropriate.

3.4 Characteristics

3.4.1 Electrical Parameters

The indicated electrical parameters apply to the full operating range, unless otherwise specified. The typical values correspond to a supply voltage V_{DD} = 5.0 V and 25 °C, unless individually specified. All other values correspond to -40 °C < T_J < 150°C.

Table 4 Electrical parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply current	I_{DD}	-	14	16	mA	
POR level	V_{POR}	2.0	-	2.9	V	Power-On Reset
POR hysteresis[1)]	V_{PORhy}	-	30	-	mV	
Pull-Up current	I_{PU}	-10	-	-225	µA	CSQ
		-10	-	-150	µA	DATA
Pull-Down current	I_{PD}	10	-	225	µA	SCK
		10	-	150	µA	CLK, IFA, IFB
Power-on time	t_{Pon}	-	5	7	ms	$V_{DD} > V_{DDmin}$[2)]

1) Not subject to production test - verified by design/characterization

2) Within “Power-On Time,” write access is not permitted

Table 5 Electrical parameters for 4.5V < V_{DD} < 5.5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input signal low level	V_{L5}	-	-	0.3 V_{DD}	V	
Input signal high level	V_{H5}	0.7 V_{DD}	-	-	V	
Output signal low level	V_{OL5}	-	-	1	V	DATA; I_Q = - 25 mA (PAD_DRV='0x'), I_Q = - 5 mA (PAD_DRV='10'), I_Q = - 0.4 mA (PAD_DRV='11')
		-	-	1	V	IFA,IFB; I_Q = - 15 mA (PAD_DRV='0x'), I_Q = - 5 mA (PAD_DRV='1x')

Table 6 Electrical parameters for 3.0V < V_{DD} < 3.6V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input signal low level	V_{L3}	-	-	0.2 V_{DD}	V	
Input signal high level	V_{H3}	0.8 V_{DD}	-	-	V	
Output signal low level	V_{OL3}	-	-	0.9	V	DATA; I_Q = - 15 mA (PAD_DRV='0x'), I_Q = - 3 mA (PAD_DRV='10'), I_Q = - 0.24 mA (PAD_DRV='11')
		-	-	0.9	V	IFA,IFB; I_Q = - 10 mA (PAD_DRV='0x'), I_Q = - 3 mA (PAD_DRV='1x')

3.4.2 ESD Protection

Table 7 ESD protection

Parameter	Symbol	Values		Unit	Notes
		min.	max.		
ESD voltage	V_{HBM}	-	±4.0	kV	Human Body Model[1)]
	V_{SDM}	-	±0.5	kV	Socketed Device Model[2)]

1) Human Body Model (HBM) according to AEC-Q100-002

2) Socketed Device Model (SDM) according to ESDA/ANSI/ESD SP5.3.2-2008

3.4.3 GMR Parameters

All parameters apply over B_{XY} = 30mT and T_A = 25°C, unless otherwise specified.

Table 8 Basic GMR parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
X, Y output range	RG_{ADC}	-	-	±23230	digits	4)
X, Y amplitude 1)	A_X, A_Y	6000	9500	15781	digits	
		3922	-	20620	digits	operating range
X, Y synchronism 2)	k	87.5	100	112.49	%	
X, Y offset 3)	O_X, O_Y	-2048	0	+2047	digits	
X, Y orthogonality error	Φ	-11.25	0	+11.24	°	
X, Y without field	X_0, Y_0	-5000	-	+5000	digits	without magnet 4)

1) See **Figure 11**

2) $k = 100*(A_X/A_Y)$

3) $O_Y=(Y_{MAX} + Y_{MIN}) / 2$; $O_X = (X_{MAX} + X_{MIN}) / 2$

4) Not subject to production test - verified by design/characterization

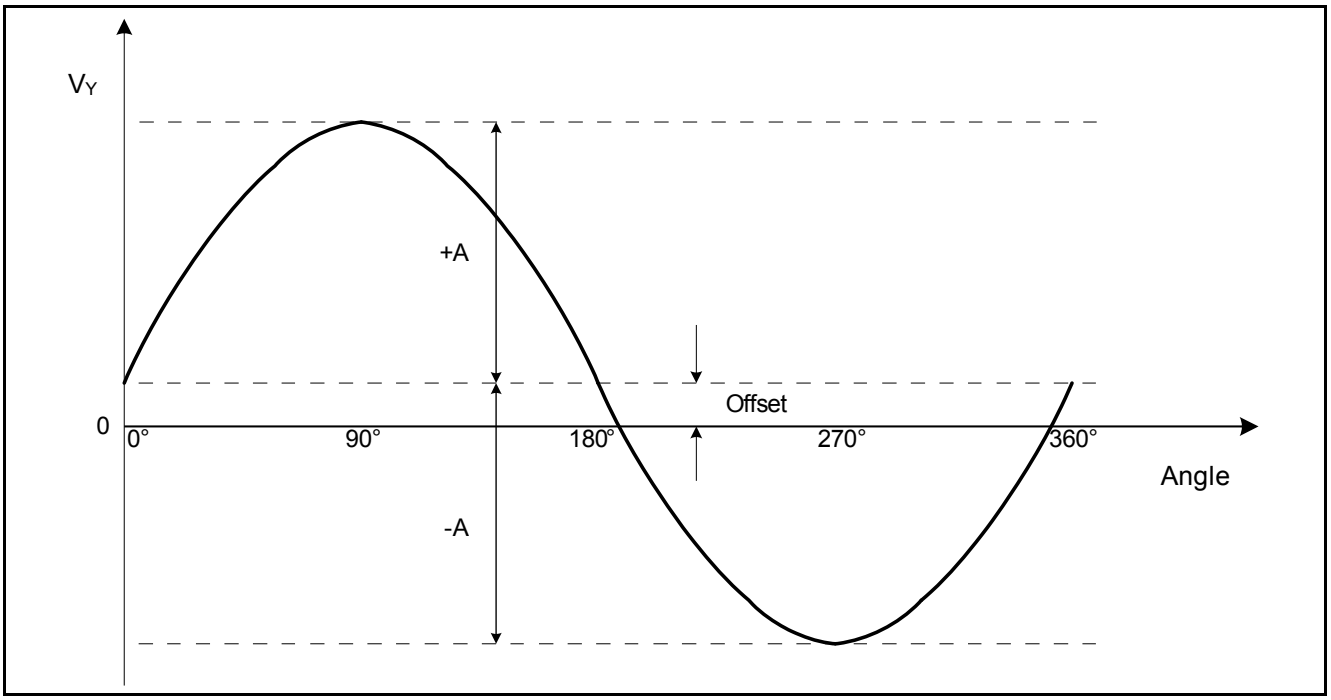


Figure 11 Offset and amplitude definition

3.4.4 Angle Performance

After internal calculation the sensor has a remaining error, as shown in **Table 11**. The error value refers to B_Z = 0mT and the operating conditions given in **Table 3 "Operating range" on Page 18**.

The overall angle error represents the relative angle error. This error describes the deviation from the reference line after zero angle definition.

Table 9 Angle performance

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overall Angle Error (with auto-calibration)	α_{Err}	-	0.6[1)]	1.0	°	including lifetime and temperature drift[2)3)4)]
Overall Angle Error (without auto-calibration)	α_{Err}	-	0.6[1)]	1.6	°	including temperature drift[2)3)5)]

1) At 25°C, B = 30 mT
2) Including hysteresis error, caused by revolution direction change.
3) Only with calibrated GMR-compensation parameters of customer setup; Relative error after zero angle definition.
4) Not subject to production test - verified by design/characterization
5) 0 h

Autocalibration

The autocalibration enables online parameter calculation and therefore reduces the angle error due to temperature drift, lifetime drift, and misalignments.

The TLE5012 is a pre-calibrated sensor. After start-up, the parameters out of the laser fuses get loaded into flip-flops. The TLE5012 needs more than a full revolution to generate new parameters. The update mode can be chosen within the Interface Mode 2 register (AUTOCAL). The parameters are updated in a smooth way to avoid an angle jump on the output. Therefore only one LSB will be changed within the choosen range or time. The autocalibration is done continuously.

AUTOCAL Modes:

- 00: No autocalibration
- 01: Autocalibration Mode 1. Only one LSB to final values within the update time t_{upd} (depending on FIR_MD setting).
- 10: Autocalibration Mode 2. Only one LSB update over one full revolution. After update of one LSB, the autocalibration will calculate the parameters again.
- 11: Autocalibration Mode 3. Only one LSB to final values within an angle range of 11.25°.

3.4.5 Signal Processing

The signal path of the TLE5012 is depicted in **Figure 12**. It consists of the GMR bridge, ADC, filter, and angle calculation. Depending on the filter configuration, various total delay times are achieved. In addition to this delay time, the delay time of the interface has to be considered. The delay time leads to an additional angle error at higher speeds. By enabling the prediction, the signal delay time can be reduced (**Figure 13**). The prediction uses the difference between current and last angle value and calculates the output value by adding this difference to the current value. A linear prediction is thereby achieved.

$$\alpha(t+1) = 2 \cdot \alpha(t) - \alpha(t-1) \quad (3)$$

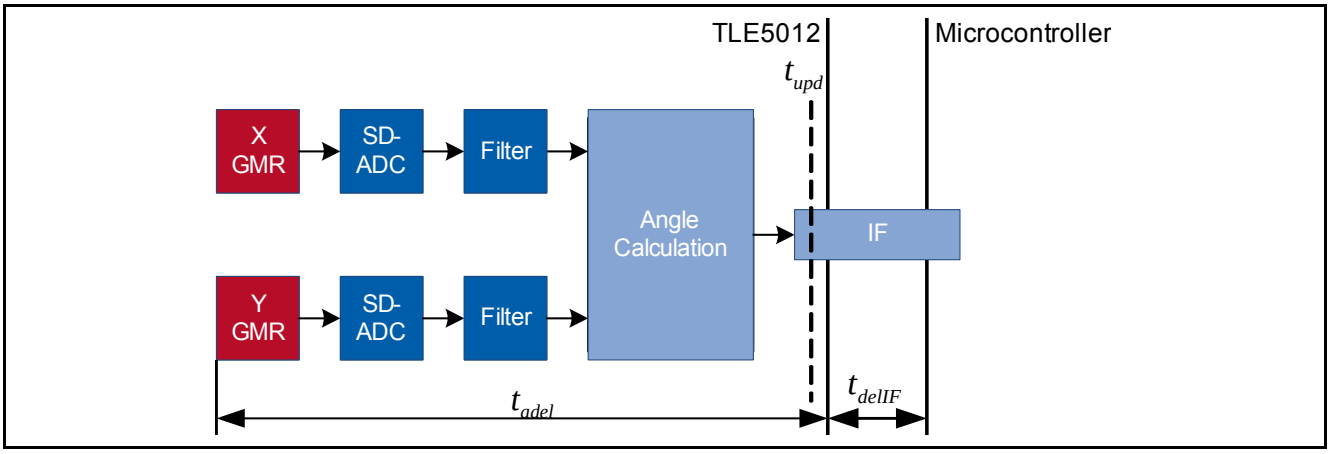


Figure 12 TLE5012 signal path

At FIR_MD = 0 only raw values can be read out, due to the more time consuming angle calculation.

Table 10 Signal processing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Update rate at interface	t_{upd}	-	21.3	-	µs	FIR_MD = 0 (only raw values)[1)2)]
		-	42.7	-	µs	FIR_MD = 1[1)2)]
		-	85.3	-	µs	FIR_MD = 2 (default)[1)2)]
		-	170.6	-	µs	FIR_MD = 3[1)2)]
Angle delay time[3)]	t_{adel}	-	60	70	µs	FIR_MD = 1[1)2)]
		-	80	95	µs	FIR_MD = 2[1)2)]
		-	120	140	µs	FIR_MD = 3[1)2)]
Angle delay time with prediction[3)]	t_{adel}	-	20	30	µs	FIR_MD = 1; PREDICT = 1 [1)2)]
		-	5	20	µs	FIR_MD = 2; PREDICT = 1 [1)2)]
		-	-40	-20	µs	FIR_MD = 3; PREDICT = 1 [1)2)]
Angle noise	N_{Angle}	-	0.11	-	°	FIR_MD = 0, (1 sigma)[2)]
		-	0.08	-	°	FIR_MD = 1, (1 sigma)[2)]
		-	0.05	-	°	FIR_MD = 2, (1 sigma)[2)] (default)
		-	0.04	-	°	FIR_MD = 3, (1 sigma)[2)]

1) Depends on internal oscillator frequency variation (**Section 3.4.6**)
2) Not subject to production test - verified by design/characterization
3) Valid at constant rotation speed

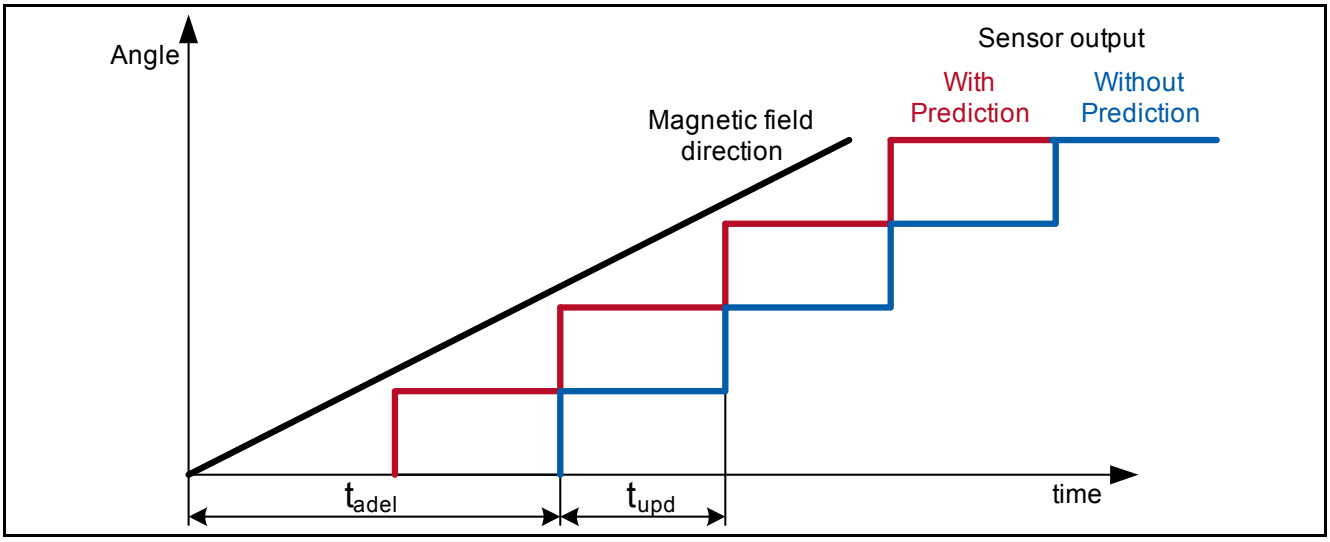


Figure 13 Delay of sensor output

3.4.6 Clock Supply (CLK Timing Definition)

If the external clock supply is selected, the clock signal input CLK must fulfill certain requirements:

- The high or low pulse width must not exceed the specified values, because the PLL needs a minimum pulse width and must be spike filtered.
- The duty cycle factor should be 0.5 but can deviate to the values limited by $t_{CLKh(f\_min)}$ and $t_{CLKl(f\_min)}$.
- The PLL is triggered at the positive edge of the clock; if more than 2 edges are missing, a chip reset is generated automatically.

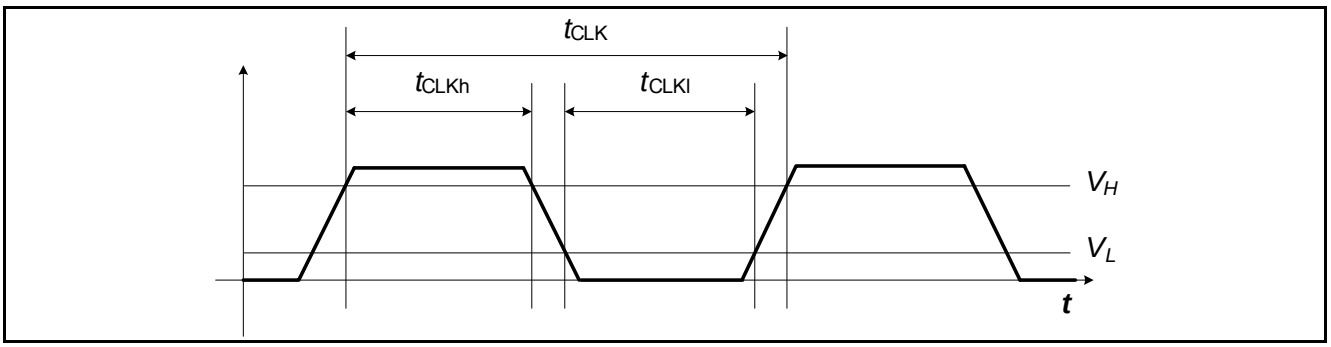


Figure 14 External CLK timing definition

Table 11 CLK timing specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{CLK}	3.8	4.0	4.2	MHz	
CLK duty cycle[1)2)]	CLK_{DUTY}	30	50	70	%	
CLK rise time	t_{CLKr}	-	-	30	ns	From V_L to V_H[3)]
CLK fall time	t_{CLKf}	-	-	30	ns	From V_H to V_L[3)]
Digital clock	f_{DIG}	22.8	24	25.2	MHz	
Internal oscillator frequency	f_{CLK}	3.8	4.0	4.2	MHz	

1) Minimum Duty Cycle Factor: $t_{CLKh(f\_min)}$ / $t_{CLK(f\_min)}$ with $t_{CLK(f\_min)}$= 1 / $f_{CLK(f\_min)}$

2) Maximum Duty Cycle Factor: $t_{CLKh(f\_max)}$ / $t_{CLK(f\_min)}$ with $t_{CLKh(f\_max)}$= $t_{CLK(f\_min)}$ - $t_{CLKl(min)}$

3) Not subject to production test - verified by design/characterization

3.5 Interfaces

Within the register MOD_3, the driver strength and so the slope for push-pull communication can be varied with the sensor output. The driver strength is specified in **Table 3** and the slope fall and rise times in **Table 12**.

Table 12 PAD characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output fall time	t_{fall}, t_{rise}	-	-	8	ns	DATA, 50 pF, PAD_DRV='00'[1)2)]
Output rise time		-	-	28	ns	DATA, 50 pF, PAD_DRV='01'[1)2)]
		-	-	45	ns	DATA, 50 pF, PAD_DRV='10'[1)2)]
		-	-	130	ns	DATA, 50pF, PAD_DRV='11'[1)2)]
		-	-	15	ns	IFA/IFB, 20 pF, PAD_DRV='0x'[1)2)]
		-	-	30	ns	IFA/IFB, 20 pF, PAD_DRV='1x'[1)2)]

1) Valid for push-pull output

2) Not subject to production test - verified by design/characterization

3.5.1 Synchronous Serial Communication (SSC) Interface

The 3-pin SSC Interface has a bi-directional push-pull data line, serial clock signal, and chip select. The SSC Interface is designed to communicate with a microcontroller peer-to-peer for fast applications.

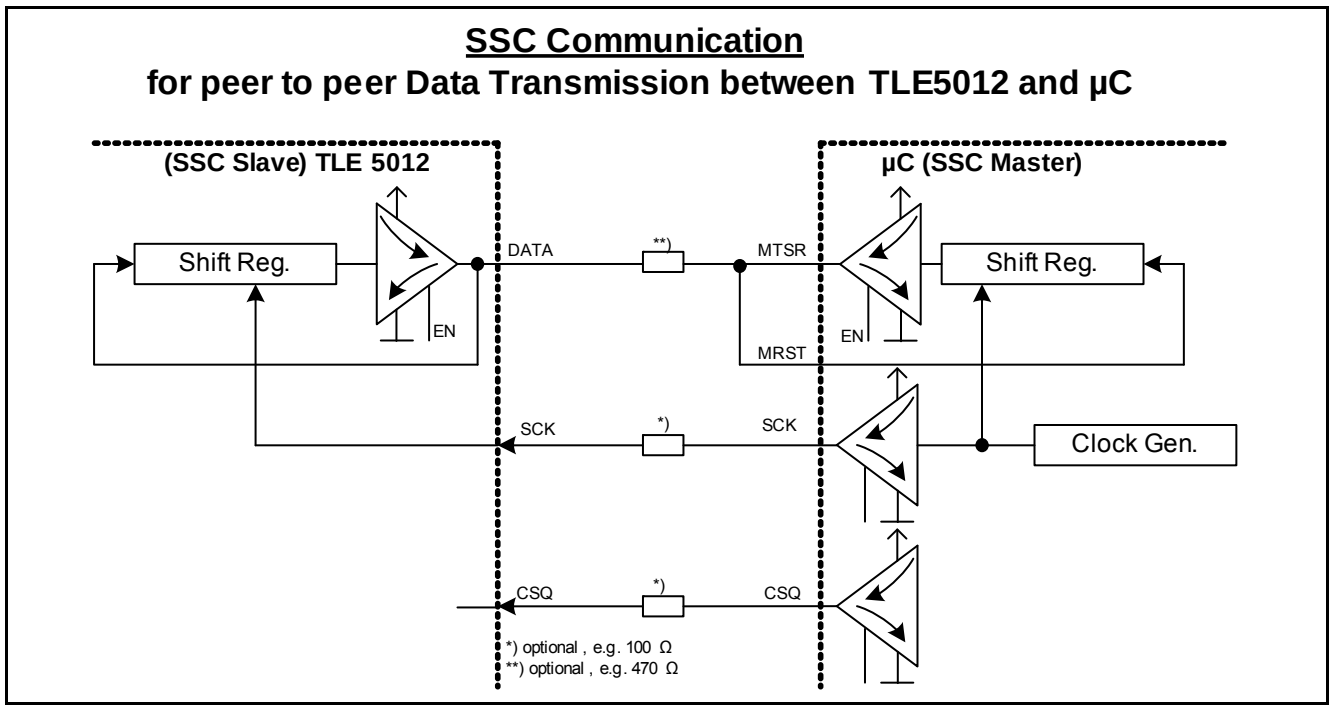


Figure 15 SSC configuration in sensor-slave mode with push-pull outputs (high speed application)

Another possibility is a 3-pin SSC Interface with bidirectional open-drain data line, serial clock signal, and chip select. This setup is designed to communicate with a microcontroller in a bus system, together with other SSC slaves (e.g. two TLE5012 devices for redundancy reasons). This mode can be activated using bit SSC_OD.

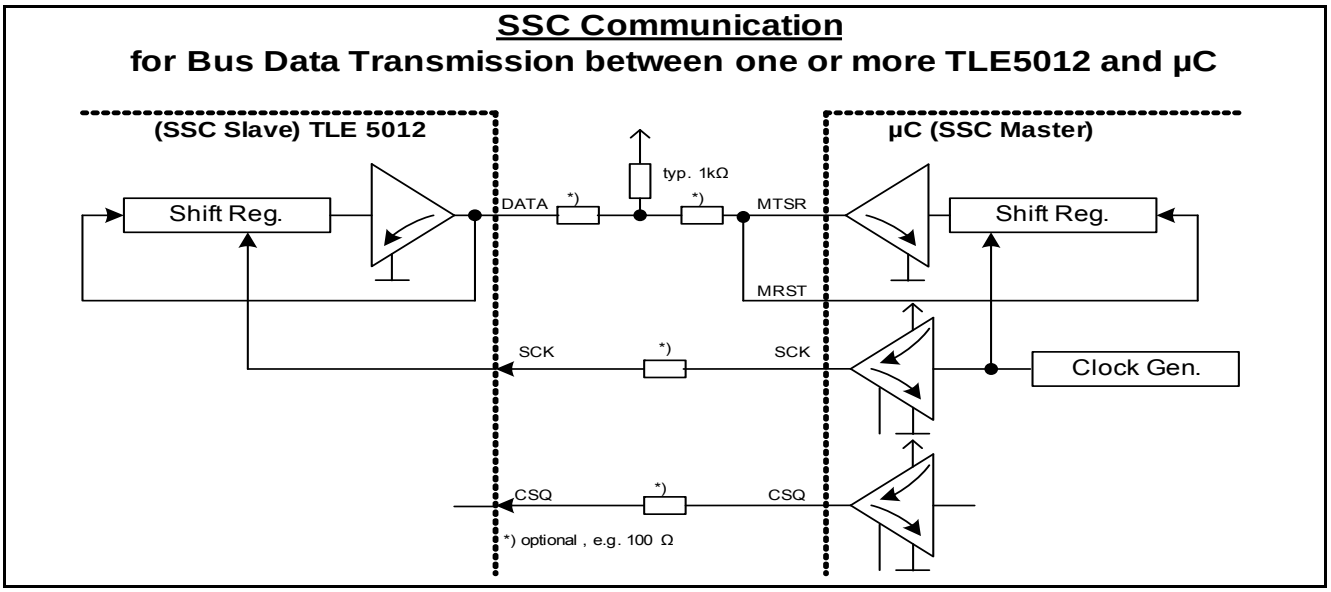


Figure 16 SSC configuration in sensor-slave mode and open drain (safe bus systems)

3.5.1.1 SSC Timing Definition

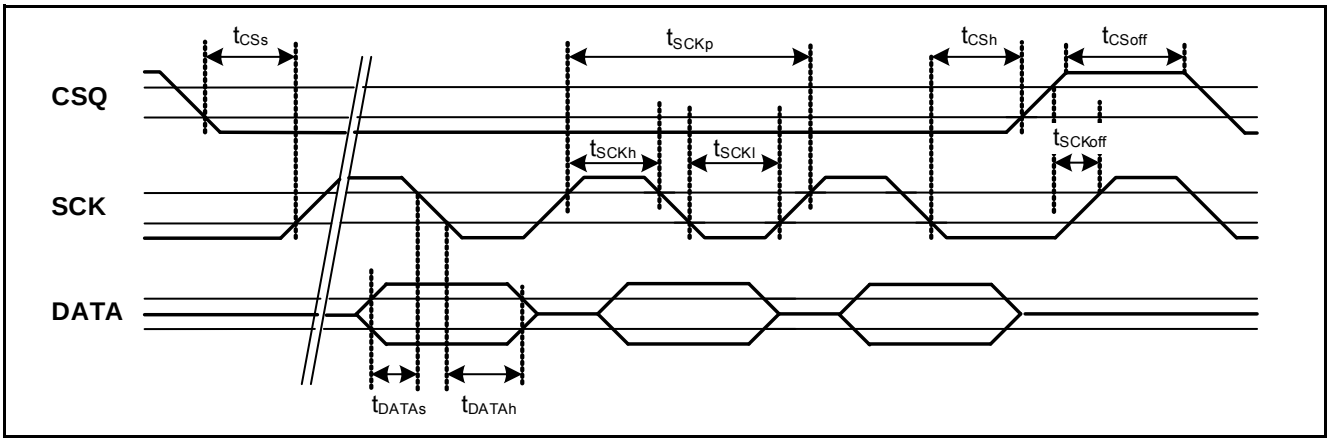


Figure 17 SSC timing

SSC Inactive Time (CS_{off})

The SSC inactive time defines the delay time after a transfer before the TLE5012 can be selected again.

Table 13 SSC push-pull timing specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SSC baud rate	f_{SSC}	-	8.0	-	Mbit/s	1)
CSQ setup time	t_{CSs}	105	-	-	ns	1)

Table 13 SSC push-pull timing specification (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CSQ hold time	t_{CSh}	105	-	-	ns	1)
CSQ off	t_{CSoff}	600	-	-	ns	SSC inactive time1)
SCK period	t_{SCKp}	120	125	-	ns	1)
SCK high	t_{SCKh}	40	-	-	ns	1)
SCK low	t_{SCKl}	30	-	-	ns	1)
DATA setup time	t_{DATAs}	25	-	-	ns	1)
DATA hold time	t_{DATAh}	40	-	-	ns	1)
Write read delay	t_{wr_delay}	130	-	-	ns	1)
SCK off	t_{SCKoff}	170	-	-	ns	1)

1) Not subject to production test - verified by design/characterization

Table 14 SSC open-drain timing specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SSC baud rate	f_{SSC}	-	2.0	-	Mbit/s	Pull-up Resistor = 1kΩ1)
CSQ setup time	t_{CSs}	300	-	-	ns	1)
CSQ hold time	t_{CSh}	400	-	-	ns	1)
CSQ off	t_{CSoff}	600	-	-	ns	SSC inactive time1)
SCK period	t_{SCKp}	500	-	-	ns	1)
SCK high	t_{SCKh}	-	190	-	ns	1)
SCK low	t_{SCKl}	-	190	-	ns	1)
DATA setup time	t_{DATAs}	25	-	-	ns	1)
DATA hold time	t_{DATAh}	40	-	-	ns	1)
Write read delay	t_{wr_delay}	130	-	-	ns	1)
SCK off	t_{SCKoff}	170	-	-	ns	1)

1) Not subject to production test - verified by design/characterization

3.5.1.2 SSC Data Transfer

The SSC data transfer is word-aligned. The following transfer words are possible:

- Command Word (to access and change operating modes of the TLE5012)
- Data Words (any data transferred in any direction)
- Safety Word (confirms the data transfer and provide status information)

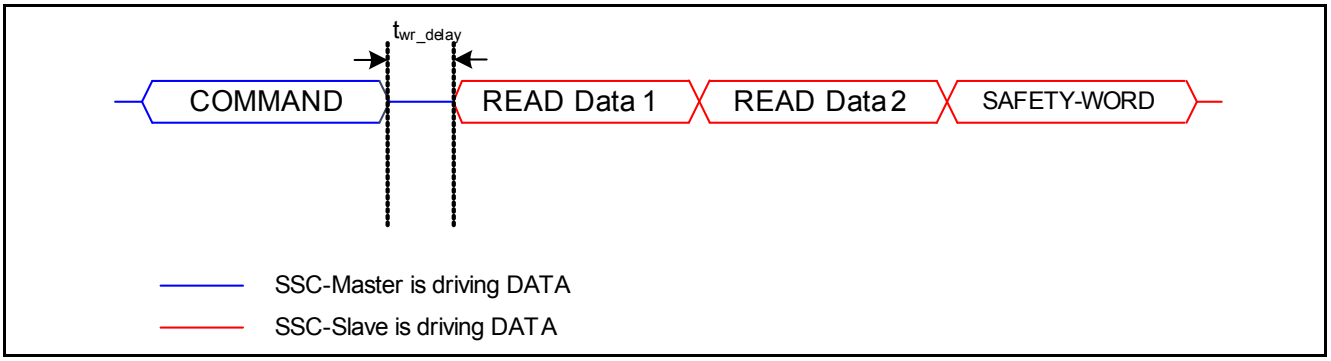


Figure 18 SSC data transfer (data-read example)

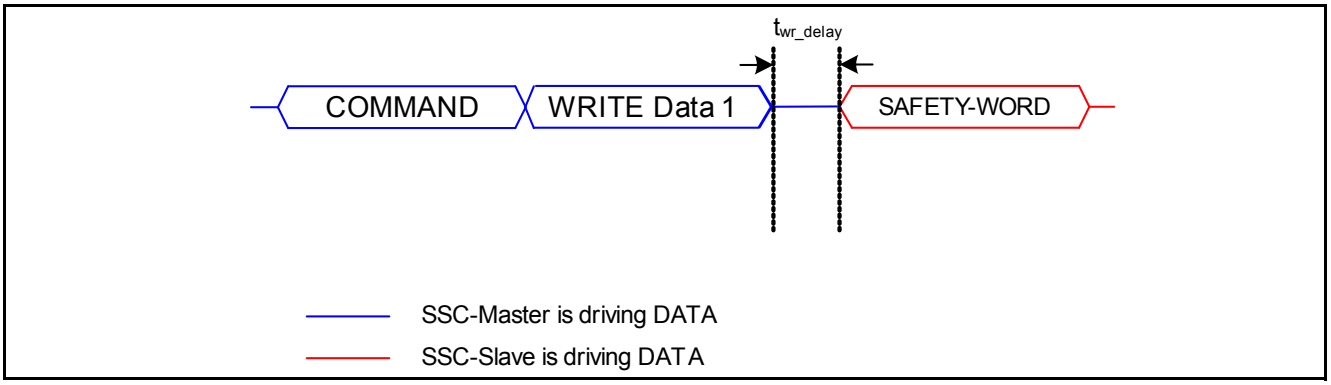


Figure 19 SSC data transfer (data-write example)

Command Word

The TLE5012 is controlled by a Command Word. It is sent first at the start of every data transmission. The structure of the Command Word is shown in **Table 15**, where the update (UPD) bit allows access to current or updated values. If an update command is issued and UPD is set, the immediate values are stored in the update buffer simultaneously. This enables a snapshot of all necessary system parameters at the same time. Bits with an update buffer are marked by an “u” in the bit type in the register description.

Table 15 Structure of the Command Word

Name	Bits	Description
RW	[15]	Read - write 0:Write 1:Read
Lock	[14..11]	4-bit lock value 0000_B: Default operating access for addresses 0x00:0x04 1010_B: Config- access for addresses 0x05:0x11
UPD	[10]	Update register access 0: Access to current values 1: Access to updated values

Table 15 Structure of the Command Word

Name	Bits	Description
ADDR	[9..4]	6-bit Address
ND	[3..0]	4-bit Number of data words

Safety Word

The Safety Word contains following bits:

Table 16 Structure of the Safety Word

Name	Bits	Description
STAT	Chip and Interface Status	
	[15]	Indication of chip reset (resets after readout) via SSC 0: Reset occurred 1: No reset Reset: 1_B
	[14]	System error (e.g. overvoltage; undervoltage; V_{DD}-, GND- off; ROM;...) 0: Error occurred (S_VR; S_DSPU; S_OV; S_XYOL: S_MAGOL; S_ADCM; S_FUSE) 1: No error
	[13]	Interface access error (access to wrong address; wrong lock) 0: Error occurred 1: No error
	[12]	Valid angle value (no system error; no interface error; NO_GMR_A = ’0’; NO_GMR_XY=’0’) 0: Angle value invalid 1: Angle value valid
RESP	[11..8]	Sensor number response indicator The sensor no. bit is pulled low and the other bits are high
CRC	[7..0]	Cyclic Redundancy Check

Bit Types

The types of bits used in the registers are listed here:

Table 17 Bit types

Abbreviation	Function	Description
R	Read	Read-only registers
W	Write	Read and write registers
U	Update	Update buffer for this bit is present. If an update is issued and the Update Register Access bit (UPD in Command Word) is set, the immediate values are stored in this update buffer simultaneously. This enables a snapshot of all necessary system parameters at the same time.

Data Communication via SSC

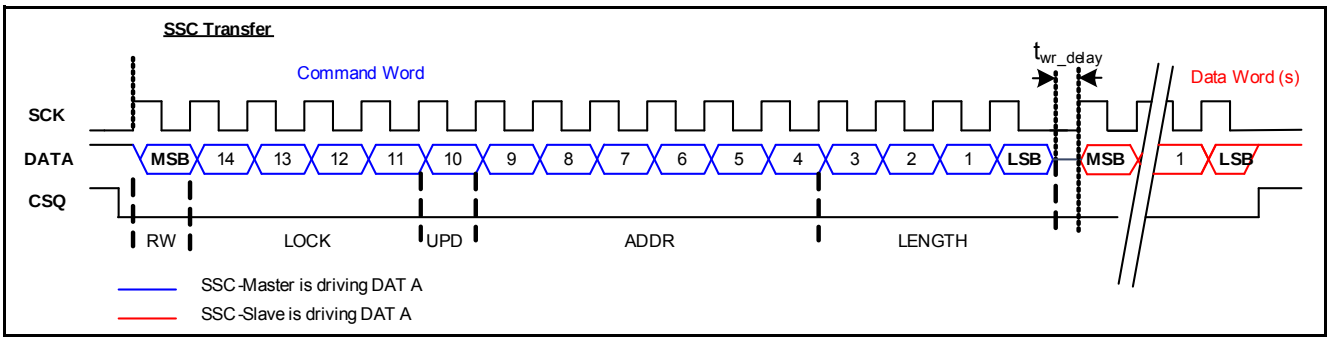


Figure 20 SSC bit ordering (read example)

The data communication via SSC Interface has the following characteristics:

- The data transmission order is “Most Significant Bit (MSB) first”.
- Data is put on the data line with the rising edge on SCK and read with the falling edge on SCK.
- The SSC Interface is word-aligned. All functions are activated after each transmitted word.
- A “high” condition on the negated Chip Select pin (CSQ) of the selected TLE5012 interrupts the transfer immediately. The CRC calculator is automatically reset.
- After changing the data direction, a delay (t_{wr_delay}) has to occur before continuing the data transfer. This is necessary for internal register access.
- Every access to the TLE5012 with the number of data (ND) ≥ 1 is performed with address auto-increment. At an overflow at address $3F_H$ the transfer continuous at address 00_H.
- With ND = 0, no auto-increment is done and a continuously readout of the same address can occur. Afterwards no Safety Word is sent and the transfer ends with high condition on CSQ.
- After every data transfer with ND ≥ 1, the 16-bit Safety Word will be appended by the selected TLE5012.
- After the Safety Word is sent, the transfer ends. To start another data transfer, the CSQ has to be deselected once for t_{CSoff}.
- The SSC is by default push-pull. The push-pull driver is active only if the TLE5012 has to send data; otherwise the push-pull is disabled for receiving data from the microcontroller.

Cyclic Redundancy Check (CRC)

- This CRC complies with the J1850 Bus Specification.
- Every new transfer resets the CRC generation.
- Every byte of a transfer will be taken into account to generate the CRC (also the sent command(s)).
- Generator polynomial: X8+X4+X3+X2+1, but for the CRC generation the fast CRC generation circuit is used (see **Figure 21**)
- The remainder of the fast CRC circuit is initial set to ’11111111_B’.
- The remainder is inverted before transmission.

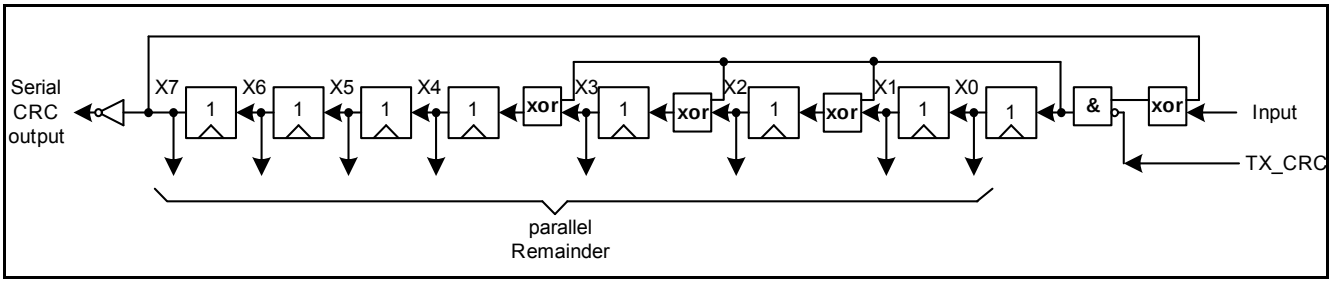


Figure 21 Fast CRC polynomial division circuit

3.5.1.3 Registers

This section describes the registers of the TLE5012. It also specifies the read/write access rights of the specific registers. **Table 18** identifies the values with symbols. Access to the registers is accomplished via the SSC Interface.

Table 18 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
Registers, TLE5012 Register			
STAT	Status Register	00_H	**34**
ACSTAT	Activation Status Register	01_H	**36**
AVAL	Angle Value Register	02_H	**37**
ASPD	Angle Speed Register	03_H	**38**
AREV	Angle Revolution Register	04_H	**39**
FSYNC	Frame Synchronization Register	05_H	**39**
MOD_1	Interface Mode1 Register	06_H	**40**
SIL	SIL Register	07_H	**41**
MOD_2	Interface Mode2 Register	08_H	**42**
MOD_3	Interface Mode3 Register	09_H	**43**
OFFX	Offset X	$0A_H$	**44**
OFFY	Offset Y	$0B_H$	**45**
SYNCH	Synchronicity	$0C_H$	**45**
IFAB	IFAB Register	$0D_H$	**46**
MOD_4	Interface Mode4 Register	$0E_H$	**47**
TCO_Y	Temperature Coefficient Register	$0F_H$	**48**
ADC_X	X-raw value	10_H	**48**
ADC_Y	Y-raw value	11_H	**49**
IIF_CNT	IIF Counter value	20_H	**49**

The register is addressed wordwise.

3.5.1.3.1 TLE5012 Register

Status Register

STAT	Offset	Reset Value
Status Register	**00_H**	**8001_H**

15	14	13	12	11	10	9	8
RD_ST	**S_NR**		**NO_GMR_A**	**NO_GMR_XY**	**S_ROM**	**S_ADCT**	Res
r	w		ru	ru	r	ru	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
S_MAGOL	**S_XYOL**	**S_OV**	**S_DSPU**	**S_FUSE**	**S_VR**	**S_WD**	**S_RST**
ru	ru	ru	ru	ru	ru	ru	ru

Field	Bits	Type	Description
RD_ST	15	r	**Read Status** 0_B status values not changed since last readout 1_B status values changed Reset: 1_B
S_NR	14:13	w	**Slave Number** is given at startup by the external circuit of IFA and IFB and can be changed via SSC-IF Reset: 00_B
NO_GMR_A	12	ru	**No valid GMR Angle Value** Cyclic check of DSPU output. 0_B valid GMR angle value on the interface 1_B no valid GMR angle value on the interface (e.g test vectors) Reset: 0_B
NO_GMR_XY	11	ru	**No valid GMR XY Values** Cyclic check of ADC input. 0_B valid GMR_XY values on the ADC input 1_B no valid GMR_XY values on the ADC input (e.g. test vectors) Reset: 0_B
S_ROM	10	r	**Status ROM**[1)] Check of ROM-CRC at startup. After fail DSPU does not start. SPI access possible. 0_B CRC OK 1_B CRC fail or running Reset: 0_B

Field	Bits	Type	Description
S_ADCT	9	ru	**Status ADC-Test**[1)] Check of signal path with test vectors. All test vectors at startup tested. Activation in operation via AS_ADCT possible. 0_B Test vectors OK 1_B Test vectors out of limit Reset: 0_B
S_MAGOL	7	ru	**Status Magnitude Out of Limit**[1)] Cyclic check of available magnetic field strength. Deactivation via AS_VEC_MAG. 0_B GMR-magnitude OK 1_B GMR-magnitude out of limit Reset: 0_B
S_XYOL	6	ru	**Status X,Y Data Out of Limit**[1)] Cylcic check of X and Y raw values. Deactivation via AS_VEC_XY 0_B X,Y data OK 1_B X,Y data out of limit (>23230 digits) Reset: 0_B
S_OV	5	ru	**Status Overflow**[1)] Cyclic check of DSPU overflow. Deactivation via AS_OV. 0_B No DSPU overflow occurred 1_B DSPU overflow occurred Reset: 0_B
S_DSPU	4	ru	**Status Digital Signal Processing Unit** Check of DSPU, CORDIC and CAPCOM at startup. Activation in operation via AS_DSPU possible. 0_B DSPU self-test OK 1_B DSPU self-test not OK, or self-test is running Reset: 0_B
S_FUSE	3	ru	**Status Fuse CRC**[1)] Cyclic CRC check of laser-cut-fuses. Deactivation via AS_FUSE and disabled by activated autocalibration. *Note: Changing of fused parameters results in new CRC, which differs from stored CRC --> Fuse CRC fail* 0_B Fuse CRC OK 1_B Fuse CRC fail Reset: 0_B
S_VR	2	ru	**Status Voltage Regulator**[1)] Permanent check of internal and external supply voltages. Deactivation via AS_VR 0_B Voltages OK 1_B V_{DD} overvoltage; V_{DD} undervoltage; V_{DD}-off; GND-off; or V_{OVG}; V_{OVA}; V_{OVD} too high Reset: 0_B

Field	Bits	Type	Description
S_WD	1	ru	**Status Watchdog** Permanent check of watchdog. After overflow, a reset is necessary. Deactivation via AS_WD 0_B after chip reset 1_B watchdog counter expired (DSPU stop), AS_RST must be activated Reset: 0_B
S_RST	0	ru	**Status Reset** Permanent check of any reset. Deactivation via AS_RST. 0_B no reset since last readout 1_B indication of power-up, short power-break or active reset Reset: 1_B

1) Reset to “0” after readout

Activation Status Register

ACSTAT	Offset	Reset Value
Activation Status Register	01_H	$5EFE_H$

15	14	13	12	11	10	9	8
Res						AS_ADCT	Res
						w	

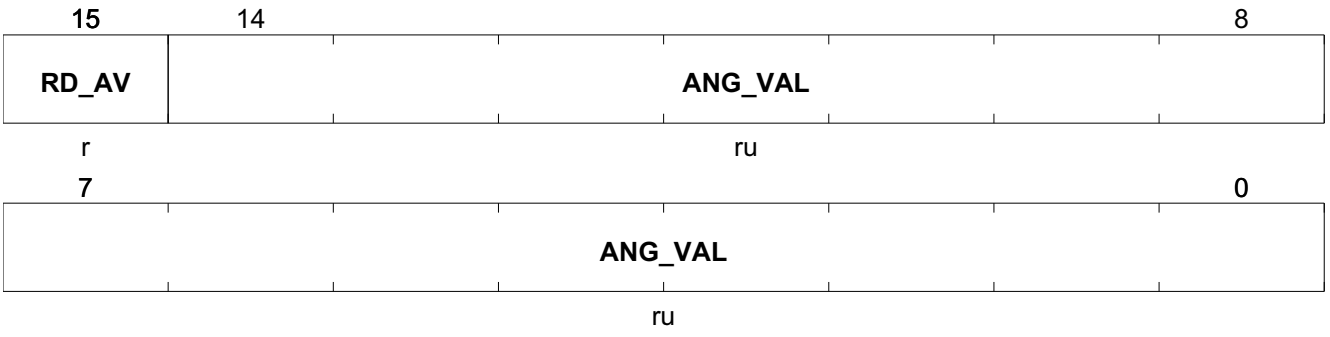
7	6	5	4	3	2	1	0
AS_VEC_MAG	AS_VEC_XY	AS_OV	AS_DSPU	AS_FUSE	AS_VR	AS_WD	AS_RST
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
Res	15:10	w	**Reserved** Reset: 010111_B
AS_ADCT	9	w	**Enable ADC Testvector Check** 0_B after execution 1_B activation of ADC Testvector Check Reset: 1_B
AS_VEC_MAG	7	w	**Activation of Magnitude Check** 0_B monitoring of magnitude disabled 1_B monitoring of magnitude enabled Reset: 1_B

Field	Bits	Type	Description
AS_VEC_XY	6	w	**Activation of X,Yout of limit Check** 0_B monitoring of X,Y out of limit disabled 1_B monitoring of X,Y out of limit enabled Reset: 1_B
AS_OV	5	w	**Enable of DSPU Overflow Check** 0_B monitoring of DSPU Overflow disabled 1_B monitoring of DSPU Overflow enabled Reset: 1_B
AS_DSPU	4	w	**Activation DSPU BIST** 0_B after execution 1_B activation of DSPU BIST or BIST running Reset: 1_B
AS_FUSE	3	w	**Activation Fuse CRC** 0_B monitoring of Fuse CRC disabled 1_B monitoring of Fuse CRC enabled Reset: 1_B
AS_VR	2	w	**Enable Voltage Regulator Check** 0_B check of regulator voltages disabled 1_B check of regulator voltages enabled Reset: 1_B
AS_WD	1	w	**Enable DSPU Watchdog-HW-Reset** 0_B DSPU Watchdog monitoring disabled 1_B DSPU Watchdog monitoring enabled Reset: 1_B
AS_RST	0	w	**Activation of Hardware Reset** Activation occurs after CSQ switches from ’0’ to ’1’ after SSC transfer. 0_B after execution 1_B activation of HW Reset Reset: 0_B

Angle Value Register

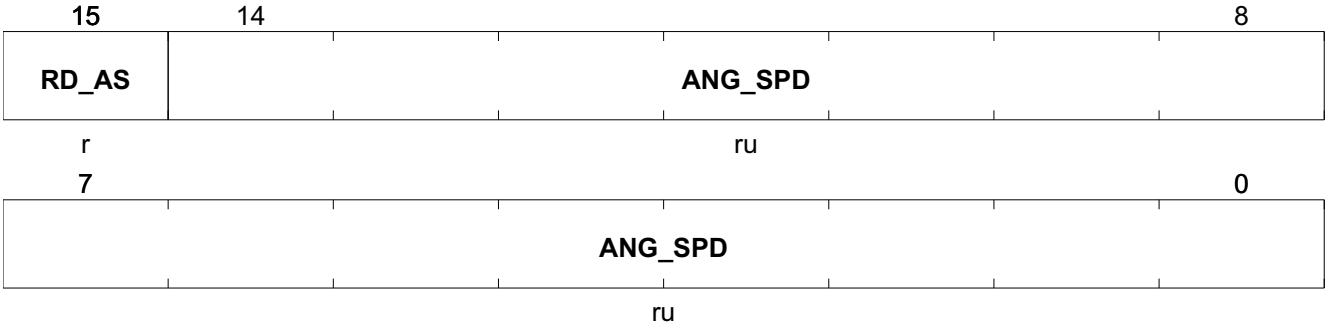
AVAL	Offset	Reset Value
Angle Value Register	**02_H**	**8000_H**



Field	Bits	Type	Description
RD_AV	15	r	**Read Status, Angle Value** 0_B no new angle value since last readout 1_B new angle value (ANG_VAL) present Reset: 1_B
ANG_VAL	14:0	ru	**Calculated Angle Value** (ANG_RANGE = 0x080) $Angle[°] = \frac{360°}{2^{15}} ANG\_VAL[digits]$ (4) 4000_H -180° 0000_H 0° $3FFF_H$ +179.99° Reset: 0_H

Angle Speed Register

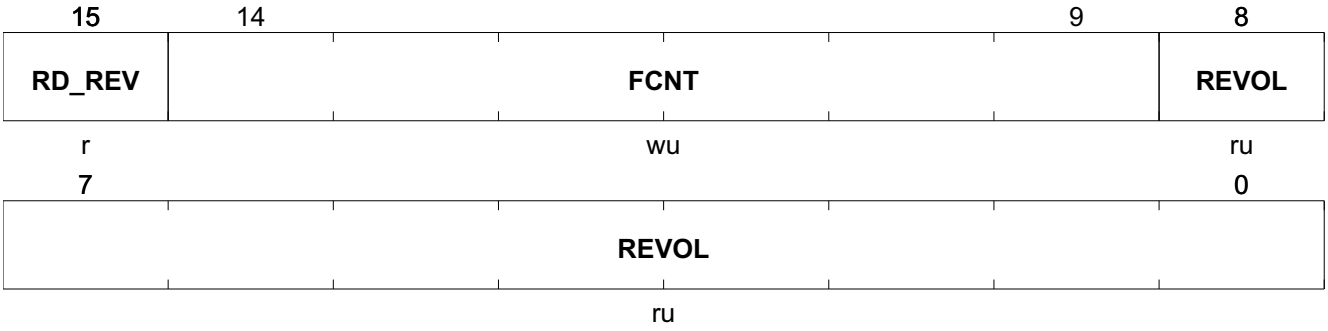
ASPD	Offset	Reset Value
Angle Speed Register	**03_H**	**8000_H**



Field	Bits	Type	Description
RD_AS	15	r	**Read Status, Angle Speed** 0_B no new angle speed value since last readout 1_B new angle speed value (ANG_SPD) present Reset: 1_B
ANG_SPD	14:0	ru	**Calculated Angle Speed** Without prediction difference among three consecutive angle values. With prediction, difference among three predicted angle values. $Speed\ [°/s] = \frac{\frac{AngleRange\ [°]}{2^{15}} ANG\_SPD\ [digits]}{2t_{upd}\ [s]}$ (5) Reset: 0_H

Angle Revolution Register

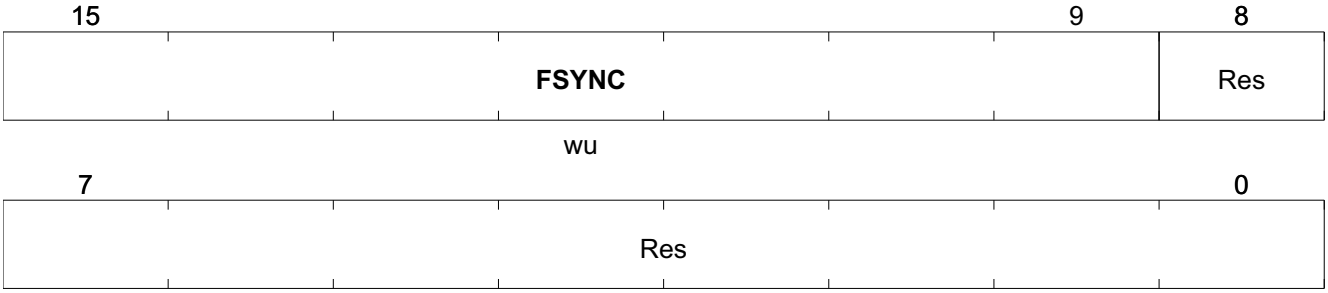
AREV	Offset	Reset Value
Angle Revolution Register	**04_H**	**8000_H**



Field	Bits	Type	Description
RD_REV	15	r	**Read Status, Revolution** 0_B no new values since last readout 1_B new value (REVOL) present Reset: 1_B
FCNT	14:9	wu	**Frame Counter (unsigned 6-bit value)** Counts every new angle value Reset: 0_H
REVOL	8:0	ru	**Number of Revolutions (signed 9-bit value)** If prediction is enabled, revolution counter is one schedule delayed related to ANG_VAL. Reset: 0_H

Frame Synchronization Register

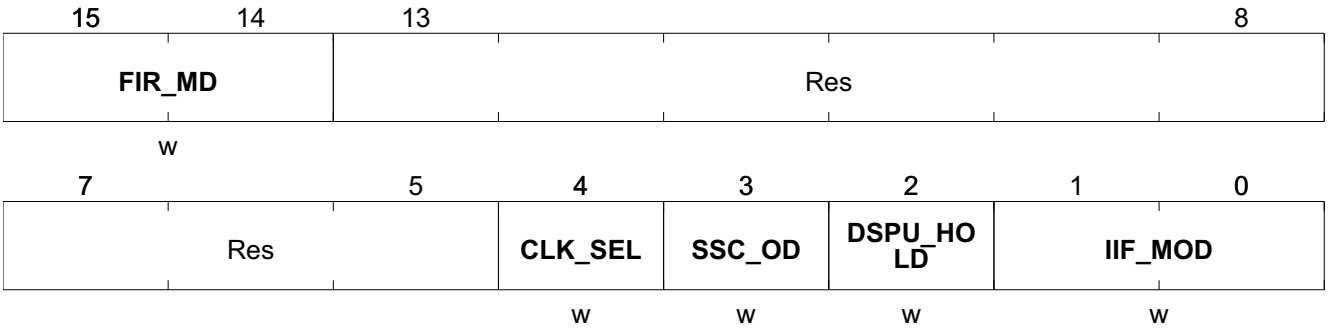
FSYNC	Offset	Reset Value
Frame Synchronization Register	**05_H**	**0000_H**



Field	Bits	Type	Description
FSYNC	15:9	wu	**Frame Synchronization Counter Value** Sub-counter within one frame. Reset: 0_H

Interface Mode1 Register

MOD_1	Offset	Reset Value
Interface Mode1 Register	**06_H**	**8001_H**



Field	Bits	Type	Description
FIR_MD	15:14	w	**Filter Decimation Setting (Update Rate Setting)** 00_B 21.3 µs (only for raw X/Y-values) 01_B 42.7 µs 10_B 85.3 µs 11_B 170.6 µs Reset: 10_B
CLK_SEL	4	w	**Clock Source Select** In absence of external clock or PLL out of lock, automatically switch to internal oscillator 0_B internal oscillator 1_B external 4-MHz clock Reset: 0_B
SSC_OD	3	w	**SSC Interface** 0_B Push-pull 1_B Open drain (default within TLE5012-E0318 and TLE5012-E0742) Reset: 0_B

Field	Bits	Type	Description
DSPU_HOLD	2	w	**Hold DSPU Operation** If DSPU is on hold, no WD reset is performed by DSPU. Deactivate watchdog with AS_WD before setting DSPU on hold. 0_B DSPU in normal schedule operation 1_B DSPU is on hold Reset: 0_B
IIF_MOD	1:0	w	**Incremental Interface Mode** 00_B IIF disabled 01_B A/B operation with Index on DATA 10_B Step/Direction operation with Index on DATA 11_B not allowed Reset: 01_B

SIL Register

SIL	Offset	Reset Value
SIL Register	07_H	0000_H

15	14	13	11	10	9	8
FILT_PAR	**FILT_INV**	Res		**FUSE_REL**	Res	
w	w			w		

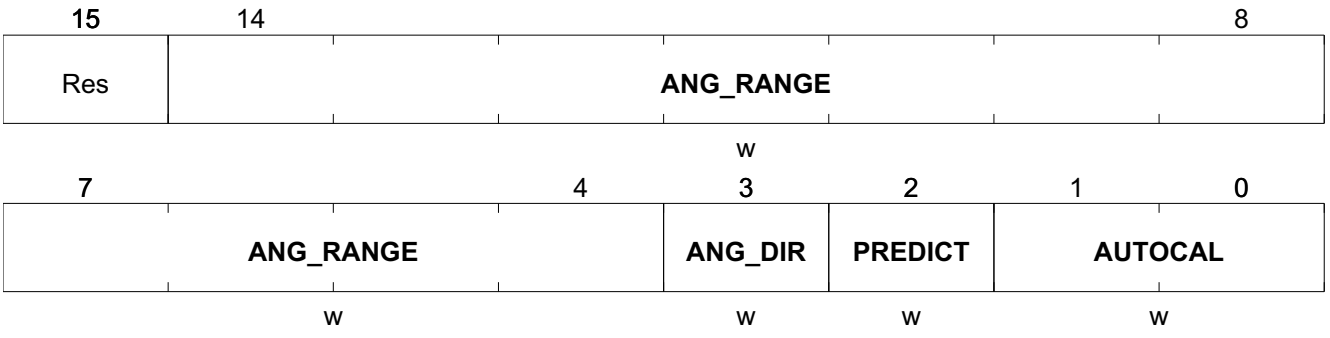
7	6	5	3	2	0
Res	**ADCTV_EN**	**ADCTV_Y**		**ADCTV_X**	
	w	w		w	

Field	Bits	Type	Description
FILT_PAR	15	w	**Filter Parallel** 0_B filter parallel disabled 1_B filter parallel enabled (source: X-value) Reset: 0_B
FILT_INV	14	w	**Filter Inverted** 0_B filter inverted disabled 1_B filter inverted enabled Reset: 0_B
FUSE_REL	10	w	**Fuse Reload** 0_B fuse reload disabled 1_B fuse parameters reloaded to DSPU at next cycle start Reset: 0_B

Field	Bits	Type	Description
ADCTV_EN	6	w	**ADC-Test vectors** 0_B ADC-Test vectors disabled 1_B ADC-Test vectors enabled Reset: 0_B
ADCTV_Y	5:3	w	**Test vector Y** 000_B 0V 001_B +70% 010_B +100% 011_B +Overflow 101_B -70% 110_B -100% 111_B -Overflow Reset: 0_H
ADCTV_X	2:0	w	**Test vector X** 000_B 0V 001_B +70% 010_B +100% 011_B +OV 101_B -70% 110_B -100% 111_B -OV Reset: 0_H

Interface Mode2 Register

MOD_2	Offset	Reset Value
Interface Mode2 Register	**08_H**	**0800_H**

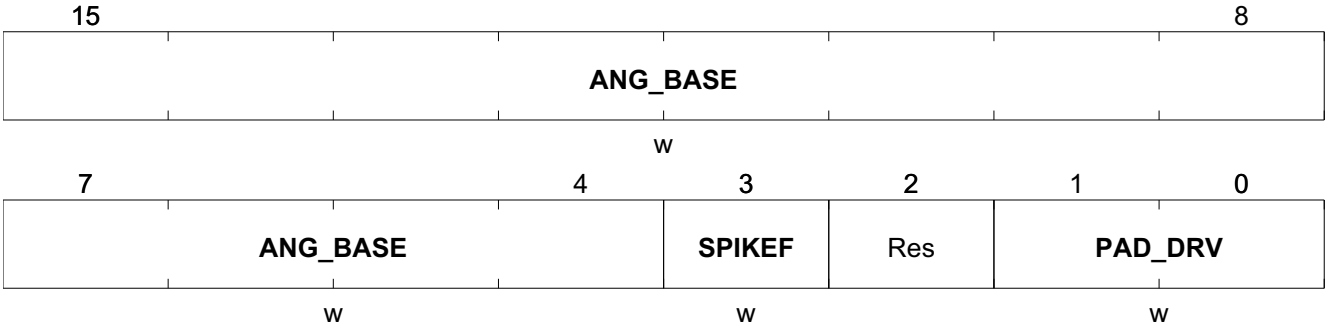


Field	Bits	Type	Description
ANG_RANGE	14:4	w	**Angle Range** Angle Range [°] = 360° * (2^7 / ANG_RANGE[digits]) 200_H represents 90° 080_H represents 360° Reset: 080_H

Field	Bits	Type	Description
ANG_DIR	3	w	**Angle Direction** 0_B counterclockwise rotation of magnet 1_B clockwise rotation of magnet Reset: 0_B
PREDICT	2	w	**Prediction** 0_B prediction disabled 1_B prediction enabled (default within TLE5012-E0318 and TLE5012-E0742) Reset: 0_B
AUTOCAL	1:0	w	**Autocalibration Mode** Autocalibration modes are described on Page 23. 00_B no autocalibration 01_B autocalibration mode 1 (default within TLE5012-E0318 and TLE5012-E0742) 10_B autocalibration mode 2 11_B autocalibration mode 3 Reset: 00_B

Interface Mode3 Register

MOD_3	Offset	Reset Value
Interface Mode3 Register	**09_H**	**0000_H**

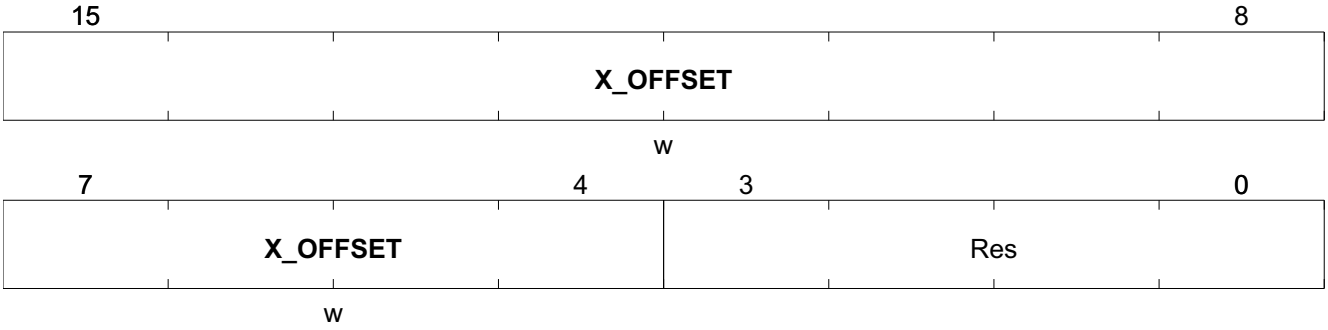


Field	Bits	Type	Description
ANG_BASE	15:4	w	**Angle Base** 800_H -180° 000_H 0° 001_H 0.0879° $7FF_H$ +179.912° Reset: 000_H
SPIKEF	3	w	**Analog Spike Filters of Input Pads** 0_B spike filter disabled 1_B spike filter enabled Reset: 0_B

Field	Bits	Type	Description
PAD_DRV	1:0	w	**Configuration of Pad-Driver** 00_B IFA/IFB: strong driver, DATA: strong driver, fast edge 01_B IFA/IFB: strong driver, DATA: strong driver, slow edge 10_B IFA/IFB: weak driver, DATA: medium driver, fast edge (default within TLE5012-E0318 and TLE5012-E0742) 11_B IFA/IFB: weak driver, DATA: weak driver, slow edge Reset: 00_B

Offset X Register

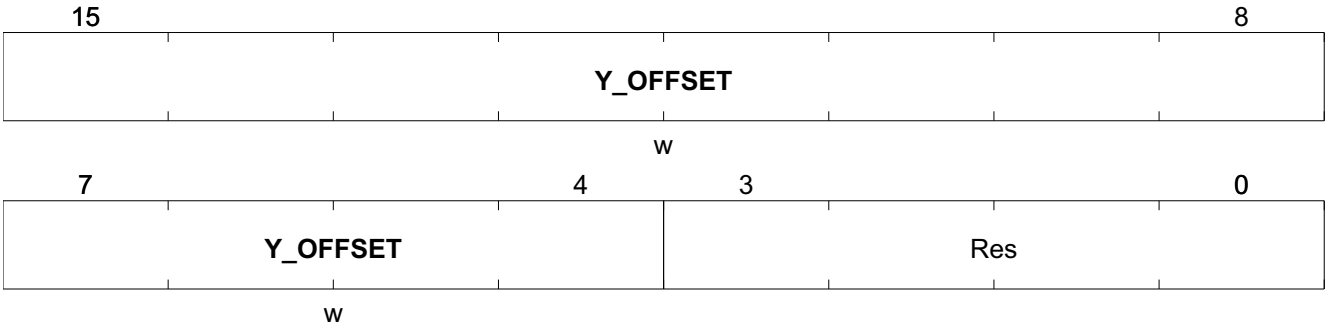
OFFX	Offset	Reset Value
Offset X	$0A_H$	0000_H



Field	Bits	Type	Description
X_OFFSET	15:4	w	**Offset Correction of X-value in digits** Reset: 0_H

Offset Y Register

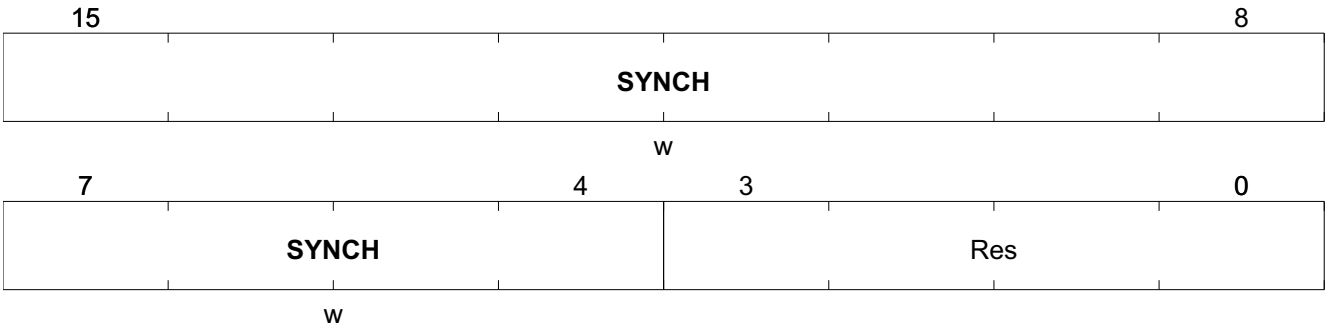
OFFY	Offset	Reset Value
Offset Y	$0B_H$	0000_H



Field	Bits	Type	Description
Y_OFFSET	15:4	w	**Offset Correction of Y-value in digits** Reset: 0_H

Synchronicity Register

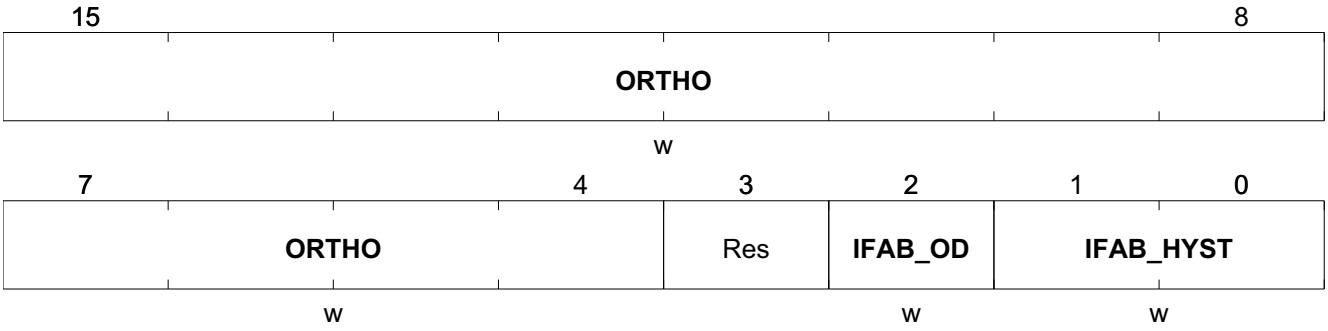
SYNCH	Offset	Reset Value
Synchronicity	$0C_H$	0000_H



Field	Bits	Type	Description
SYNCH	15:4	w	**Amplitude Synchronicity** $+2047_D$ 112.494% 0_D 100% -2048_D 87.500% Reset: 0_H

IFAB Register

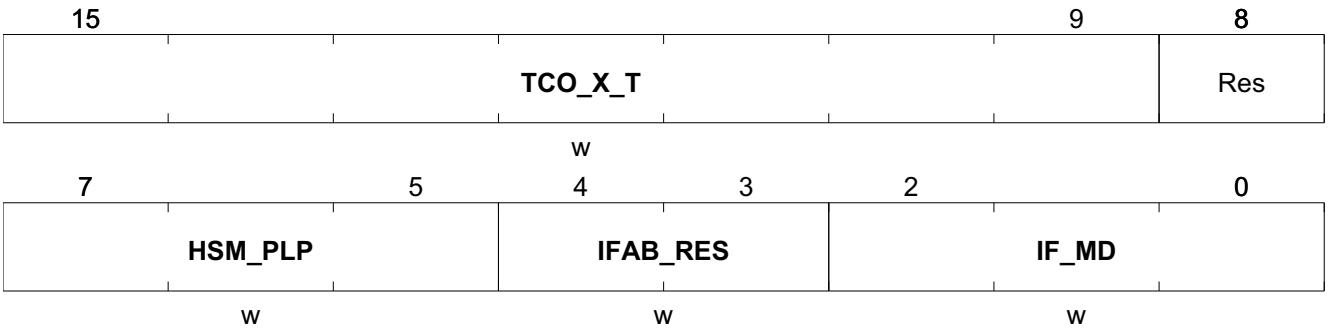
IFAB	Offset	Reset Value
IFAB Register	$0D_H$	0003_H



Field	Bits	Type	Description
ORTHO	15:4	w	**Orthogonality Correction of X and Y Components** $+2047_D$ 11.2445° 0_D 0° -2048_D -11.2500° Reset: 0_H
IFAB_OD	2	w	**IFA & IFB Open Drain** 0_B Push-pull 1_B Open drain (default within TLE5012-E0318 and TLE5012-E0742) Reset: 0_B
IFAB_HYST	1:0	w	**HSM Hysteresis** 00_B 0° 01_B 0.09° 10_B 0.27° 11_B 0.625° Reset: 11_B

Interface Mode4 Register

MOD_4	Offset	Reset Value
Interface Mode4 Register	$0E_H$	0000_H

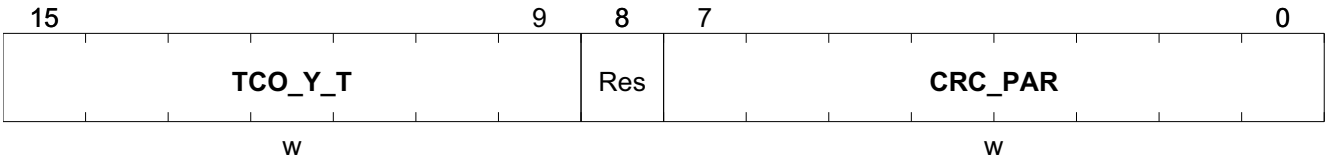


Field	Bits	Type	Description
TCO_X_T	15:9	w	**Offset Temperature Coefficient for X-Component** Reset: 0_H
HSM_PLP	7:5	w	**Hall Switch Mode; Pole pair Configuration** 000_B 2 pole pairs 001_B 3 pole pairs (default within TLE5012-E0318) 010_B 4 pole pairs 011_B 6 pole pairs 100_B 7 pole pairs (default within TLE5012-E0742) 101_B 8 pole pairs 110_B 12 pole pairs 111_B 16 pole pairs Reset: 000_B
IFAB_RES	4:3	w	**IFAB Resolution** 00_B 12 bit = 0.088° (244Hz) 01_B 11 bit = 0.176° (488Hz) 10_B 10 bit = 0.352° (977Hz) 11_B 9 bit = 0.703° (1953Hz) Reset: 00_B

Field	Bits	Type	Description
IF_MD	2:0	w	**Interface Mode** Selected by external circuit of CLK pin at Power-On Time. CLK pin connected to V_{DD} --> Incremental Interface is selected; CLK pin connected to GND --> IF_MD stored Interface is used. Switching to another interface during operation needs to stop the DSPU (DSPU_HOLD). *Note: Combinations not listed below are not allowed* 000_B SSC mode; IIF 001_B SSC mode; PWM 010_B SSC mode; HSM (default within TLE5012-E0318 and TLE5012-E0742) Reset: 000_B

Temperature Coefficient Register

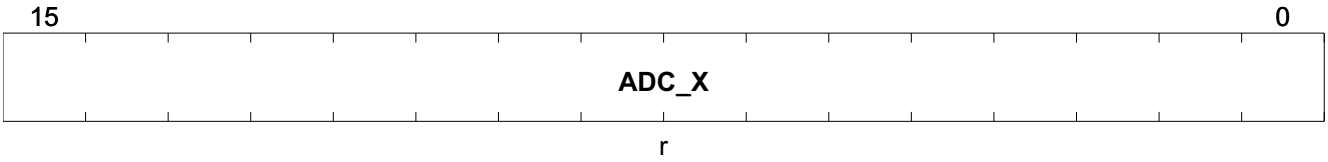
TCO_Y	Offset	Reset Value
Temperature Coefficient Register	**$0F_H$**	**0000_H**



Field	Bits	Type	Description
TCO_Y_T	15:9	w	**Offset Temperature Coefficient for Y-Component** Reset: 0_H
CRC_PAR	7:0	w	**CRC of Parameters** CRC of parameters from address 08_H to $0F_H$. When changing any settings within these registers, this CRC has to be updated. Reset: 0_H

X-raw Value Register

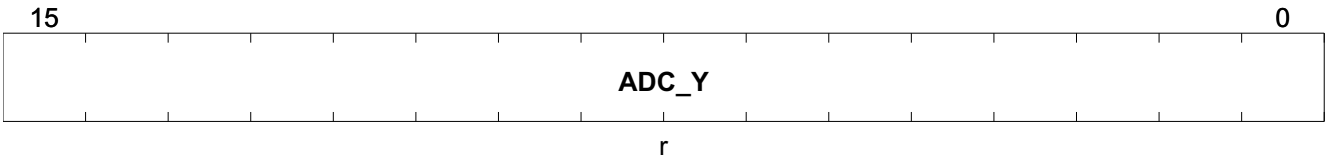
ADC_X	Offset	Reset Value
X-raw value	**10_H**	**0000_H**



Field	Bits	Type	Description
ADC_X	15:0	r	**ADC value of X-GMR** Read out of this register will update ADC_Y Reset: 0_H

Y-raw Value Register

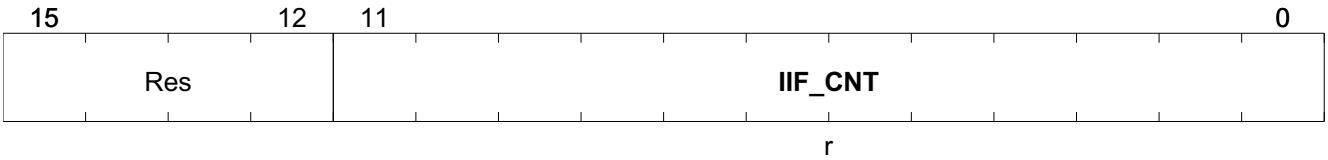
ADC_Y	Offset	Reset Value
Y-raw value	**11_H**	**0000_H**



Field	Bits	Type	Description
ADC_Y	15:0	r	**ADC value of Y-GMR** Updated when ADC_X or ADC_Y is read. Reset: 0_H

Increment Counter Register

IIF_CNT	Offset	Reset Value
IIF Counter value	**20_H**	**0000_H**



Field	Bits	Type	Description
IIF_CNT	11:0	r	**Counter value of increments** This value can be used for synchronization purposes between sensor and counter value on microcontroller side. Reset: 0_H

3.5.1.4 Communication Examples

This section gives some short SPI communication examples. The sensor has to be selected first via CSQ, and SCK must be available for the communication.

Table 19 SSC command to read the angle value

SSC Word No.	Description	Master transmitting	TLE5012 transmitting	Note
1	Command	1_0000_0_000010_0001		
2	Read Data		1_xxxxxxxxxxxxxxx	Read angle value
3	Safety Word		1_1_1_1_xxxx_xxxxxxxx	Read Safety Word

Table 20 SSC command to read angle speed and angle revolution

SSC Word No.	Description	Master transmitting	TLE5012 transmitting	Note
1	Command	1_0000_0_000011_0010		
2	Read Data		1_xxxxxxxxxxxxxxx	Read angle speed
3	Read Data		1_xxxxxx_xxxxxxxxx	Read angle revolution
4	Safety Word		1_1_1_1_xxxx_xxxxxxxx	Read Safety Word

Table 21 SSC command to change Interface Mode2 register

SSC Word No.	Description	Master transmitting	TLE5012 transmitting	Note
1	Command	0_1010_0_001000_0001		
2	Write Data	0_00010000000_1_0_01		ANG_Range: 080_H; ANG_DIR: 1_B; PREDICT: 0_B; AUTOCAL: 01_B
3	Safety Word		1_1_1_1_xxxx_xxxxxxxx	Read Safety Word

3.5.2 Pulse-Width Modulation Interface

The Pulse-Width Modulation (PWM) Interface can be selected via SPI.

The PWM update rate can be changed within the register $0E_H$ (IFAB_RES) in following steps:

- 0.25 kHz with 12-bit resolution
- 0.5 kHz with 12-bit resolution
- 1.0 kHz with 12-bit resolution
- 2.0 kHz with 12-bit resolution

PWM uses a square wave with constant frequency whose duty cycle is modulated, resulting in an average value of the waveform.

Figure 22 shows the principal behavior of a PWM with various duty cycles and the definition of timing values. The duty cycle of a PWM is defined by following general formulas:

$$Duty\ Cycle = \frac{t_{on}}{t_{PWM}}$$

$$t_{PWM} = t_{on} + t_{off}$$

$$f_{PWM} = \frac{1}{t_{PWM}} \quad (6)$$

The range between 0 - 6.25% and 93.75 - 100% is used only for diagnostic purposes. More details are given in **Table 22**.

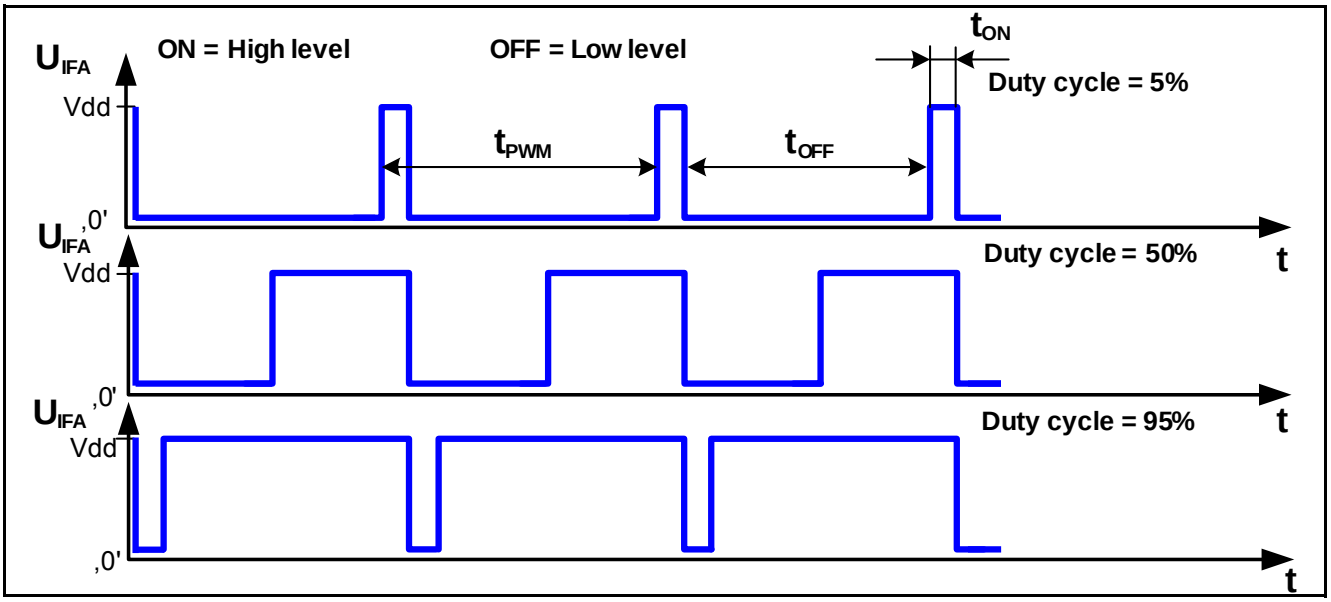


Figure 22 Typical Example for a PWM Signal

Table 22 PWM Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PWM output frequency	f_{PWM}	244	-	1953	Hz	selectable by IFAB_RES[1)2)]

Table 22 PWM Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output duty cycle range	DY_{PWM}	6.25	-	93.75	%	Absolute angle[2]
		-	2	-	%	Electrical error (S_RST; S_VR)[2]
		-	98	-	%	System error (S_FUSE; S_OV; S_XYOL; S_MAGOL; S_ADCT)[2]
		0	-	1	%	Short to GND[2]
		99	-	100	%	Short to V_{DD}, Power-Loss[2]
PWM period variation	t_{PWMvar}	-5	-	5	%	2)3)

1) $f_{PWM} = (f_{DIG} * 2^{IFAB\_RES}) / (24 * 4096)$
2) Not subject to production test - verified by design/characterization
3) Depends on internal oscillator frequency variation (**Section 3.4.6**)

3.5.3 Hall Switch Mode

The Hall Switch Mode (HSM) within the TLE5012 makes it possible to emulate the output of three Hall switches. Hall switches are often used in electrical commutated motors to get information about the rotor position. With these three output signals, the motor will be commutated in the right way. Depending on which pole pairs of the rotor are used, various electrical periods have to be utilized. This is selectable within $0E_H$ (HSM_PLP). Within the TLE5012-E0318 three pole pairs are fused; within the TLE5012-E0742, seven pole pairs are fused. **Figure 23** depicts the three output signals with the relationship between electrical angle and mechanical angle. The mechanical 0° point is always used as a reference.

The HSM is generally used with open-drain output, but it can be changed to push-pull within SSC_OD and IFAB_OD.

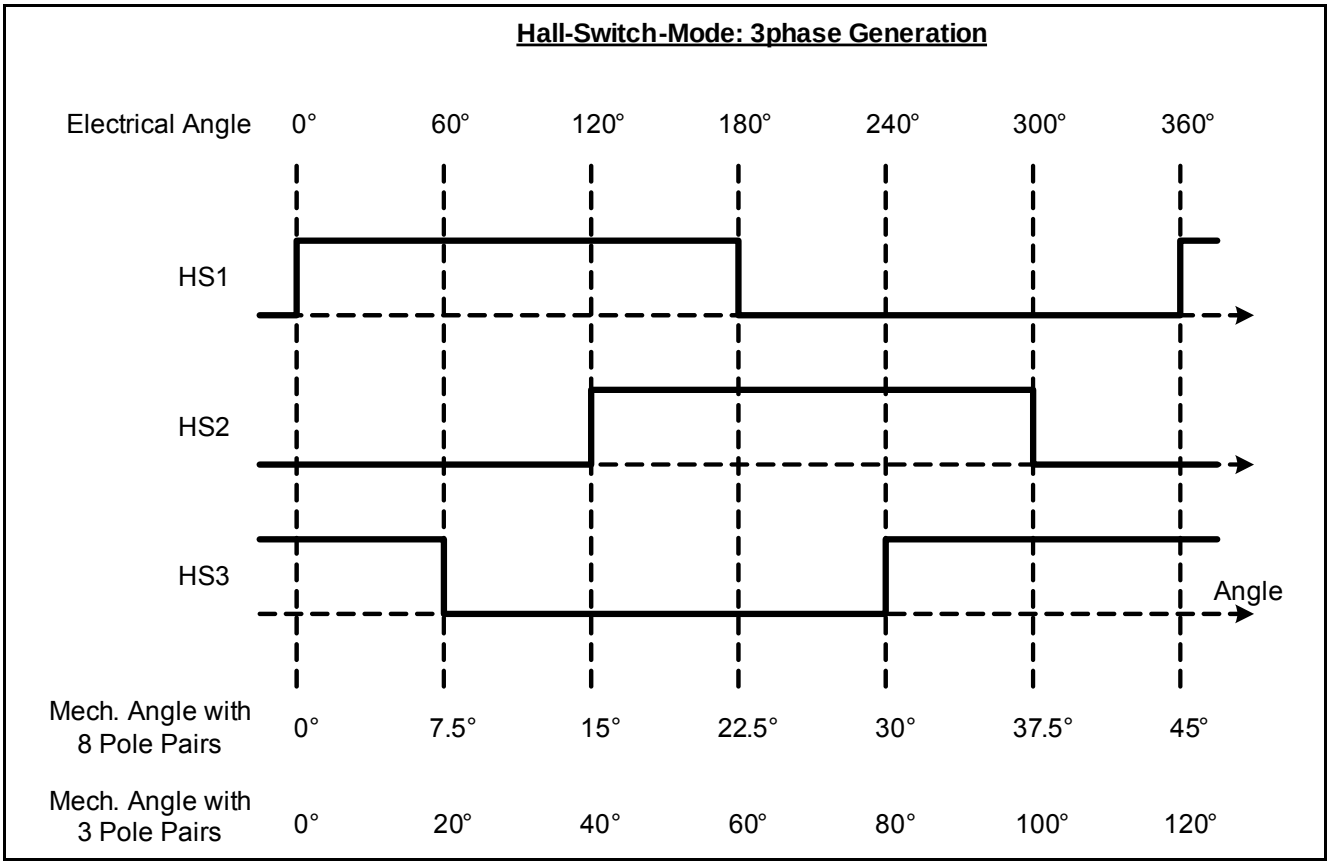


Figure 23 Hall Switch Mode

The HSM Interface can be selected by connecting CLK to GND, and CSQ has to be logic “1”.

Table 23 Hall Switch Mode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rotation speed	n	-	-	10000	rpm	2)

Table 23 Hall Switch Mode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Electrical angle accuracy	α_{elect}	-	1.2	2	°	2 pole pairs with autocalibration[1)2)]
		-	1.8	3		3 pole pairs with autocal.[1)2)]
		-	2.4	4		4 pole pairs with autocal.[1)2)]
		-	3.6	6		6 pole pairs with autocal.[1)2)]
		-	4.2	7		7 pole pairs with autocal.[1)2)]
		-	4.8	8		8 pole pairs with autocal.[1)2)]
		-	7.2	12		12 pole pairs with autocal.[1)2)]
		-	9.6	16		16 pole pairs with autocal.[1)2)]
Mechanical angle switching hysteresis	$\alpha_{HShystm}$	0	-	0.625	°	selectable by IFAB_HYST[2)3)4)]
Electrical angle switching hysteresis[5)]	$\alpha_{HShystel}$	-	1.25	-	°	2 pole pairs; IFAB_HYST=11[1)2)]
		-	1.88	-		3 pole pairs; IFAB_HYST=11[1)2)]
		-	2.50	-		4 pole pairs; IFAB_HYST=11[1)2)]
		-	3.75	-		6 pole pairs; IFAB_HYST=11[1)2)]
		-	4.38	-		7 pole pairs; IFAB_HYST=11[1)2)]
		-	5.00	-		8 pole pairs; IFAB_HYST=11[1)2)]
		-	7.50	-		12 pole pairs; IFAB_HYST=11[1)2)]
		-	10	-		16 pole pairs; IFAB_HYST=11[1)2)]
Fall time	t_{HSfall}	-	0.02	1	µs	R_L = 2.2 kΩ; C_L < 50 pF[2)]
Rise time	t_{HSrise}	-	0.4	1	µs	R_L = 2.2 kΩ; C_L < 50 pF[2)]

1) Depends on internal oscillator frequency variation (**Section 3.4.6**)
2) Not subject to production test - verified by design/characterization
3) GMR hysteresis not considered
4) Minimum hysteresis without switching
5) The hysteresis has to be considered only when rotation direction is changed.

To avoid toggling on the HS outputs during mechanical vibration of the rotor, hysteresis (IFAB_HYST) is recommended (**Figure 24**).

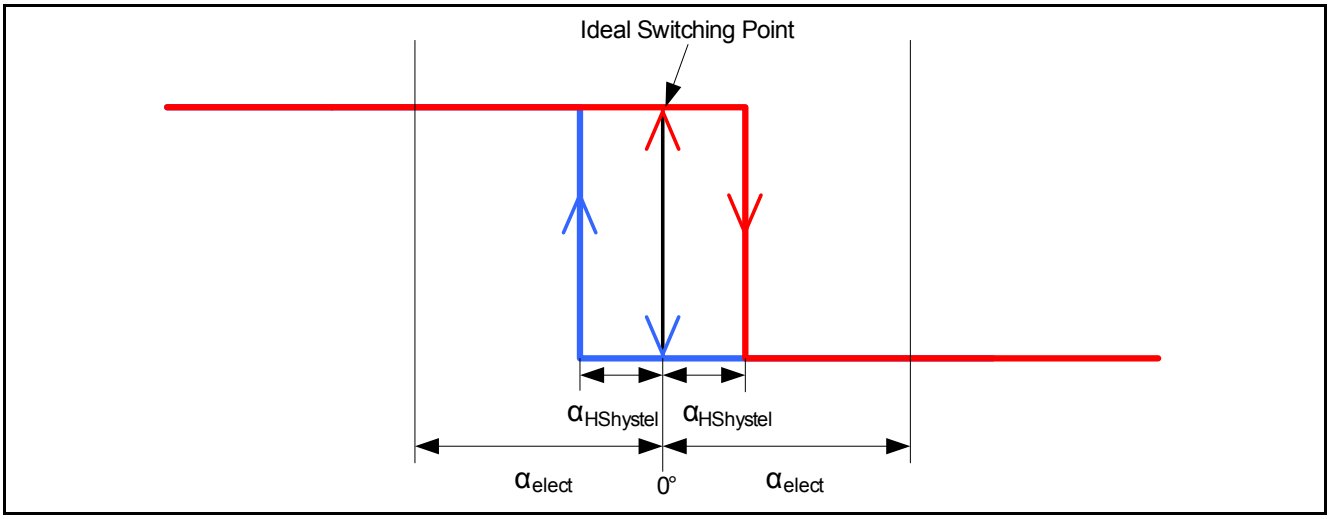


Figure 24 HS hysteresis

3.5.4 Incremental Interface

The Incremental Interface (IIF) uses an up/down counter of a microcontroller for the angle transmission. The synchronization is done by the parallel active SSC Interface. The angle value read out by the SSC Interface can be compared to the stored counter value. In case of a non-synchronization, the microcontroller adds the difference to the actual counter value to synchronize the TLE5012 with the microcontroller. The resolution of the IIF can be selected within the interface mode4 register (MOD_4) under IFAB_RES.

After startup, the IIF pulses out the actual absolute angle value to notify the microcontroller about the absolute position.

In register MOD_1 the IIF can be set in A/B mode or Step/Direction mode (IIF_MOD).

A/B Mode

The phase shift between phase A and B indicates a clockwise (A follows B) or a counterclockwise (B follows A) rotation of the magnet.

Step/Direction Mode

Phase A pulses out the increments and phase B indicates the direction (**Figure 25**).

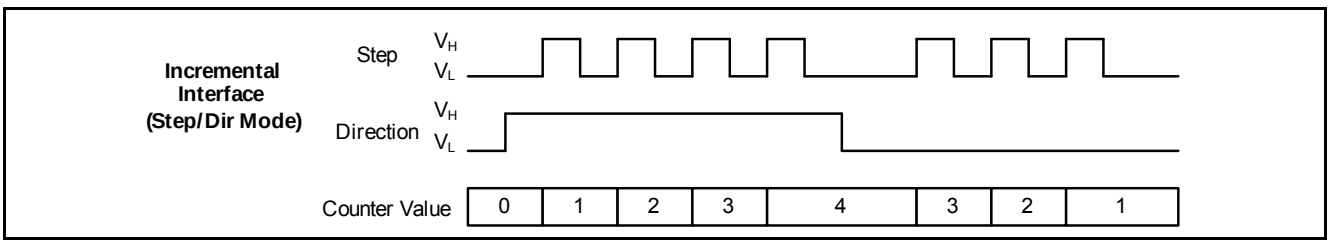


Figure 25 Incremental Interface with Step/Direction mode

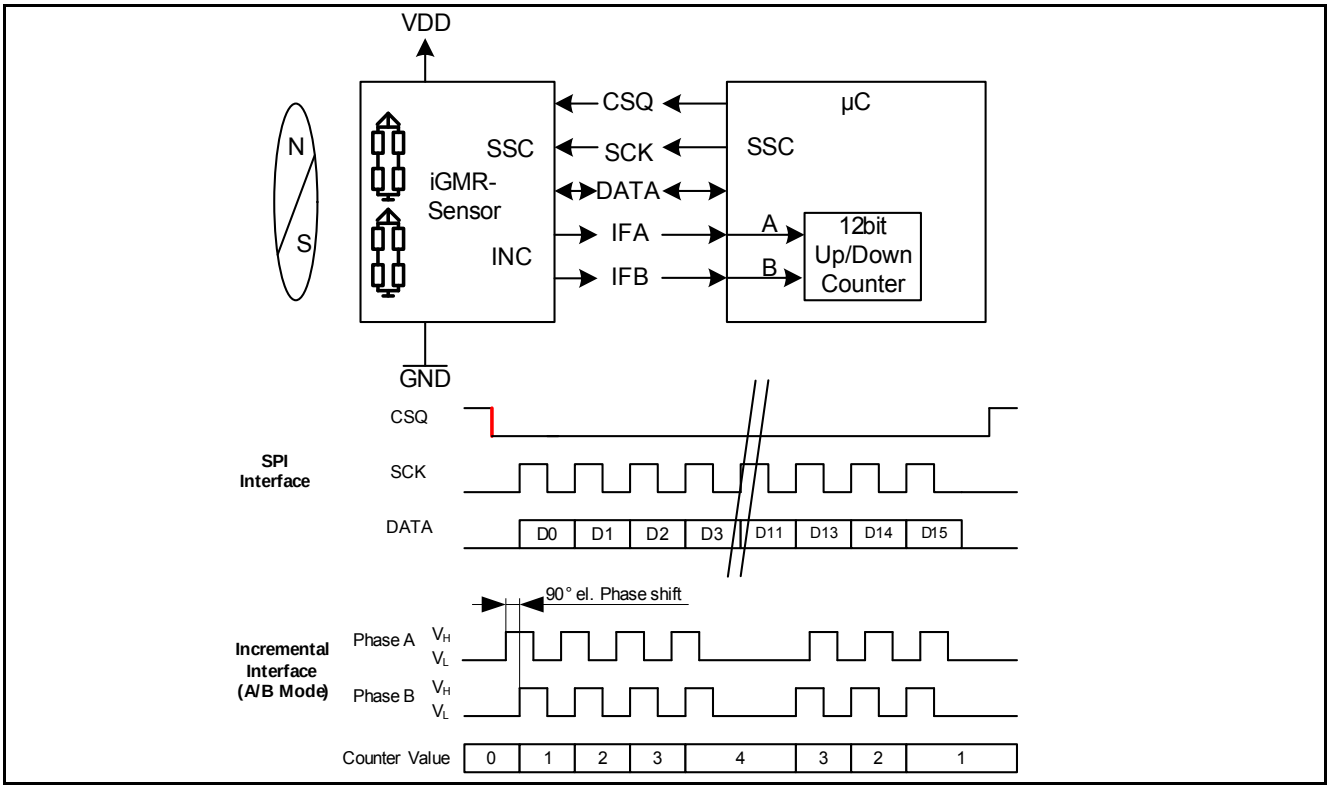


Figure 26 Incremental Interface Protocol with symbolic illustration of SPI Interface

Index Signal

The Index Signal is generated via the Data pin while CSQ is high (no SSC communication). The Index Signal is coded in quadrants via a PWM sequence, **Figure 27**.

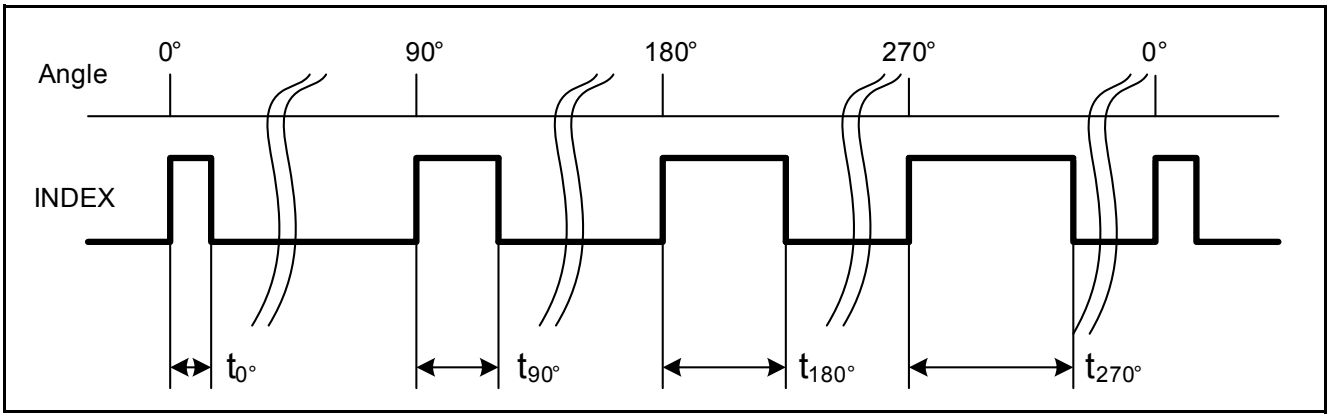


Figure 27 IIF index coding

Table 24 Incremental Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Incremental output frequency	f_{Inc}	-	-	1.0	MHz	Frequency of Phase A and Phase B[1)]

Table 24 Incremental Interface (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Index	$t_{0°}$	-	5	-	µs	0°[1]
	$t_{90°}$	-	10	-	µs	90°[1]
	$t_{180°}$	-	15	-	µs	180°[1]
	$t_{270°}$	-	20	-	µs	270°[1]

1) Not subject to production test - verified by design/characterization

3.6 Test Structure

3.6.1 ADC Test Vectors

It is possible to feed the ADCs with appropriate values to simulate a certain magnet position and other GMR effects. This test can be activated within the SIL register (ADCTV_EN). With ADCTV_Y and ADCTV_X the vector length can be adjusted as shown in **Figure 28**.

The values are generated with resistors on the chip.

The following X/Y ADC values can be programmed:

- 4 points, circle amplitude = 70% (0°,90°, 180°, 270°)
- 8 points, circle amplitude = 100% (0°, 45°, 90°, 135°, 180°, 225°, 270°, 315°)
- 8 points, circle amplitude = 122.1% (35.3°, 54.7°, 125.3°, 144.7°, 215.3°, 234.7°, 305.3°, 324.7°)
- 4 points, circle amplitude = 141.4% (45°, 135°, 225°, 315°)

Note: The 100% values typically correspond to 21700 digits and the 70% values to 15500 digits.

Table 25 ADC Test Vectors

Register bits	X/Y values (decimal)		
	min.	typ.	max.
000		0	
001		15500	
010		21700	
011		32767	
100[1]		0	
101		-15500	
110		-21700	
111		-32768	

1) Invalid

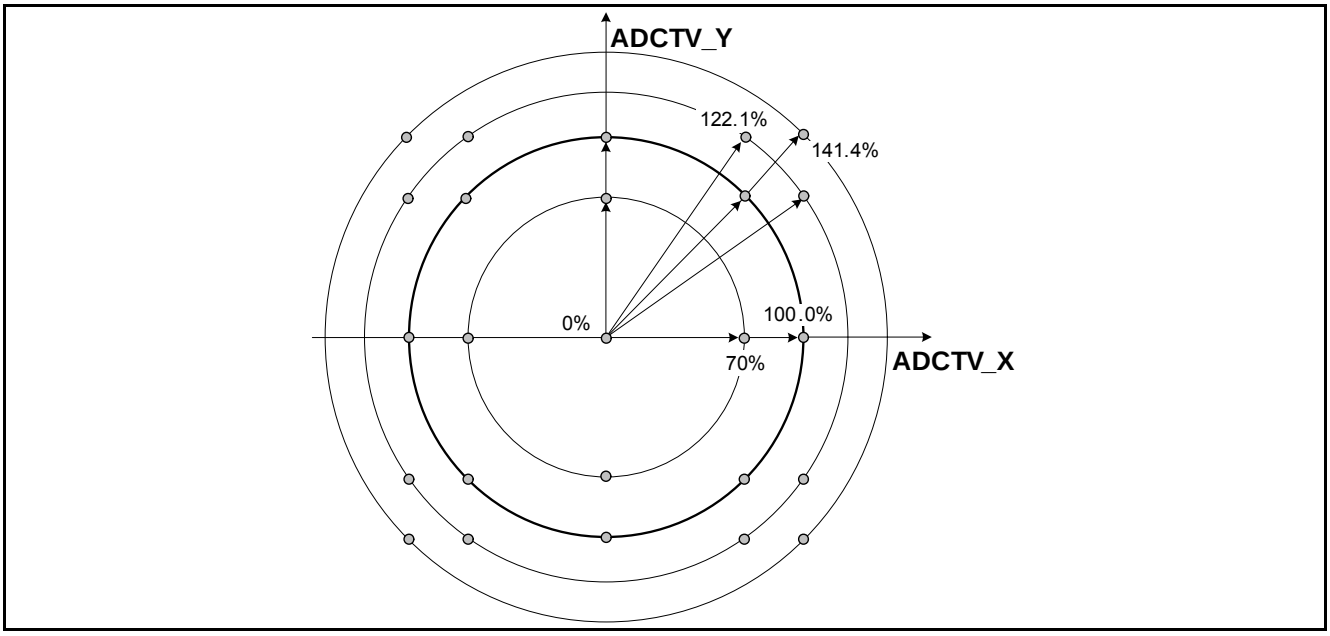


Figure 28 ADC test vectors

Examples for ADC test vector check

The sensor has to be selected first via CSQ and SCK must be available for the communication. **Table 26** shows the structure of the communication to enable the ADC test vector for 54.7°.

Table 26 SSC command to enable ADC test vector check

SSC Word No.	Description	Master transmitting	TLE5012 transmitting	Note
1	Command	0_1010_0_000111_0001		
2	Write Data	0_0_000_0_000_1_010_001		check of 54.7°
3	Safety Word		1_1_1_0_xxxx_xxxxxxxx	

Table 27 Structure of Write Data for some different test vectors

SSC Word No.	Description	Master transmitting	TLE5012 transmitting	Note
1	Write Data	0_0_000_0_000_1_001_101		~135°
2	Write Data	0_0_000_0_000_1_010_110		~135°
3	Write Data	0_0_000_0_000_1_101_110		~215.3°
4	Write Data	0_0_000_0_000_1_101_000		~270°
5	Write Data	0_0_000_0_000_1_101_010		~324.7°

3.7 Overvoltage Comparators

Various comparators monitor the voltage in order to ensure error-free operation. The overvoltage must be active at least 256 periods of t_{DIG} to set the test comparator bits in the SSC Interface registers. This serves as digital spike suppression.

Table 28 Test comparators

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overvoltage Detection	V_{OVG}	-	2.80	-	V	
	V_{OVA}	-	2.80	-	V	
	V_{OVD}	-	2.80	-	V	
V_{DD} Overvoltage	V_{DDOV}	-	6.05	-	V	
V_{DD} Undervoltage	V_{DDUV}	-	2.70	-	V	
GND - Off Voltage	V_{GNDoff}	-	-0.55	-	V	
V_{DD} - Off Voltage	V_{VDDoff}	-	0.55	-	V	
Spike Filter Delay	t_{DEL}	-	10	-	µs	1)

1) Not subject to production test - verified by design/characterization

3.7.1 Internal Supply Voltage Comparators

Every voltage regulator has an overvoltage (OV) comparator to detect a malfunction. If the nominal output voltage of 2.5 V is larger than V_{OVG}, V_{OVA} and V_{OVD}, then this overvoltage comparator is activated.

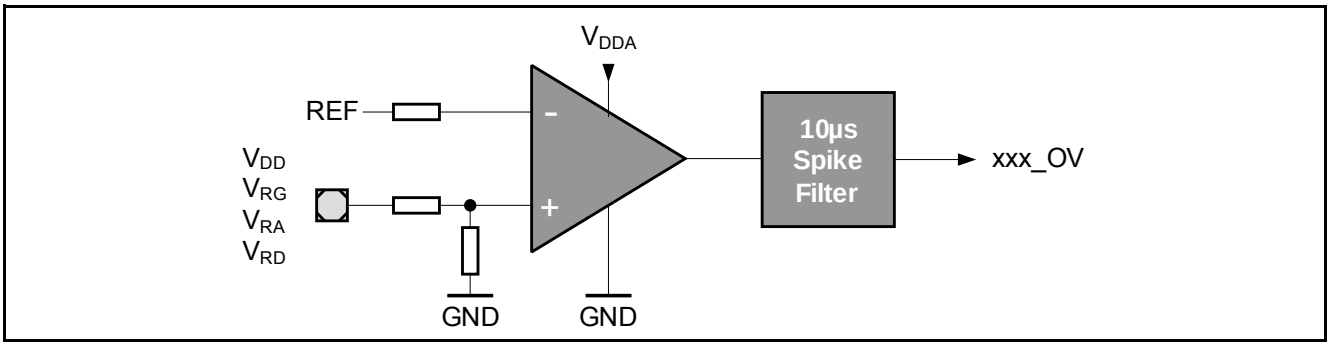


Figure 29 OV comparator

3.7.2 V_{DD} Overvoltage Detection

The Overvoltage Detection comparator monitors the external supply voltage at the V_{DD} pin. It activates the S_VR bit (**Figure 29**).

3.7.3 GND - Off Comparator

The GND - Off comparator is used to detect a voltage difference between the GND pin and SCK. It activates the S_VR bit of the SSC Interface. This circuit can detect a disconnection of the supply GND pin.

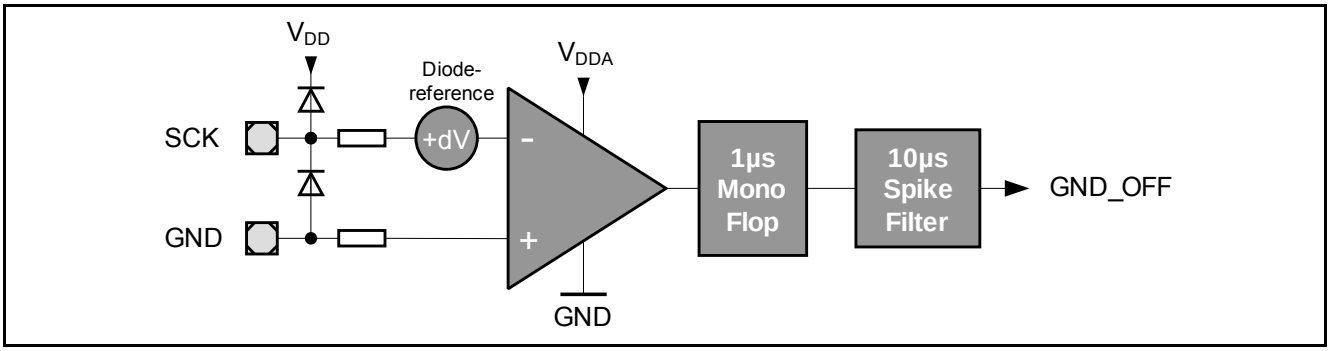


Figure 30 GND - Off comparator

3.7.4 V_{DD} - Off Comparator

The V_{DD} - Off comparator detects a disconnection of the VDD pin supply voltage. In this case, the TLE5012 is supplied by the SCK and CSQ input pins via the ESD structures. It activates the S_VR bit.

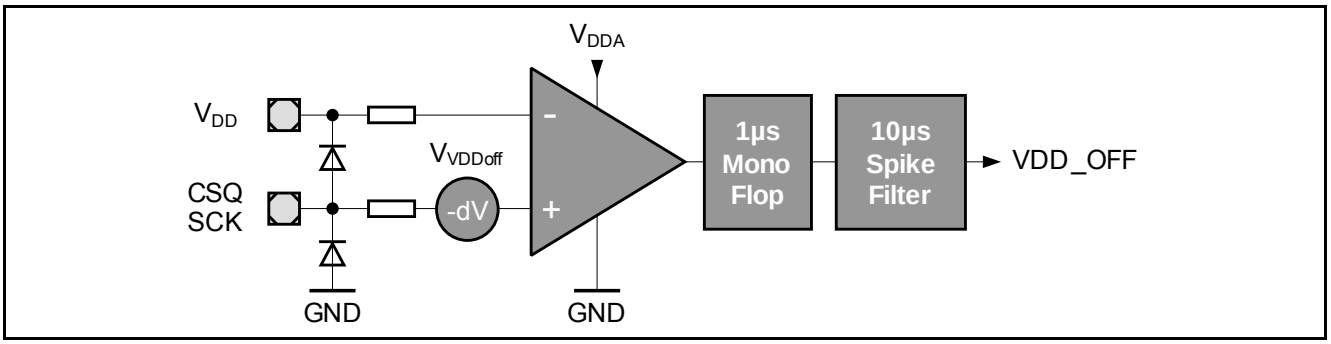


Figure 31 V_{DD} - Off comparator

4 Package Information

4.1 Package Parameters

Table 29 Package parameters

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Thermal resistance	R_{thJA}	-	150	200	K/W	Junction to air[1)]
	R_{thJC}	-	-	75	K/W	Junction to case
	R_{thJL}	-	-	85	K/W	Junction to lead
Soldering moisture level	MSL 3					260°C
Lead frame	Cu					
Plating	Sn 100%					> 7 µm

1) According to Jedec JESD51-7

4.2 Package Outline

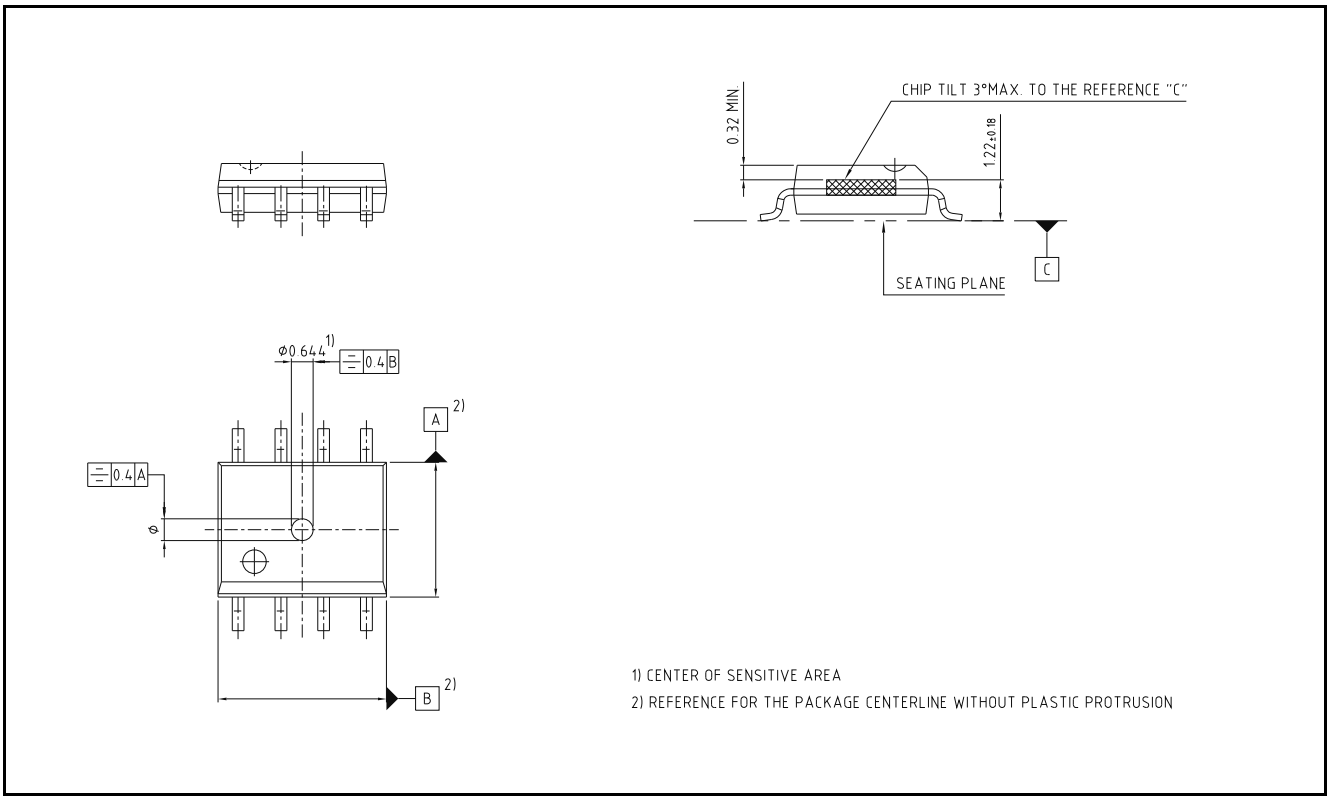


Figure 32 PG-DSO-8 package dimensions

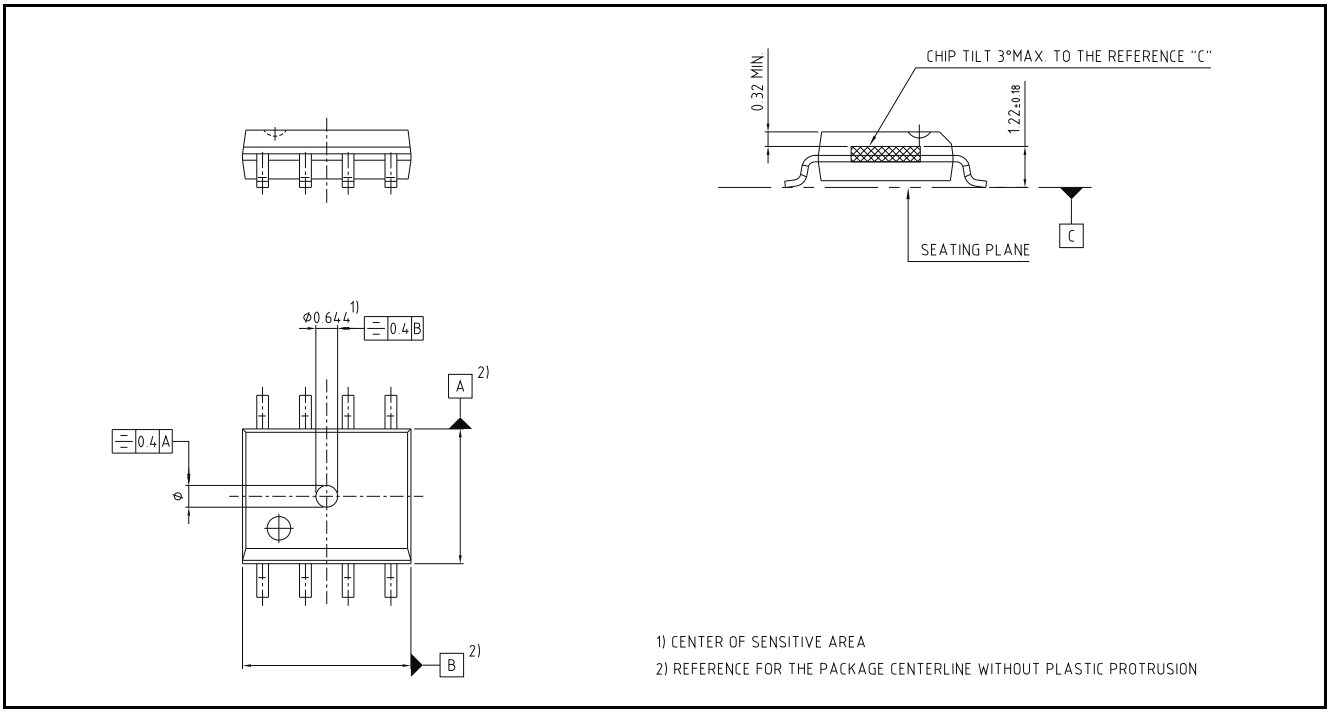


Figure 33 Position of sensing element

4.3 Footprint

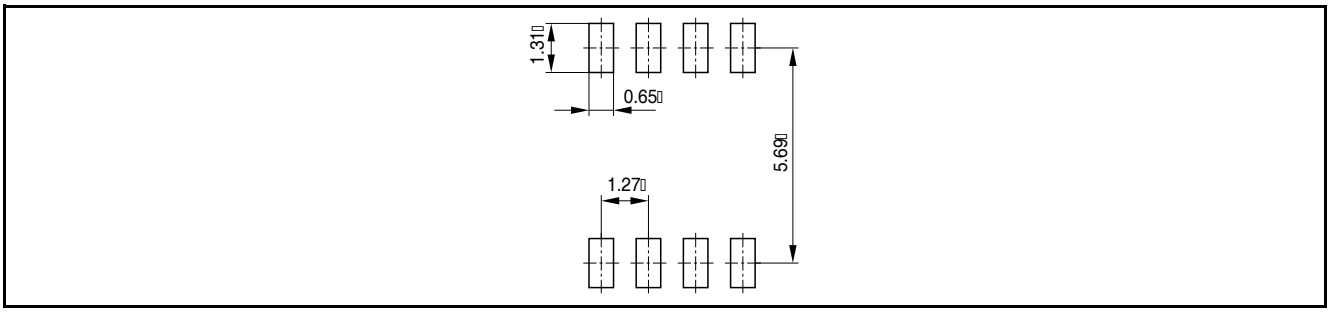


Figure 34 Footprint of PG-DSO-8

4.4 Packing

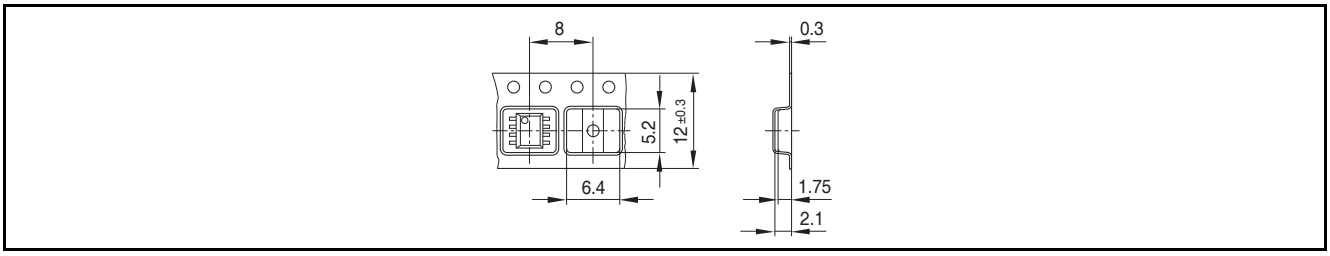


Figure 35 Tape and Reel

4.5 Marking

Position	Marking	Description
1st Line	5012xx	See ordering table on **Page 8**
2nd Line	xxx	Lot code
3rd Line	Gxxxx	G..green, 4-digit..date code

Processing

Note: For processing recommendations, please refer to Infineon's Notes on processing

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单击下面可查看定价，库存，交付和生命周期等信息

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