

# EiceDRIVER™ 2EDi product family

## Fast, robust, dual-channel, functional and reinforced isolated MOSFET gate-driver with accurate and stable timing

### Description

The EiceDRIVER™ 2EDi is a family of fast dual-channel isolated MOSFET gate-driver ICs providing functional (2EDFx) or reinforced (2EDSx) input-to-output isolation by means of coreless transformer (CT) technology. Due to high driving current, excellent common-mode rejection and fast signal propagation, 2EDi is particularly well suited for driving medium- to high-voltage MOSFETs (CoolMOS™, OptiMOS™, CoolSiC™) in fast-switching power systems.

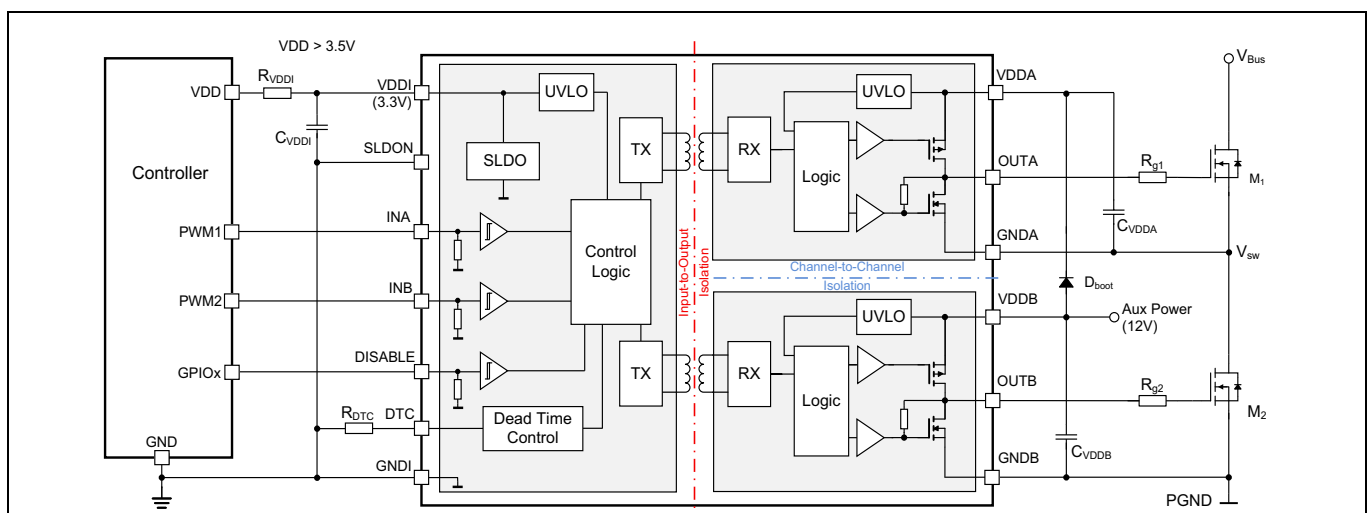
### Features

- 4 A / 8 A or 1 A / 2 A source / sink output current
- Up to 10 MHz PWM switching frequency
- PWM signal propagation delay typ. 37 ns with
  - 3 ns channel-to-channel mismatch
  - +7/-6 ns propagation delay variance
- Resistor-programmable Dead Time Control (DTC) ranging from 15 ns to 250 ns
- Common Mode Transient Immunity CMTI >150 V/ns
- Fast safety turn-off in case of input side Undervoltage Lockout (UVLO)
- Output supply voltage from 4.5 V to 20 V with 4 V or 8 V UVLO threshold
- Wide temperature operating range  $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$
- RoHS compliant wide /narrow-body (WB/NB) DSO16 and 5 mm x 5 mm LGA packages
- Fully qualified according to JEDEC for Industrial Applications



### Isolation and safety certificates

- **2EDSx with reinforced isolation:**
  - DIN VDE V 0884-10 (2006-12) compliant with  $V_{IOTM} = 8 \text{ kV}_{pk}$  and  $V_{IOSM} = 6.25 \text{ kV}_{pk}$  (tested at  $10 \text{ kV}_{pk}$ )
  - certified according to UL1577 (Ed. 5) opto-coupler component isolation standard with  $V_{ISO} = 5700 V_{RMS}$
  - certified according to DIN EN 62368-1 and DIN EN 60950-1 and corresponding CQC certificates
  - certified according to EN 61010-1 (reinforced isolation,  $300 V_{RMS}$  mains voltage, overvoltage category III)
  - certified according to EN 60601-1 (2 MOPP,  $250 V_{RMS}$  mains voltage, overvoltage category II)
- **2EDFx with functional isolation:** Production test with  $1.5 \text{ kV}_{DC}$  for 10 ms



**Potential Applications**

- Server, telecom and industrial SMPS
- Synchronous rectification, brick converters, UPS and battery storage
- EV charging industry automation, motor drives and power tools

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**Description**

**1 Description**

The gate drivers of the EiceDRIVER™ 2EDi product family are designed for fast-switching, medium to high power systems with MOSFET switches. They are optimized for high timing accuracy over temperature and production spread. The reliable accurate timing simplifies system design and provides better power conversion efficiency.

The 2EDSx, 2EDFx dual-channel reinforced (safe) and functional isolated product variants are available with different drive strengths: 4 A/8 A for low-ohmic power MOSFETs, 1 A/2 A for higher  $R_{on}$  MOSFETs or slower switching transients (EMI). The 1 A/2 A reinforced isolation driver can also be used as a PWM Data Coupler in combination with a non-isolated boost gate driver such as 1EDNx 4 A/8 A placed in closest proximity to the Superjunction power switches.

Two independent and galvanically isolated gate driver channels ensure that all 2EDi versions can be used in any possible configuration of low- and high-side switches.

Improved system robustness is supported by min. 150 V/ns Common Mode Transient Immunity (CMTI), PWM inputs with 18 ns noise filter, UVLO on output side including a safety self-lock-down of driver outputs in case of input UVLO ( $V_{DDI} < 3 V$ ), PWM outputs with up to 5 A peak reverse current capability and an intrinsically robust gate driver design.

**1.1 EiceDRIVER™ 2EDi product family device overview**

**Table 1 EiceDRIVER™ 2EDi product family device overview**

Part number <sup>1)</sup>	Package	Source/sink current	UVLO	Input-to-output isolation				DTC
				Isolation class	Rating	Surge testing	Safety certification <sup>2)</sup>	
2EDF7275F	NB-DSO16 10mm x 6mm	4 A/8 A	4 V	Functional	$V_{IO} = 1.5 kV_{DC}$	n.a	n.a	no
2EDF8275F			8 V					no
2EDF9275F			13 V					no
2EDF7175F		1 A/ 2 A	4 V					no
2EDF7275K	LGA13 5mm x 5mm	4 A/8 A	4 V					no
2EDF7235K			yes					
2EDS8265H	WB-DSO16 10.3mm x 10.3mm	4 A/8 A	8 V	Reinforced	$V_{IOTM} = 8 kV_{pk}$ (VDE0884-10 <sup>3)</sup> )	$V_{IOSM} = 10 kV_{pk}$ (IEC60065)	VDE0884-10 <sup>3)</sup> UL1577 EN 60950-1, EN 62368-1, EN 61010-1	no
2EDS9265H			13 V					no
2EDS7165H			4 V					no
2EDS8165H		1 A/2 A	8 V					no

1) for device ordering information and device marking see **Chapter 7.1, Table 31**

2) for 2EDS9265H and 2EDS7165H, only the UL 1577 certification is planned (and pending)

3) tested according to VDE0884-10 specifications with certification no longer available due to standard expiration

The 2EDi product table is provided as a first quick device selection guide; more detailed specifications are provided in the product features, package dimension and testing chapters of this datasheet.

Find current information on configurations and application notes under [www.infineon.com/2EDi](http://www.infineon.com/2EDi)

**Description**

**1.2 Input-to-output isolation testing**

- 2EDSx Reinforced isolation (2EDSx in WB PG-DSO-16-30 package), for details see [Table 26](#) to [Table 29](#).
  - 8 kV<sub>pk</sub> transient isolation voltage applied according to DIN V VDE V 0884-10 (2006-12)
  - 10 kV<sub>pk</sub> surge isolation tested with 25 positive and 25 negative pulses according to VDE-0884-10
- Functional isolation (2EDFx in NB PG-DSO-16-11 and PG-TFLGA-13-1 packages), for details see [Table 21](#) to [Table 23](#)
  - Production test with 1.5 kV<sub>DC</sub> for 10 ms

**1.3 Channel-to-channel isolation testing**

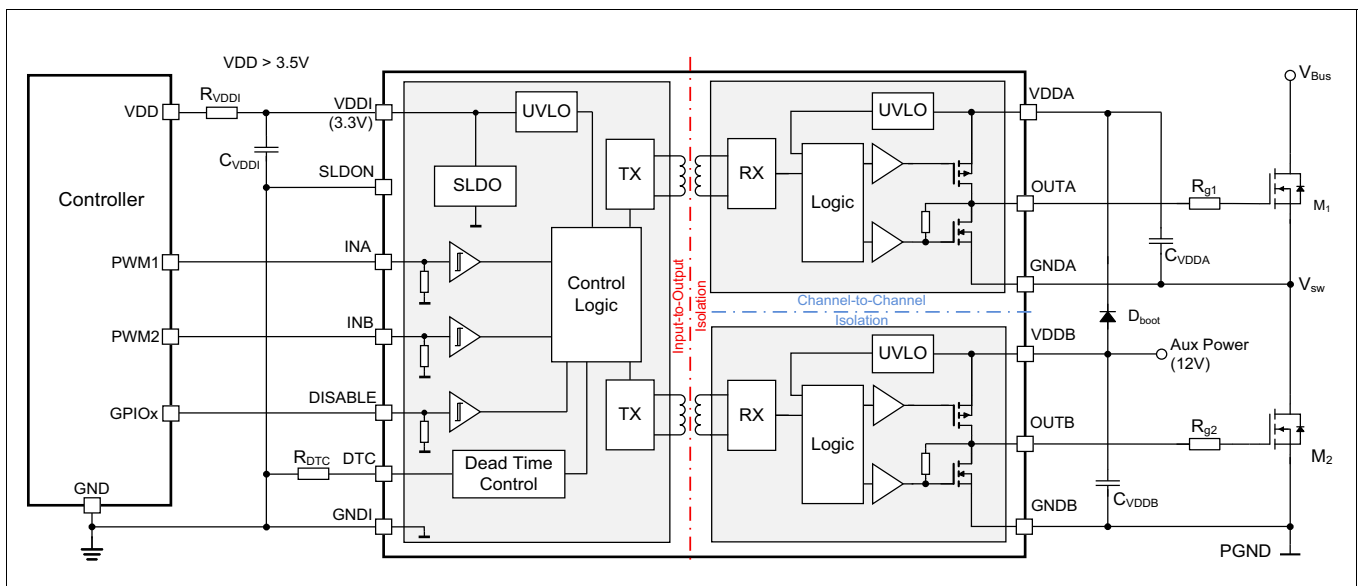
- The functional isolation between the two channels are verified by the following tests
  - sample test with 1.5 kV<sub>DC</sub> for 10 ms (NB PG-DSO-16-11, WB PG-DSO-16-30)
  - sample test with 0.65 kV<sub>DC</sub> for 10 ms (PG-TFLGA-13-1)

**1.4 Application overview and system block diagram**

2EDi gate drivers are perfectly suited to substitute bulky pulse transformers and drive power MOSFETs in half-bridge configuration as depicted in [Figure 1](#).

The input side is usually powered by the same power supply as the PWM controllers (VDDI = 3.3 V or VDDI > 3.5 V if SLDO is activated). The output-side gate driver voltages VDDA, VDDB are generated by separate isolated auxiliary supplies. In some topologies like LLC, the high side driver supply VDDA can be generated via a bootstrapping circuitry.

For further application implementation guidance please refer to dedicated application notes.



**Figure 1 Typical application with 5 V controller and bootstrapped high-side VDDA**

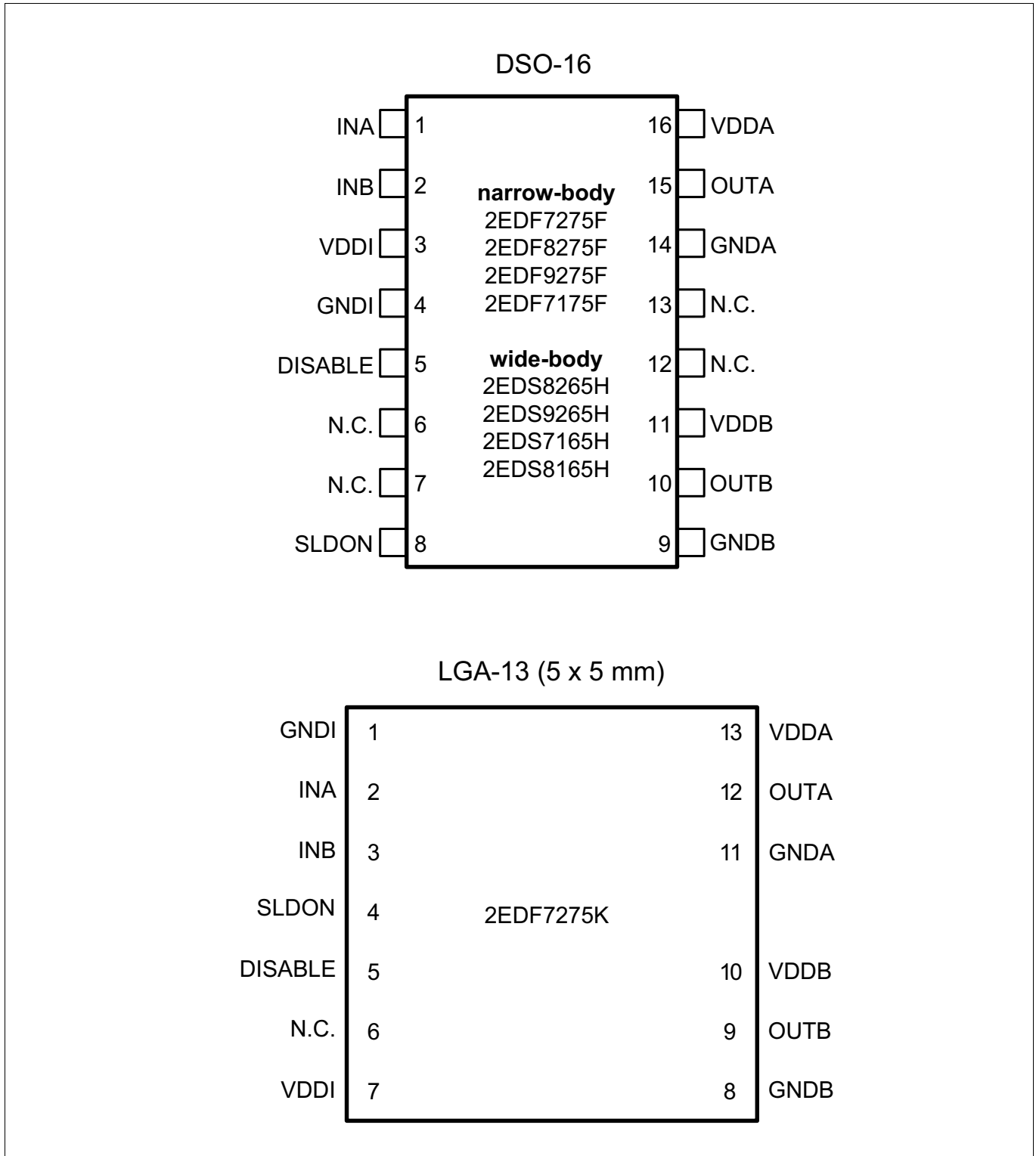
**Pin configurations by device type**

**2 Pin configurations by device type**

Functional behavior and electrical characteristics are independent of package configuration

**2.1 Pin configuration for dual-channel input mode with (with DISABLE, SLDON)**

The pin configurations for the different package variants 2EDFx75F, 2EDF7x75K and 2EDSxx65H are outlined in **Figure 2**.



**Figure 2 Pin configuration DSO-16 and LGA-13 packages (2EDF7x75F, 2EDF7x75K and 2EDF8x65H)**

**EiceDRIVER™ 2EDi product family**  
**2EDSx reinforced, 2EDFx functional isolated 4A/8A, 1A/2A gate drivers**

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**Pin configurations by device type**

(Top view, figure is not to scale)

**Pin configurations by device type**

For package drawing details see [Chapter 7 Package](#).

**Table 2 Pin description for dual-channel input mode (with DISABLE, SLDON)**

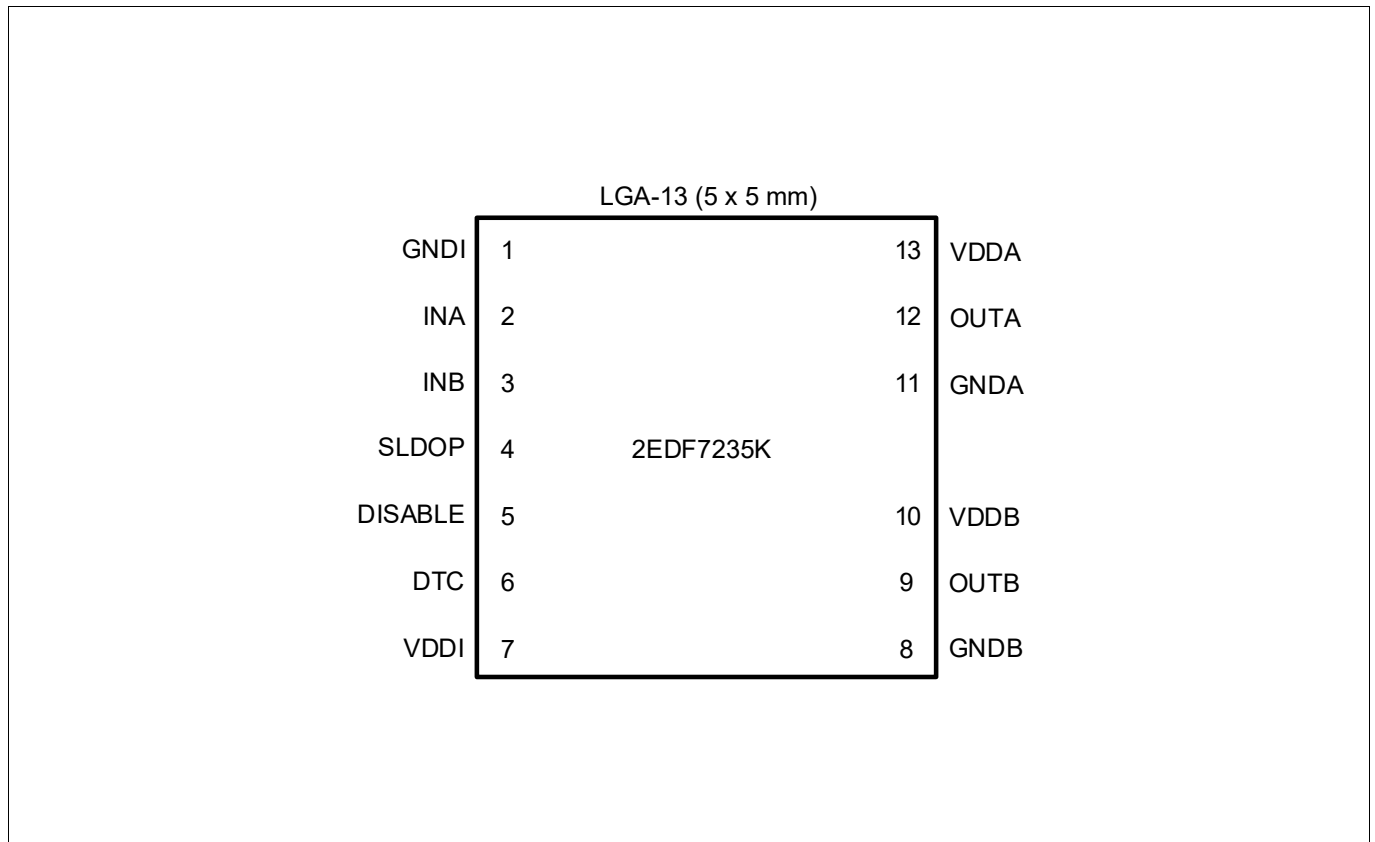
Pin# DSO	Pin# LGA	Symbol	Description
1	2	INA	Digital CMOS / TTL logic signal input for channel A with internal pull-down resistor to GNDI If channel is not used it is recommended to connect pin to GNDI (see <a href="#">Chapter 3.4</a> )
2	3	INB	Digital CMOS / TTL logic signal input for channel B with internal pull-down resistor to GNDI If channel is not used it is recommended to connect pin to GNDI (see <a href="#">Chapter 3.4</a> )
3	7	VDDI	Supply voltage (input side) 3.3 V (Internal SLDO available) It is recommended to place a bypass capacitor from VDDI to GNDI (see <a href="#">Chapter 3.3.1</a> )
4	1	GNDI	Ground input side (all signals on input side are referenced to this pin) (see <a href="#">Chapter 3.3.1</a> )
5	5	DISABLE	Digital CMOS / TTL logic input for both channels A and B; logic input high disables both output channels Internal pull-down resistor (see <a href="#">Chapter 3.4</a> )
6	6	N.C.	Not connected; keep pin floating
7	-	N.C.	Not connected; keep pin floating
8	4	SLDON	Default 3.3 V supply selected, if N.C. or connected to VDDI If SLDON pin is connected to GNDI, SLDO is activated and a supply voltage higher than 3.5 V can be used (see <a href="#">Chapter 3.3.1</a> ) Internal pull-up resistor to VDDI; hard-wired PCB connection recommended
9	8	GNDB	Ground for output channel B
10	9	OUTB	Output gate driver for channel B
11	10	VDDB	Supply voltage for output channel B It is recommended to place a bypass capacitor from VDDB to GNDB (see <a href="#">Chapter 3.3.2</a> )
12	N.P.	N.C.	Not present; not connected; for channel-to-channel isolation
13	-	N.C.	Not connected; for channel-to-channel isolation
14	11	GNDA	Ground for output channel A
15	12	OUTA	Output gate driver for channel A
16	13	VDDA	Supply voltage for output channel A It is recommended to place a bypass capacitor from VDDA to GNDA (see <a href="#">Chapter 3.3.2</a> )



**Pin configurations by device type**

**2.2 Pin configuration for dual-channel input mode (with DISABLE, SLDOP, DTC)**

The pin configuration for the LGA-version with Dead Time Control (2EDF7235K) is outlined in **Figure 3**



**Figure 3 Pin configuration dual-channel input mode (with DISABLE, SLDOP, DTC) for 2EDF7235K**  
 (Top view, Figure is not to scale)

**Pin configurations by device type**

For package drawing details see [Chapter 7 Package](#).

**Table 3 Pin description for dual-channel input mode (with DISABLE, SLDOP, DTC)**

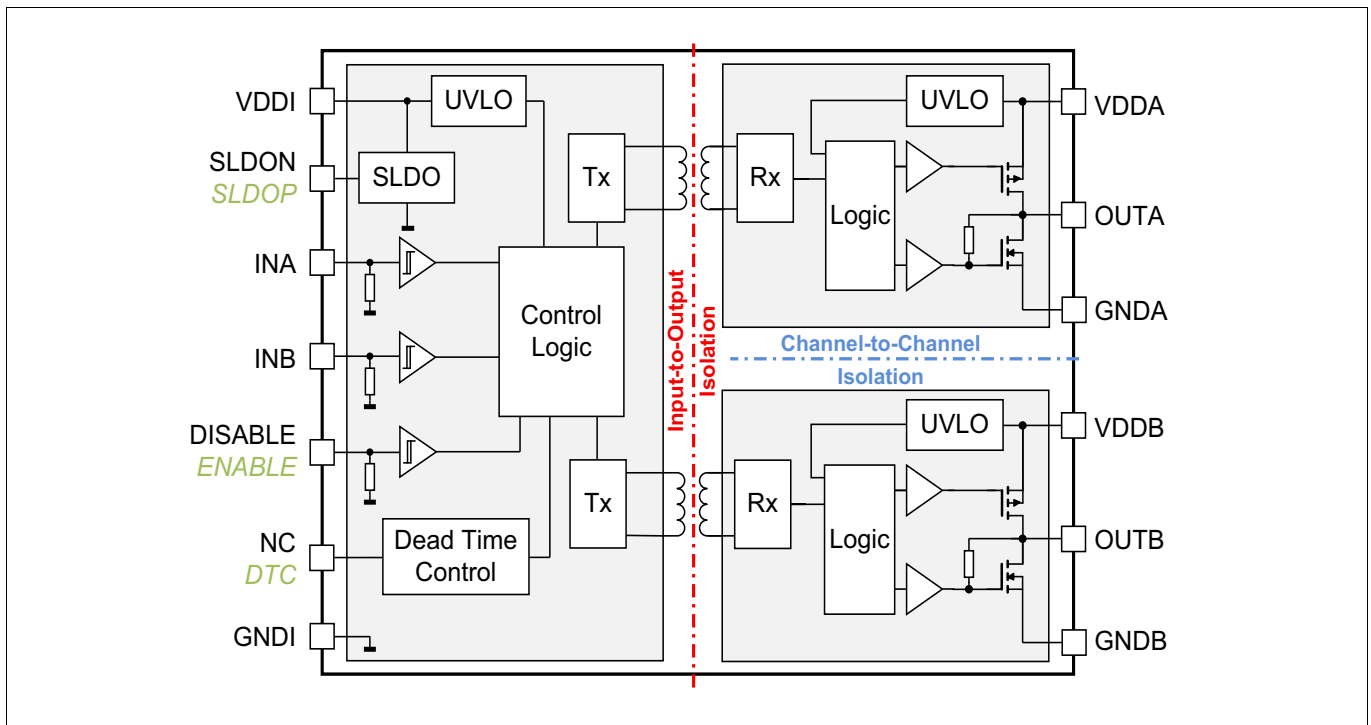
Pin# LGA	Symbol	Description
2	INA	Digital CMOS / TTL logic signal input for channel A with internal pull-down resistor to GNDI If channel is not used it is recommended to connect pin to GNDI (see <a href="#">Chapter 3.4</a> )
3	INB	Digital CMOS / TTL logic signal input for channel B with internal pull-down resistor to GNDI If channel is not used it is recommended to connect pin to GNDI (see <a href="#">Chapter 3.4</a> )
7	VDDI	Supply voltage (input side) 3.3 V (Internal SLDO available) It is recommended to place a bypass capacitor from VDDI to GNDI (see <a href="#">Chapter 3.3.1</a> )
1	GNDI	Ground input side (all signals on input side are referenced to this pin) (see <a href="#">Chapter 3.3.1</a> )
5	DISABLE	Digital CMOS / TTL logic input for both channels A and B Logic input high disables both output channels Internal pull-down resistor (see <a href="#">Chapter 3.4</a> )
6	DTC	Dead time control Programmable from 15 ns to 350 ns via resistor to GNDI see <a href="#">Chapter 3.8 Dead Time Control</a> Internal pull-up resistor; no connection or connection to VDDI disables DTC functionality
4	SLDOP	Default mode: supply voltage > 3.5V (with external shunt resistor), if pin N.C. or connected to VDDI If SLDOP pin is connected to GNDI SLDO Operation is deactivated, for use with 3.3 V supply on VDDI(see <a href="#">Chapter 3.3.1</a> ) Internal pull-up resistor to VDDI; hard-wired PCB connection recommended
8	GNDB	Ground for output channel B
9	OUTB	Output gate driver for channel B
10	VDDB	Supply voltage for output channel B It is recommended to place a bypass capacitor from VDDB to GNDB (see <a href="#">Chapter 3.3.2</a> )
-	N.P.	Not present; for channel-to-channel isolation creepage requirements
11	GNDA	Ground for output channel A
12	OUTA	Output gate driver for channel A
13	VDDA	Supply voltage for output channel A It is recommended to place a bypass capacitor from VDDA to GNDA (see <a href="#">Chapter 3.3.2</a> )

**Functional description**

### 3 Functional description

#### 3.1 Block diagram

A simplified functional block diagram for the the EiceDRIVER™ 2EDi gate-driver family is given in **Figure 4**.



**Figure 4 EiceDRIVER™ 2EDi product family block diagram**

#### 3.2 Input-to-output isolation

All EiceDRIVER™ 2EDi dual-channel isolated products are tested in accordance with their respective isolation class.

- **2EDFx for functional isolation**, typically used as primary-side controlled galvanically isolated driver.  
 Device part numbers: 2EDFxxxxK (2EDF7275K, 2EDF7235K) and 2EDFxxxxF (2EDF7275F, 2EDF8275F, 2EDF9275F, 2EDF7175F)
- **2EDSx for reinforced safe isolation**, typically used as secondary-side controlled isolated gate driver.  
 Device part numbers: 2EDSxxxH (2EDS7165H, 2EDS8165H, 2EDS9265H, 2EDS8265H)

In combination with the different package dimensions and material characteristics, e.g. WB DSO-16 wide-body (PG-DSO-16-30), NB DSO-16 narrow-body (PG-DSO-16-11) or LGA - 13 at 5mm x 5mm (PG-TFLGA-13-1) the maximum input-to-output and channel-to-channel creepage and clearance distances and the possible working voltages of the IC as a semiconductor component are defined (see **Table 18** to **Table 29**)

*Note: The achievable system isolation depends on PCB design, materials, manufacturing- and working environment. It is the customer's obligation to verify that the outlined semiconductor component isolation of the 2EDSx, 2EDFx device fits to application, manufacturing, working environment and end system safety requirement standards.*

**Functional description**

**3.2.1 Typical applications by isolation type**

Isolated gate drivers are typically deployed in the following applications.

**Table 4**

Isolation type	Potential applications
Functional	<ul style="list-style-type: none"> <li>High-power hard-switching high-voltage PFC, Vienna Rectifier, Totem Pole PFC or Synchronous Rectification</li> <li>Driving switches with Kelvin source connection (4-pin package)</li> <li>Secondary-side control in low voltage isolated DC/DC topologies and brick converters</li> </ul>
Reinforced	<ul style="list-style-type: none"> <li>Secondary-side control of high voltage SJ-MOSFETs in LLC or PS-ZVS</li> <li>Primary-side controlled synchronous rectification</li> <li>1 A / 2 A PWM data- / signal-coupler for local boost gate drivers</li> </ul>

**3.3 Supply voltages**

Three different power domains with independent internal power management are utilized to supply the input chip and the two output drivers. An undervoltage lockout functionality (UVLO) in each domain enables a defined startup and ensures a robust operation under all conditions.

**3.3.1 Input-side power supply**

The input side is powered via VDDI with nominal 3.3 V. For using the device with a supply voltage > 3.5 V the on-chip switched low-dropout regulator (SLDO) must be activated and an external shunt resistor  $R_{VDDI}$  has to be connected to VDDI.

It is recommended to use a ceramic bypass capacitor (10 nF - 22 nF) between VDDI and GNDI.

The SLDO is activated, if the pin SLDON is connected to GNDI. In devices with the inverted pin SLDOP (e.g. 2EDF7235K) the SLDO is active by default and will be deactivated if connected to GNDI. A hard-wired connection is recommended.

The SLDO regulates the current through an external resistor  $R_{VDDI}$  connected between the external supply voltage  $V_{DD}$  and pin VDDI as depicted in **Figure 1** to generate the required voltage drop. For proper operation it has to be ensured that the current through  $R_{VDDI}$  always exceeds the maximum supply current  $I_{VDD}$  of the input chip (see **Figure 8**).

Thus,  $R_{VDDI}$  has to fulfill:

$$R_{VDDI} < (V_{DD} - 3.3) / I_{VDD, max}$$

A typical choice for  $V_{DD} = 12 V$  is  $R_{VDDI} = 3 k\Omega$ , resulting in sufficient margin between resistor current and VDDI operating current. Dynamic current peaks are eliminated by a blocking cap (10 to 22 nF) between VDDI and GNDI.

The total power consumption of 2EDi is dominated by the output side and depends on switching frequency, gate resistor and gate charge, while for typical switching frequencies the input supply current stays relatively constant (see **Figure 7** to **Figure 8**)

**3.3.2 Output-side power supply**

Each gate driver channel has to be powered separately. It is recommended to use a ceramic bypass capacitor (minimum value 20 x Ciss of MOSFET) from VDDA to GNDA and from VDDB to GNDB in close proximity to the device.

The operating supply voltage can range from 4.5 V to 20 V for each gate drive channel.

The minimum gate driver turn-on voltage is set by the device Undervoltage Lockout (UVLO) to protect the power MOSFETs from operating in the saturation region.

Devices with 4 V, 8 V and 13 V UVLO thresholds for the output supply are currently available (see **Chapter 1.1.**)

**Functional description**

**3.4 Input configurations**

The inputs INA and INB control two independent PWM channels. The input signal is transferred non-inverted to the corresponding gate driver outputs OUTA and OUTB. All inputs are compatible with LV-TTL threshold levels and provide a hysteresis of typ. 0.8 V. The hysteresis is independent of the supply voltage VDDI.

The PWM inputs are internally pulled down to a logic low voltage level (GNDI). In case the PWM-controller signals have an undefined state during the power-up sequence, the gate driver outputs are forced to the "off"-state (low).

If the DISABLE input is “high”, this unconditionally drives both channel outputs to “low” regardless of the state of INA or INB.

**Table 5 Logic table**

Inputs					Gate Drive Output	
DISABLE	INA	INB	UVLO input side <sup>1)</sup>	UVLO output side <sup>1)</sup>	OUTA	OUTB
x	x	x	active	x	L	L
x	x	x	x	ch A/B active	L	L
L	x	L	inactive	ch A activ, ch B inactive	L	L
L	x	H	inactive	ch A active, ch B inactive	L	H
L	L	x	inactive	ch A inactive, ch B active	L	L
L	H	x	inactive	ch A inactive, ch B active	H	L
H	x	x	inactive	ch A/B inactive	L	L
L	L	L	inactive	ch A/B inactive	L	L
L	L	H	inactive	ch A/B inactive	L	H
L	H	H	inactive	ch A/B inactive	H	H

1) “inactive” means that VDD is above UVLO threshold voltage (normal operation)  
 “active” means that UVLO disables the gate driver output stages

**3.5 Driver outputs**

The two rail-to-rail output stages, realized with complementary PMOS, NMOS transistors, are able to provide the necessary sourcing and sinking current and shoot-through protection and active current limitation have been implemented with a very low on-resistance (see [Table 15](#)). The use of a p-channel sourcing transistor PMOS is crucial for achieving true rail-to-rail behavior without any source follower voltage drop.

Gate Drive Outputs OUTA, OUTB are held actively low in case of floating inputs or during startup or power down as long as the UVLO thresholds are not exceeded.

## Functional description

### 3.6 Undervoltage Lockout

#### 3.6.1 Input-side UVLO

During startup (rise of the input-side supply), as long as VDDI is below UVLO, no data is transferred to the output side. All gate driver outputs are held low (Safety Lock-down at startup).

When VDDI exceeds the UVLO level, the PWM input signal is transferred to the output side. If the output side is ready (not in UVLO condition), the output reacts according to the logic input. At any time, if the VDDI voltage drops below the UVLO threshold, an immediate “switch-to-low” command is sent to all output channels. The gate driver outputs are held low (Safety Lock-down is active at missing VDDI supply).

#### 3.6.2 Output-side UVLO

The Undervoltage Lockout function (UVLO) ensures that the output can be switched to its high level only if the gate driver supply voltage exceeds the UVLO threshold voltage. Thus it can be guaranteed, that the power switch transistors always stay within their Safe Operating Area (SOA). Otherwise a too low driving voltage could cause the power MOSFET to enter its saturation (ohmic) region with potentially destructive power dissipation.

The UVLO of each channel VDDA/VDDDB is controlled independently. There is no feedback to the input side.

### 3.7 Data transmission input-side to output-side

Coreless Transformer (CT) based communication modules situated on the input die are used for signal transfer between input and output devices. A proven high-resolution pulse repetition scheme in the transmitter combined with a watchdog time-out at the receiver side enables recovery from communication fails and ensures safe system shutdown in failure cases.

### 3.8 Dead Time Control

Dead Time Control function (DTC) increases the propagation delay of the rising output voltage by a time  $t_{DT}$ . This feature is used in half-bridge applications to prevent the switches from a shoot-through current due to overlapping or jitter on the PWM signals.

If the DTC feature is available, it can be enabled by connecting a resistor from DTC to GND. If this pin is not connected or set to VDDI, DTC is disabled.

Recommended DTC resistor ( $R_{DTC}$ ) values are between 4.7 k $\Omega$  and 150 k $\Omega$ .

$R_{DTC}$  is related to  $t_{DT}$  by the formula:  $R_{DTC} [k\Omega] = (t_{DT}[ns] - 3) / 1.8$

The resistor values and dead time delays are shown in [Table 17](#) and [Figure 15](#).

**Device characteristics**

**4 Device characteristics**

The absolute maximum ratings are listed in **Table 6**. Stresses beyond these values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**4.1 Absolute maximum ratings**

**Table 6 Absolute maximum ratings**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Voltage at pin VDDI	$V_{DDI}$	-0.3	–	4.0	V	1)
Output supply voltage	$V_{DDO}$	-0.3	–	22	V	–
Voltage at pins PWM and DISABLE	$V_{IN}$	-0.3	–	17	V	–
		-5	–	–	V	< 50 ns for transient <sup>2)</sup>
Voltage at pins DTC and TEST/SLDO	$V_{DTC} / V_{TEST/SLDO}$	-0.3	–	$V_{DDI} + 0.3$	V	–
Voltage at pins OUTA, OUTB	$V_{OUTA/B}$	-0.3	–	$V_{DDO} + 0.3$	V	–
		-2	–	$V_{DDO} + 1.5$	V	< 200 ns <sup>2)</sup>
Reverse current peak at pins OUTA, OUTB	$I_{SRC\_rev}$	-5	–	–	$A_{pk}$	< 500 ns <sup>2)</sup>
	$I_{SNK\_rev}$	–	–	5	$A_{pk}$	
Non-destructive Common Mode Transient Immunity	CMTI	400	–	–	V/ns	input to each output channel
Junction temperature	$T_J$	-40	–	150	°C	–
Storage temperature	$T_{STG}$	-65	–	150	°C	–
Soldering temperature	$T_{SOL}$	–	–	260	°C	reflow / wave soldering <sup>3)</sup>
ESD capability	$V_{ESD\_CDM}$	–	–	0.5	kV	Charged Device Model (CDM) <sup>4)</sup>
ESD capability	$V_{ESD\_HBM}$	–	–	2	kV	Human Body Model (HBM) <sup>5)</sup>

- 1) if the SLDO is activated (SLDON pin tied to GNDI), the input-side supply voltage does not correspond to  $V_{DDI}$  and can be higher
- 2) not subject to production test - specified by design
- 3) according to JESD22A111
- 4) according to ESD-CDM: ANSI/ESDA/JEDEC JS-002
- 5) according to ESD-HBM: ANSI/ESDA/JEDEC JS-001 (discharging 100 pF capacitor through 1.5 kΩ resistor)

**Device characteristics**

**4.2 Thermal characteristics**

**Table 7 Thermal characteristics at  $T_{amb} = 25^{\circ}\text{C}$**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
<b>PG-TFLGA-13-1</b>						
Thermal resistance junction-ambient <sup>1)</sup>	$R_{thJA25}$	–	112	–	K/W	–
Thermal resistance junction-case (top) <sup>2)</sup>	$R_{thJC25}$	–	44	–	K/W	–
Thermal resistance junction-board <sup>3)</sup>	$R_{thJB25}$	–	66	–	K/W	–
Characterization parameter junction-top <sup>4)</sup>	$\Psi_{thJT25}$	–	7.7	–	K/W	–
Characterization parameter junction-board <sup>4)</sup>	$\Psi_{thJB25}$	–	5.6	–	K/W	–
<b>PG-DSO-16-11</b>						
Thermal resistance junction-ambient <sup>1)</sup>	$R_{thJA25}$	–	51	–	K/W	–
Thermal resistance junction-case (top) <sup>2)</sup>	$R_{thJC25}$	–	25	–	K/W	–
Thermal resistance junction-board <sup>3)</sup>	$R_{thJB25}$	–	36	–	K/W	–
Characterization parameter junction-top <sup>4)</sup>	$\Psi_{thJT25}$	–	4.4	–	K/W	–
Characterization parameter junction-board <sup>4)</sup>	$\Psi_{thJB25}$	–	5.4	–	K/W	–
<b>PG-DSO-16-30</b>						
Thermal resistance junction-ambient <sup>1)</sup>	$R_{thJA25}$	–	59	–	K/W	–
Thermal resistance junction-case (top) <sup>2)</sup>	$R_{thJC25}$	–	32	–	K/W	–
Thermal resistance junction-board <sup>3)</sup>	$R_{thJB25}$	–	33	–	K/W	–
Characterization parameter junction-top <sup>4)</sup>	$\Psi_{thJT25}$	–	8.9	–	K/W	–
Characterization parameter junction-board <sup>4)</sup>	$\Psi_{thJB25}$	–	7.7	–	K/W	–

- 1) obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- 2) obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- 3) obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- 4) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $R_{th}$ , using a procedure described in JESD51-2a (sections 6 and 7).



**Device characteristics**

**4.3 Operating range**

**Table 8 Operating range**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Voltage at pin VDDI	$V_{DDI}$	3.0	–	3.5	V	<sup>1)</sup> Min. defined by UVLO
Output supply voltage	$V_{DDA} / V_{DDB}$	4.5	–	20	V	Min. defined by UVLO
Logic input voltage at pins INA, INB, DISABLE	$V_{IN}$	0	–	15	V	–
Voltage at pins DTC and SLDO	$V_{DTC} / V_{TEST/SLDO}$	0	–	3.5	V	–
Junction temperature	$T_J$	-40	–	150	°C	<sup>2)</sup>
Ambient temperature	$T_{amb}$	-40	–	125	°C	–

1) if the SLDO is activated (SLDON pin tied to GNDI), the input-side supply voltage does not correspond to  $V_{DDI}$  and can be higher

2) continuous operation above 125°C may reduce lifetime.

**4.4 Electrical characteristics**

Unless otherwise noted, min./max. values of characteristics are the lower and upper limits, respectively. They are valid within the full operating range. The supply voltage is  $V_{DDA}, V_{DDB} = 12\text{ V}$  and  $V_{DDI} = 3.3\text{ V}$ . Typical values are given at  $T_J = 25^\circ\text{C}$ .

**Table 9 Power supply (see Figure 7, Figure 8 and Figure 9)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
$I_{VDDI}$ quiescent current	$I_{VDDIqu1}$	–	1.4	–	mA	no switching
$I_{VDDA}, I_{VDDB}$ quiescent current	$I_{VDDAQu2} / I_{VDDBQu2}$	–	0.6	–	mA	Outx = low, no switching (4 V, 8 V UVLO options)
		–	0.7	–	mA	Outx = low, no switching, $V_{DDA/B} = 15\text{ V} > UVLO\_CM_{on}$ (13 V UVLO options)

**Table 10 Undervoltage Lockout  $V_{DDI}$  (See Figure 11)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn-on threshold $V_{DDI}$	$UVLO_{on}$	2.75	2.85	2.95	V	–
Undervoltage Lockout (UVLO) turn-off threshold $V_{DDI}$	$UVLO_{off}$	–	2.70	–	V	–
UVLO threshold hysteresis $V_{DDI}$	$UVLO_{hys}$	0.1	0.15	0.2	V	–

**Device characteristics**

**Table 11 Undervoltage Lockout  $V_{DDA}$ ,  $V_{DDB}$  13 V-versions for SiC MOSFETs (see Figure 13)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn-on threshold $V_{DDA}$ , $V_{DDB}$	UVLO_ CM <sub>on</sub>	13.0	13.7	14.2	V	–
Undervoltage Lockout (UVLO) turn-off threshold $V_{DDA}$ , $V_{DDB}$	UVLO_ CM <sub>off</sub>	–	12.9	–	V	–
UVLO threshold hysteresis $V_{DDA}$ , $V_{DDB}$	UVLO_ CM <sub>hys</sub>	0.4	0.8	1.2	V	–

**Table 12 Undervoltage Lockout  $V_{DDA}$ ,  $V_{DDB}$  8 V-versions for standard MOSFETs (see Figure 12)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn-on threshold $V_{DDA}$ , $V_{DDB}$	UVLO_ CM <sub>on</sub>	7.6	8.0	8.4	V	–
Undervoltage Lockout (UVLO) turn-off threshold $V_{DDA}$ , $V_{DDB}$	UVLO_ CM <sub>off</sub>	–	7.0	–	V	–
UVLO threshold hysteresis $V_{DDA}$ , $V_{DDB}$	UVLO_ CM <sub>hys</sub>	0.7	1	1.3	V	–

**Table 13 Undervoltage Lockout  $V_{DDA}$ ,  $V_{DDB}$  4 V-versions for logic-level MOSFETs (see Figure 12)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold $V_{DDA}$ , $V_{DDB}$	UVLO_ CM <sub>on</sub>	4.0	4.2	4.4	V	–
Undervoltage Lockout (UVLO) turn off threshold $V_{DDA}$ , $V_{DDB}$	UVLO_ CM <sub>off</sub>	–	3.9	–	V	–
UVLO threshold hysteresis $V_{DDA}$ , $V_{DDB}$	UVLO_ CM <sub>hys</sub>	0.2	0.3	0.4	V	–

**Table 14 Logic inputs INA, INB and DISABLE (see Figure 11)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage threshold for transition LH	$V_{INH}$	1.65	2.0	2.35	V	–
Input voltage threshold for transition HL	$V_{INL}$	–	1.2	–	V	–
Input voltage threshold hysteresis	$V_{IN\_hys}$	0.4	0.8	1.2	V	–
Input pull-down resistor	$R_{IN}$	–	150	–	k $\Omega$	–

**Device characteristics**

**Table 15 Static output characteristics 4 A/8 A devices (see Figure 10)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High-level (Sourcing) Output Resistance	$R_{on\_SRC}$	0.42	0.85	1.6	$\Omega$	$I_{SNK} = 50 \text{ mA}$
Peak Sourcing Output Current	$I_{SRC\_pk}$	–	4	1)	A	–
Low-level (Sinking) Output Resistance	$R_{on\_SNK}$	0.18	0.35	0.75	$\Omega$	$I_{SRC} = 50 \text{ mA}$
Peak Sinking Output Current	$I_{SNK\_pk}$	2)	-8	–	A	–

1) actively limited by design at approx.  $5.2 A_{pk}$ , parameter is not subject to production test - specified by design / characterization

2) actively limited by design at approx.  $-10.2 A_{pk}$ , parameter is not subject to production test - specified by design / characterization

**Table 16 Static output characteristics 1 A / 2 A devices (see Figure 10)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High-level (Sourcing) Output Resistance	$R_{on\_SRC}$	1.4	3.1	5.8	$\Omega$	$I_{SNK} = 50 \text{ mA}$
Peak Sourcing Output Current	$I_{SRC\_pk}$	–	1	1)	A	–
Low-level (Sinking) Output Resistance	$R_{on\_SNK}$	0.6	1.2	2.5	$\Omega$	$I_{SRC} = 50 \text{ mA}$
Peak Sinking Output Current	$I_{SNK\_pk}$	2)	-2	–	A	–

1) actively limited by design at approx.  $1.3 A_{pk}$ , parameter is not subject to production test - specified by design / characterization

2) actively limited by design at approx.  $-2.6 A_{pk}$ , parameter is not subject to production test - specified by design / characterization

**Table 17 Dynamic characteristics (see Figure 5 and Figure 14)**

$T_{J,max} = 125^\circ\text{C}$ ,  $C_{LOAD} = 1.8 \text{ nF}$  for 4 A / 8 A version,  $C_{LOAD} = 0.47 \text{ nF}$  for 1 A / 2 A version

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
INA- /INB-to-output turn-on / turn-off propagation delay	$t_{PDOn}, t_{PDOff}$	31	37	44	ns	4 A/8 A version
INA- /INB-to-output turn-on propagation delay	$t_{PDOn}$	31	37	44	ns	1 A/2 A version
INA- /INB-to-output turn-off propagation delay	$t_{PDOff}$	29	35	44	ns	1 A/2 A version
DISABLE-to-output turn-on/ -off propagation delay	$t_{PDDISoff}, t_{PDDISoff}$	–	–	100	ns	–
Output turn-on propagation delay mismatch between channels	$\Delta t_{PDOn}$	–	–	3	ns	INA, INB shorted
Rise time	$t_{rise}$	–	6.5	12 <sup>1)</sup>	ns	–

**Device characteristics**

**Table 17 Dynamic characteristics (see Figure 5 and Figure 14) (cont'd)**

$T_{J,max} = 125^{\circ}\text{C}$ ,  $C_{LOAD} = 1.8 \text{ nF}$  for 4 A / 8 A version,  $C_{LOAD} = 0.47 \text{ nF}$  for 1 A / 2 A version

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Fall time	$t_{fall}$	–	4.5	8 <sup>1)</sup>	ns	–
Minimum input pulse width that changes output state	$t_{PW}$	–	18	–	ns	–
Input-side start-up time <sup>1)</sup>	$t_{START,VDDI}$	–	7	–	μs	see <a href="#">Figure 6</a>
Input-side deactivation time <sup>1)</sup>	$t_{STOP,VDDI}$	–	255	–	ns	see <a href="#">Figure 6</a>
Output-side start-up time <sup>1)</sup>	$t_{START,VDDA/B}$	–	5	–	μs	see <a href="#">Figure 6</a>
Output-side deactivation time <sup>1)</sup>	$t_{STOP,VDDA/B}$	–	110	–	ns	see <a href="#">Figure 6</a>

1) not subject to production test - specified by design

**Device characteristics**

**4.5 Functional and reinforced isolation specifications**

Each individual part number and package variant has its own safety isolation characteristic due to package dimension and respective isolation test voltages and methods applied. The table heading references each unique part number.

For reinforced safety, the regulatory tests described in the component and system standards are applied by Infineon. For functional isolation, the outlined in-house test methods have been applied.

As soon as the regulatory certificates are available, the reference and or documents will become available for public download on the Infineon website [www.infineon.com/2EDi](http://www.infineon.com/2EDi)

*Note: Final creepage and clearance of component, must be verified in conjunction with PCB design layout and manufacturing choice like PCB material (CTI), stubs, grooves, lacquer which might increase or reduce safety distances. Meeting the isolation requirements on system level is therefore the responsibility of the application owner.*

**4.5.1 Functional isolation specifications**

**4.5.1.1 Functional isolation of devices in PG-TFLGA-13-1 package**

The PG-TFLGA-13-1 package is available for 2EDF7275K and 2EDF7235K. The isolation related parameters are shown in [Table 18](#), [Table 19](#) and [Table 20](#); for a component with basic or reinforced safety approval, choose a different part number (e.g. [Chapter 4.5.2](#): 2EDS8265H, 2EDS9265H and 2EDS8165H)

**Table 18 Functional isolation input-to-output (PG-TFLGA-13-1)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Functional isolation test voltage	$V_{IO}$	1500	–	–	$V_{DC}$	Impulse test >10 ms, production tested
Maximum isolation working voltage	$V_{IOWM}$	460	–	–	$V_{RMS}$	according to IEC 60664-1 (PD 2; MG II)
Package clearance	CLR	–	3.4	–	mm	Shortest distance over air, from any input pin to any output pin
Package creepage	CPG	–	3.4	–	mm	Shortest distance over surface, from any input pin to any output pin
Common Mode Transient Immunity	CMTI	150	–	–	V/ns	according to DIN V VDE V0884-11, static and dynamic test
Capacitance input-to-output	$C_{IO}$	–	2	–	pF	<sup>1)</sup>
Resistance input-to-output	$R_{IO}$	–	>1000	–	MΩ	<sup>2)</sup>

1) not subject to production test - specified by design

**Device characteristics**

**Table 19 Package characteristics (PG-TFLGA-13-1)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Comparative Tracking Index of package mold	CTI	400	–	600	V	according to DIN EN 60112 (VDE 0303-11)
Material group	–	–	II	–	–	according to IEC 60112

**Table 20 Functional isolation channel-to-channel (PG-TFLGA-13-1)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Functional isolation test voltage	$V_{Ch2Ch-DC-Test}$	650	–	–	$V_{DC}$	Impulse Test > 10 ms; sample tested
Package creepage	CPG	–	1.0	–	mm	Shortest distance over surface, from output pin Ch1-GND to output pin Ch2-VDD

**4.5.1.2 Functional isolation of devices in NB PG-DSO-16-11 package**

The PG-DSO-16-11 package is available for 2EDF7175F, 2EDF9275F and 2EDF7275F. The isolation related parameters are shown in [Table 21](#), [Table 22](#) and [Table 23](#)

**Table 21 Input-to-output isolation specification (NB PG-DSO-16-11)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Functional isolation test voltage	$V_{IO}$	1500	–	–	$V_{DC}$	Impulse test > 10 ms, sample tested
Maximum isolation working voltage	$V_{IOWM}$	510	–	–	$V_{RMS}$	according to IEC 60664-1 (PD2; MG II)
Package clearance	CLR	–	4.0	–	mm	Shortest distance over air, from any input pin to any output pin
Package creepage	CPG	–	4.0	–	mm	Shortest distance over surface, from any input pin to any output pin
Common Mode Transient Immunity	CMTI	150	–	–	V/ns	according to DIN V VDE V0884-11, static and dynamic test
Capacitance input-to-output	$C_{IO}$	–	2	–	pF	1)
Resistance input-to-output	$R_{IO}$	–	>1000	–	MΩ	2)

1) not subject to production test - specified by design

**Device characteristics**

**Table 22 Package characteristics (NB PG-DSO-16-11)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Comparative Tracking Index of package mold	CTI	400	–	600	V	according to DIN EN 60112 (VDE 0303-11)
Material group	–	–	II	–	–	according to IEC 60112

**Table 23 Channel-to-channel isolation (NB PG-DSO-16-11)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Functional isolation test voltage	$V_{\text{Ch2Ch-DC-Test}}$	1500	–	–	$V_{\text{DC}}$	Impulse Test >10 ms; sample tested
Package Creepage	CPG	–	2.5	–	mm	Shortest distance over surface, from Output pin Ch1-GND to output pin Ch2-VDD

**4.5.2 Reinforced isolation of devices in WB PG-DSO-16-30 package**

The PG-DSO-16-30 package is available for 2EDS8265H, 2EDS9265H and 2EDS8165H. The safety related certifications are listed in [Table 24](#), [Table 25](#) and the isolation related parameters are shown in [Table 26](#) to [Table 30](#)

**Table 24 Component safety-related certificates for WB PG-DSO-16-30<sup>1)</sup>**

Certification	Issuing certification body	Certification status	Certification number
DIN V VDE V 0884-10	VDE	Certified <sup>2)</sup>	40043864
UL 1577	UL	Certified	E311313

1) certifications planned for 2EDS9265H

2) certification no longer available due to standard expiration

**Table 25 Sistem safety-related certifications for WB PG-DSO-16-30 <sup>1)</sup>**

Certification	Issuing certification body	Certification status	Certification number
DIN EN 62368-1 (VDE 0868-1), DIN 60950-1 (VDE 0805-1)	VDE	Certified	40050289
EN 61010-1	VDE	Certified	40051533
EN 60601-1	VDE	Certified	40051732
GB 4943.1-2011	CQC	Certified	CQC20001244015

1) certifications planned for 2EDS9265H

**Device characteristics**

**Table 26 Input-to-output isolation specification according to DIN V, VDE0884-10 (2016-06)<sup>1)</sup> in WB PG-DSO-16-30**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Maximum transient isolation voltage	$V_{IOTM}$	8000	–	–	$V_{pk}$	qualification for $t = 60$ s; production test with $V_{IOTM} > 10$ kV <sub>pk</sub> for $t = 1$ s
Maximum repetitive peak isolation voltage	$V_{IORM}$	1420	–	–	$V_{pk}$	Time Dependent Dielectric Breakdown test method
Maximum isolation working voltage	$V_{IOWM}$	1420	–	–	$V_{DC}$	
		1000	–	–	$V_{RMS}$	
Partial discharge voltage	$V_{PD}$	4500	–	–	$V_{pk}$	Test sequence: 10.2 kV <sub>pk</sub> for $t = 1$ s followed by partial discharge 4.5 kV <sub>pk</sub> > 1.875 x $V_{IOWM}$ , $Q_{PD} < 5$ pC; production test
Maximum surge isolation voltage	$V_{IOSM}$	6250	–	–	$V_{pk}$	$V_{IOSM\_test} = 1.6 \times V_{IOSM} > 10$ kV <sub>pk</sub> ; sample tested <sup>2)</sup>
Package clearance	CLR	–	8.0	–	mm	from any input pin to any output pin
Package creepage	CPG	–	8.0	–	mm	from any input pin to any output pin
Overvoltage category per IEC 60664-1 table F.1	–	I	–	IV		Rated mains voltage $\leq 150$ V <sub>RMS</sub>
		I	–	III		$\leq 300$ V <sub>RMS</sub>
		I	–	II		$\leq 600$ V <sub>RMS</sub>
Capacitance input-to-output	$C_{IO}$	–	2	–	pF	–
Resistance input-to-output	$R_{IO}$	–	>1000	–	MΩ	–
Common Mode Transient Immunity	CMTI	150	–	–	V/ns	according to DIN V VDE V0884-11, static and dynamic test

1) VDE encompasses former VDE0884-10, IEC60747-5-5 (opto-coupler standard)

2) Surge pulse tests applied according to IEC60065-10.1 (Ed 8.0 2014), 61000-4-5, 60060-1; waveforms (1.2 μs slope, 50 μs decay)

**Table 27 Reinforced isolation package characteristics (in WB PG-DSO-16-30)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Comparative Tracking Index of package mold	CTI	400	–	600	V	according to DIN EN 60112 (VDE 0303-11)
Material group	–	–	II	–	–	according to IEC 60112



**Device characteristics**

**Table 27 Reinforced isolation package characteristics (in WB PG-DSO-16-30)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Pollution degree	–	–	2	–	–	–
Climatic category	–	–	40/125/ 21	–	–	–

**Table 28 Reinforced input-to-output isolation according to UL1577 Ed 5 (in WB PG-DSO-16-30)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Withstand isolation voltage	$V_{ISO}$	5700	–	–	$V_{RMS}$	$V_{ISO} = 5700 V_{RMS}$ for t = 60 s (qualification); $V_{ISO} > 1.2 \times V_{RMS} = 6840 V$ for t = 1 s (production test)

**Table 29 Functional isolation channel-to-channel (in WB PG-DSO-16-30)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Functional isolation test voltage	$V_{Ch2Ch-DC-test}$	1500	–	–	$V_{DC}$	Impulse Test >10 ms; sample tested
Package creepage	CPG	–	2.5	–	mm	Shortest distance over surface, from Output pin Ch1-GND to output pin Ch2-VDD

**4.5.3 Safety-limiting values**

**Table 30 Reinforced isolation safety-limiting values as outlined in VDE-0884-10 (WB PG-DSO-16-30)**

Parameter	Side	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Safety supply power	Input chip	–	–	20.0	mW	$R_{thJA} = 59 K/W^{1)}$ , $T_{amb} = 25^{\circ}C$ , $T_J = 150^{\circ}C$
	Output A	–	–	1050	mW	
	Output B	–	–	1050	mW	
	Total	–	–	2120	mW	
Safety supply currents	Output A	–	–	87.5	mA	$R_{thJA} = 59 K/W^{1)}$ , $V_{DDA}/V_{DDB} = 12 V$ , $T_{amb} = 25^{\circ}C$ , $T_J = 150^{\circ}C$
	Output B	–	–	87.5	mA	
	Output A	–	–	53.5	mA	
Output B	–	–	53.5	mA		
Safety temperature	$T_s$	–	–	150	$^{\circ}C$	$T_s = T_{J,max}$

1) calculated with the  $R_{th}$  of WB PG-DSO-16-30 package (see [Table 7](#))

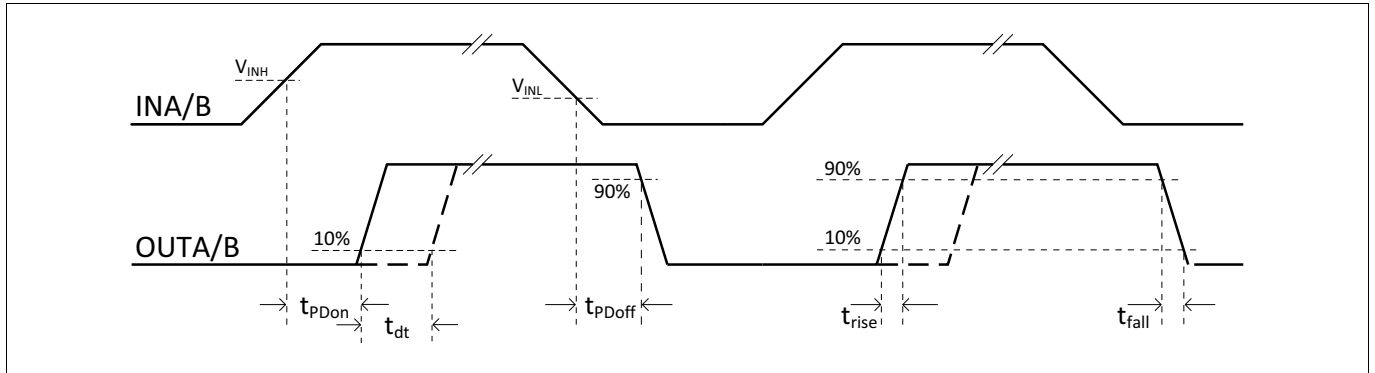
### **Device characteristics**

According to VDE0884-10 and UL1577, safety-limiting values define the operating conditions under which the isolation barrier can be guaranteed to stay unaffected. This corresponds with the maximum allowed junction temperature, as temperature-induced failures might cause significant overheating and eventually damage the isolation barrier.

**Timing diagrams**

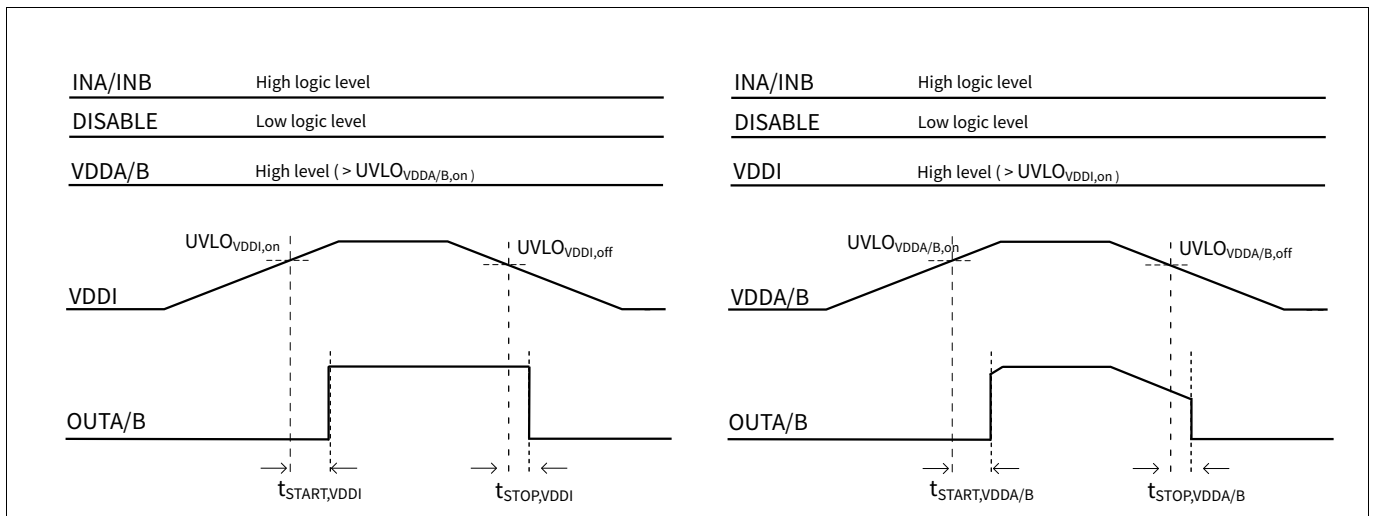
**5 Timing diagrams**

**Figure 5** depicts rise, fall and delay times for 2EDi 4 A/8 A. Besides, the effect of an activated dead time control (resistor connected to pin DTC) is indicated.



**Figure 5 Propagation delays, rise, fall and dead time**

**Figure 6** illustrates the UVLO behavior. It depicts the reaction time to UVLO events when the supply crosses the UVLO thresholds during rising or falling transitions (power-up, power-down, supply noise).

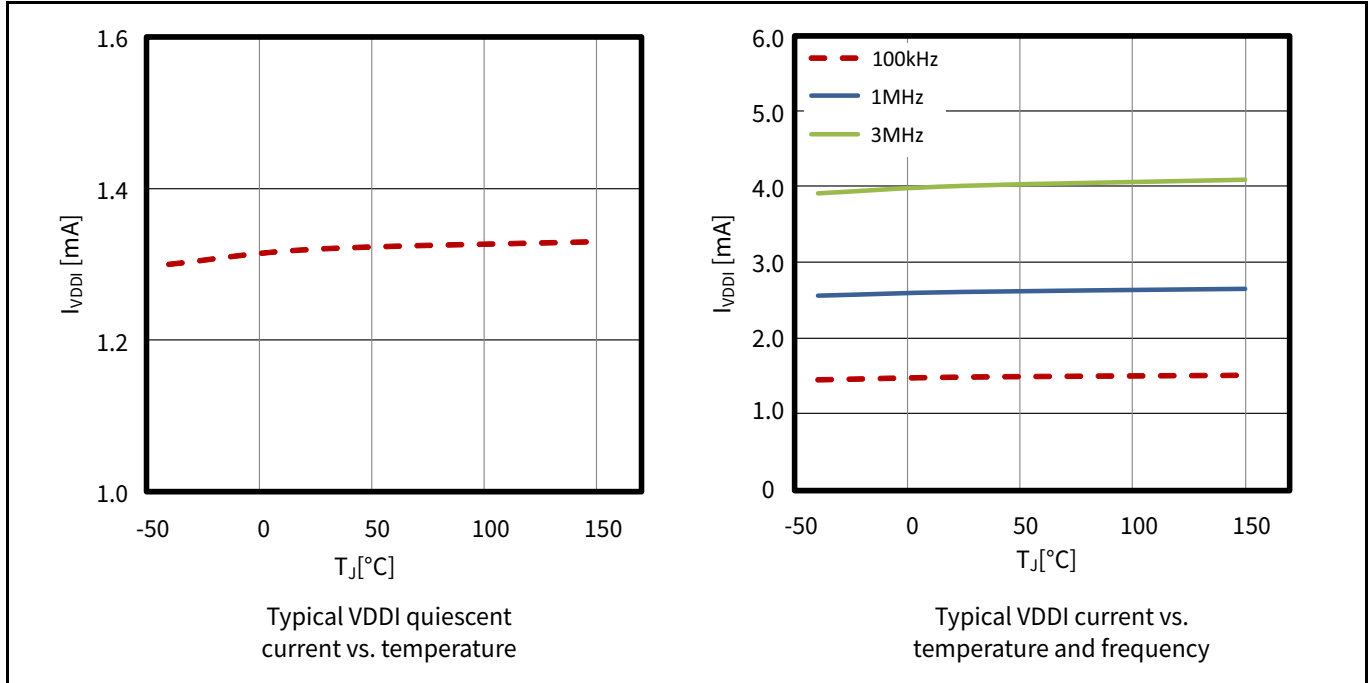


**Figure 6 UVLO behavior, start-up and deactivation time (unloaded output)**

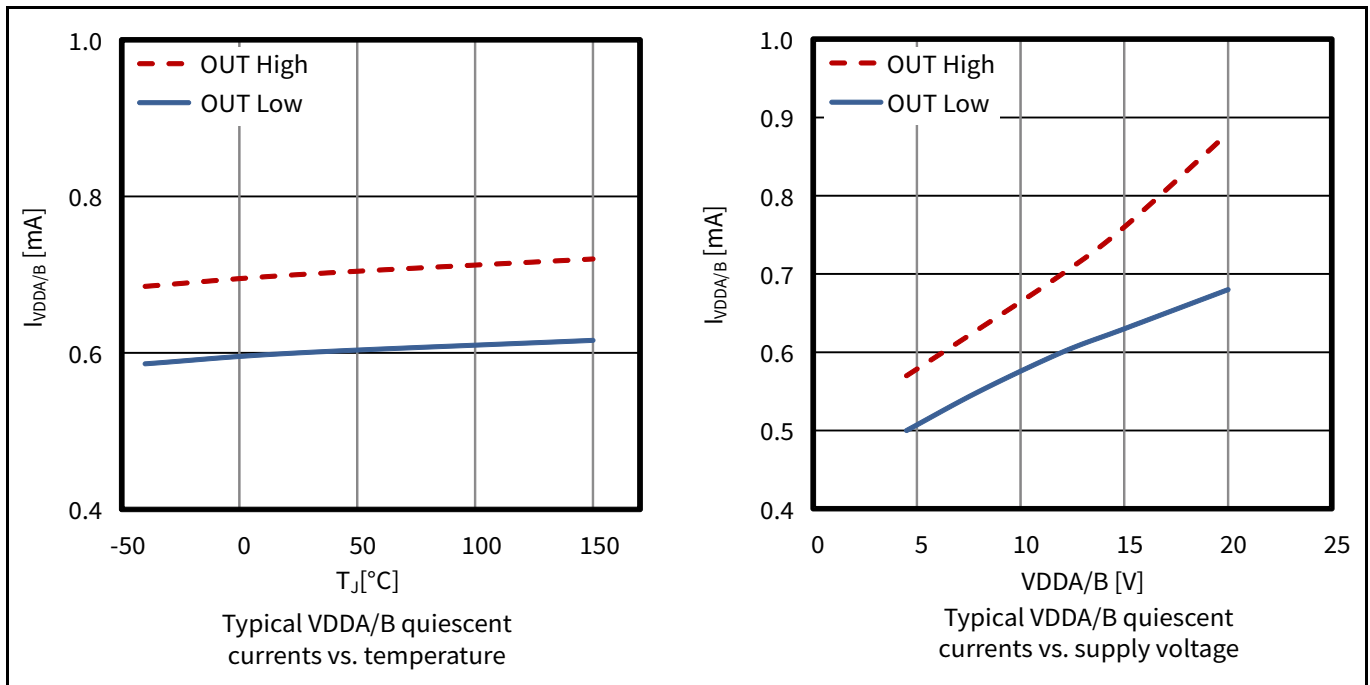
Typical characteristics

**6 Typical characteristics**

VDDA = VDDB = 12 V, VDDI = 3.3 V,  $T_{amb} = 25^{\circ}\text{C}$ , 2EDF7235K (PG-TFLGA-13-1) and no load unless otherwise noted.

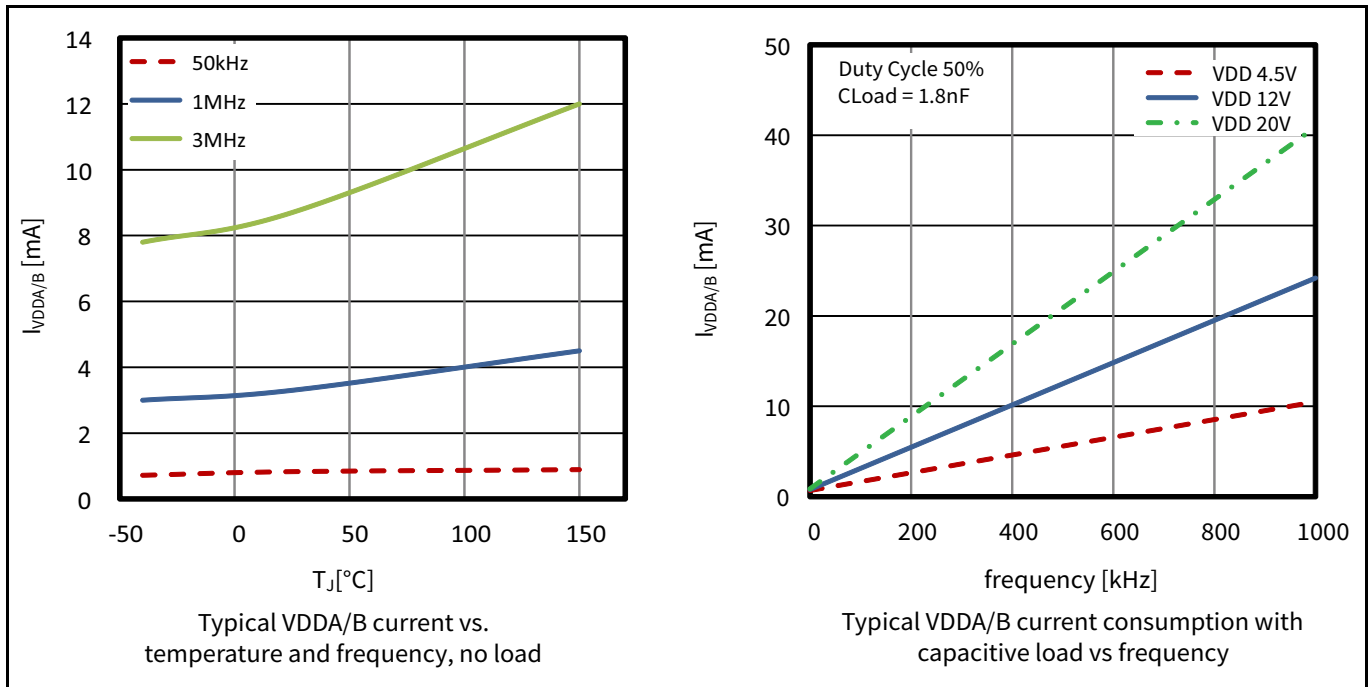


**Figure 7 Supply current VDDI**

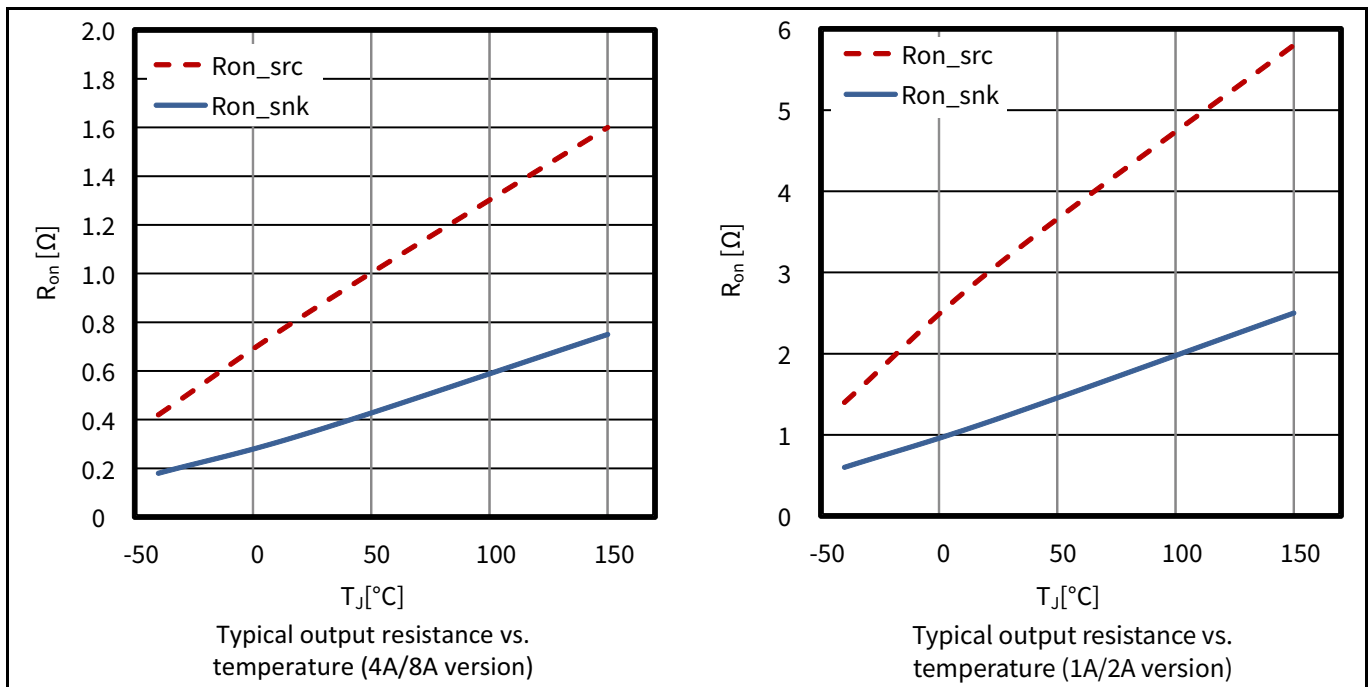


**Figure 8 Supply current VDDA, VDDB**

**Typical characteristics**



**Figure 9 Supply current VDDA, VDDB (with / without load)**



**Figure 10 Output resistance**

Typical characteristics

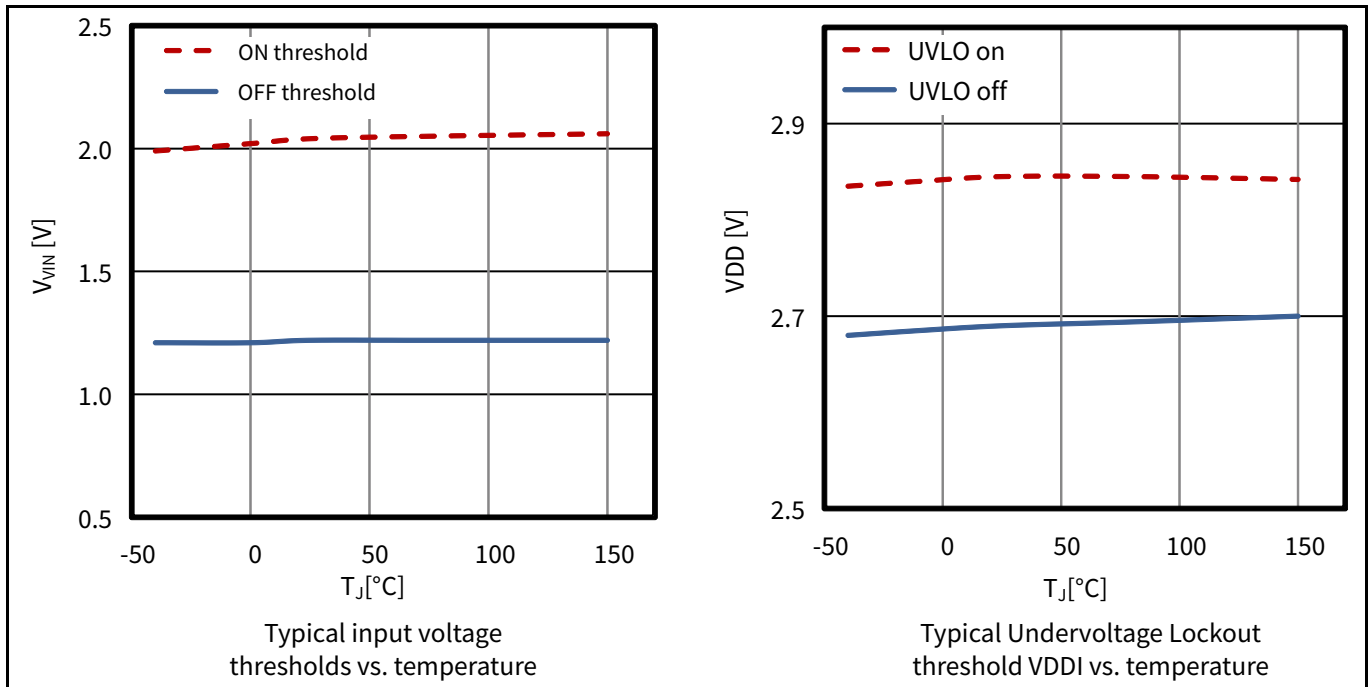


Figure 11 Logic input thresholds and VDDI UVLO

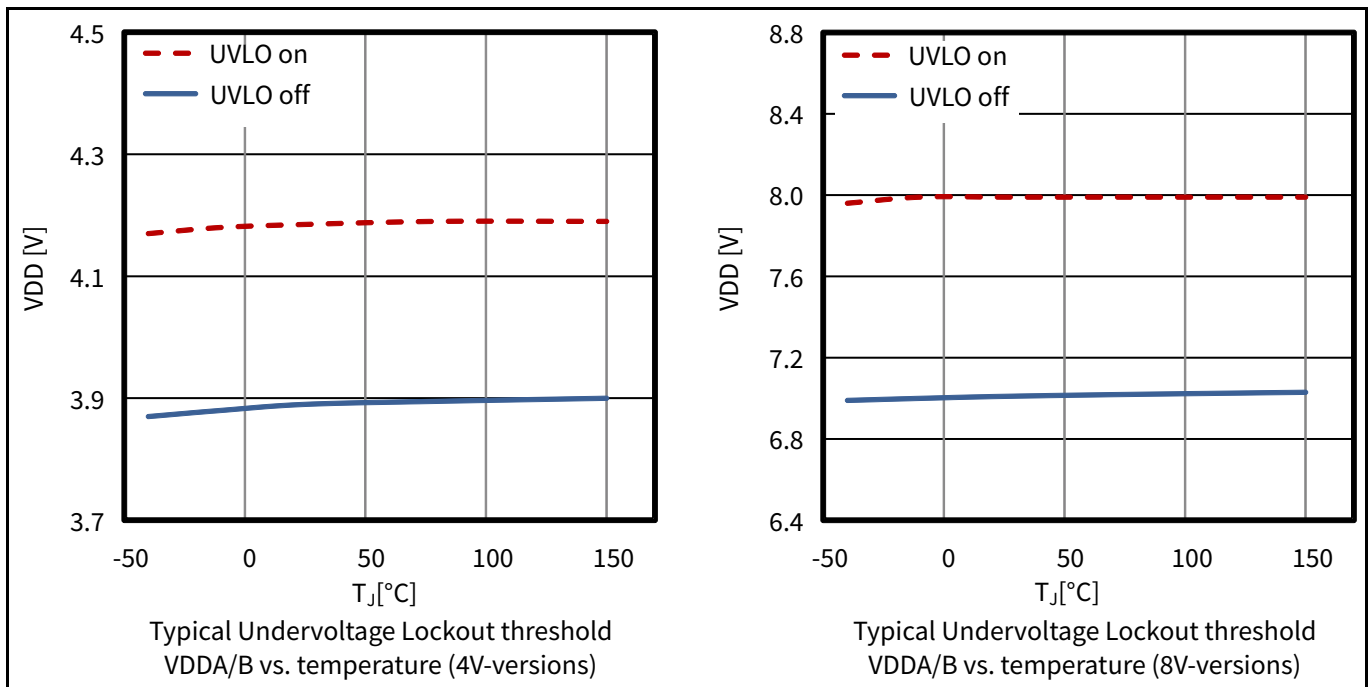


Figure 12 VDDA/B UVLO (4 V and 8 V)

Typical characteristics

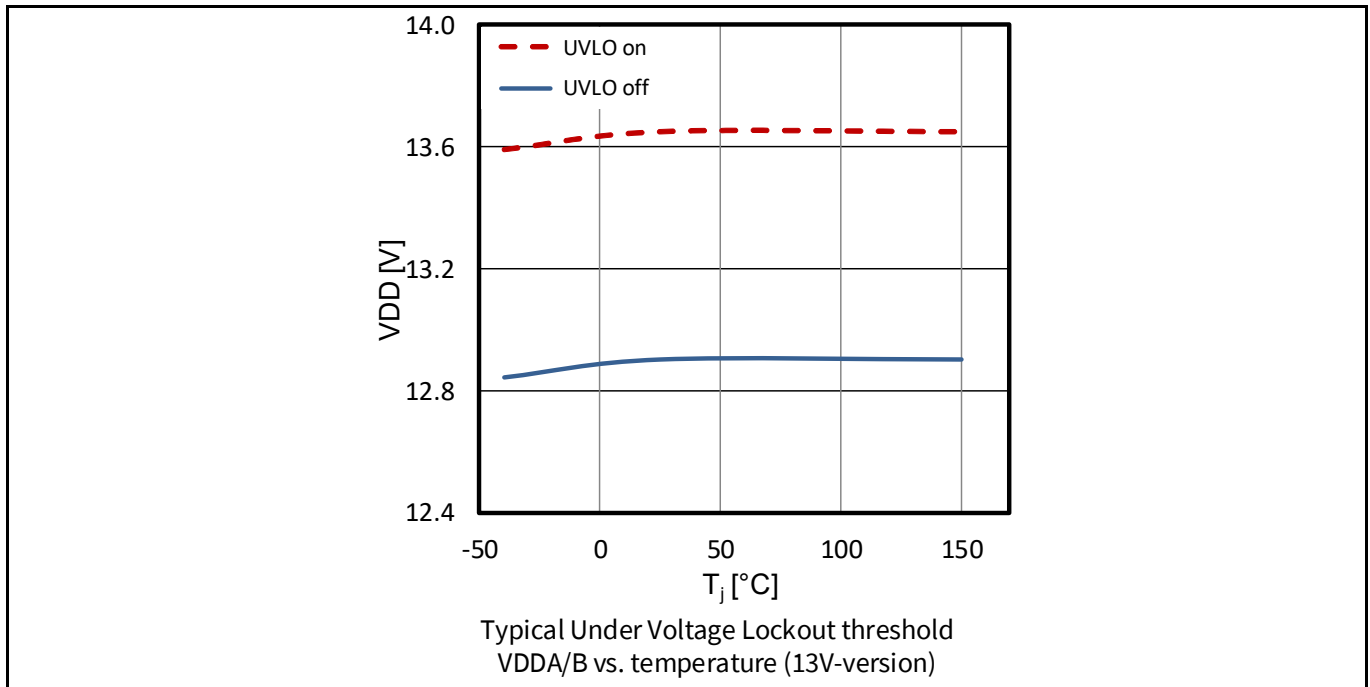


Figure 13 VDDA/B UVLO (13 V)

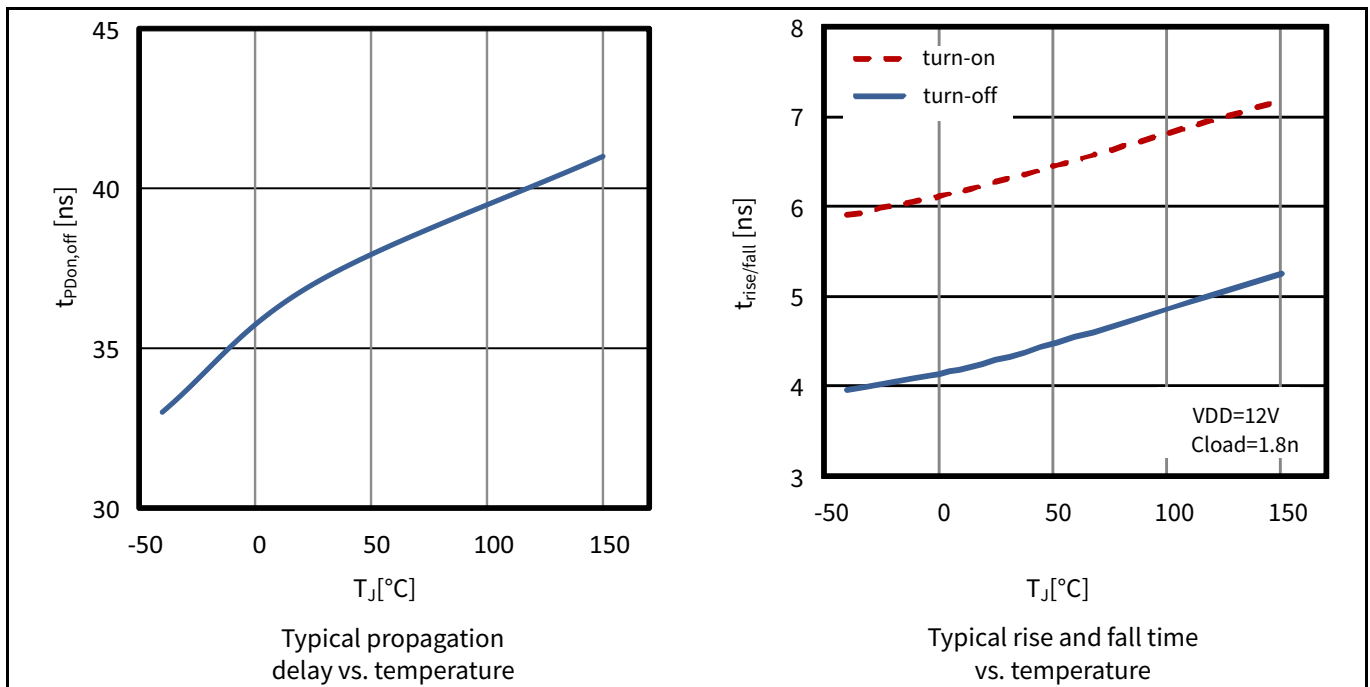
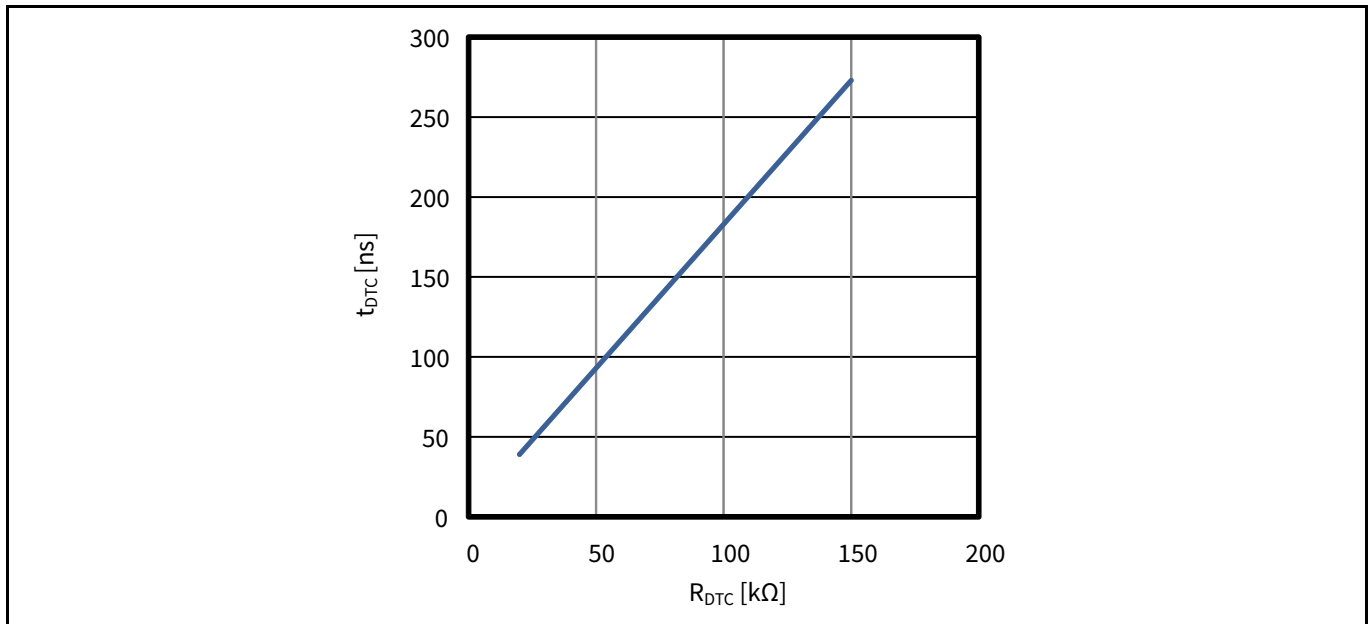
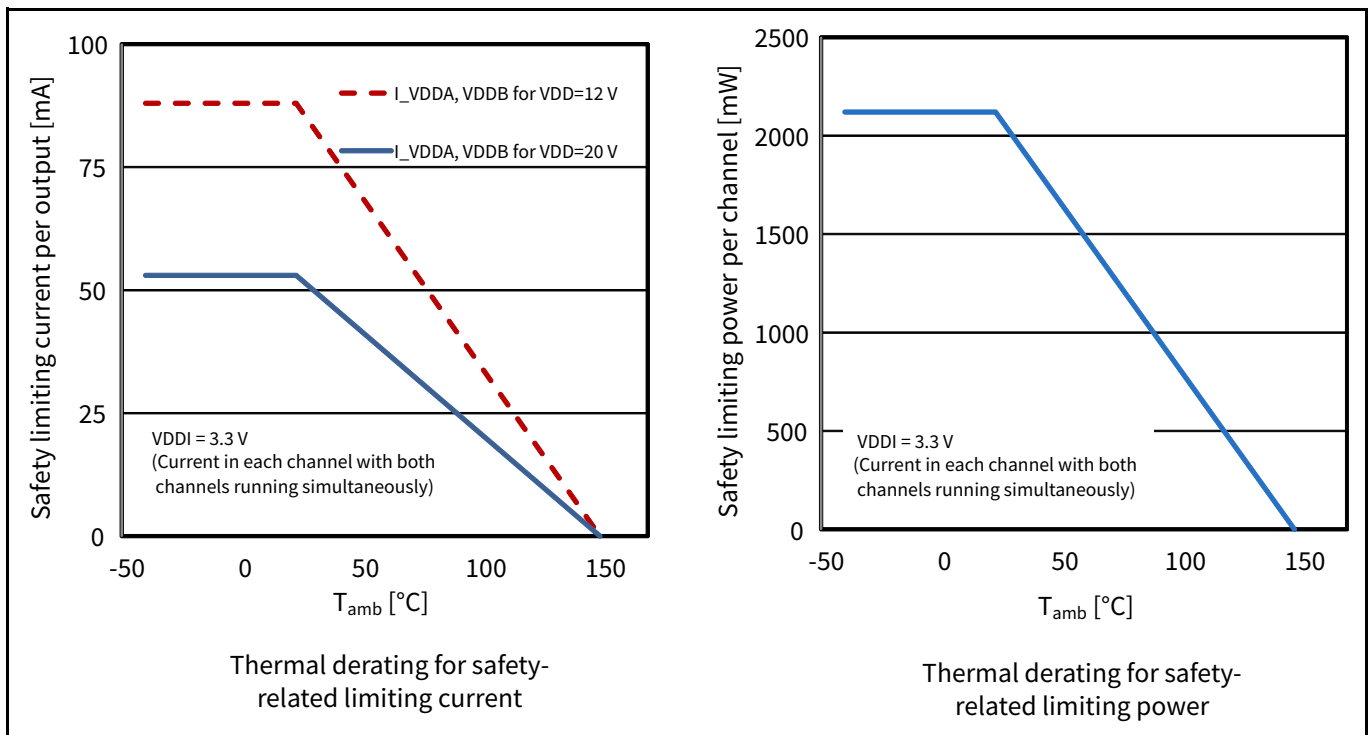


Figure 14 Propagation delay and rise / fall time

**Typical characteristics**



**Figure 15** Dead time control: rising edge delay vs R<sub>DTC</sub>



**Figure 16** Thermal derating curves



## Package

# 7 Package

The following package versions are available.

- an NB PG-DSO-16-11 package with typ. 4 mm creepage input to output
- an area optimized 5 x 5 mm<sup>2</sup> PG-TFLGA-13-1
- a WB PG-DSO-16-30 package with typ. 8 mm creepage input to output

*Note:* For further information on package types, recommendation for board assembly, please go to:  
[www.infineon.com/2EDi](http://www.infineon.com/2EDi)

## 7.1 Device numbers and markings

**Table 31** Device numbers and markings

Part number	Orderable part number (OPN)	Device marking
2EDF7275F	2EDF7275FXUMA2	2F7275B
2EDF8275F	2EDF8275FXUMA1	2F7875B
2EDF9275F	2EDF9275FXUMA1	2F9275B
2EDF7175F	2EDF7175FXUMA2	2F7175B
2EDF7275K	2EDF7275KXUMA2	2F7275B
2EDF7235K	2EDF7235KXUMA1	2F7235A
2EDS8265H	2EDS8265HXUMA2	2S8265B
2EDS9265H	2EDS9265HXUMA1	2S9265B
2EDS7165H	2EDS7165HXUMA1	2S7165B
2EDS8165H	2EDS8165HXUMA2	2S8165B

Package

7.2 Package PG-DSO-16-11

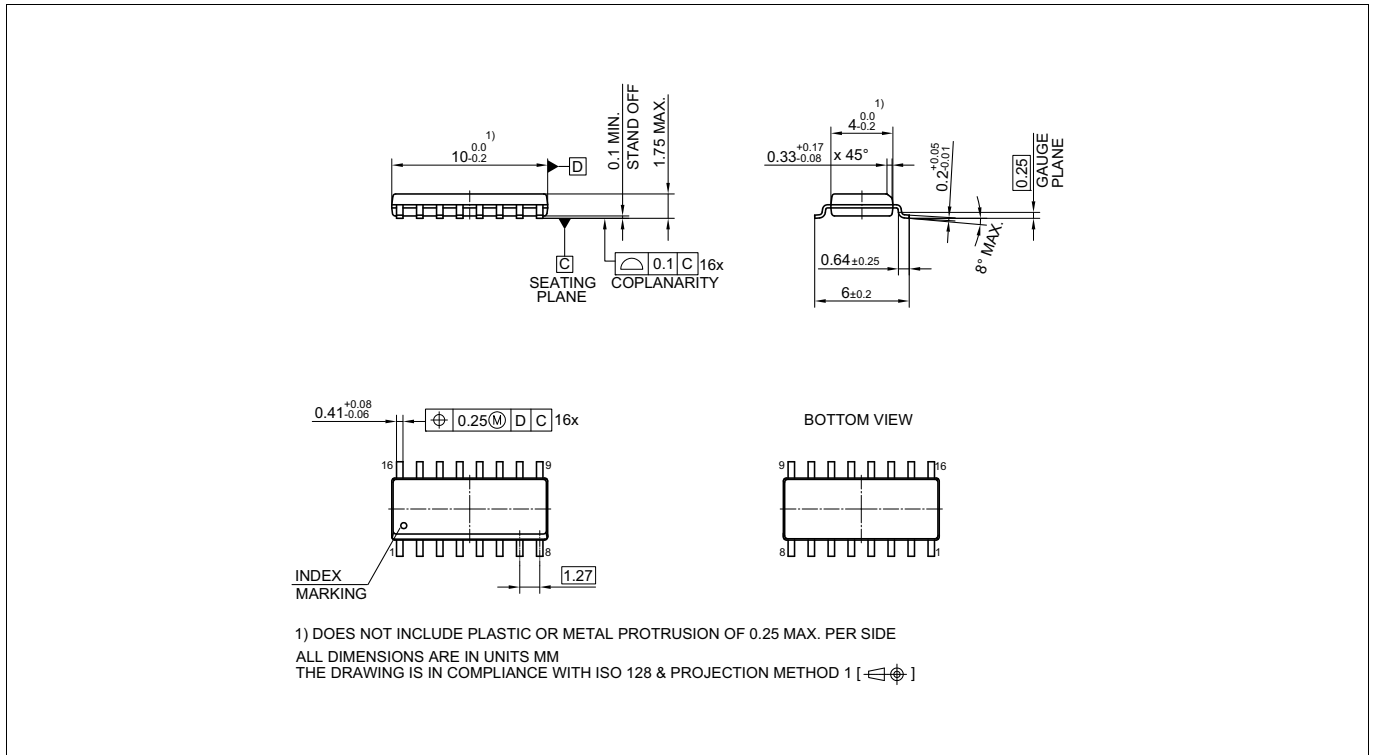


Figure 17 PG-DSO-16-11 outline

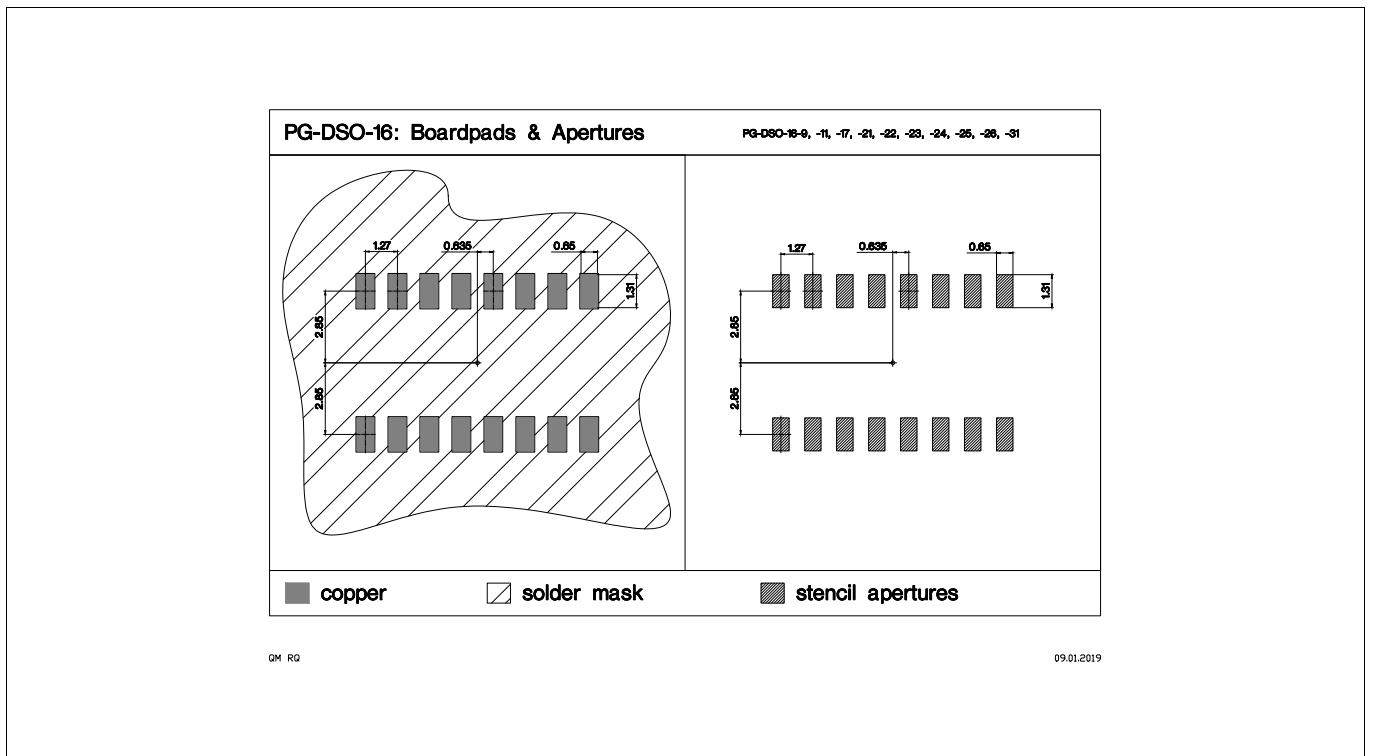
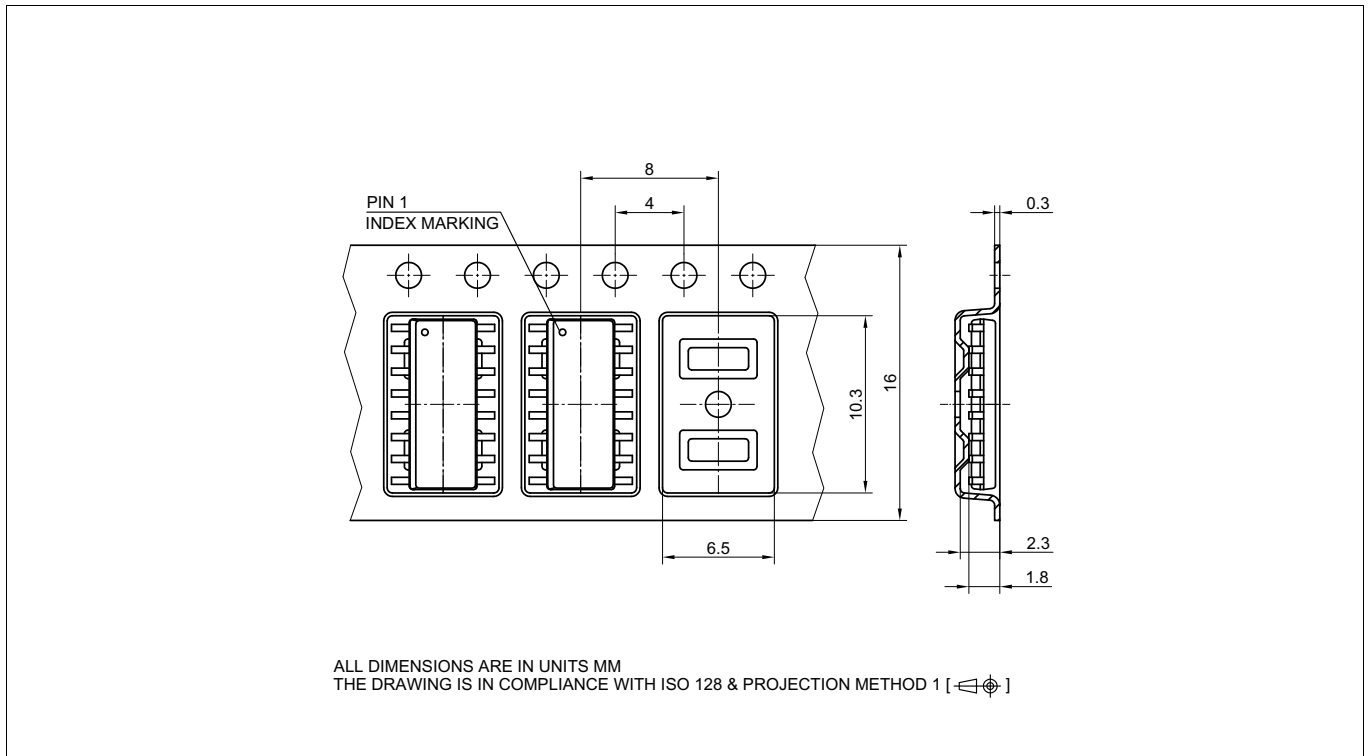


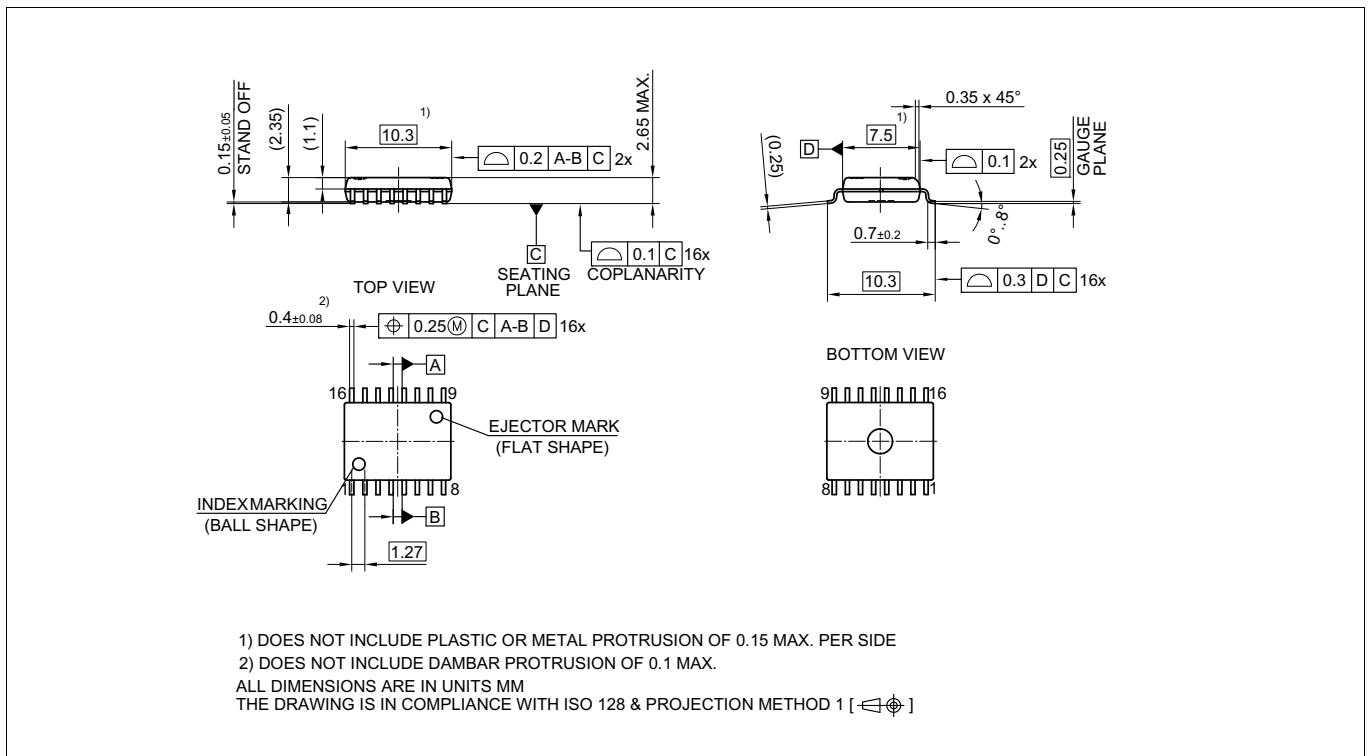
Figure 18 PG-DSO-16-11 footprint

**Package**



**Figure 19 PG-DSO-16-11 packaging**

**7.3 Package PG-DSO-16-30**



**Figure 20 PG-DSO-16-30 outline**

Package

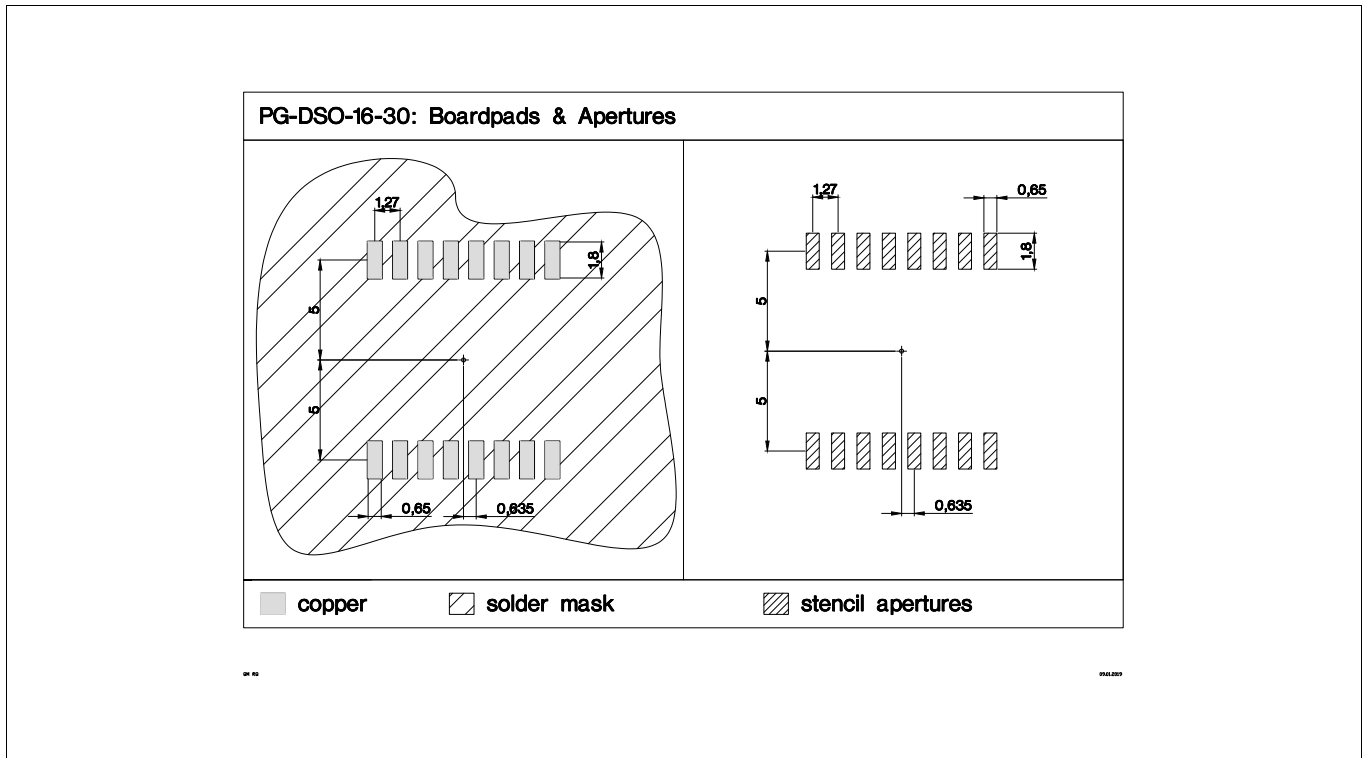


Figure 21 PG-DSO-16-30 footprint

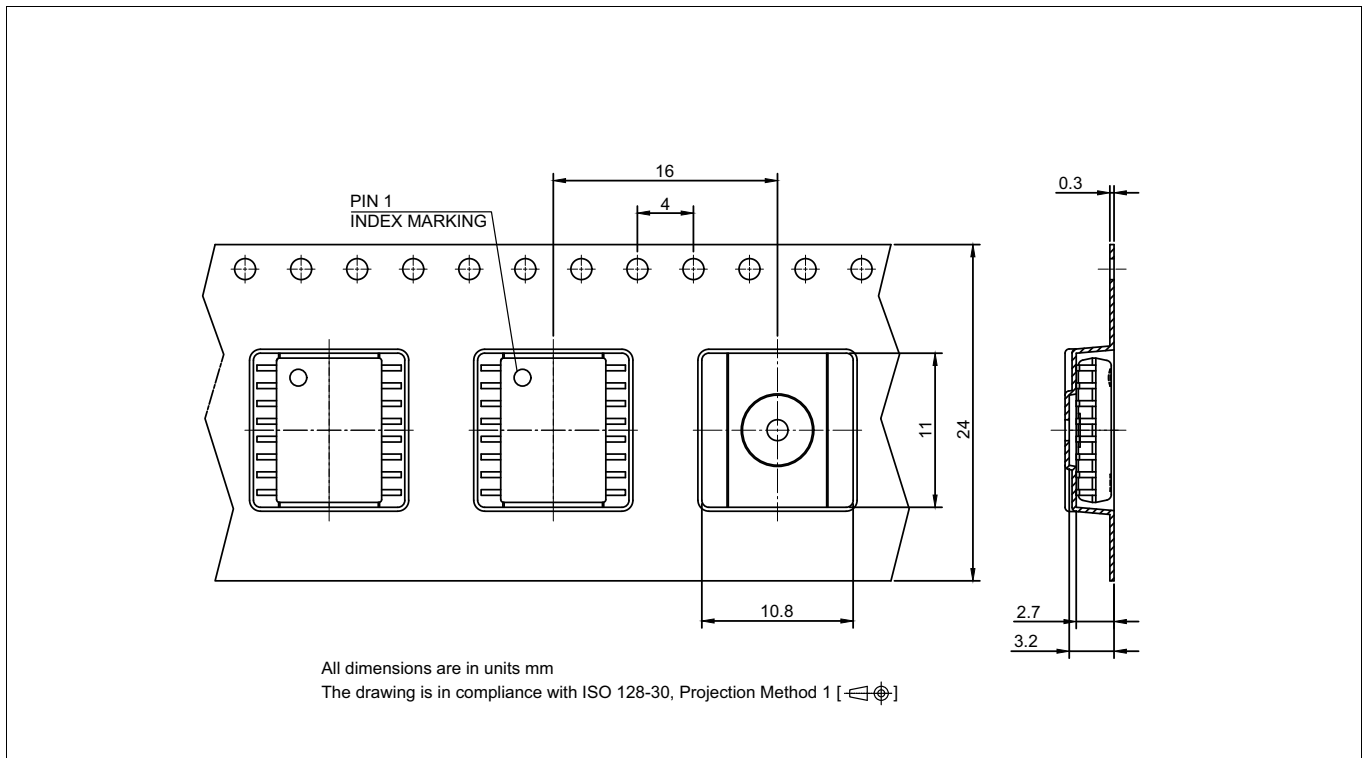


Figure 22 PG-DSO-16-30 packaging

Package

7.4 Package PG-TFLGA-13-1

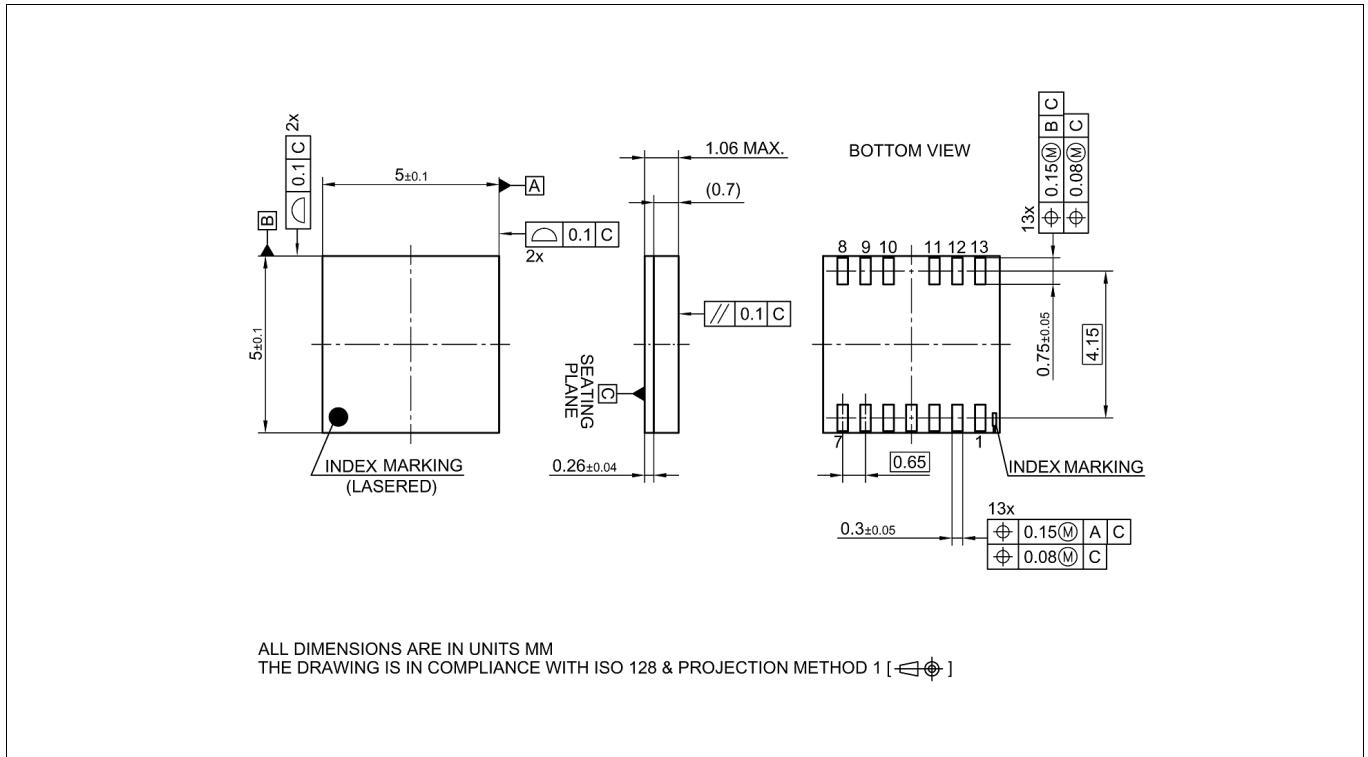


Figure 23 PG-TFLGA-13-1 outline

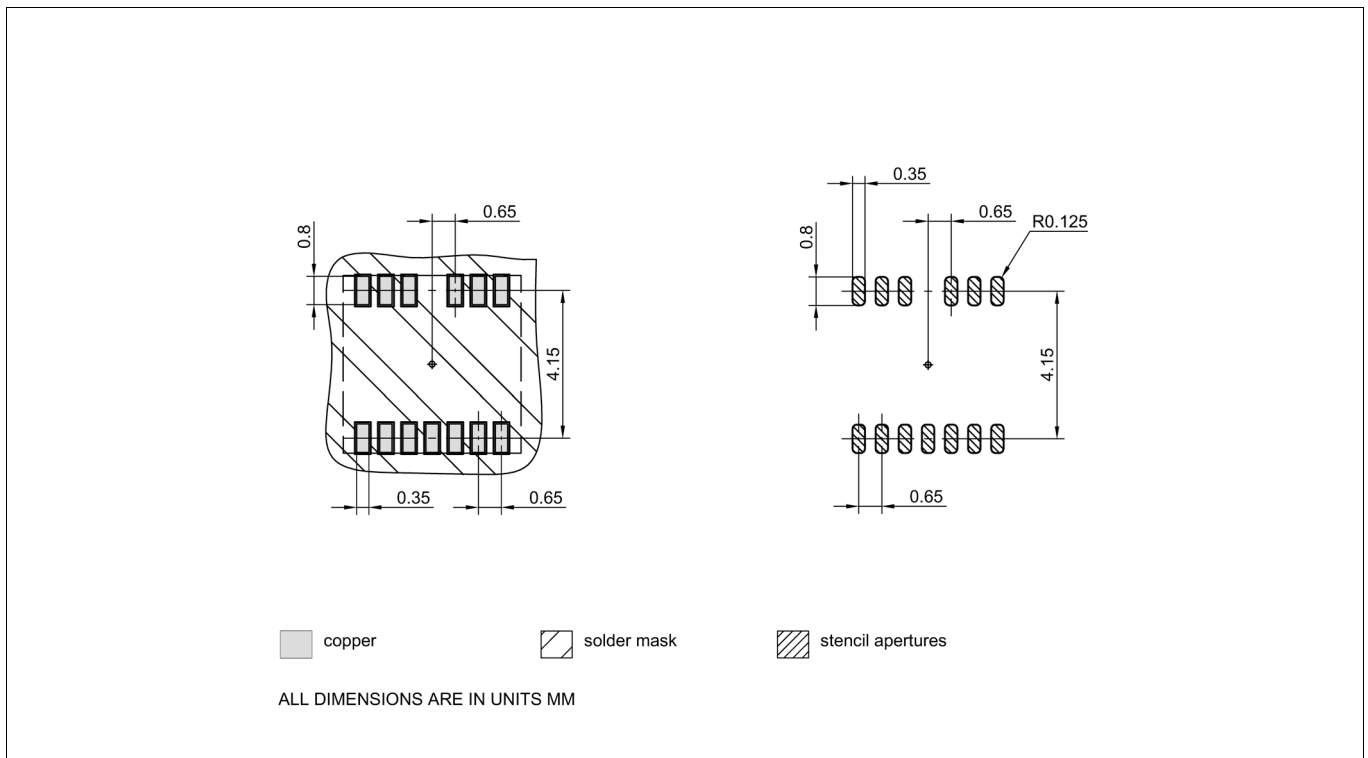


Figure 24 PG-TFLGA-13-1 footprint

Package

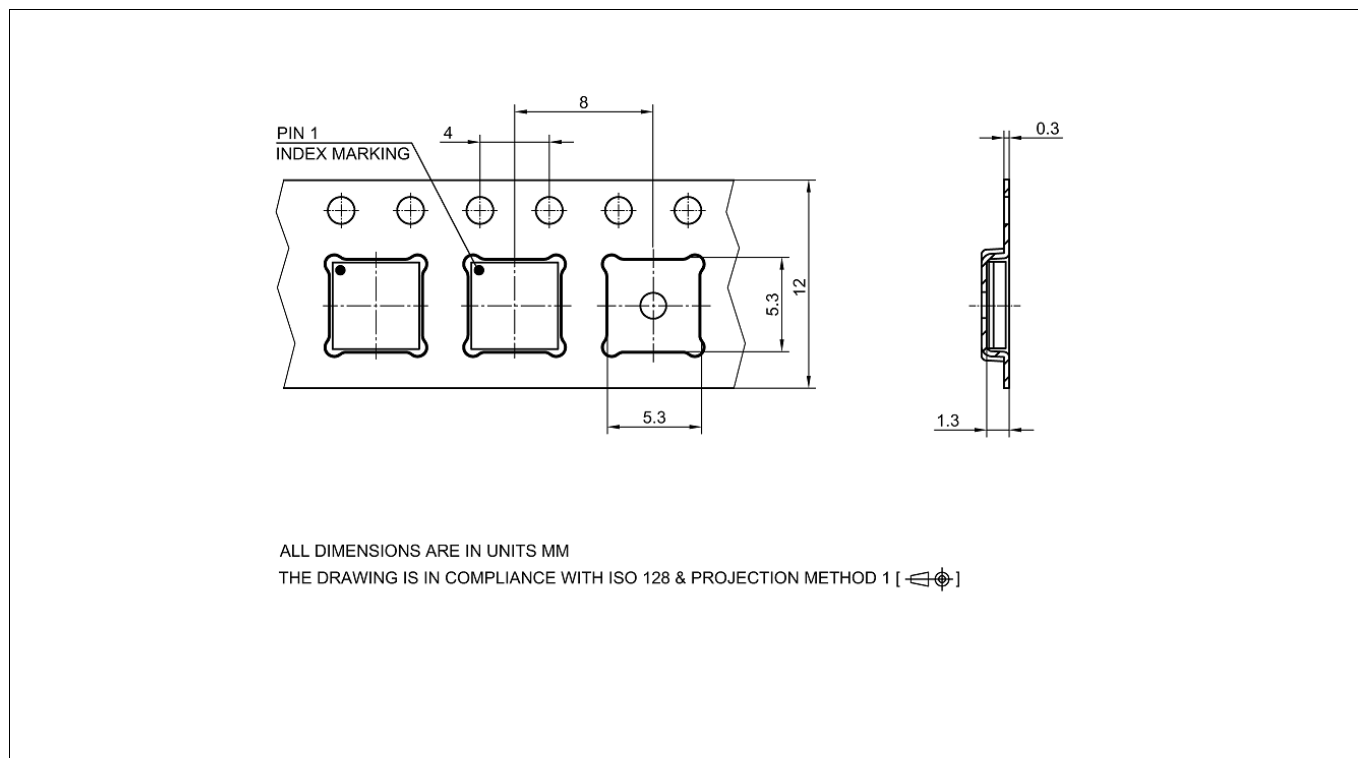


Figure 25 PG-TFLGA-13-1 packaging

## Revision history

Page or Item	Subjects (major changes since previous revision)
<b>Rev 2.7 Datasheet, 2021-09-10</b>	
<b>Table 6, Table 8</b>	“Input supply voltage” → “Voltage at pin VDDI” to highlight that the supply voltage can be higher if the SLDO is activated
Whole document, <b>Table 1, Table 31</b>	added 2EDS7165H, 2EDF8275F products
<b>Table 1</b>	modified footnote 2
<b>Figure 6</b>	fixed typo
<b>Rev 2.6 Datasheet, 2021-04-23</b>	
<b>Page 1, Table 1, Table 25</b>	added reference to issued EN 60601-1 certification
<b>Page 1, Table 1, Table 25</b>	added reference to issued GB4943.1 certification
<b>Page 1, Table 1, Table 25</b>	removed reference to CSA C22.2 No. 62368-1 as it is not anymore planned
<b>Table 17</b>	added UVLO start-up and deactivation time
<b>Rev 2.5 Datasheet, 2020-02-07</b>	
<b>Page 1</b>	“certified according to DIN V VDE V0884-10” changed in “DIN V VDE V0884-10 compliant” due to standard expiration on 2019.12.31
Whole document	added references to 2EDF9275F and 2EDS9265H (13 V UVLO options for SiC MOSFETs driving)
<b>Page 1, Table 1</b>	added reference to EN 61010-1 certification
<b>Page 1</b>	update of term DIN EN 62368-1 and DIN EN 60950-1
<b>Table 1</b>	CQC removed from <b>Table 1</b> due to presence of footnote <sup>2)</sup>
<b>Table 1</b>	added footnote <sup>3)</sup> due to expiration of VDE0884-10 certification
<b>Table 1, Table 31</b>	added 2EDF9275F and 2EDS9265H products
<b>Table 1</b>	removed OPN for better readability; OPN shown in <b>Table 31</b>
<b>Table 13</b>	$V_{IN}$ max. value 6.5 V → 15 V
<b>Table 9</b>	added $I_{V_{DDA}}$ , $I_{V_{DDB}}$ quiescent current for 2EDF9275F and 2EDS9265H
<b>Table 11</b>	added $V_{DDA}$ , $V_{DDB}$ Undervoltage Lockout table for 2EDF9275F and 2EDS9265H
<b>Table 13</b>	added “UVLO threshold vs temperature” for the 13 V UVLO options (2EDF9275F, 2EDS9265H)
<b>Table 24, Table 25</b>	added tables for overview on safety-related certifications of PG-DSO-16-30
<b>Table 26</b>	“see VDE certificate” footnote removed due to certification expiration
<b>Table 28</b>	fixed typo in the test condition: 5700 kV <sub>RMS</sub> → 5700 V <sub>RMS</sub>
<b>Table 31</b>	new OPN and “B” marking: improved secondary-side clamping performance
<b>Rev 2.4 Datasheet, 2019-02-08</b>	
<b>Table 6</b>	max. $V_{DDI}$ : 3.7 V → 4.0 V
<b>Rev. 2.3 Datasheet, 2019-01-31</b>	
Whole document	removed “certification pending” because certification has been issued (see <b>Table 1</b> )

Page or Item	Subjects (major changes since previous revision)
<a href="#">Chapter 7</a>	latest footprints, outlines and packaging for PG-DSO-16-11 and PG-DSO-16-30
<a href="#">Figure 7</a>	adjusted values
<a href="#">Page 1</a>	propagation delay variance in “ <a href="#">Features</a> ” updated
<a href="#">Table 1</a> and <a href="#">Table 31</a>	OPN inserted for 2EDF7235K
<a href="#">Table 6</a>	reference to max. value $\rightarrow V_{DDO}$ for voltage at pins OUTA and OUTB
<a href="#">Table 6</a>	removed footnote 1 from parameter “Non-destructive Common Mode Transient Immunity”
<a href="#">Table 8</a>	$T_{amb}$ max. value 85°C $\rightarrow$ 125°C
<a href="#">Table 17</a>	$C_{LOAD}$ in "Note or test condition" moved to table description
<a href="#">Table 18</a> , <a href="#">Table 21</a> and <a href="#">Table 26</a>	Non-destructive Common Mode Transient Immunity transferred to <a href="#">Table 6</a> , <a href="#">Absolute maximum ratings</a>
<a href="#">Table 18</a>	added footnote to “Capacitance” and “Resistance” parameters
<a href="#">Table 21</a>	footnotes assignation patched
<b>Rev. 2.2 Datasheet, 2018-11-07</b>	
<a href="#">Chapter 3.2</a>	Update device part numbers
<a href="#">Chapter 4</a>	Update of term “DIN V, VDE V0884-10”
<a href="#">Page 1</a>	Update product validation in “ <a href="#">Features</a> ”
<a href="#">Table 1</a> , <a href="#">Table 31</a>	Update of OPN
<a href="#">Table 6</a>	Removed typos
<b>Rev. 2.1 Datasheet, 2018-10-24</b>	
<a href="#">Table 1</a> , <a href="#">Table 6</a> , <a href="#">Table 31</a>	Updates
<b>Rev. 2.0 Datasheet, 2018-06-04</b>	
	Initial data sheet available



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