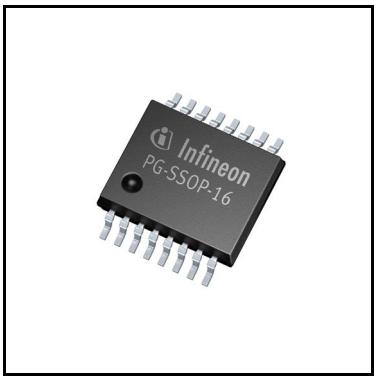
TLE9221SX

FlexRay Transceiver

AEC Qualified RoHS



1 Overview

Features

- Compliant with the FlexRay Electrical Physical Layer Specification, version 3.0.1 and ISO 17458
- Optimized for time-triggered in-vehicle networks with data transmission rates from 1 Mbit/s up to 10 Mbit/s
- Optimized electromagnetic immunity (EMI)
- Very low electromagnetic emission (EME), supporting large networks and complex bus topologies
- Very high level of ESD robustness, 11 kV according to IEC-61000-4-2
- Supports 60 ns minimum bit time
- Optimized digital inputs to minimize jitter
- Integrated Bus Guardian Interface
- Bus failure protection and error detection
- Automatic voltage adaptation on the digital interface pins
- High current digital outputs, optimized to drive long wires and high capacitive loads
- Green Product (RoHS compliant)

Potential applications

- Electronic power steering
- Engine control unit
- Chassis domain control

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

FlexRay is a serial, deterministic bus system for real-time control applications. It is designed for future requirements of in-vehicle control applications, providing data transmission rates up to 10 Mbit/s. FlexRay is designed for collision-free data communication. The nodes do not arbitrate and the FlexRay Communication Controller (CC) guarantees a collision-free bus access during normal operation.

Overview

The TLE9221SX FlexRay transceiver is a FlexRay bus driver (BD) and it accomplishes the physical interface between the Communication Controller and the bus medium. Fully compliant with the FlexRay Electrical Physical Layer Specification, version 3.0.1 (acronym EPL) and ISO 17458.

The TLE9221SX supports the following functional classes:

- Functional class “bus driver voltage regulator control”
- Functional class “bus driver bus guardian interface”
- Functional class “bus driver logic level adaption”
- Functional class “bus driver remote wake-up”

The TLE9221SX supports data transmission rates from 1 Mbit/s up to 10 Mbit/s. Besides the transmit and receive capability of the bus, the TLE9221SX provides arrangements for low power supply management, supply voltage monitoring and bus failure detection.

In BD_Sleep mode, the TLE9221SX quiescent current decreases to a typical, total current consumption of 47.5 mA, while the device is still able to wake up by a dedicated wake-up pattern on the FlexRay data bus or by a local wake-up event on the pin WAKE. The INH output pin allows the control of external circuitry depending on the selected mode of operation.

Fail-safe features, like bus failure detection or the power supply monitoring, combined with an easy accessible Status Information Register support the requirements of safety-related applications with extended diagnostic features.

The TLE9221SX is internally protected against transients on all global pins. Global pins are BP, BM, WAKE and V_{BAT}. It is possible to use the TLE9221SX without any additional external protection circuitry while the TLE9221SX meets the ESD and ISO pulse requirements of the car manufactures.

The TLE9221SX is designed on the latest Infineon Smart Power Technology SPT, which combines power devices with a highly integrated logic process. Based on its digital design concept, the TLE9221SX provides very high immunity against RF disturbances over a wide frequency range.

Based on the high symmetry of the BP and BM signals, the TLE9221SX provides the lowest level of electromagnetic emission (EME) within a wide frequency range.

The TLE9221SX is integrated in a RoHS compliant PG-SSOP-16 package. The TLE9221SX and the Infineon Smart Power Technology SPT are especially tailored to withstand the harsh conditions of the automotive environment and qualified according to the AEC-Q100 standard.

Type	Package	Marking
TLE9221SX	PG-SSOP-16	9221

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2 Block Diagram

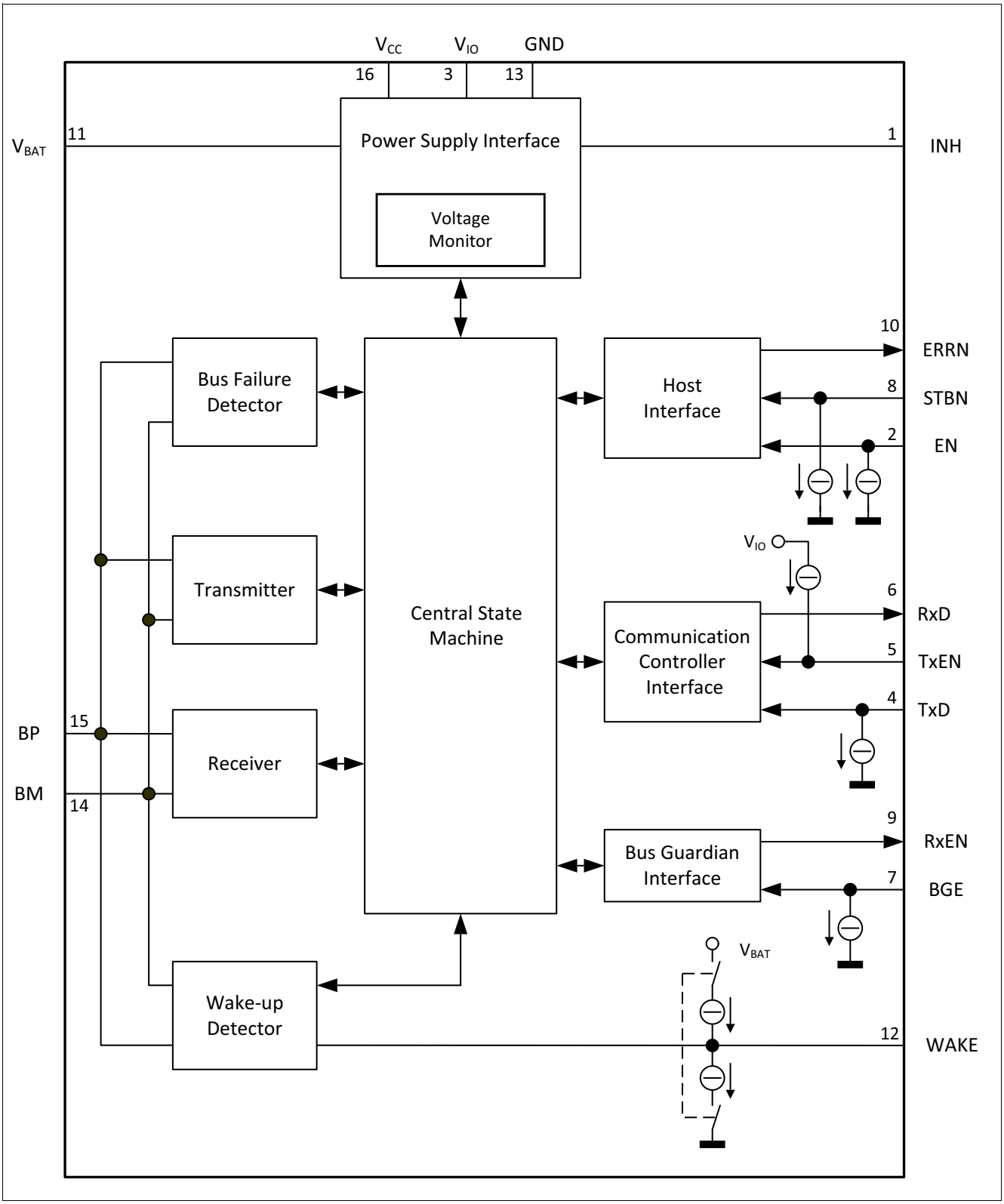


Figure 1 Block diagram

3 Pin Configuration

3.1 Pin Assignment

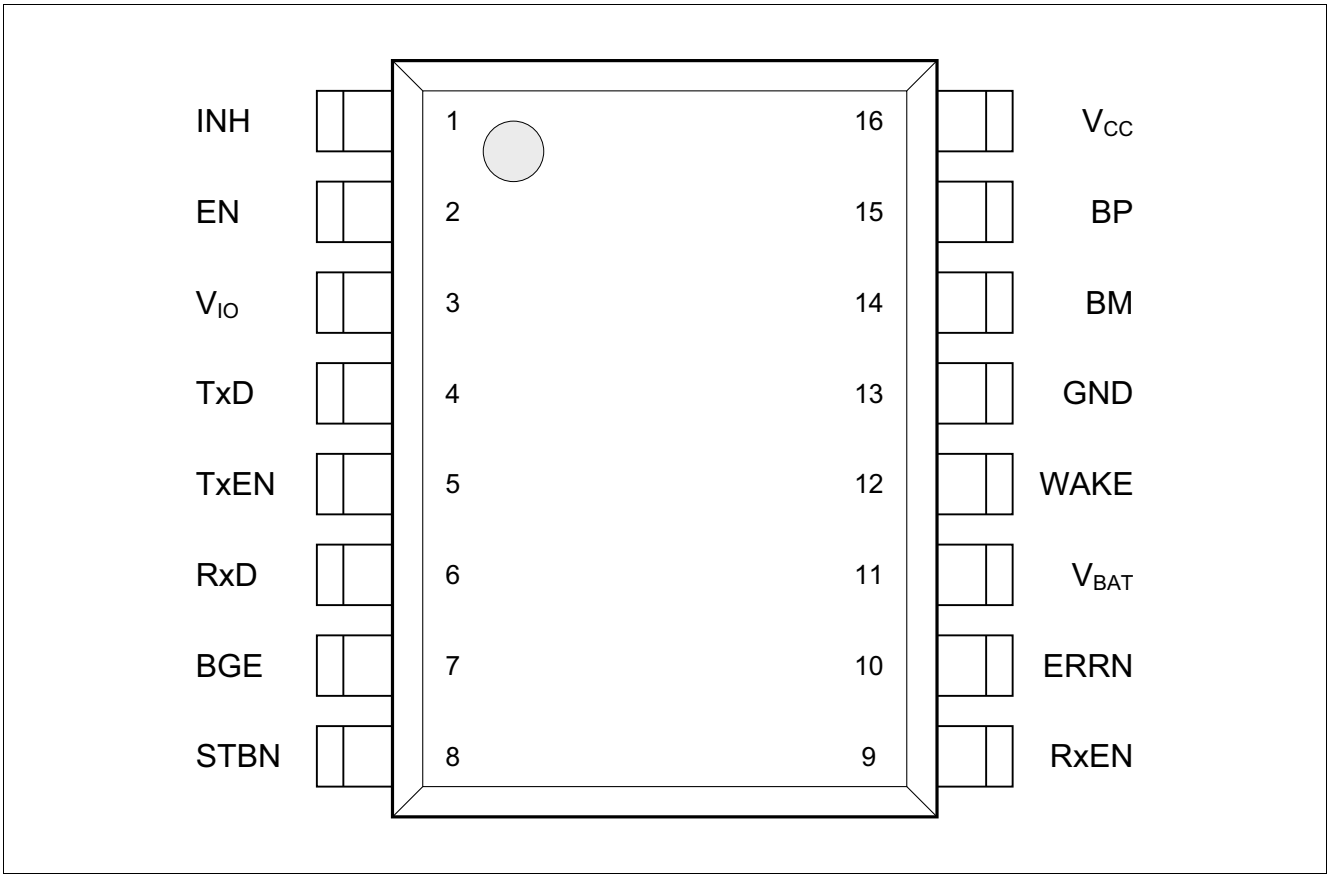


Figure 2 Pin configuration

3.2 Pin Definitions

Table 1 Pin definition and functions

Pin	Symbol	Function
1	INH	**Inhibit Output;** open drain output to control external circuitry, “high” impedance in BD_Sleep mode.
2	EN	**Enable Mode Control Input;** digital input for the mode selection, integrated “pull-down” resistor to GND.
3	V_{IO}	**Level Shift Input;** reference voltage for the digital input and output pins, 100 nF decoupling capacitor to GND recommended.
4	TxD	**Transmit Data Input;** integrated “pull-down” current source to GND, logical “low” to drive “Data_0” to the FlexRay bus.

Pin Configuration

Table 1 Pin definition and functions

Pin	Symbol	Function
5	TxEN	**Transmitter Enable Not Input;** integrated “pull-up” current source to V_{IO}, logical “low” to enable the Transmitter.
6	RxD	**Receive Data Output;** logical “low” while “Data_0” is on the FlexRay bus, output voltage adapted to the voltage on the V_{IO} level shift input.
7	BGE	**Bus Guardian Enable Input;** logical “high” to enable the Transmitter, integrated “pull-down” current source to GND.
8	STBN	**Stand-by Not Mode Control Input;** digital input for the mode selection, integrated “pull-down” current source to GND.
9	RxEN	Receive Data Enable Not Output; logical “low” indicates activity on the FlexRay bus, logical “high” in case the FlexRay Bus is “Idle”, output voltage adapted to the voltage on the V_{IO} level shift input.
10	ERRN	Error Not Diagnosis Output; logical “low” in failure case, output voltage adapted to the voltage on the V_{IO} level shift input.
11	V_{BAT}	Battery Voltage Supply; 100 nF decoupling capacitor to GND recommended.
12	WAKE	Wake-up Input; local wake-up input, terminated against GND and V_{BAT}, wake-up input sensitive to signal changes in both directions.
13	GND	Ground;
14	BM	Bus Line Minus; negative input/output to the FlexRay bus.
15	BP	Bus Line Plus; positive input/output to the FlexRay bus.
16	V_{CC}	Supply Voltage; Transmitter supply voltage, 100 nF decoupling capacitor to GND recommended.

4 Functional Overview

4.1 Functional Description

FlexRay is a differential bus system. The data is exchanged via a dual wire bus medium on the wires BP (Bus Line Plus) and BM (Bus Line Minus).

Three different bus symbols are supported: “Data_0”, “Data_1” and bus “Idle”. An active Transmitter of the TLE9221SX drives “Data_0” or “Data_1” to the bus medium, depending on the TxD input signal. To sustain an “Idle” signal on the FlexRay bus, the Transmitter is turned off, the voltage difference between BP and BM is below 30 mV, and the absolute voltage level on both bus lines, BP and BM depends on the Bus Biasing (see **Figure 3**):

- “Data_1”: uBus = uBP - uBM ≥ 300 mV → positive voltage between BP and BM
- “Data_0”: uBus = uBP - uBM ≤ - 300 mV → negative voltage between BP and BM
- “Idle”: |uBus| = |uBP - uBM| ≤ 30 mV

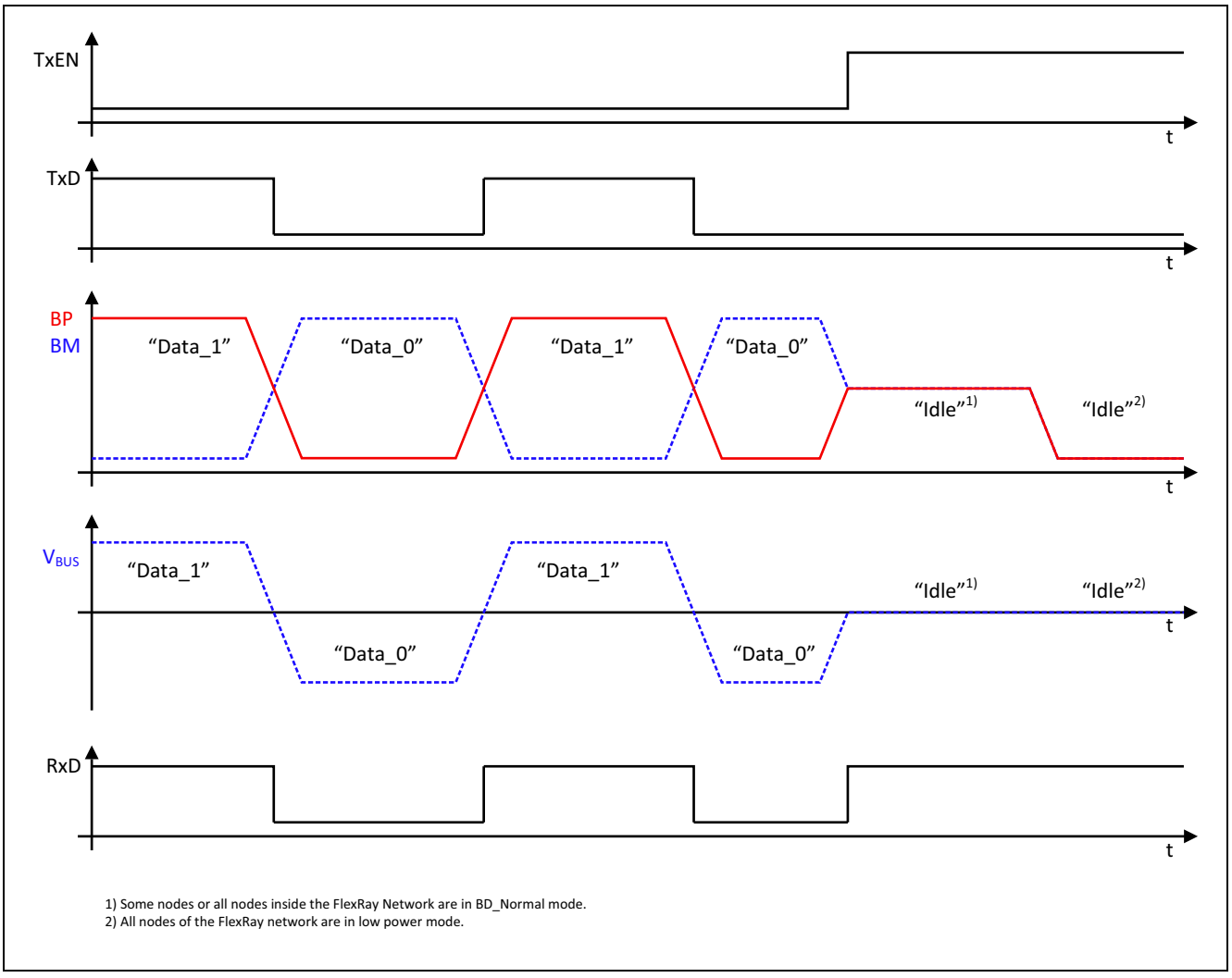


Figure 3 FlexRay EPL bus signals without Bus Guardian Interface

4.2 Modes of Operation

The FlexRay bus driver TLE9221SX supports four different modes of operation:

- BD_Normal mode
- BD_ReceiveOnly mode
- BD_Standby mode
- BD_Sleep mode

Each mode has specific characteristics in terms of quiescent current, data transmission or failure diagnostic. To enter the BD_Sleep mode, the TLE9221SX provides an intermediate mode, the so-called BD_GoToSleep command.

Mode changes on the TLE9221SX are either triggered by:

- The Host Interface and a host command on the input pins EN and STBN.
- The Power Supply Interface and an undervoltage event on one of the two power supplies or the reference supply uV_{IO}.
- The Wake-up Detector and wake-up events either on the FlexRay bus or on the local wake-up pin WAKE.

While all power supplies are turned off, the transceiver TLE9221SX is in BD_Off condition or also called “without supply”.

In BD_Sleep mode and in BD_Standby mode the quiescent current consumption at all three supplies is tailored to reach the minimum, and therefore only a limited set of the functions of the TLE9221SX is available. BD_Sleep mode and BD_Standby mode are also called low power modes. Conversely the modes BD_Normal and BD_ReceiveOnly are called non-low power modes.

4.3 Behavior of Unconnected Digital Input Pins

The integrated pull-up and pull-down resistors at the digital input pins force the TLE9221SX into a secure, fail safe behavior if the input pins are not connected and floating (see **Table 2** for details).

If the TxEN pin or the BGE pin is not connected in BD_Normal mode, the Transmitter is disabled. If the TxD input pin is open in BD_Normal mode and the Transmitter is active, the transceiver TLE9221SX drives a “Data_0” signal to the bus.

If the mode control input pins of the Host Interface are not connected, the pull-down resistors on the EN pin and on the STBN pin set the TLE9221SX by default to BD_Standby mode.

Table 2 Logical inputs when unconnected

Input Signal	Default State	Comment
TxD[1)]	“low”	pull-down to GND
TxEN[1)]	“high”	pull-up to uV_{IO}
STBN	“low”	pull-down to GND
EN	“low”	pull-down to GND
BGE[1)]	“low”	pull-down to GND

1) In BD_Sleep, BD_Standby, and also in BD_ReceiveOnly mode, the inputs TxD, TxEN and BGE are blocked by the internal logic. To optimize the total quiescent current consumption, the pull-up and pull-down structures are disabled in BD_Sleep mode, BD_Standby mode and BD_ReceiveOnly mode.

The Power Supply Interface detects missing supply voltages or a missing reference supply. The Central State Machine sets the TLE9221SX into a fail safe mode when a supply is not available (details see **Chapter 8.3**).

5 Overview Functional Blocks

5.1 Transmitter

The Transmitter is the output driver for the FlexRay bus. It is based on a “high” side and “low” side push-pull unit. The push-pull units are supplied by the power supply uV_{CC} (see **Figure 4**).

While driving a “Data_1” or “Data_0” signal on to the FlexRay bus, the transceiver is active and enabled. During an “Idle” signal, the transceiver is turned off.

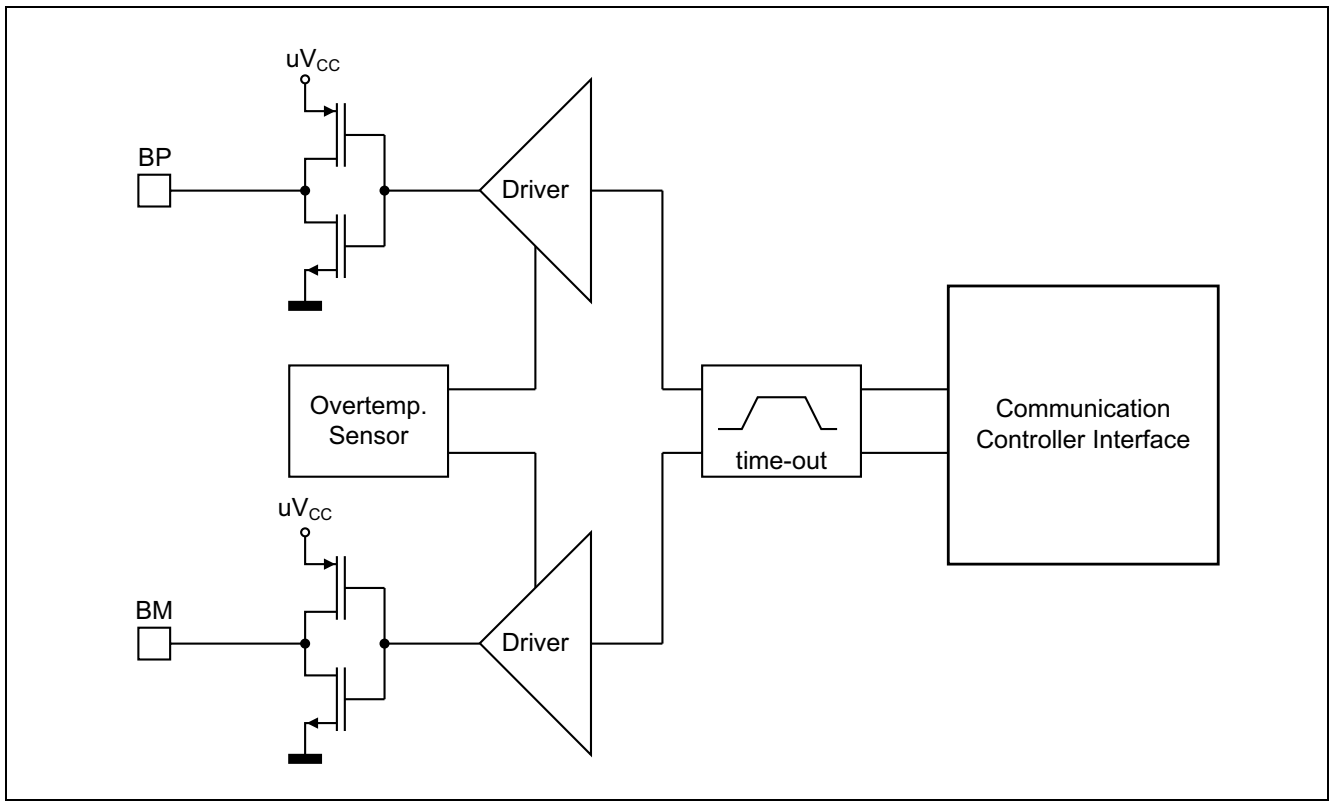


Figure 4 Block diagram of the Transmitter

The Transmitter is protected by an internal temperature sensor against overheating in terms of a short circuit on the bus lines BM or BP. The Transmitter is controlled by the Communication Controller Interface (see **Chapter 5.3**). The Transmitter is only active in BD_Normal mode.

5.2 Receiver

The Receiver detects communication elements, like “Idle”, “Data_1” and “Data_0”, when it is not in low power mode. It is connected to the BP and BM I/O pins of the TLE9221SX, together with the Transmitter, the Bus-Failure Detector, and the Wake-up Detector (see **Figure 1**). Based on a digital sampling concept, the Receiver is optimized to withstand the RF immunity requirements of the automotive industry.

The low pass input filter is tailored to support analog bit times down to 60 ns. Data bits below 60 ns may not be detected as valid communication elements. When the Receiver detects activity on the FlexRay bus behind the input filter, the differential Receiver distinguishes whether “Data_0” or “Data_1” is signaled by the differential bus voltage. The bus activity information is provided to the Bus Guardian Interface. The information regarding the FlexRay data bits is provided to the Communication Controller (see **Figure 5**).

The thresholds and the timings of the Receiver are available in **Figure 44** and **Figure 45**.

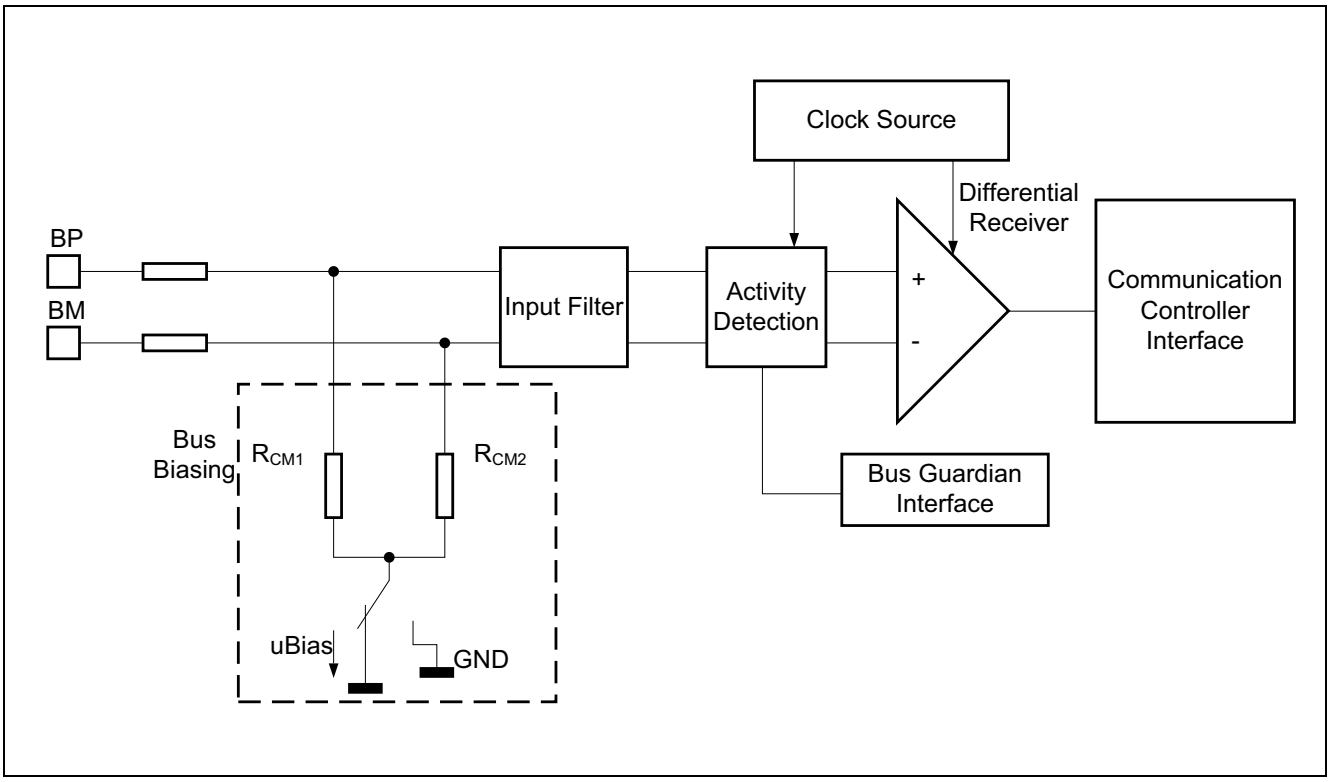


Figure 5 Block diagram of the Receiver

Apart from receiving data, the Receiver is responsible for biasing the FlexRay bus. The biasing of the FlexRay bus depends on the selected mode of operation.

In BD_Normal mode and BD_ReceiveOnly mode, the voltage uBias is connected to the BP and BM pins across the common mode resistors R_{CM1} and R_{CM2}. In BD_Sleep mode, BD_Standby mode and in the BD_GoToSleep command the I/O pins BP and BM are connected to GND via the common mode resistors R_{CM1} and R_{CM2}.

When TLE9221SX is not supplied, the bus biasing is open and is neither switched to uBias nor to GND, the BP and BM pins appear to the FlexRay bus as a high-impedance input (see **Table 3** and **Figure 5**).

Table 3 Bus biasing

Mode of Operation	Bus Biasing	Transmitter
BD Normal	uBias	active or disabled
BD_ReceiveOnly	uBias	disabled
BD_Standby	GND	disabled
BD_GoToSleep command	GND	disabled
BD_Sleep	GND	disabled
BD_Off condition	Open	disabled

5.3 Communication Controller Interface

The Communication Controller Interface is the interface between the FlexRay transceiver TLE9221SX and the FlexRay Communication Controller (CC). It comprises three digital signals:

- The TxEN (Transmit Data Enable Not) input pin
- The TxD (Transmit Data) input pin
- The RxD (Receive Data) output pin

The logical I/O levels of all three digital pins are adapted to the reference voltage uV_{IO}. In case uV_{IO} is not available or in an undervoltage condition, the RxD output is set to logical “low” and the input pins TxD and TxEN are set to their default condition (see **Table 2**).

The Communication Controller logic block handles the interlock between TxD and TxEN. The Central State Machine provides the interface to other TLE9221SX function blocks and handles the dependency based on the selected mode of operation (see **Figure 6**).

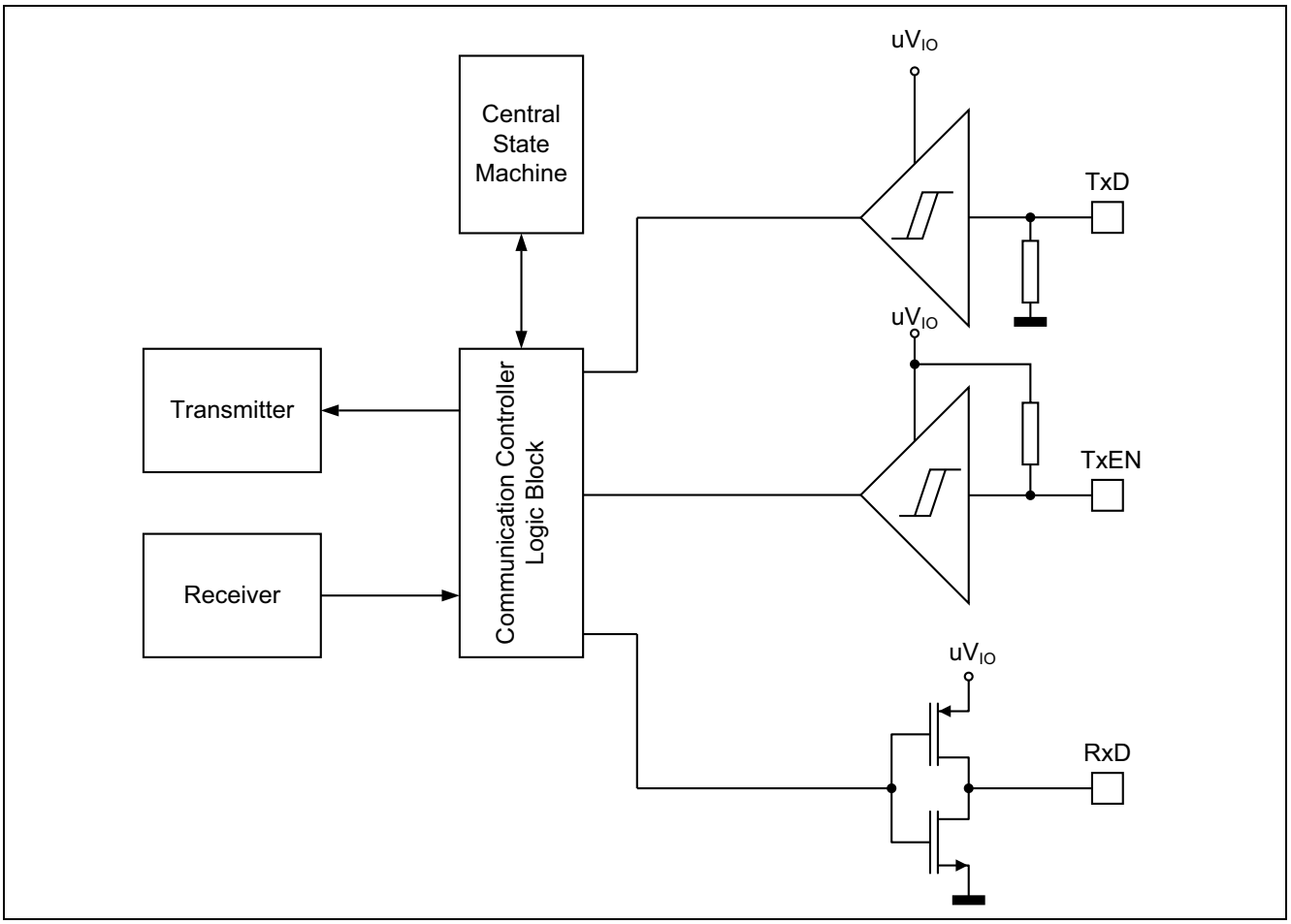


Figure 6 Block diagram of the Communication Controller Interface

The TxD input of the Communication Controller Interface is active only when the Transmitter is activated. To activate the Transmitter, the transceiver TLE9221SX needs to be in BD_Normal mode, the TxEN input must be at logical “low” and the BGE input pin must be at logical “high” (see **Table 4**).

The FlexRay transceiver shall never start data transmission with the communication element “Data_1”. Therefore, the activation of the Transmitter via the TxEN signal is only possible while the TxD signal is at logical “low” (see **Figure 7**).

While the Transmitter is enabled, the Communication Controller Interface drives the serial digital data stream available at the TxD input pin to the FlexRay bus via the Transmitter. A logical “high” signal at the TxD pin drives a “Data_1” signal to the FlexRay bus and a logical “low” signal drives a “Data_0” signal (see **Table 4**).

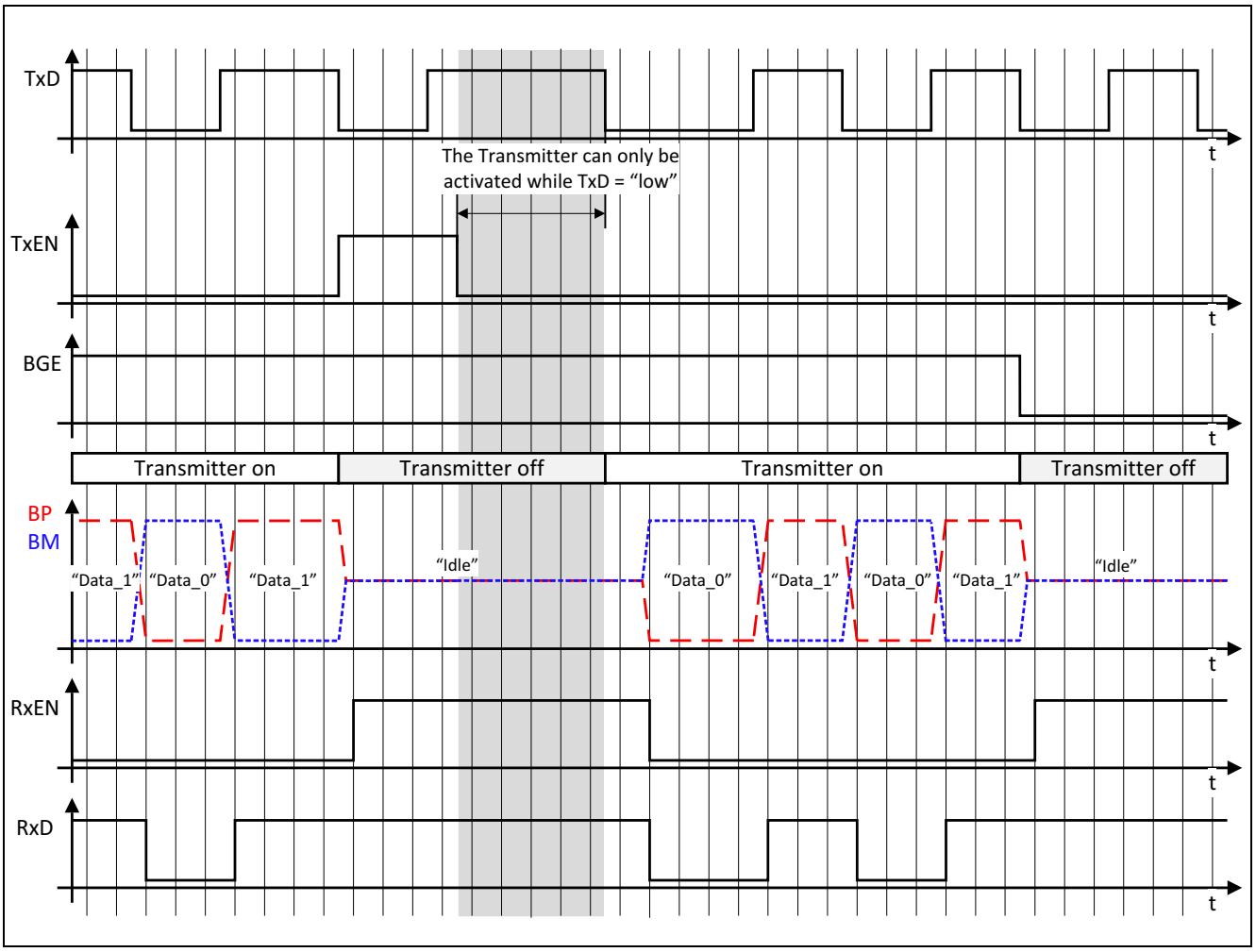


Figure 7 FlexRay physical layer bus signals with Bus Guardian Interface

The Receiver of the TLE9221SX is active in all non-low power operating modes. Similar to the TxD input, the RxD output indicates a “Data_1” signal on the FlexRay bus by a logical “high” signal and the “Data_0” signal by a logical “low” signal.

In every low power mode, the TxD and TxEN input pins are disabled. The RxD output pin is used to indicate the wake-up flag, while the transceiver is in low power mode (see **Table 5**).

5.4 Bus Guardian Interface

The Bus Guardian Interface comprises two digital signals:

- The BGE (Bus Guardian Enable) input pin.
- The RxEN (Receive Enable Not) output pin.

The logical I/O levels of the input and the output pin are adapted to the reference voltage uV_{IO}. In case uV_{IO} is not available or in undervoltage condition, the RxEN output is set to logical “low” and the input pin BGE is set to its default condition (see **Table 2**).

The Bus Guardian logic block handles the connection to the Transmitter and the Receiver. The Central State Machine provides the interface to other TLE9221SX function blocks and handles the dependency on the selected mode of operation (see **Figure 8**).

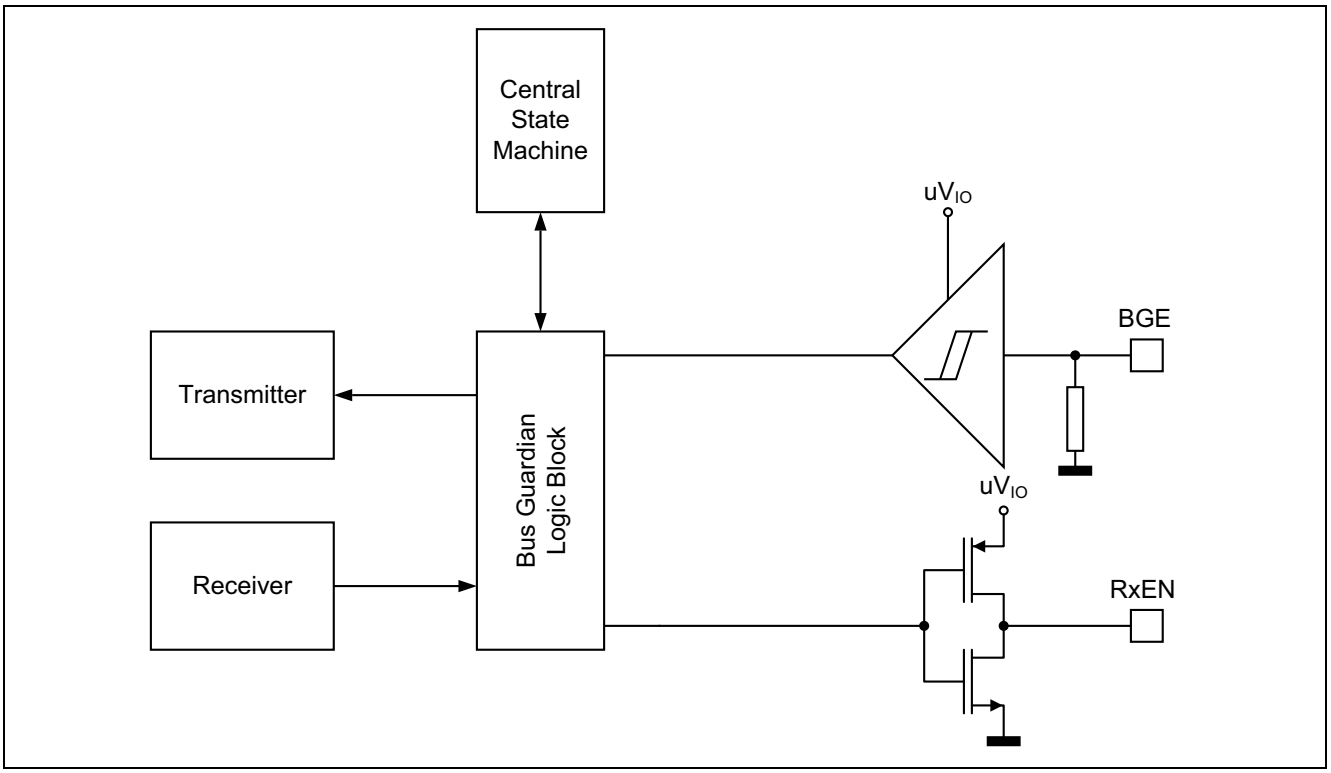


Figure 8 Block diagram of the Bus Guardian Interface

The BGE input is an additional fail safe input, allowing external hardware to block the data stream driven to the FlexRay bus medium. Switching the BGE input to logical “low” disables the Transmitter of TLE9221SX regardless of the signals on all the other digital input pins. The BGE input is active only in BD_Normal mode (see **Table 4** and **Figure 7**).

Table 4 TxD/TxEN interface, acting as a Transmitter

Mode of Operation	TxEN	BGE	TxD	Resulting Signal on the Bus
BD_Normal	“high”	X[1)]	X	“Idle”
	X	“low”	X	“Idle”
	“low”	“high”	“low”	“Data_0”
	“low”	“high”	“high”	“Data_1”
All other modes	X	X	X	“Idle”

1) X = don’t care

The RxEN (Receive Enable Not) indicates the activity on the FlexRay bus. In case the FlexRay bus is “Idle”, the logical signal on the RxEN is “high”. Any active data signal on the FlexRay bus, regardless of whether it is “Data_0” or “Data_1”, is indicated by a logical “low” signal on the RxEN output pin. Like the RxD output pin, the RxEN output pin indicates also the wake-up flag while the transceiver is in low power mode (see **Table 5** and **Figure 7**).

Table 5 RxD/RxEN interface, acting as Receiver with Bus Guardian Interface

Mode of Operation	Signal on the Bus Wires	Wake-up Flag	RxD	RxEN
BD_Normal, BD_ReceiveOnly	“Idle”	X[1)]	“high”	“high”
	“Data_0”	X	“low”	“low”
	“Data_1”	X	“high”	“low”
BD_Sleep, BD_StandBy	X	“low” (set)	“low”	“low”
	X	“high” (not set)	“high”	“high”

1) X = don’t care

5.5 Host Interface

The Host Interface is the interface between the FlexRay transceiver TLE9221SX and the FlexRay host controller. It allows the host to control the operating modes and to read status and diagnostics information. It comprises three digital signals:

- The EN (Enable) input pin
- The STBN (Stand-By Not) input pin
- The ERRN (Error Not) output pin

The logical I/O levels of the pins are adapted to the reference voltage uV_{IO}. In case uV_{IO} is not available or in undervoltage condition, the ERRN output is set to logical “low” and the input pins EN and STBN are set to their default condition (see **Table 2**).

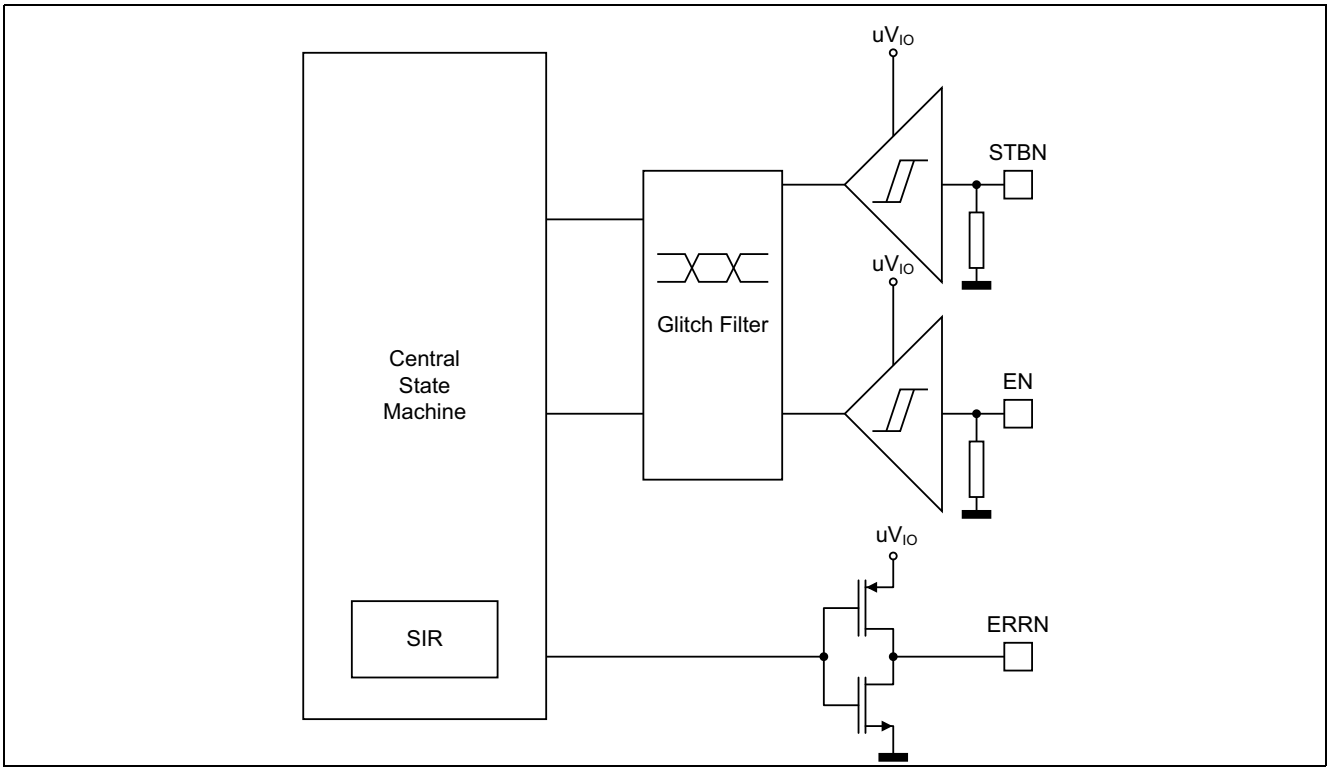


Figure 9 Block diagram of the Host Interface

The EN and STBN pins control the modes of operation. The pins are connected to the Central State Machine via an input filter. The input filter protects the transceiver TLE9221SX against unintentional mode changes caused by spikes on the EN and STBN.

The ERRN output signals failures, diagnostic and status information to the external host controller. The TLE9221SX also contains a Status Information Register. Access to the Status Information Register is given by the Host Interface (see details **Chapter 6**).

Table 6 Modes of operation[1)]

STBN	EN	Mode of Operation
“high”	“high”	BD_Normal
“high”	“low”	BD_ReceiveOnly
“low”	“high”	BD_GoToSleep, automatically transferred to BD_Sleep
“low”	“low”	BD_Standby

1) No undervoltage flag and no wake-up flag is set.

5.6 Wake-up Detector

The Wake-up Detector is a separate internal function block to detect wake-up events, be it a local or a remote wake-up event. The Wake-up Detector also enables the filtering unit to differentiate between real wake-up signals and floating signals or glitches on the wake-up lines. Active in every operation mode, and also in the BD_Normal or BD_ReceiveOnly mode, the Wake-up Detector ensures that no wake-up signal gets lost due to a concurrent change of the operating mode. The Wake-up Detector provides feedback on the wake-up information to the Central State Machine for further processing (details see **Chapter 7**).

5.7 Power Supply Interface

The Power Supply Interface is the interface from the bus driver to the external supply voltages. It hosts the inputs to the power supplies V_{BAT} and V_{CC} and also the level shift input to the reference voltage V_{IO}.

To enable the control of external circuitry, like a voltage regulator for example, the Power Supply Interface of the TLE9221SX provides an INH output.

All power supplies and the reference voltage are monitored and undervoltage conditions are indicated via the ERRN output on the Host Interface (details see **Chapter 8**).

5.8 Bus Failure Detector

The Bus Failure Detector monitors the data stream on the BM and BP I/O pins and compares the bus data with the digital data stream available at the Communication Controller Interface. Discrepancies between the bus data and the digital data are interpreted as a bus failure. The Bus Failure Detector is active only in BD_Normal mode. All detected failures are signaled on the ERRN output by the Host Interface (see **Chapter 10**).

5.9 Central State Machine

The Central State Machine is the main logic block of the TLE9221SX. It controls all functions of the TLE9221SX, the failure management as well as the power-up and power-down operations. The Central State Machine also provides some internal registers to store status, diagnostic and failure information.

- Information about the operating mode handling (see **Chapter 9**)
- Information about the Status Information Register (see **Chapter 6**)
- Information about the power management (see **Chapter 8**)
- Information about the bus failure flag (see **Chapter 10**)

6 Host Interface and Status Information Register

The Host Interface is the main interface for:

- Selecting and controlling the operation modes of the TLE9221SX by host commands.
- Receiving status information of the TLE9221SX at the ERRN output pin.
- Retrieving diagnostics information of the TLE9221SX by reading the Status Information Register.

The Host Interface is operational when the reference voltage uV_{IO} is in its functional range. In case the supply uV_{IO} is in undervoltage condition, the Host Interface is blocked and the operating mode of the TLE9221SX FlexRay transceiver is automatically set to BD_Sleep mode (compare with **Chapter 9.3**).

6.1 Host Commands

The digital inputs EN and STBN have dual functionality:

- EN and STBN are used to select the operating mode.
- EN and STBN are used to trigger the read-out of the Status Information Register.

The STBN, EN and all other digital inputs of the TLE9221SX are level-triggered and protected with a glitch input filter. Additionally, a digital input filter is provided at the mode selection pins STBN and EN.

To get a valid host command, which triggers a change of the operating mode, the external signals at the pins EN and STBN need to be stable at least for time $t \geq dBDLogic_{Filter}$. Signal changes with a smaller pulse width than the internal filter time $t < dBDLogic_{Filter}$ are not considered valid host commands and the TLE9221SX remains in its previous operating mode.

Within the time for mode change $t = dBD_{ModeChange}$ the FlexRay transceiver TLE9221SX changes to the selected mode of operation (see **Figure 10**). All output signals are valid after the mode transition and when the time for mode change $t = dBD_{ModeChange}$ has expired.

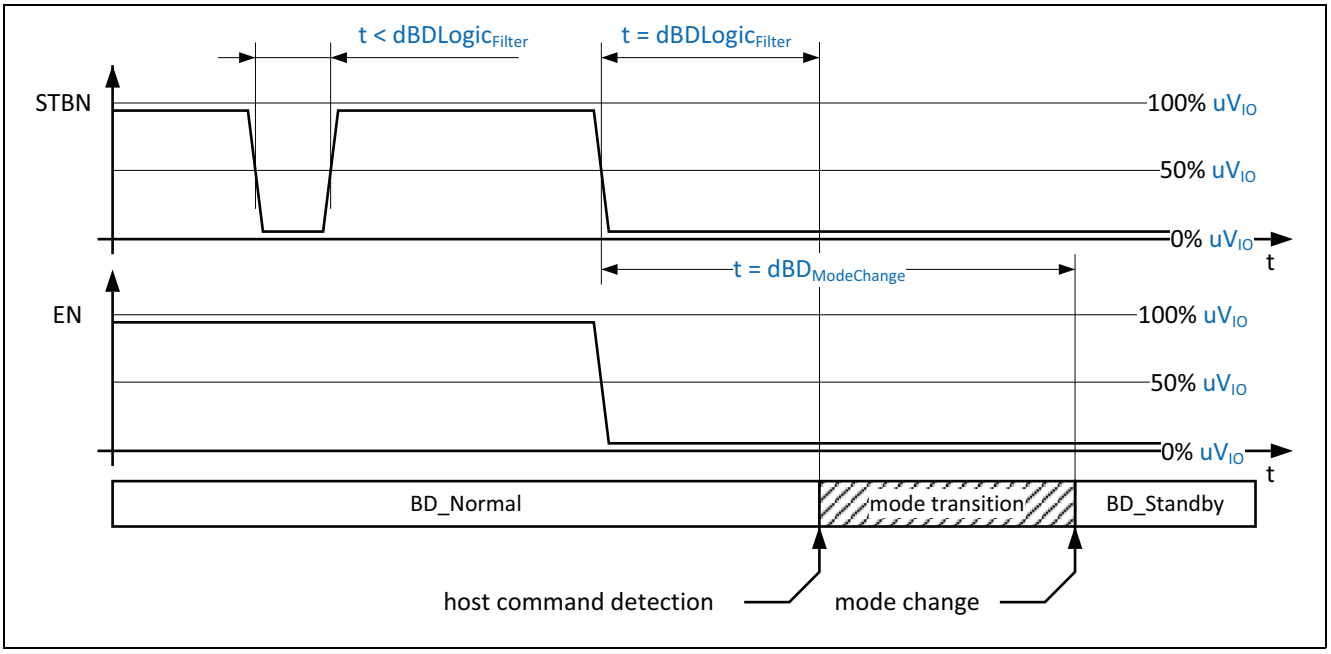


Figure 10 Example of a valid host command

Note: The time for mode change has to be considered for every change of the operation mode. All definitions in this data sheet are made considering the time for mode change $dBD_{ModeChange}$, even if the time for mode change is not explicitly mentioned, for example in logical status tables, mode diagrams or in elementary timing diagrams.

6.2 Status Information Register

6.2.1 Definition of the Status Information Register

Failure, wake-up and diagnostic information is stored internally in a 16-bit wide register in the TLE9221SX, the so-called Status Information Register, or abbreviated to SIR (see **Table 7**).

Table 7 Bit definition of the Status Information Register[1)]

Bit	Description	Summary Flag / Bit
Bit 0	local wake-up bit	wake-up flag
Bit 1	remote wake-up bit	wake-up flag
Bit 2	reserved, always “high”	–
Bit 3	power-up bit	–
Bit 4	bus error bit	error bit
Bit 5	overtemperature error bit	error bit
Bit 6	overtemperature warning bit	error bit
Bit 7	Transmitter time-out bit	error bit
Bit 8	V_{BAT} undervoltage bit	error bit
Bit 9	V_{CC} undervoltage bit	error bit
Bit 10	V_{IO} undervoltage bit	error bit
Bit 11	error bit	–
Bit 12	wake-up source bit	–
Bit 13	EN mode indication bit	–
Bit 14	STBN mode indication bit	–
Bit 15	even parity bit	–

1) The bits are “low” active. For example bit = 0, when set.

6.2.2 SIR Readout Mechanism

The SIR is a “read-only” register and the data can be read out serially by using EN input as a data clock. While the SIR readout procedure is running, no operation mode change applies to the TLE9221SX. This allows regular data communication and read-out of the SIR at the same time.

Like all the other functions using the Host Interface, the reference supply uV_{IO} needs to be operational to read out the SIR.

The SIR readout is possible in all non-low power modes and in BD_Standby mode (see **Table 8**).

Table 8 Readout mechanism and modes of operation

Modes of Operation	Active / Not Active
BD_Normal	active
BD_ReceiveOnly	active
BD_GoToSleep Command	not active

Table 8 Readout mechanism and modes of operation

Modes of Operation	Active / Not Active
BD_Standby	active
BD_Sleep	not active

Note: The SIR readout depends on the current operating mode selected and not on the host command applied. In case of undervoltage events, the host command could be BD_Normal mode, but the operating mode is BD_Sleep mode. In BD_Sleep mode, no SIR read-out is possible.

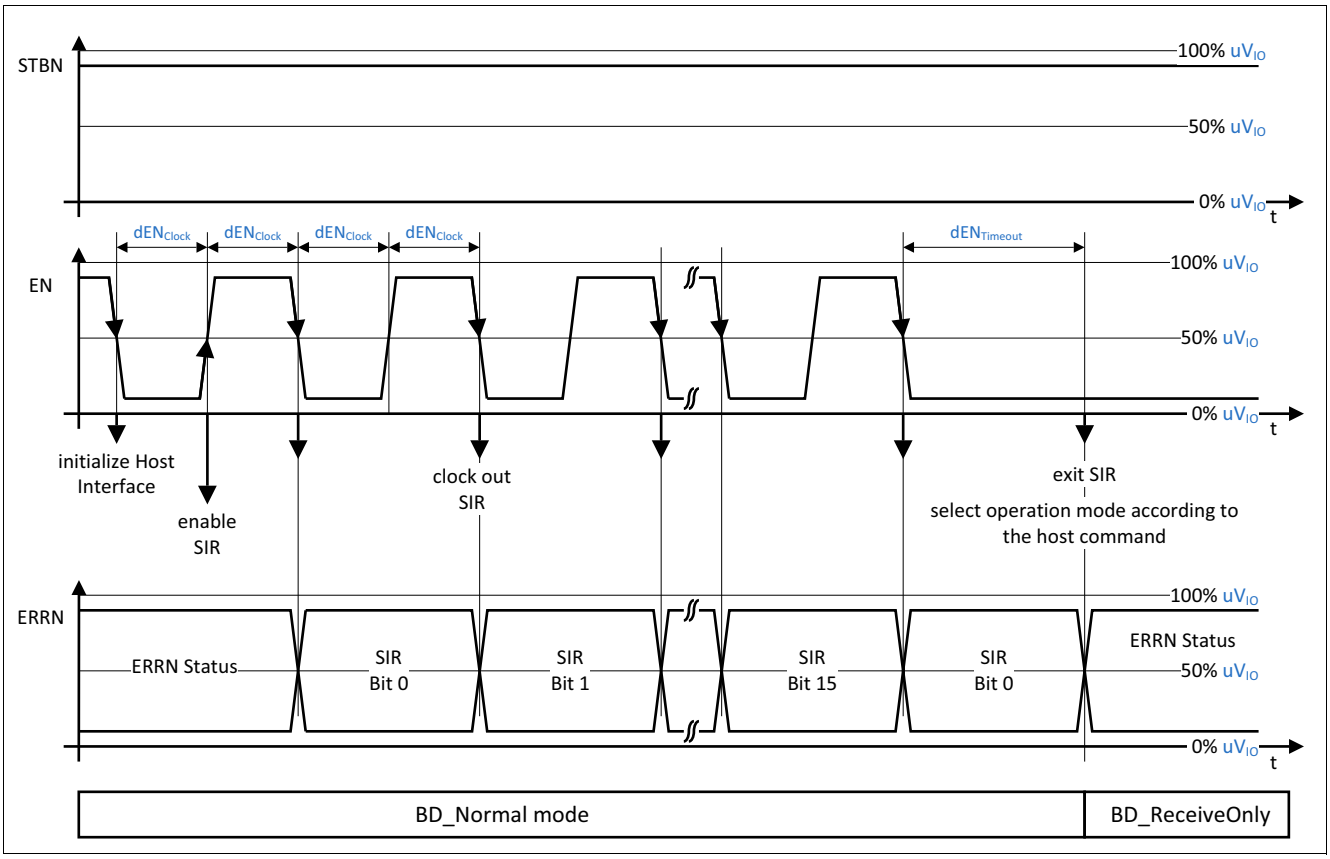


Figure 11 Timing diagram for the SIR readout in BD_Normal mode

During the SIR readout, the EN input acts as the clock and the ERRN output pin acts as the serial “data_out”. Irrespective of the digital signal at the STBN input, the SIR readout is always initialized by a signal change at the EN input pin. When the host command BD_Normal is applied to the Host Interface, the SIR read-out starts with the falling edge at the EN input (see **Figure 11**). For the host commands BD_Standby and BD_ReceiveOnly the read-out starts with the rising edge at the EN pin (see **Figure 12**).

After initialization, the internal timer starts and the TLE9221SX awaits the next signal change within the timing window $dEN_{CLOCK}(min) < t < dEN_{CLOCK}(max)$. The next rising edge[1)] enables the SIR and the bits can be clocked out.

If no signal change occurs after the initialization within the time frame $t < dEN_{Timeout}$, the TLE9221SX exits the SIR readout procedure and changes the operating mode according to the host command applied.

1) While the TLE9221SX is in BD_Normal mode, the rising edge is the first signal change after initialization and enables the SIR readout. For the BD_ReceiveOnly and the BD_Standby mode, there is an additional falling edge between initialization and the SIR being enabled (compare with **Figure 11** and **Figure 12**).

When the SIR is enabled, every falling edge at the EN input serially shifts out the SIR information at the ERRN output pin. With the first falling edge of the clock at the EN input, the least significant bit, bit 0, is clocked out to the ERRN output successively followed by bit 1, bit 2, etc, with every successive falling edge of the clock at the EN input.The SIR bits are “low” active, meaning that the ERRN signal = “low” when the SIR bit is set.

Note: The STBN input pin has no function when the SIR readout is enabled and the readout procedure is running. Nevertheless, it is recommended to keep the STBN pin stable (“high” or “low”) during the SIR readout procedure.

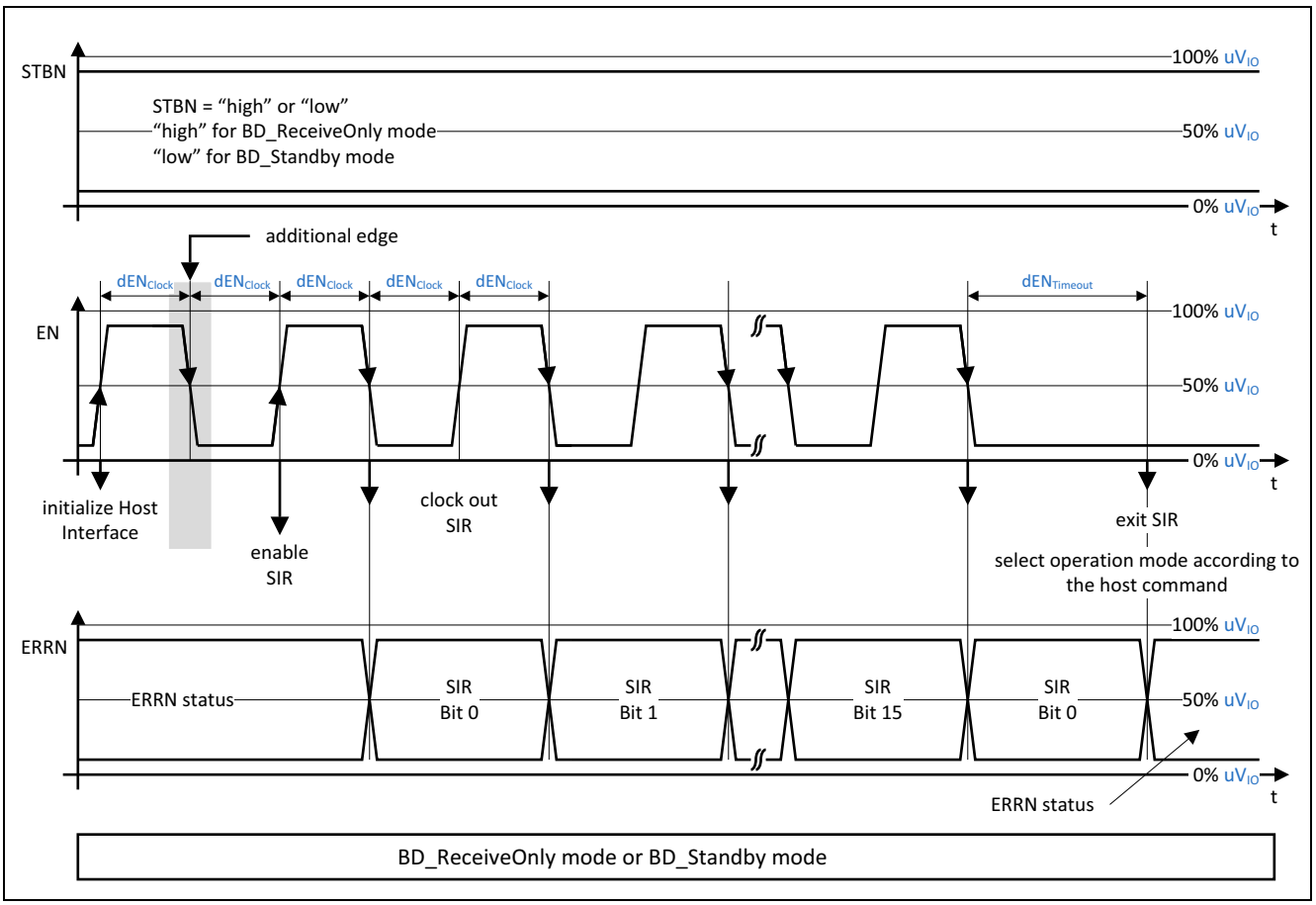


Figure 12 SIR readout in BD_ReceiveOnly or BD_Standby mode

The SIR readout procedure can be terminated at any time by stopping the clock at the EN input pin. While the signal at the EN pin is stable for the time $t > dEN_{Timeout}$, the TLE9221SX exits the SIR and changes to the operating mode according to the host command applied.

Note: It is recommended to leave the SIR read out procedure with the same EN signal that was present when the read out procedure was started. When time $t = dEN_{Timeout}$ expires, the mode change is triggered immediately.

6.2.3 Clearing Sequence of SIR

Failure and status information is latched in the SIR and the bits need to be cleared by a host command. In order to avoid any status bit from being cleared, while the root cause of the bit entry is still present, the TLE9221SX is equipped with a dedicated sequence to clear the bits of the Status Information Register. Before clearing any bits, the TLE9221SX checks, if the root cause of the bit entry is resolved. Only if the root cause of the bit entry has disappeared, the bit will be cleared.

The sequence to clear the bits of the SIR is started by:

- Entering BD_Normal mode via a host command.
- A complete readout of all 16 bits in the SIR.

In case the readout of the SIR is incomplete, for instance, due to a microcontroller interrupt during the readout procedure, the bits in the SIR remain set.

In case the SIR readout continues after the last bit (bit 15) has been clocked out, the TLE9221SX continues and clocks out the first bit (bit 0) again. On the second readout the bits in the SIR have been cleared. The bits will only be cleared if the root cause of setting them has been resolved.

*Note: Applying TLE9221SX the host command BD_Normal does not necessarily clear the SIR, since entering BD_Normal mode can be prevented by an undervoltage event (see **Table 13**).*

6.3 Status Information at the ERRN Output Pin

The ERRN output pin functions as a serial “data-out” during the SIR readout procedure. In any other case, the ERRN output pin indicates the status information. The ERRN pin indicates failure, wake-up events and the wake-up source.

The host command applied determines the incident that is signed at the ERRN output pin. The ERRN output pin is active “low” (details see **Table 9**).

Table 9 Signaling at ERRN

STBN	EN	Host Command	Error Bit[1)]	Wake-up Flag[1)]	ERRN	Condition
Error Indication						
“high”	“high”	BD_Normal	“high”	X[2)]	“high”	–
“high”	“high”	BD_Normal	“low”	X	“low”	–
“high”	“low”	BD_ReceiveOnly	“high”	“high”	“high”	–
“high”	“low”	BD_ReceiveOnly	“low”	“high”	“low”	–
Wake-up Source Indication						
“high”	“low”	BD_ReceiveOnly	X	“low”	“high”	wake-up source bit = “high”
“high”	“low”	BD_ReceiveOnly	X	“low”	“low”	wake-up source bit = “low”
Wake-up Indication						
“low”	“high”	BD_GoToSleep command	X	“high”	“high”	automatically transferred to BD_Sleep
“low”	“high”	BD_GoToSleep command	X	“low”	“low”	automatically transferred to BD_Sleep
“low”	“low”	BD_Standby	X	“high”	“high”	–
“low”	“low”	BD_Standby	X	“low”	“low”	–
“low”	X	BD_Sleep	X	“high”	“high”	–
“low”	X	BD_Sleep	X	“low”	“low”	–

1) “Low” active, the error bit and the wake-up flag are set while active “low”.

2) “X” = don’t care.

Note: The status signal at the ERRN output depends directly on the host command applied. Since the selection of the operation mode doesn’t implicitly depend on the host command but also on failure cases and wake-up events, it is possible that the TLE9221SX is in BD_Sleep mode while the host

*command BD_Normal mode is applied to the Host Interface (details see also **Table 15**, **Table 16** and **Table 17**).*

As an example in **Figure 13** the TLE9221SX indicates the error flag while the device is in BD_Sleep mode due to an undervoltage event on uV_{BAT}.

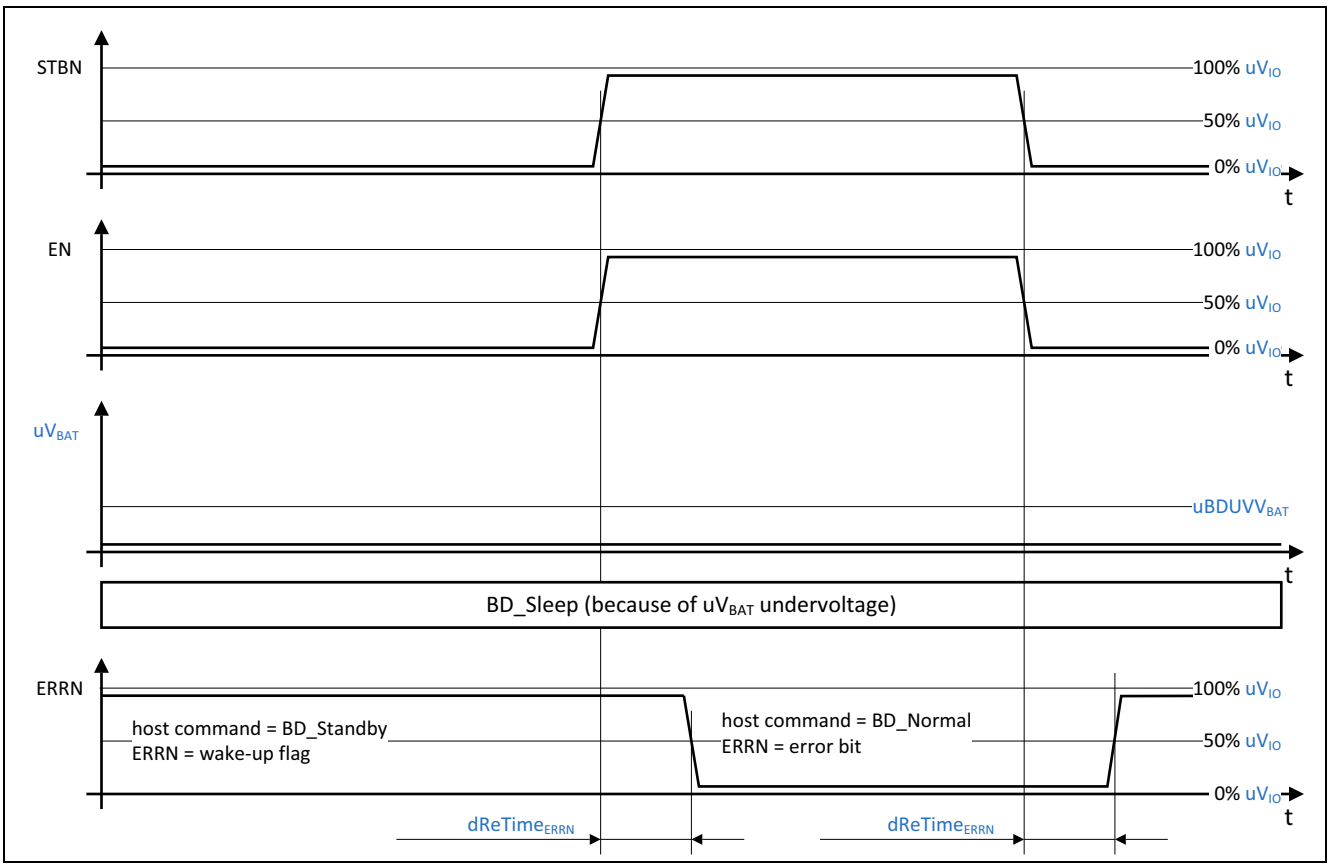


Figure 13 Status at the ERRN while uV_{BAT} undervoltage

6.3.1 Reset the ERRN Output Pin

The ERRN output depends directly on the status bits in the SIR. Resetting the bits in the SIR automatically also clears the ERRN output and, vice versa, one bit in SIR sets the ERRN output.

As described in **Chapter 6.2.3** the SIR can be reset by a dedicated host command or by the readout of the SIR. Since the SIR and consequently also the ERRN output can only be reset by a dedicated host command, toggling at the ERRN pin is not possible.

7 Wake-up Detector

The FlexRay transceiver TLE9221SX can detect different wake-up events via the central Wake-up Detector. These can be either remote wake-up events provided by the FlexRay bus or local wake-up events provided to the local wake-up pin WAKE.

Wake-up signals are:

- A falling edge at the local wake-up pin WAKE (see **Chapter 7.1.1**).
- A rising edge at the local wake-up pin WAKE (see **Chapter 7.1.2**).
- A dedicated wake-up pattern at the FlexRay bus (see **Chapter 7.2.1** and **Chapter 7.2.2**).
- A wake-up pattern implemented in a standard FlexRay frame (see **Chapter 7.2.3**).

The Wake-up Detector is active in every mode of operation and works over the entire operating range as long as uV_{BAT} is in its functional range (see **Table 20**).

Detected wake-up events are analyzed by the Central State Machine and are compared with the overall device status. They may cause a change of the operation mode (details see **Chapter 9.5**) and they may set a wake-up flag or a wake-up bit (details see **Chapter 7.3**).

7.1 Local Wake-up

The TLE9221SX provides a local wake-up input WAKE, tailored to withstand voltages up to uV_{BAT}(Max). Positive and negative signal changes on the WAKE pin trigger the Wake-up Detector.

The WAKE input is provided with an internal pull-up and pull-down structure and an internal wake pulse filter (see **Figure 14**).

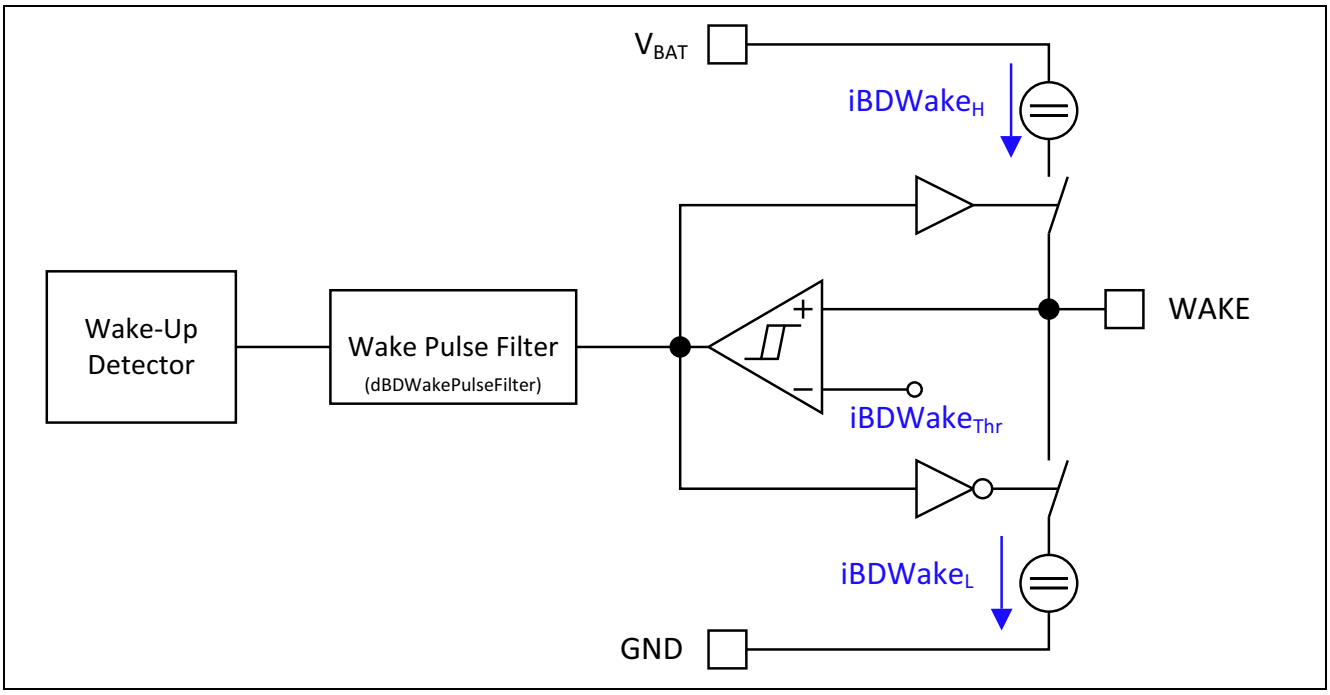


Figure 14 Block diagram of the WAKE input

Depending on the signal at the WAKE input, either the pull-up structure or the pull-down structure is connected to the WAKE input. While a voltage uV_{WAKE} > uBDWake$_{Thr}$ is applied to the WAKE input, the internal pull-up structure is connected to the WAKE input. Conversely, while a voltage uV_{WAKE} < uBDWake$_{Thr}$ is applied to the WAKE input, the internal pull-down structure is activated (see **Figure 15**).

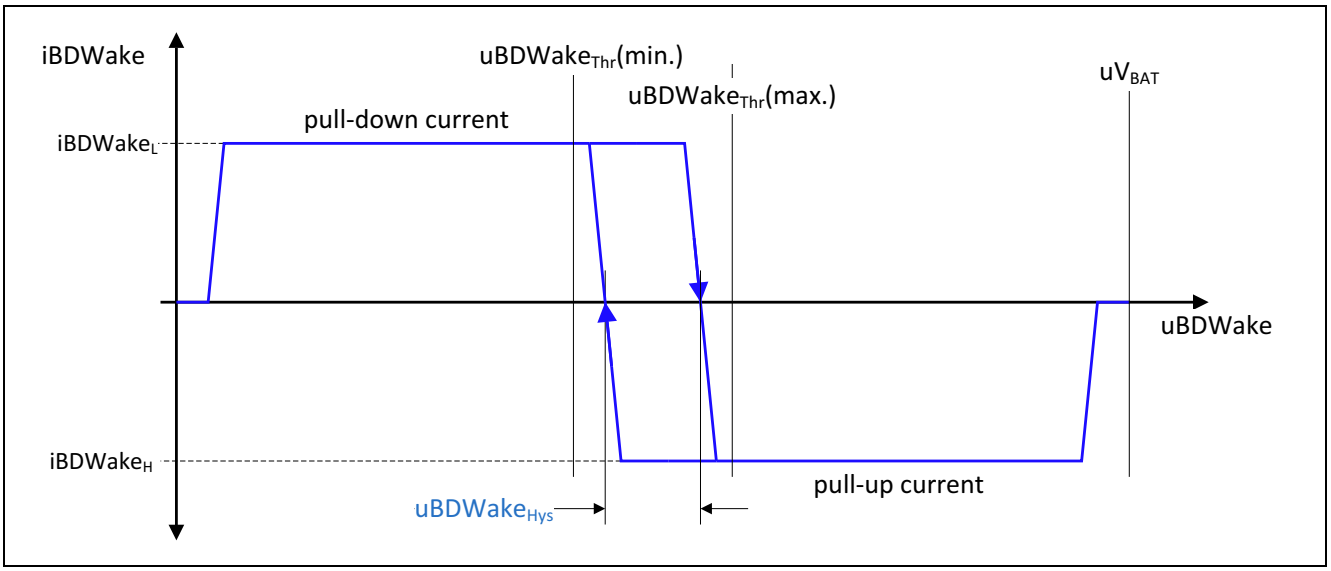


Figure 15 Pull-up and pull-down at the WAKE input

7.1.1 Local Wake-up Falling Edge

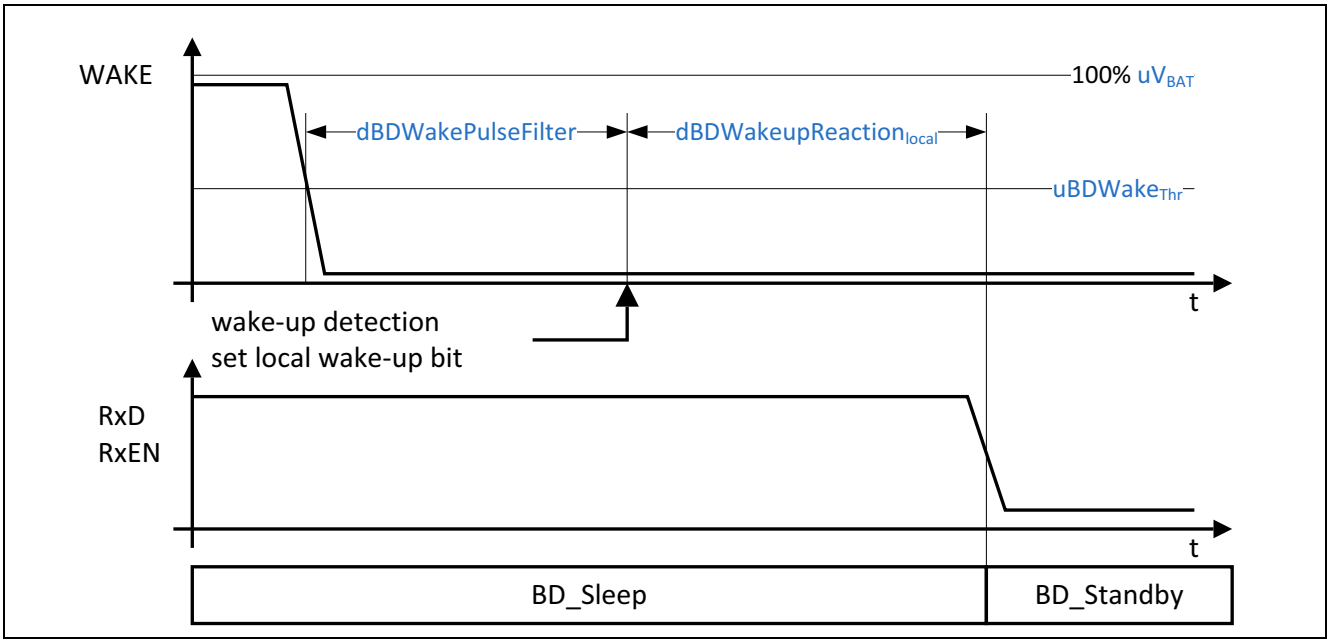


Figure 16 Local wake-up falling edge

The TLE9221SX detects a falling edge (signal change from uV_{BAT} to GND) at the WAKE pin, followed by a “low” signal for the time period dBDWakePulseFilter as a local wake-up event (see **Figure 16**). The implemented filter time dBDWakePulseFilter avoids that spikes at the WAKE signal are considered as valid wake-up events.

In BD_Sleep mode, BD_Standby mode and during the BD_GoToSleep command the state machine of the TLE9221SX sets the local wake-up bit (bit 0) in the SIR (active logical “low”), when detecting a local wake-up event. In non-low power modes, the detection of a local wake-up event is ignored and no status bit is set. Together with the local wake-up bit, the TLE9221SX also sets the wake-up flag (active logical “low”). The wake-up source bit (bit 12) remains at logical “high”, when a local wake-up event is detected.

In low power modes or in the BD_GoToSleep command an active wake-up flag is indicated at the RxD and RxEN output within the time period $dBDWakeupReaction_{local}$ (see **Table 5**). In case the transceiver is in

BD_Sleep mode, an active wake-up flag also triggers a mode change to BD_Standby mode (for details see **Table 17**).

A local wake-up signal can be detected by the TLE9221SX only if the power supply uV_{BAT} is available. The detection of a local wake-up is working over the whole operating range of uV_{BAT} (for details see **Table 20**).

The ERRN output indicates the wake-up event after the time dBDWake$_{Local}$:

dBDWake$_{Local}$ = dBDWakePulseFilter + dBDWakeupReaction$_{local}$

7.1.2 Local Wake-up Rising Edge

The WAKE input on the TLE9221SX is a bi-sensitive input and also a rising edge (signal change from GND to uV_{BAT}) at the pin WAKE is detected as a wake-up event (see **Figure 17**).

As on a local wake-up, triggered by a falling edge at the input pin WAKE, a rising edge also sets the local wake-up bit and the wake-up flag respectively.

The internal state machine does not differentiate between a local wake-up triggered by a rising edge and a falling edge at the pin WAKE. There is no possibility of distinguishing between the rising and falling edge, since only one SIR entry is available.

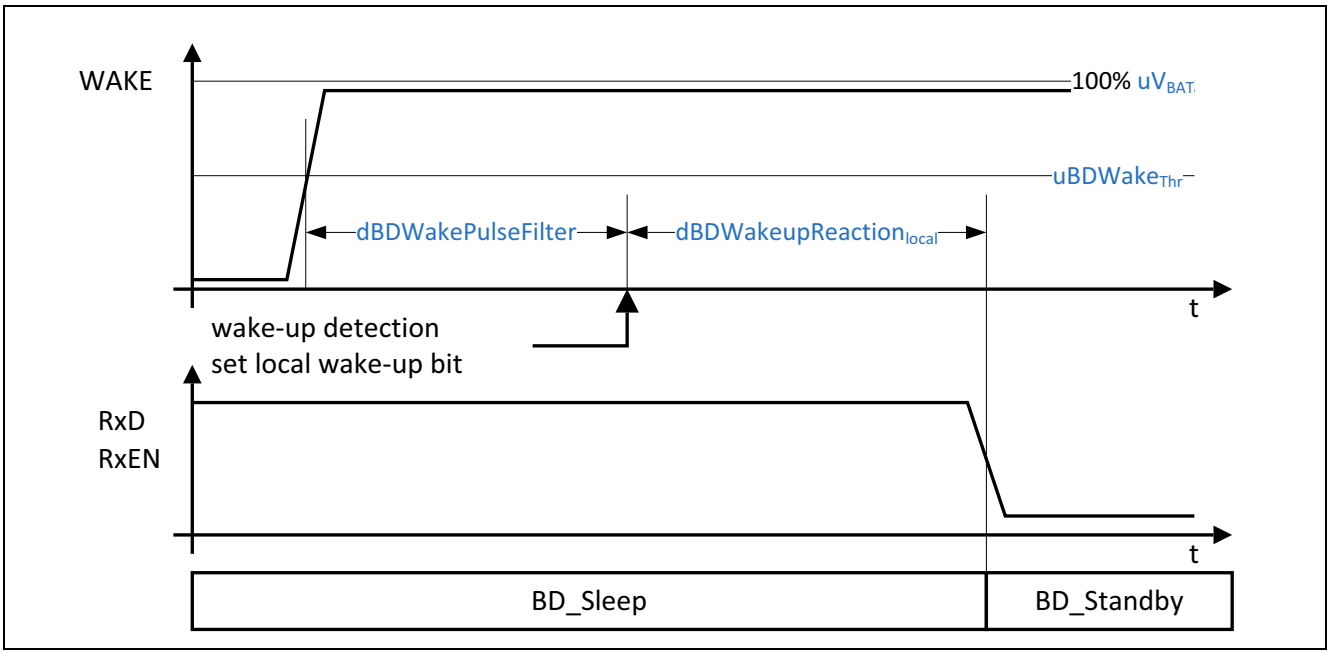


Figure 17 Local wake-up rising edge

7.2 Remote Wake-up

For a remote wake-up, also called bus wake-up, a dedicated wake-up pattern is defined in FlexRay systems. A wake-up pattern consists of at least two wake-up symbols. A wake-up symbol on the FlexRay bus is defined as a phase of “Data_0” followed by a phase of “Idle” or alternatively a phase of “Data_0” followed by a phase of “Data_1”. Bus wake-up patterns are detected by the Wake-up Detector and fed to the internal state machine.

The remote wake-up bit (bit 1) in the SIR is set, if the TLE9221SX detects a remote wake-up event in a low power mode or during the BD_GoToSleep command, regardless of whether the wake-up was triggered by a standard wake-up pattern or triggered by an alternative wake-up pattern or by a wake-up signal via payload. At the same time that it sets the remote wake-up bit, the TLE9221SX also sets the wake-up flag and the wake-up source bit. In non-low power modes, the detection of a remote wake-up event is ignored and neither the remote wake-up bit nor the wake-up flag is set.

In low power modes or in the BD_GoToSleep command, an active wake-up flag is indicated at the RxD and RxEN outputs within the time period $dBDWakeupReaction_{remote}$ (see **Figure 18** and **Table 5**). In case the transceiver remains in BD_Sleep mode an active wake-up flag also triggers a mode change to BD_Standby mode (for details see **Table 20**).

To detect a remote wake-up event, at least one of the two power supplies needs to be available.

7.2.1 Standard Wake-up Pattern

The standard wake-up pattern is defined by at least two wake-up symbols starting with “Data_0”, followed by an “Idle” signal. The pulse width for the “Data_0” needs to be at least $t = dWU_{0Detect}$ or longer. The pulse width for the “Idle” phase shall not be below $t = dWU_{IdleDetect}$. The maximum time for the standard wake-up pattern shall not exceed $t = dWU_{Timeout}$ (see **Figure 18**). The pulse width for “Data_0” may vary between the two wake-up symbols as long as the pulse width is not below $t = dWU0_{Detect}$ and the standard wake-up pattern does not exceed $t = dWU_{Timeout}$. Variation of the pulse width of the “Idle” phase is possible with the same limitations. The standard wake-up pattern is independent of the data transmission rate.

The Wake-up Detector of the TLE9221SX distinguishes between “Data_0” and “Idle” by the differential bus voltage. The bus voltage below the threshold uDATA0_LP is identified as a “Data_0” signal and the bus voltage above the threshold uDATA0_LP is identified as an “Idle” or a “Data_1” signal. The Wake-up Detector does not differentiate between an “Idle” or a “Data_1” signal.

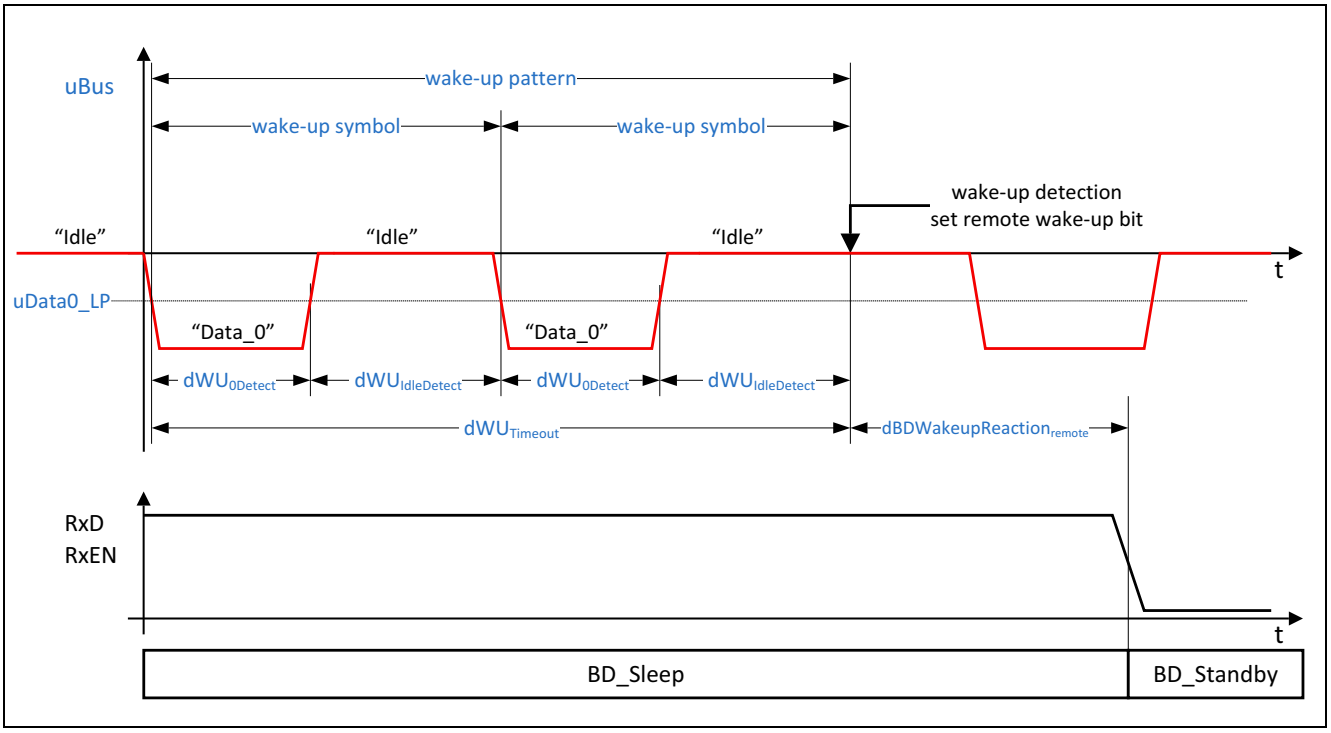


Figure 18 Standard wake-up pattern

7.2.2 Alternative Wake-up Pattern

The definition of the alternative wake-up pattern is similar to that of the standard wake-up pattern, the only difference is that the wake-up symbols have no “Idle” signal. The “Idle” signal is replaced by a “Data_1” signal (see **Figure 19**). The timing requirements for pulse width and time-out are the same as for the standard wake-up pattern. The alternative wake-up pattern is also independent of the data rate.

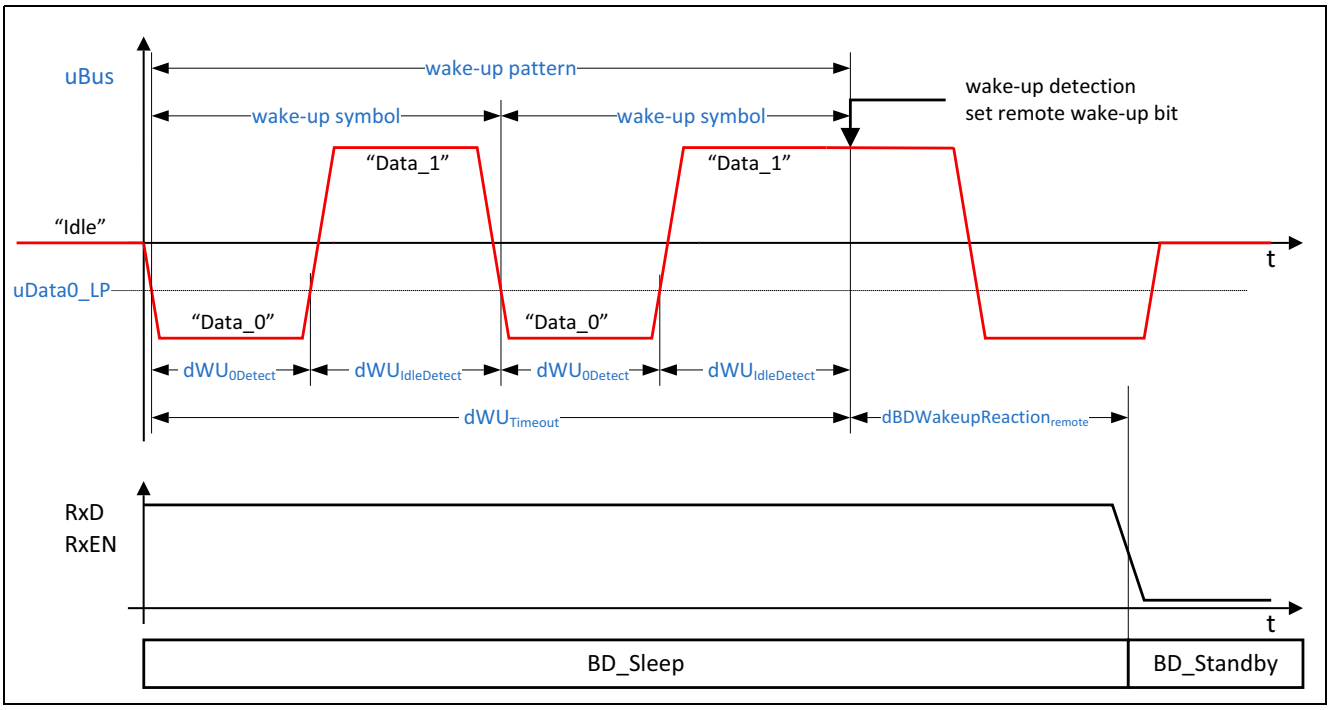


Figure 19 Alternative wake-up pattern

7.2.3 Wake-up by Payload

Besides sending a dedicated wake-up pattern on the FlexRay bus, it is also possible to wake up the TLE9221SX with a wake-up message hidden in the data field of the standard FlexRay frame, called wake-up by payload.

In comparison to the wake-up by standard pattern or to the wake-up with an alternative pattern, the wake-up by payload is limited to a data transmission rate of 10 Mbit/s.

A dedicated Byte Start Sequence is transmitted before each byte of the payload within the FlexRay data frame.The Byte Start Sequence (BSS) consists of one “high” bit followed by one “low” bit. To transmit a “Data_0” byte to the FlexRay bus, the FlexRay controller sends 10 bits. First a “high” bit as part of the Byte Start Sequence, followed by a “low” bit which also belongs to the Byte Start Sequence and after the Byte Start Sequence, the controller sends eight “low” bits (HL= BSS; LLLLLLLL= “Data_0”). Sending a “Data_1” byte the FlexRay controller sends a “high” bit followed by a “low” bit and then sends eight consecutive “high” bits (HL= BSS; HHHHHHHH= “Data_1”) (see **Figure 20**).

At a data rate of 10 Mbit/s, one bit in the FlexRay data frame has a bit length of 100 ns. This means that each data byte in a wake-up pattern has one glitch of 100 ns.

The Wake-up Detector of TLE9221SX has an analog input filter implemented, which filters out the glitches on the wake-up pattern for glitches shorter than t = $dWU_{Interrupt}$.

Receiving a complete wake-up by payload, the TLE9221SX sets the remote wake-up bit, the wake-up flag and also the wake-up source bit. The wake-up flag is set in case the following data pattern is detected in a FlexRay frame.

Table 10 Wake-up Payload Content

0xFF	0xFF	0xFF	0xFF	0xFF	0x00	0x00	0x00	0x00	0x00
0xFF	0xFF	0xFF	0xFF	0xFF	0x00	0x00	0x00	0x00	0x00
0xFF	0xFF	0xFF	0xFF	0xFF	0x00	0x00	0x00	0x00	0x00
0xFF	0xFF	0xFF	0xFF	0xFF	0xFF				

In case any incomplete wake-up pattern is received, no wake-up flag is set and no entry is made to the SIR.

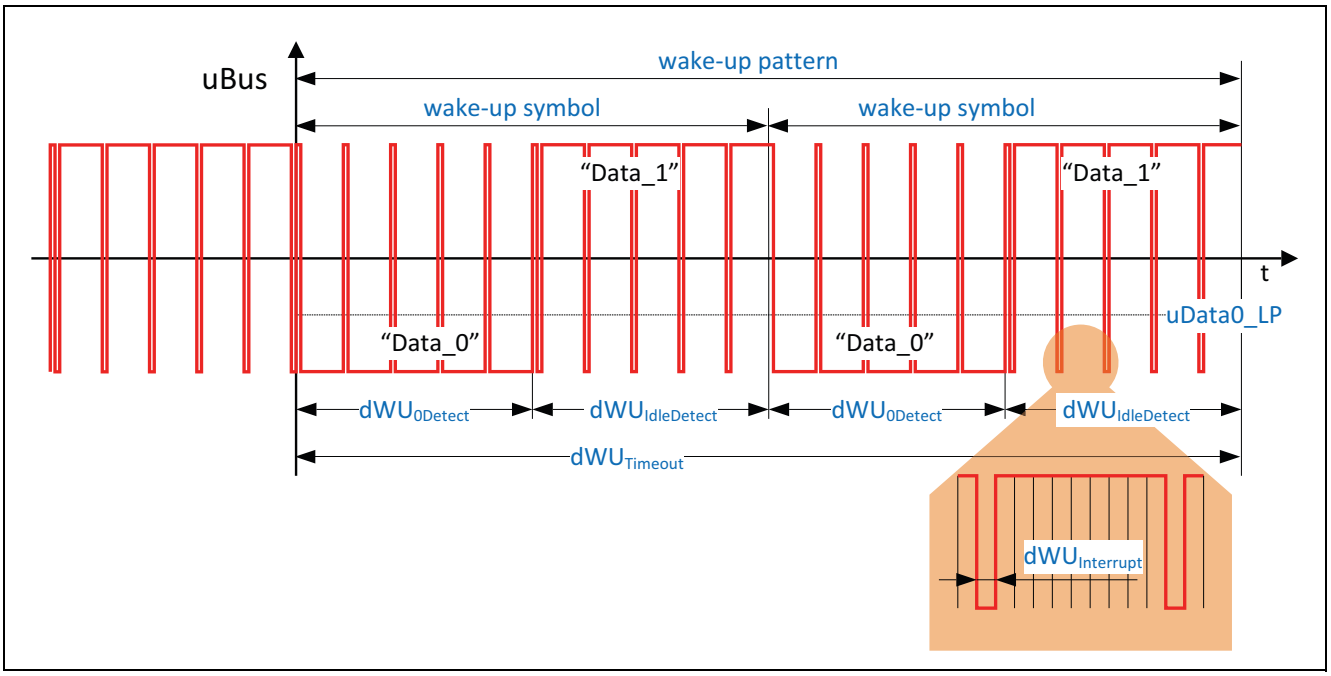


Figure 20 Wake-up by payload

7.3 Wake-up Flag and Wake-up Bits

The wake-up flag and the SIR latch the wake-up event and allow an external microcontroller to read out the wake-up source. The TLE9221SX provides three bits in the SIR for the wake-up information:

- The local wake-up bit (bit 0)
- The remote wake-up bit (bit 1)
- The wake-up source bit (bit 12)

Even if the Wake-up detector is active in every operation mode, the wake-up bits can only be set in low power mode or in the BD_GoToSleep command. In every other operation mode no wake-up bit is set (see **Table 11**).

The local wake-up bit is set in case the TLE9221SX detects a local wake-up event and in case of a remote wake-up event the remote wake-up bit is set. A remote wake-up can be a wake-up either by a standard pattern, a wake-up by an alternative pattern or a wake-up by payload.

In case the TLE9221SX detects a local and a remote wake-up event, both entries in the SIR bits are set.

Table 11 Setting the wake-up flag and the wake-up bits

Modes of Operation	Wake-up Event	Local Wake-up Bit[1)]	Remote Wake-up Bit[1)]	Wake-up Source Bit[1)]	Wake-up Flag[1)]
BD_GoToSleep	Remote	“high”	“low”	“low”	“low”
	Local	“low”	“high”	“high”	“low”
BD_Standby	Remote	“high”	“low”	“low”	“low”
	Local	“low”	“high”	“high”	“low”
BD_Sleep	Remote	“high”	“low”	“low”	“low”
	Local	“low”	“high”	“high”	“low”

1) Not set = logical “high”, Set = logical “low”

Concurrent with the local wake-up bit or with the remote wake-up bit, the wake-up source bit and the wake-up flag are set. The wake-up source bit is “high” when detecting a local wake-up event and “low” when a remote wake-up event is detected. Only the first wake-up event is indicated in the wake-up source bit. In case the TLE9221SX detects a local and a remote wake-up event simultaneously, the wake-up source bit output indicates the remote wake-up event.

The SIR is reset either after a complete read-out of the SIR (see **Chapter 6.2.3**) or when the TLE9221SX enters into BD_Normal mode. The wake-up flag is reset if both bits, the local wake-up bit and the remote wake-up bit are reset.

The wake-up flag and the wake-up source bit are indicated at the ERRN output pin of the Host Interface (see **Table 9**).

8 Power Supply Interface

The Power Supply Interface distributes the correct voltages to the single function blocks within the TLE9221SX. It manages the power-up and power-down procedures, monitors the supply voltages uV_{BAT}, uV_{CC} and also the reference voltage uV_{IO}. To control external circuitry, an INH output is available (see **Figure 22**).

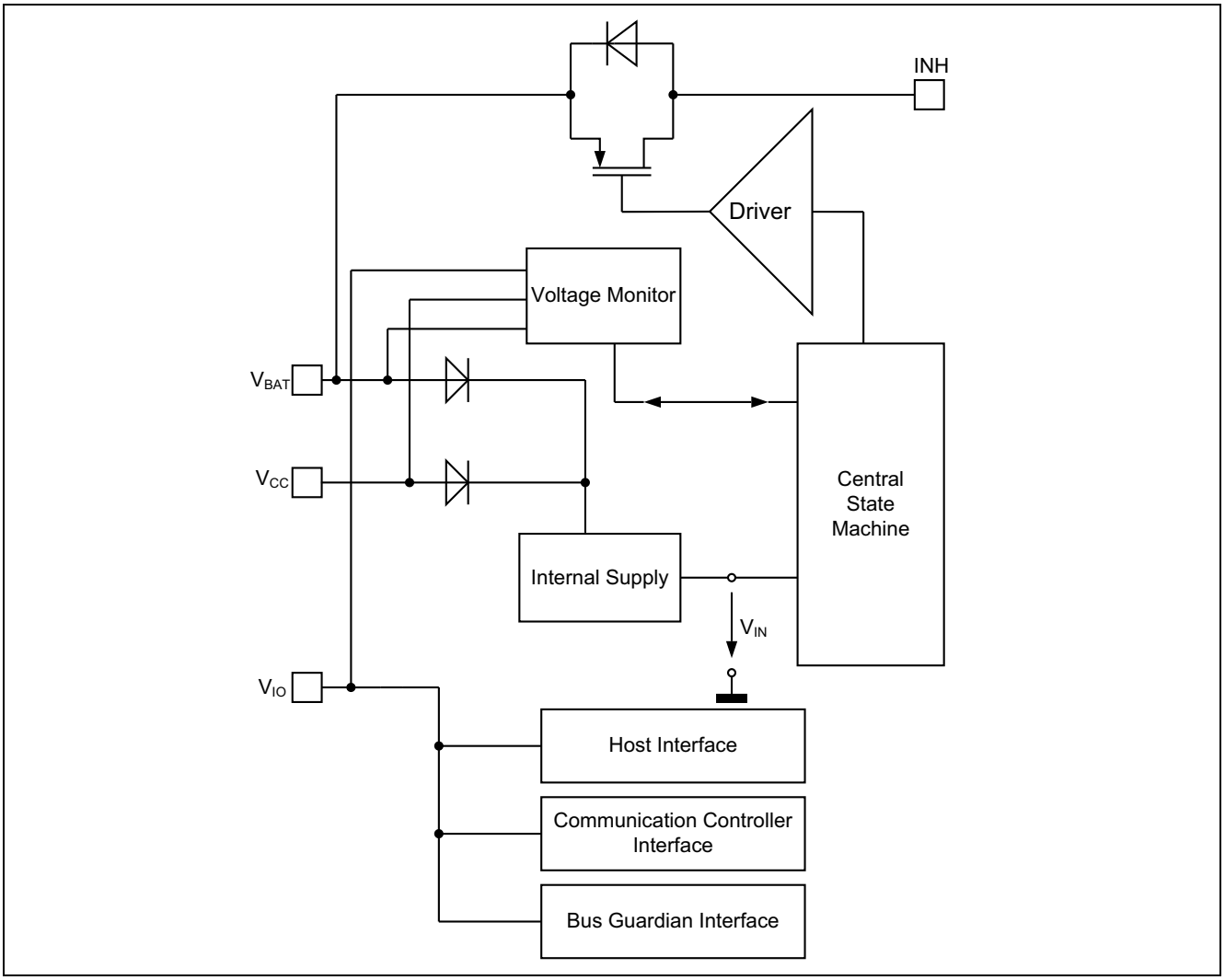


Figure 21 Block diagram of Power Supply Interface

The Central State Machine is the main logic control unit of the TLE9221SX. All functions, including operation mode management, the diagnostic function and failure management are controlled and handled by the Central State Machine. To ensure correct failure management, the Central State Machine is the first function block which is powered up and the last function block which is powered down. For this reason, the Central State Machine is supplied by an internal supply uV_{IN} (see **Figure 21**).

The internal supply uV_{IN} is in its operational range, if at least one of the two power supplies, uV_{CC} or uV_{BAT}, is above their power-down threshold, $uBDBPV_{BAT}$ or $uVBDPDV_{CC}$.

Note: The reference voltage uV_{IO} is the level shift supply for all digital inputs and outputs. It is not connected with the internal supply of the central state machine. Nevertheless, if the reference voltage uV_{IO} is not available or in undervoltage condition, the internal state machine blocks all host commands and changes the mode of operation to a low power mode.

8.1 INH Output

The INH output signal is intended to control an external voltage regulator. When the FlexRay transceiver TLE9221SX is in BD_Sleep mode, the INH output is open and floating. In every other operation mode the INH output voltage is $uINH1_{Not\text{-}Sleep}$. The voltage $uINH1_{Not\text{-}Sleep}$ is derived from the power supply uV_{BAT} by an internal open drain transistor (see **Figure 22**).

The transceiver TLE9221SX signals “Sleep” at the INH pin, while the device is in BD_Sleep mode and “Not_Sleep” in any other mode of operation (BD_Standby, BD_Normal, BD_ReceiveOnly and the BD_GoToSleep command).

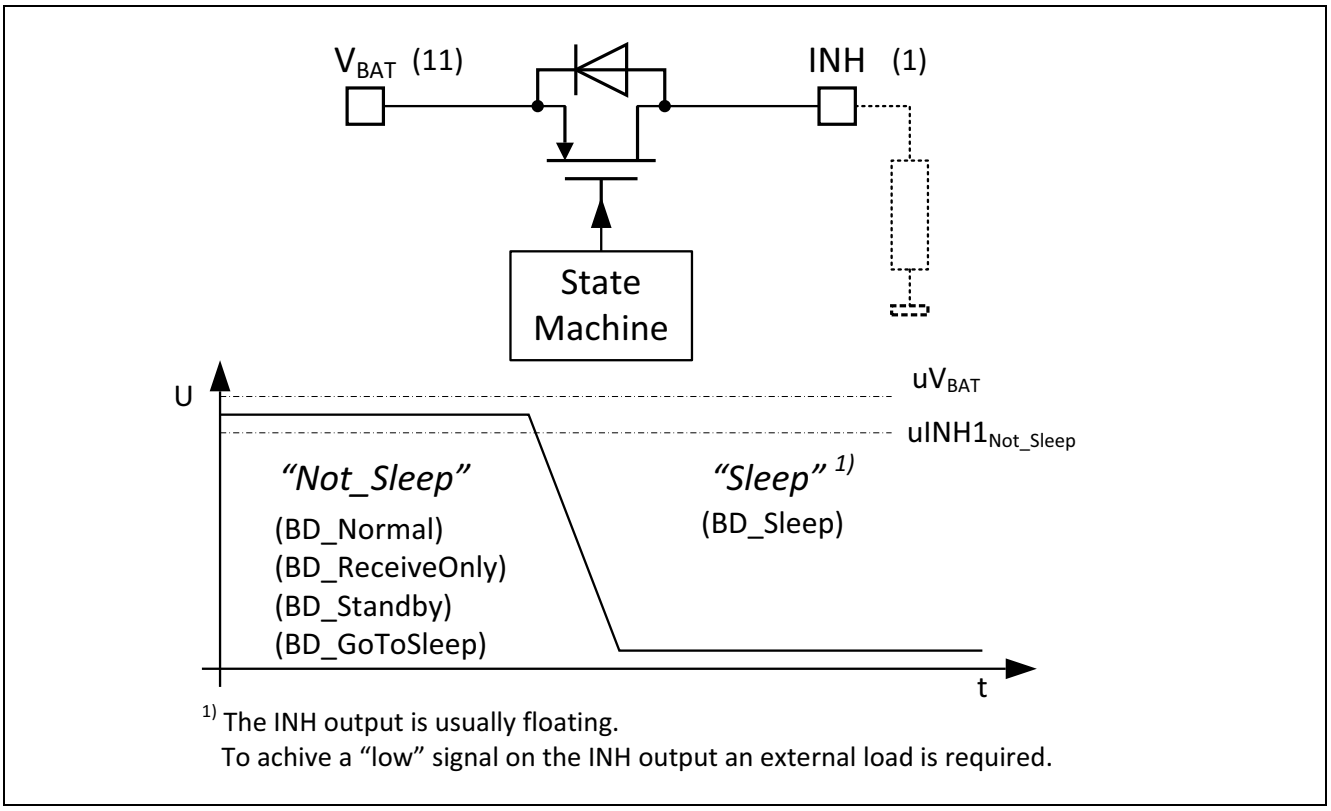


Figure 22 Circuit diagram of the INH output

8.2 BD_Off and Undervoltage

The FlexRay transceiver TLE9221SX monitors the two power supplies uV_{CC} and uV_{Bat} and also the reference voltage uV_{IO}. In case one of the three voltages falls below its dedicated undervoltage detection threshold, the TLE9221SX changes its mode of operation to low power mode (see **Figure 23**). For undervoltage condition, the Central State Machine is still functional.

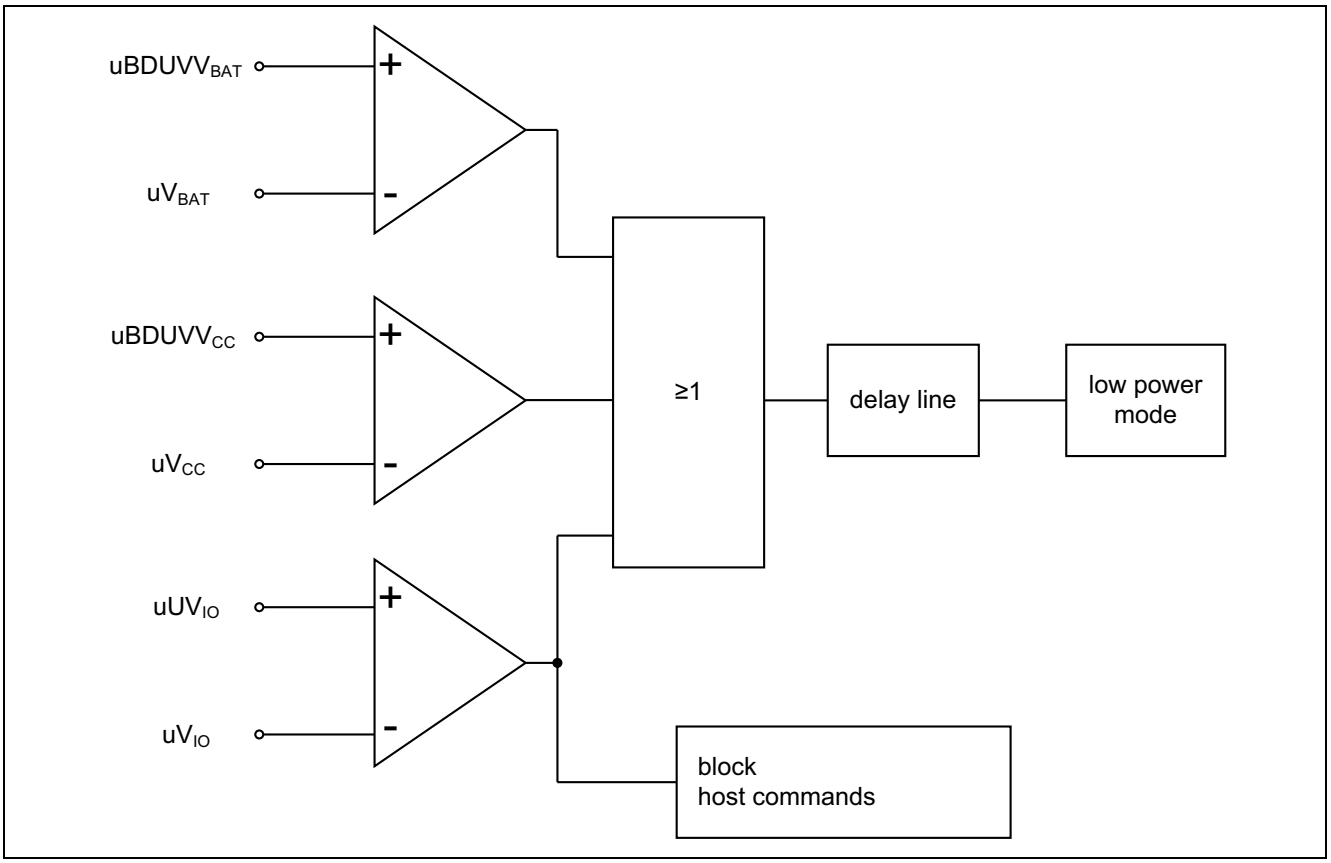


Figure 23 Logic diagram of undervoltage detection

The BD_Off state of the FlexRay transceiver TLE9221SX is reached, if both power supplies, uV$_{BAT}$ and uV$_{CC}$ are below the power-down thresholds uBDPDV$_{BAT}$ and uBDPDV$_{CC}$. In comparison to undervoltage detection the reference supply uV$_{IO}$ has no effect on the BD_Off state. Regardless of whether the uV$_{IO}$ voltage is available or not, the FlexRay transceiver TLE9221SX always changes over to the power-down state BD_Off in case uV$_{BAT}$ and uV$_{CC}$ are not present (see **Figure 24**).

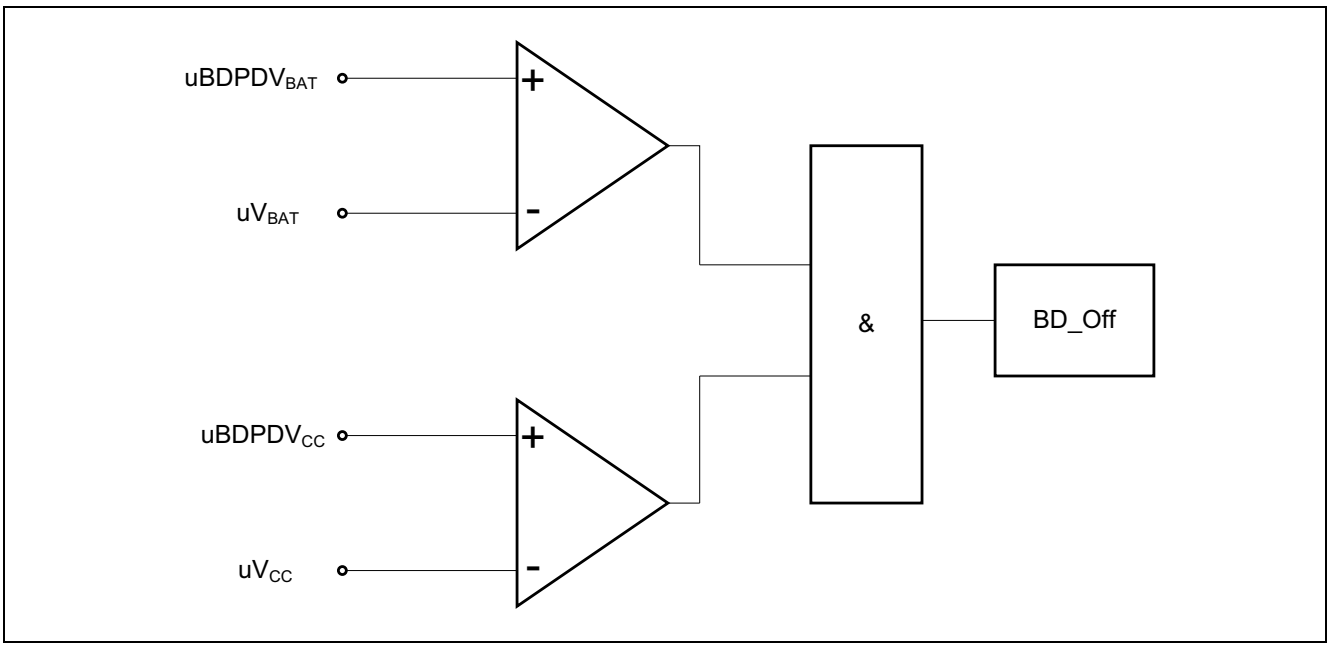


Figure 24 Logic diagram of BD_Off detection

Note: When the transceiver TLE9221SX is in BD_Off state, the Central State Machine is powered down. All registers in TLE9221SX are built of volatile memory and therefore, all status, diagnostic, and failure information is reset.

8.3 Undervoltage Events

8.3.1 Undervoltage Flags and Undervoltage Bits

Detected undervoltage events are stored using a dedicated undervoltage bit and they are visible in the SIR. Along with the undervoltage bit a summary bit, the error bit (bit 11), is set. The error bit is indicated at the ERRN output, depending on the selected operation mode (see **Table 9** and the example in **Figure 25**).

The TLE9221SX provides three bits in the SIR to signal undervoltage events:

- uV_{BAT} undervoltage bit (bit 8)
- uV_{CC} undervoltage bit (bit 9)
- uV_{IO} undervoltage bit (bit 10)

Undervoltage bits are used to store the information for further use. Therefore undervoltage bits get cleared only by a power-down or by clearing the SIR (see **Chapter 6.2.3**).

In comparison to the undervoltage bits, undervoltage flags are not latched and they are only used to trigger the changes of the operation mode. Undervoltage flags are not visible externally.

An undervoltage event on any supply line directly sets the dedicated undervoltage bit and also the error bit. The undervoltage flags are set by internal timers. An internal undervoltage detection timer is available for every supply, uV_{BAT}, uV_{CC} and uV_{IO}. While setting the undervoltage bit, the appropriate undervoltage detection timer is also triggered. When the undervoltage detection timer expires, while the undervoltage event is still present, the undervoltage flag is set (see **Figure 25**).

In case the undervoltage situation gets cleared while the undervoltage detection timer is running, the TLE9221SX does not set the undervoltage flag. According to the mode change table, an active undervoltage flag changes the mode of operation to low power mode (see

and **Table 16**).

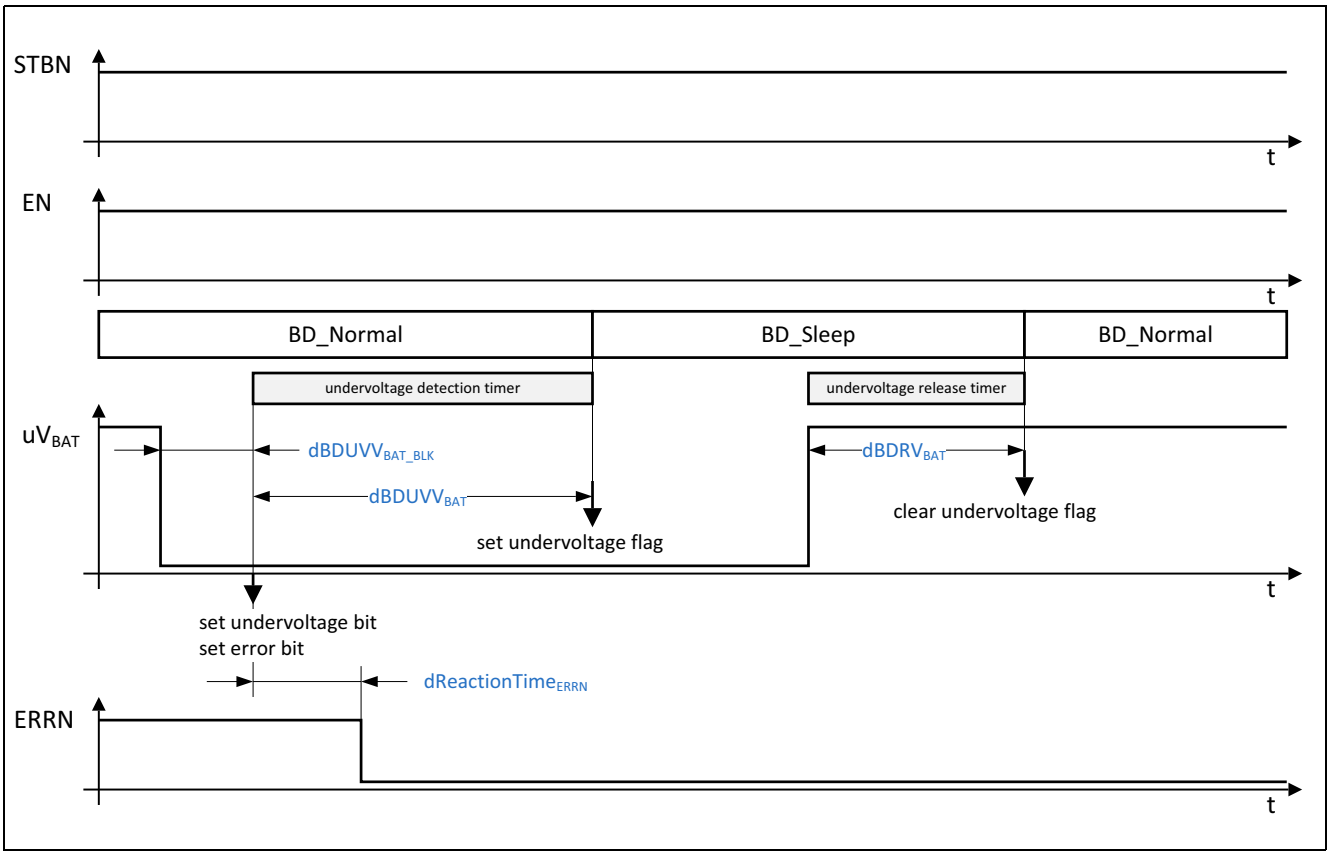


Figure 25 Example of setting the undervoltage flag

Besides the undervoltage detection timer, each supply is also equipped with an undervoltage recovery timer. The undervoltage recovery timer starts when the external power supply recovers. When the undervoltage recovery timer expires, the undervoltage flag gets reset (see **Figure 25**). If the external power supply recovers only temporarily and the supply line falls back to the undervoltage situation while the undervoltage recovery timer is still running, the undervoltage flag remains set. Clearing the undervoltage flag allows the transceiver TLE9221SX to return from low power mode to the previous operational mode selected by the host command (see **Chapter 9.4** and **Table 17**).

Note: Undervoltage bits are set by an undervoltage event. Undervoltage bits are stored in the SIR and also indicated at the ERRN output.
Undervoltage flags are set by the undervoltage detection timer. Undervoltage flags are not visible in the SIR and they are not indicated at the ERRN output. Undervoltage flags are only used to change the mode of operation after the undervoltage detection timer has expired!

8.3.2 Undervoltage Event at uV_{BAT}

The FlexRay transceiver TLE9221SX considers a voltage fluctuation on the power supply uV_{BAT}, which falls below the detection threshold $uBDUVV_{BAT}$ and exceeds the blanking time $dBDUV_{BAT\_BLK}$, as an undervoltage event. Voltage fluctuations on uV_{BAT} shorter than $dBDUV_{BAT\_BLK}$ are ignored and not recognized by the Power Supply Interface. To indicate the undervoltage event on the supply voltage uV_{BAT}, the uV_{BAT} undervoltage bit (bit 8) and the error bit (bit 11) are set (see **Figure 26**). After the uV_{BAT} undervoltage detection timer $dBDUVV_{BAT}$ expires, the uV_{BAT} undervoltage flag is set and the mode of operation changes to BD_Sleep mode.

The Host Interface and the Communication Controller Interface are active while the $dBDUVV_{BAT}$ undervoltage detection timer is running and the reference supply uV_{IO} is present. When the $dBDUVV_{BAT}$ undervoltage detection timer expires and the uV_{BAT} undervoltage flag is set, the Host Interface and the Communication

Controller Interface are blocked as long as the uV_{BAT} undervoltage flag remains active (compare also with **Chapter 9.3** and **Table 16**).

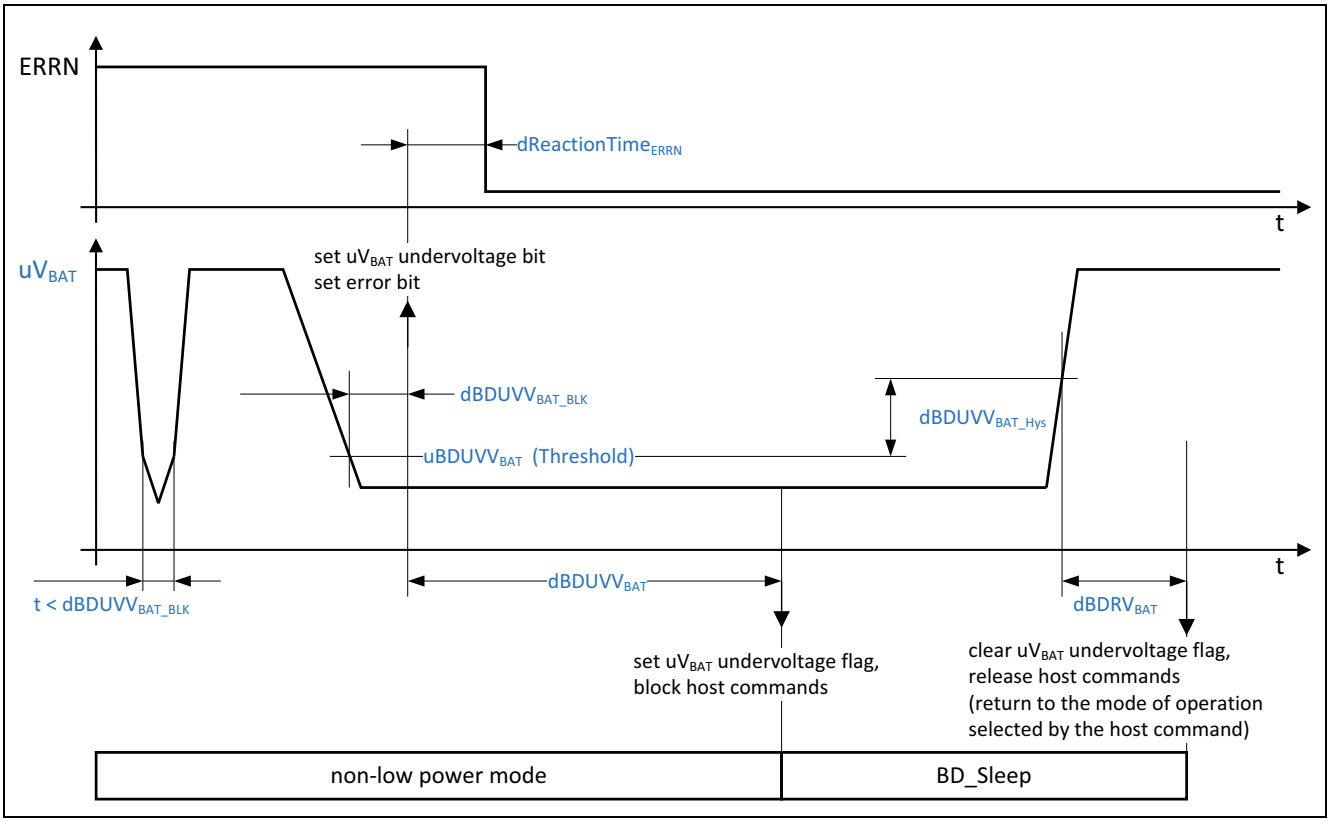


Figure 26 Undervoltage event at uV_{BAT} in non-low power mode

8.3.3 Undervoltage Event at uV_{CC}

Power supply voltage fluctuations on the uV_{CC} power supply, falling below the threshold $uBDUVV_{CC}$ for a time longer than the blanking time $dBDUVV_{CC\_BLK}$, are considered as undervoltage events. Voltage fluctuations on uV_{CC} shorter than the time $dBDUV_{CC\_BLK}$ are ignored and not recognized by the Power Supply Interface.

Detecting an undervoltage event on uV_{CC}, the FlexRay transceiver TLE9221SX sets the uV_{CC} undervoltage bit (bit 9) and the error bit (bit 11) (see **Figure 27**). After the uV_{CC} undervoltage detection timer $dBDUVV_{CC}$ expires, the uV_{CC} undervoltage flag is set, the mode of operation changes to BD_Standby mode.

The Host Interface remains active while the uV_{CC} undervoltage detection timer is running and the reference supply uV_{IO} is present. Setting the uV_{CC} undervoltage flag blocks the Host Interface and forces the mode of operation to BD_Standby mode (compare also with **Chapter 9.3** and **Table 16**).

While the power supply uV_{CC} is in undervoltage condition, the TLE9221SX also disables the Transmitter and sets the bus error bit (bit 4).

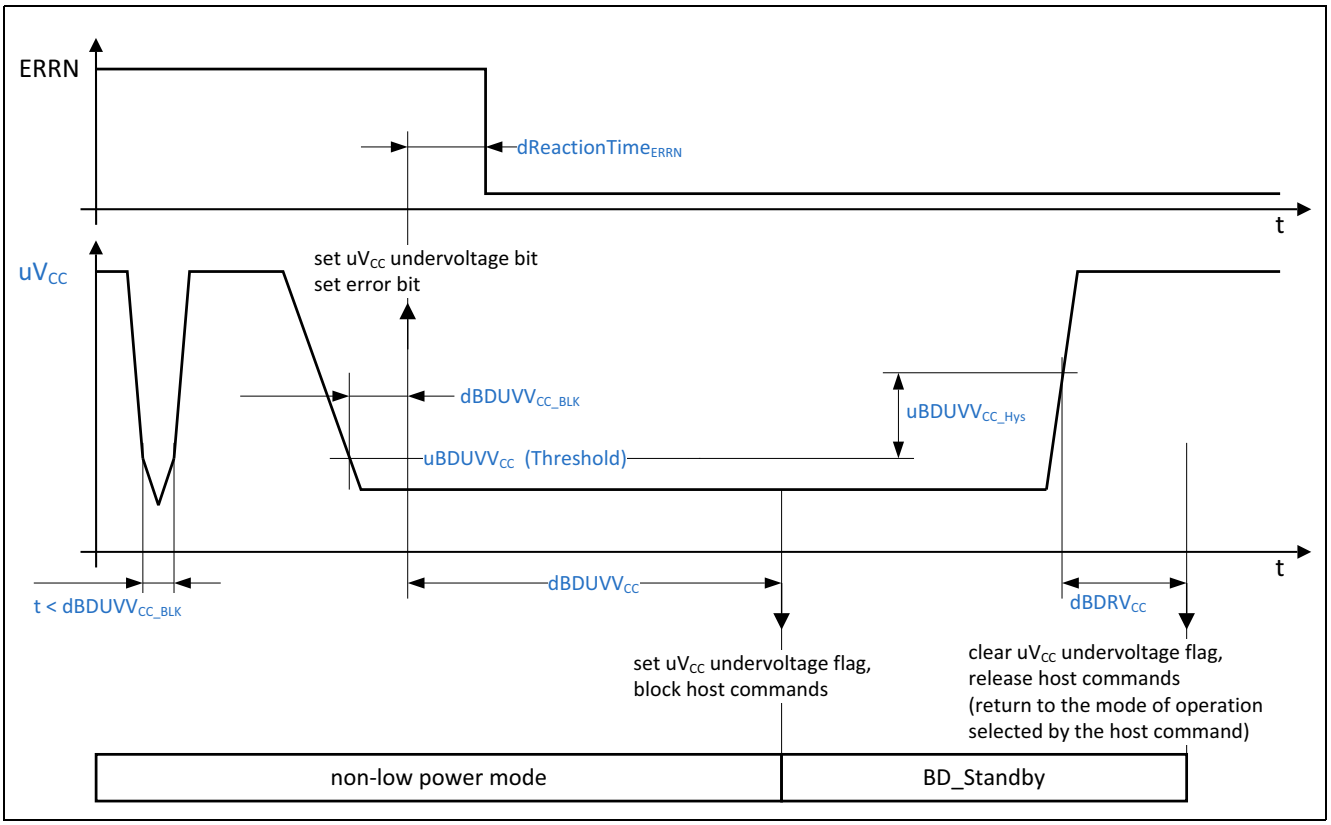


Figure 27 Undervoltage event at uV_{CC} in non-low power mode

8.3.4 Undervoltage Event at uV_{IO}

The Central State Machine of the TLE9221SX handles an undervoltage event at the reference supply uV_{IO} in a manner identical to an undervoltage event on the power supply uV_{BAT}.

The supply on the level shift input V_{IO} is the main reference for all digital inputs and outputs of the TLE9221SX. It is also connected to the pad supply of the external microcontroller (see **Figure 50**). An undervoltage event on the level shift input V_{IO} could lead to a misinterpretation of the digital input levels and could generate a false signal at the digital outputs.

For fail-safe reasons, the TLE9221SX blocks the Host Interface, the Communication Controller Interface and the Bus Guardian Interface after a small processing time ($dReactionTime_{ERRN}$) when an undervoltage event has been detected on the reference supply uV_{IO} (see **Figure 28**). According to **Table 2**, all digital inputs are set to their default level. All digital outputs are set to logical “low”.

The transceiver TLE9221SX detects an undervoltage event, if the supply at the pin V_{IO} drops for the time period $t > dBDUVV_{IO\_BLK}$ below the undervoltage detection threshold uUV_{IO} (see **Figure 28**). Voltage fluctuations on uV_{IO} shorter than $dBDUV_{CC\_BLK}$ are ignored and not recognized by the Power Supply Interface.

Although the Host Interface is blocked and the SIR is not accessible while the reference supply uV_{IO} is in undervoltage condition, the transceiver sets the uV_{IO} undervoltage bit (bit 10) and the error bit (bit 11) (see **Figure 28**). After the uV_{IO} undervoltage detection timer $dBDUVV_{IO}$ expires, the uV_{IO} undervoltage flag is set and the mode of operation changes to BD_Sleep mode (compare also to **Chapter 9.3** and **Table 16**).

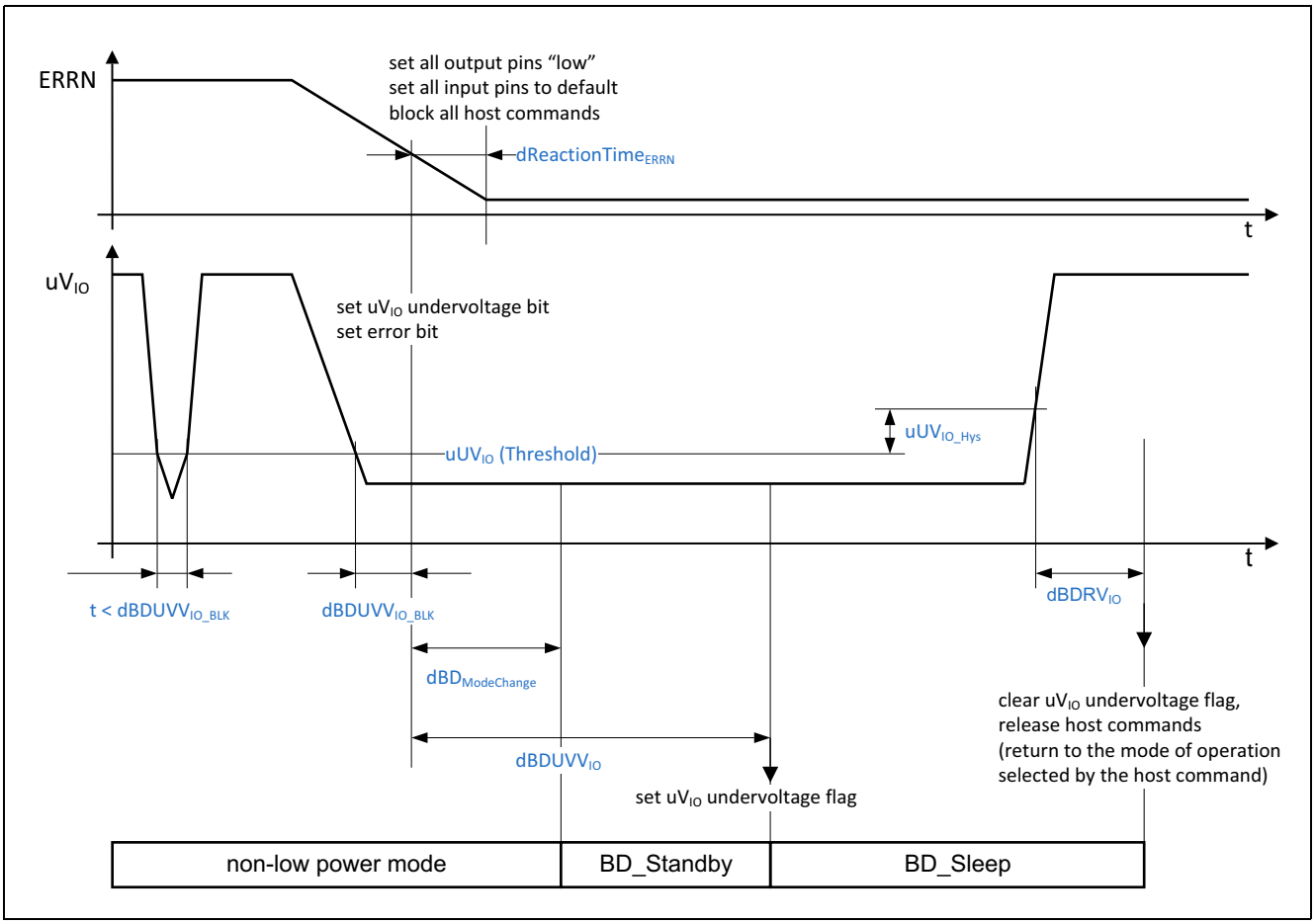


Figure 28 Undervoltage event at uV_{IO} in non-low power mode

Note: While the TLE9221SX is in undervoltage condition at the reference supply uV_{IO}, all digital outputs are set to “low”. The outputs do not reflect the status of the transceiver anymore.
For example, wake-up events cannot be indicated at the ERRN, RxD, and RxEN output anymore, since these outputs are set permanently to “low”.

8.4 Power-up and Power-down

8.4.1 BD_Off State

BD_Off state is reached, when the transceiver does not receive any supply.

The transceiver TLE9221SX is in BD_Off state when the internal supply voltage uV_{IN} is turned off and the Central State Machine is powered down. When both power supplies, uV_{CC} and uV_{BAT} fall below their power-down thresholds ($uBDPDV_{BAT}$ and $uBDPDV_{CC}$), the internal supply is off and the BD_Off state is reached (see **Figure 29**).

The status of the reference supply uV_{IO} has no influence on the power-down sequence of the Flexray transceiver TLE9221SX.

When the FlexRay transceiver TLE9221SX is in BD_Off state, all outputs are logical “low”, the Transmitter and the Receiver are turned off and the wake-up functions are not operational. If the reference supply uV_{IO} is available, the inputs are set to their default values (compare with **Table 2**).

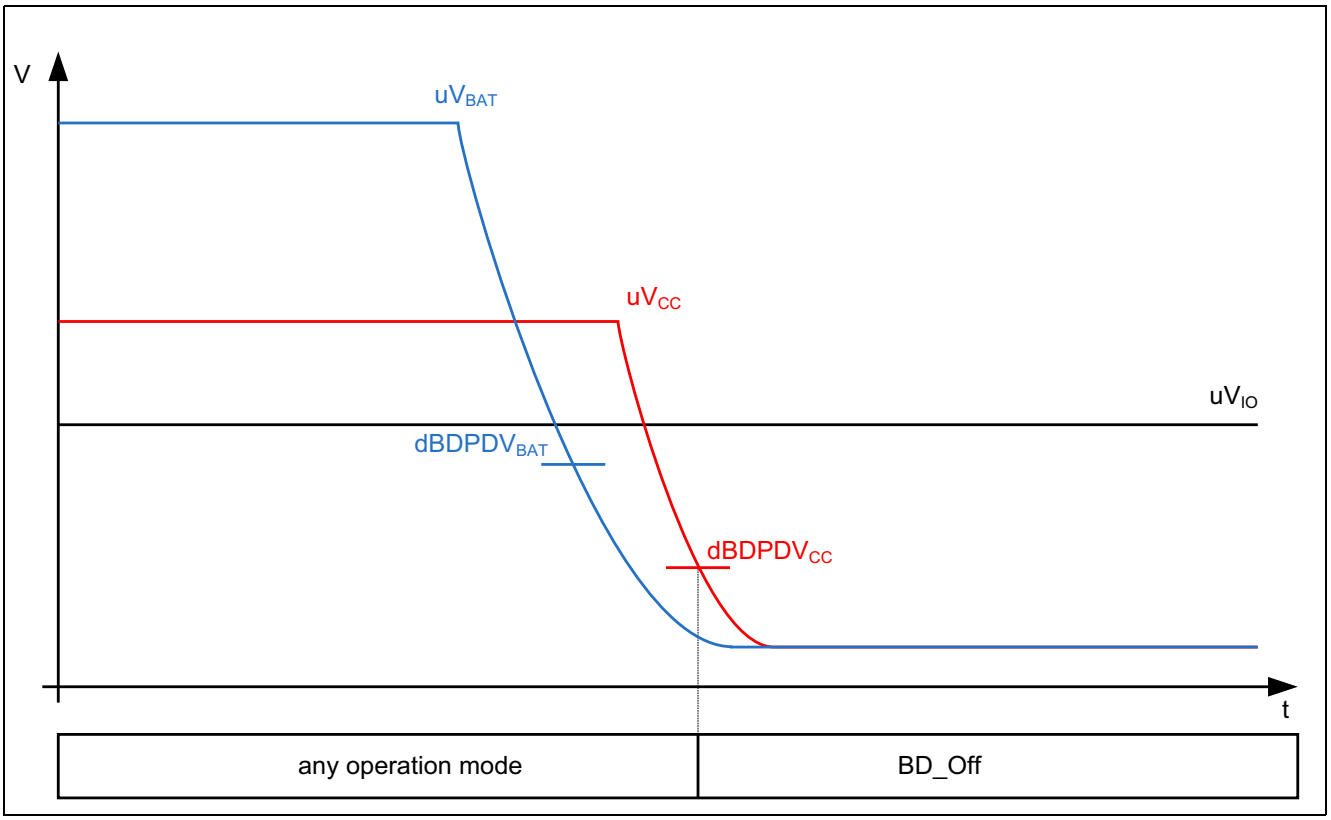


Figure 29 Power-down

8.4.2 Power-up

For the power-up, only the power supplies uV_{BAT} and uV_{CC} are significant. As soon as at least one power supply is above its reset threshold the internal supply uV_{IN} is available and the Central State Machine gets powered up. The device TLE9221SX enters into BD_Standby mode within the time period $dBD_{PowerUp}$ as soon as the voltage values of the power supplies uV_{BAT} and uV_{CC} are above their undervoltage detection threshold limits $uBDUVV_{BAT}$ and $uBDUVV_{CC}$ (see **Figure 30**).

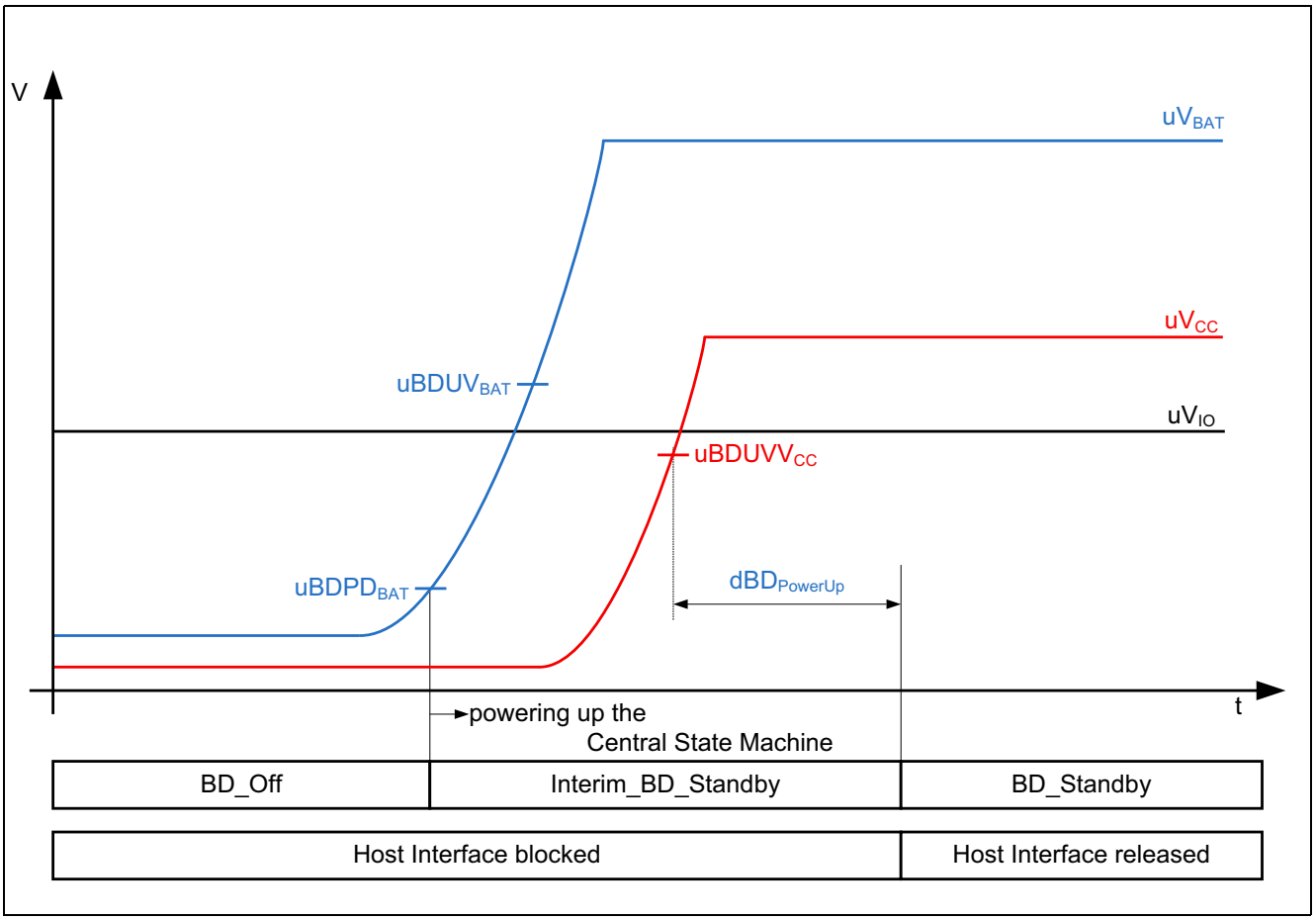


Figure 30 Power-up

8.4.3 Interim BD_Standby Mode

As a safety measure, the TLE9221SX provides an Interim BD_Standby mode. Changeover to the Interim_BD_Standby mode takes place during an incomplete power-up procedure (see **Figure 31**).

In Interim_BD_Standby mode, the TLE9221SX provides the same functions as in BD_Standby mode, except for the host commands. The host commands are blocked in Interim BD_Standby mode. Therefore, a host command cannot be used to change the mode of the TLE9221SX, while the power-up has not completed. With switching over to the interim BD_Standby mode, at least one undervoltage detection timer is started. In case the power-up is completed before the undervoltage detection timer expires, the TLE9221SX changes the mode of operation to BD_Standby mode. In case the undervoltage detection timer expires before the power-up is completed, the undervoltage flag is set depending on which power supply is missing, and the mode of operation changes to low power mode (compare with **Chapter 9.3**).

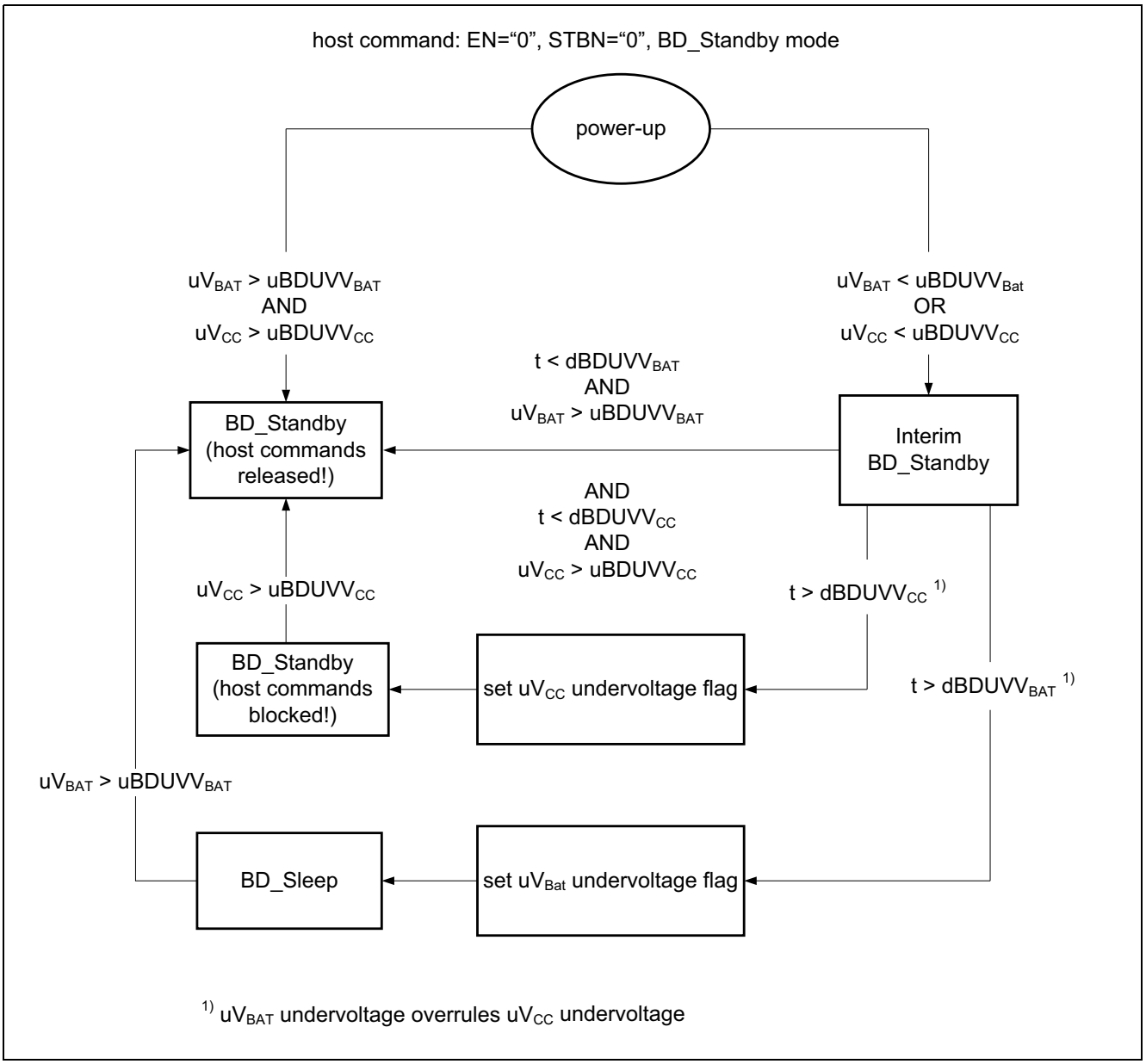


Figure 31 Changing over to Interim_BD_Standby mode

9 Operating Mode Description

The FlexRay transceiver TLE9221SX provides several different operating modes. The four main operating modes are implemented to handle the requirements of a FlexRay ECU. Two product-specific interim operation modes are implemented to guarantee secure mode changes even under failure conditions. The BD_Off state describes the behavior of the TLE9221SX, while it is not supplied (see **Table 12**).

Table 12 Operating modes overview

Modes of Operation	Description	Clustering
Operating mode		
BD_Normal	Normal operating mode to transmit data to the bus and receive data from the bus.	non-low power mode
BD_ReceiveOnly	The TLE9221SX can receive data from the bus, but the Transmitter is blocked.	non-low power mode
BD_Standby	Transmitter and Receiver are turned off, the diagnostic functions and wake-up detection are available.	low power mode
BD_Sleep	All functions, except the wake-up detection are turned off.	low power mode
Product-specific operating modes		
BD_GoToSleep	Transition mode to change over to the BD_Sleep mode via a host command.	interim mode
Interim_BD_Standby	Transition mode, to which a changeover is made only after an incomplete power-up	interim mode
Power-Down		
BD_Off	State of the TLE9221SX when no supply is fed to it	power-down state

9.1 Operating Mode Transitions Overview

Depending on the currently selected operating mode, several events can trigger a change of the operating mode. The options are:

- A valid host command at the Host Interface.
- Setting an undervoltage flag, either for the power supplies uV_{BAT} and uV_{CC} or for the reference voltage uV_{IO}.
- Recovery from an undervoltage event, either for the power supplies uV_{BAT} and uV_{CC} or for the reference voltage uV_{IO}.
- Wake-up detection either on the FlexRay bus or on the local wake-input WAKE.
- A power-up event at the power supplies uV_{BAT} and $uV_{CC.}$

It is not possible to change over to every operating mode by a trigger event. There are limitations and dependencies (see **Table 13**).

Table 13 Options for changeover to various operating modes

Target Mode	Trigger Event for the Mode Change	Limitation
BD_Normal	Changeover to BD_Normal mode can be made only by a valid host command.	Host commands are blocked if any undervoltage flag is set.
BD_ReceiveOnly	Changeover to BD_ReceiveOnly mode can be made only by a valid host command.	Host commands are blocked if any undervoltage flag is set.

Table 13 Options for changeover to various operating modes

Target Mode	Trigger Event for the Mode Change	Limitation
BD_Standby	Changeover to BD_Standby mode can be made by: • A valid host command • An undervoltage event at uV_{CC} • A wake-up event • A power-up event at uV_{CC} and uV_{BAT}	Changeover to BD_Standby mode cannot be made from BD_Sleep mode via host command (see **Figure 32**). Host commands are blocked if any undervoltage flag is set.
BD_Sleep	Changeover to BD_Sleep mode can be made by: • A valid host command • An undervoltage event at uV_{IO} or uV_{BAT}	Changeover to BD_Sleep mode by a host command is possible only via the BD_GoToSleep command (see **Figure 32**). Host commands are blocked if any undervoltage flag is set.
BD_GoToSleep	Changeover to BD_GoToSleep command can only be made by a valid host command.	The BD_GoToSleep command can not be executed while the wake-up flag is active (see **Table 14**). Host commands are blocked if any undervoltage flag is set.
Interim_BD_Standby	Changeover to Interim_BD_Standby mode takes place only after an incomplete power-up.	–
BD_Off	Changeover to BD_Off condition takes place if the power supplies uV_{BAT} and uV_{CC} are below their reset thresholds.	–

9.2 Operating Mode Change by Host Command

Changeover can be made to every operation mode, except the BD_Sleep mode by a valid host command, when no undervoltage flag is set. Changeover to BD_Sleep mode can be made only via the BD_GoToSleep command (see **Figure 32** and **Table 14**).

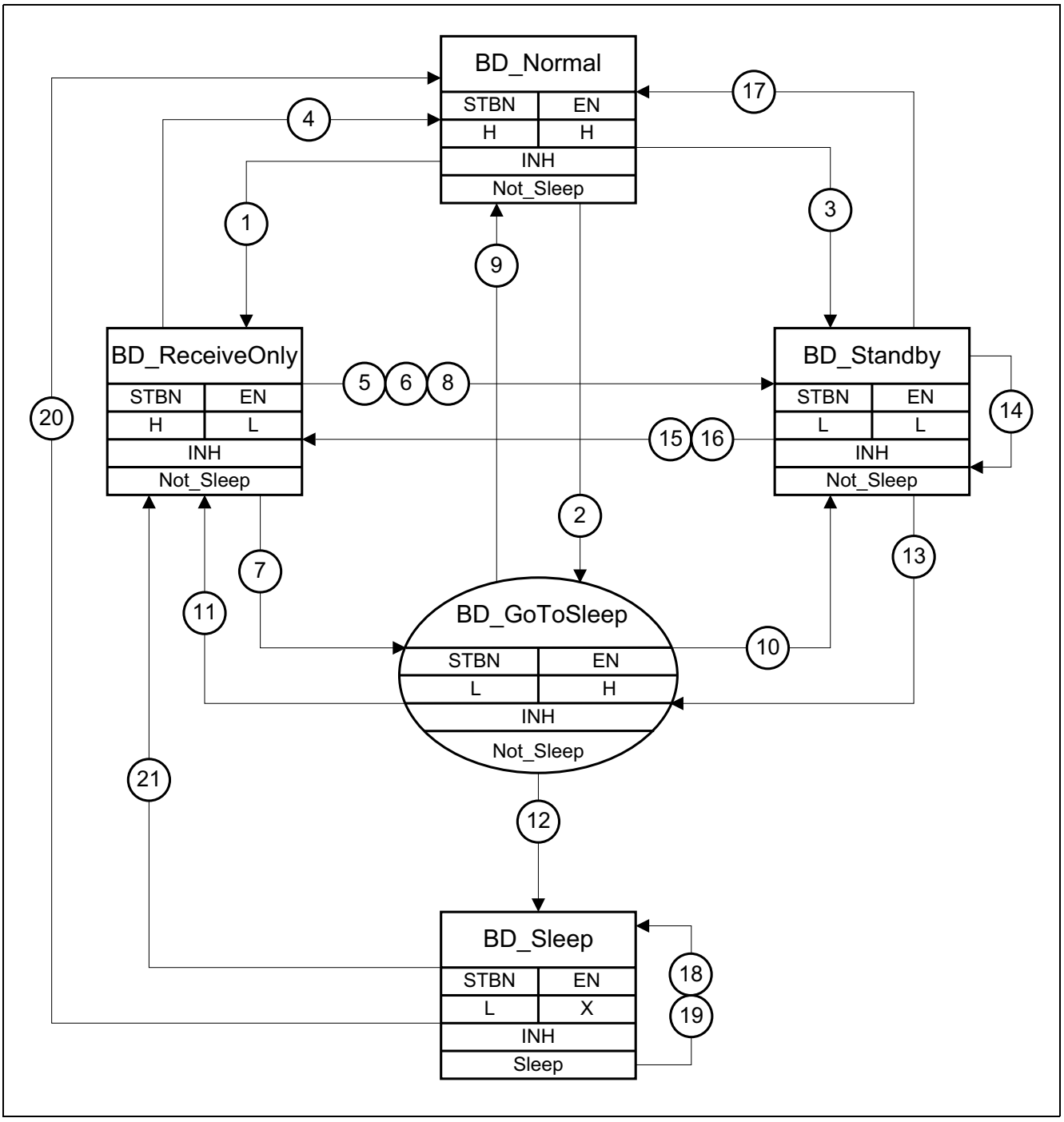


Figure 32 Operating mode change by host command

Table 14 Mode changes by host command[1) 2) 3) 4)]

No.	Primary Operating Mode	STBN	EN	Wake-up Flag	uV_{BAT} Flag	uV_{IO} Flag	uV_{CC} Flag	Secondary Operating Mode	ERRN[5)]	RxD[6)]	RxEN[6)]	INH	Remarks
BD_Normal Mode													
1	BD_Normal	H	set “L”	H	H	H	H	1 => BD_ReceiveOnly	H	FB	FB	Not_Sleep	7)
2	BD_Normal	set “L”	H	H	H	H	H	1 => BD_GoToSleep	H	1 => H	1 => H	Not_Sleep	7)
3	BD_Normal	set “L”	set “L”	H	H	H	H	1 => BD_Standby	H	1 => H	1 => H	Not_Sleep	7)
BD_ReceiveOnly Mode													
4	BD_ReceiveOnly	H	set “H”	2 => H	H	H	H	1 => BD_Normal	2 => H	FB	FB	Not_Sleep	7)
5	BD_ReceiveOnly	set “L”	L	H	H	H	H	1 => BD_Standby	H	1 => H	1 => H	Not_Sleep	7)
6	BD_ReceiveOnly	set “L”	L	L	H	H	H	1 => BD_Standby	1 => L	1 => L	1 => L	Not_Sleep	8)
7	BD_ReceiveOnly	set “L”	set “H”	H	H	H	H	1 => BD_GoToSleep	H	1 => H	1 => H	Not_Sleep	9)
8	BD_ReceiveOnly	set “L”	set “H”	L	H	H	H	1 => BD_Standby	1 => L	1 => L	1 => L	Not_Sleep	8), 10)
BD_GoToSleep Command													
9	BD_GoToSleep	set “H”	H	2 => H	H	H	H	1 => BD_Normal	2 => H	1=>FB	1=>FB	Not_Sleep	9), 11)
10	BD_GoToSleep	L	set “L”	H	H	H	H	1 => BD_Standby	H	H	H	Not_Sleep	9), 11)
11	BD_GoToSleep	set “H”	set “L”	H	H	H	H	1 => BD_ReceiveOnly	H	1=>FB	1=>FB	Not_Sleep	9), 11)
12	BD_GoToSleep	L	H	H	H	H	H	1 => BD_Sleep	H	H	H	1 => Sleep	9), 11)
BD_Standby													
13	BD_Standby	L	set “H”	H	H	H	H	1 => BD_GoToSleep	H	H	H	Not_Sleep	9)
14	BD_Standby	L	set “H”	L	H	H	H	BD_Standby	L	L	L	Not_Sleep	10)
15	BD_Standby	set “H”	L	H	H	H	H	1 => BD_ReceiveOnly	H	1=>FB	1=>FB	Not_Sleep	–
16	BD_Standby	set “H”	L	L	H	H	H	1 => BD_ReceiveOnly	1 => H/L	1=>FB	1=>FB	Not_Sleep	12)
17	BD_Standby	set “H”	set “H”	2 => H	H	H	H	1 => BD_Normal	2=> H	1=>FB	1=>FB	Not_Sleep	7)
BD_Sleep													
18	BD_Sleep	L	set “H”	H	H	H	H	BD_Sleep	H	H	H	Sleep	13), 14)

Table 14 Mode changes by host command[1) 2) 3) 4)]

No.	Primary Operating Mode	STBN	EN	Wake-up Flag	uV_{BAT} Flag	uV_{IO} Flag	uV_{CC} Flag	Secondary Operating Mode	ERRN[5)]	RxD[6)]	RxEN[6)]	INH	Remarks
19	BD_Sleep	L	set “L”	H	H	H	H	BD_Sleep	H	H	H	Sleep	[13), 14)]
20	BD_Sleep	set “H”	set “H”	2 => H	H	H	H	1 => BD_Normal	2 => H	1=>FB	1=>FB	1 => Not_Sleep	[7), 14)]
21	BD_Sleep	set “H”	set “L”	H	H	H	H	1 => BD_ReceiveOnly	H	1=>FB	1=>FB	1 => Not_Sleep	[14)]

1) The table describes the states and signals of flags, operating modes and output pins. This table does not contain any timing information. Time for mode changes or the response time of the digital outputs are specified in the electrical characteristics (compare with **Table 22**).

2) All flags are “low” active. “L” means the flag is set. “X” = “don’t care”.
The color red stands for the event which triggered the mode transition.
For example: set “L” or set “H”.
The color blue stands for the consequence of the trigger event.
The numbers, “1 =>”, “2 =>” indicate the order of the consequences.
For example: “1=> BD_Normal” means the transceiver TLE9221SX changes over to BD_Normal mode.
“2=> H” means the flag is cleared after the TLE9221SX has changed over to BD_Normal mode.
“FB” stands for “Follow Bus” and means that depending on the signal on the FlexRay bus, the pins RxD and RxEN can either be “high” or “low”.

3) The wake-up flag stands for a detected wake-up event (compare with **Chapter 7.3** and **Table 10**).
The uV_{BAT} flag is the same as the uV_{BAT} undervoltage flag, which is set after the uV_{BAT} undervoltage detection timer expires (compare with **Chapter 8.3.1**).
The uV_{IO} flag is the same as the uV_{IO} undervoltage flag, which is set after the uV_{IO} undervoltage detection timer expires (compare with **Chapter 8.3.1**).
The uV_{CC} flag is the same as the uV_{CC} undervoltage flag, which is set after the uV_{CC} undervoltage detection timer expires (compare with **Chapter 8.3.1**).

4) The ERRN output indicates the wake-up flag, the wake-up source bit and the error bit (compare with **Table 9**). The error bit is set only by the undervoltage bits, such as the uV_{BAT} undervoltage bit (bit 8), the uV_{CC} undervoltage bit (bit 9) and the uV_{IO} undervoltage bit (bit 10). All other possible sources setting the error bit, such as, for example a bus failure or an overtemperature event, are considered as not set in this table.

5) The signal at the ERRN output pin depends on the host command applied and not on the current operating mode (compare with **Chapter 6.3**).

6) The signals at the RxD and RxEN outputs depend on the current operation mode, and are independent of the host command applied (compare with **Table 5**).

7) While TLE9221SX changes over to BD_Normal mode, the wake-up flag is cleared. Moreover, the wake-up flag cannot be set in non-low power mode, and therefore the wake-up flag is always “high” in BD_Normal mode (see **Chapter 7.3**).

8) The wake-up flag was set during a previous wake-up event while the TLE9221SX was in low power mode.

9) The interim mode will automatically be left to BD_Sleep when the timer dBD_{Sleep} expires. If the host command does not change within the time $dBD_{Sleep,}$ the TLE9221SX changes over by default to BD_Sleep mode (see **Chapter 9.2.1**).

10) The BD_GoToSleep command cannot be executed while the wake-up flag is active (see **Figure 34**). The TLE9221SX changes over directly to BD_StandBy mode.

11) Since the BD_GoToSleep command can be executed only when the wake-up flag is cleared, the wake-up flag is always “high” while the TLE9221SX executes the BD_GoToSleep command.
12) If the host command BD_ReceiveOnly mode is applied, the ERRN output indicates the wake-up source bit (see **Table 9**).
13) The EN input pin of the Host Interface is disabled in BD_Sleep mode, as long the STBN input pin remains “low” (see **Chapter 9.2.2**).
14) A wake-up event would change the operation mode from BD_Sleep to BD_Standby, therefore, the wake-up flag is always “high” while the TLE9221SX remains in BD_Sleep mode.

9.2.1 Entering BD_Sleep Mode via the BD_GoToSleep Command

The BD_GoToSleep command can be executed from every non-low power mode and from BD_Standby mode by applying the host command STBN = “L” and EN = “H”. The BD_GoToSleep command cannot be executed from BD_Sleep mode (see **Figure 32**).

When the transceiver TLE9221SX recognizes the host command BD_GoToSleep, the TLE9221SX changes over to the interim mode “BD_GoToSleep command” and starts an internal timer. In case the EN input and the STBN input remain unchanged during the BD_Sleep mode detection window ($t = dBD_{Sleep}$), the operating mode automatically changes over to BD_Sleep mode. The time for the mode change, $dBD_{ModeChange}$, is defined as the time interval between applying the host command and changing over to BD_Sleep mode (see **Figure 33**).

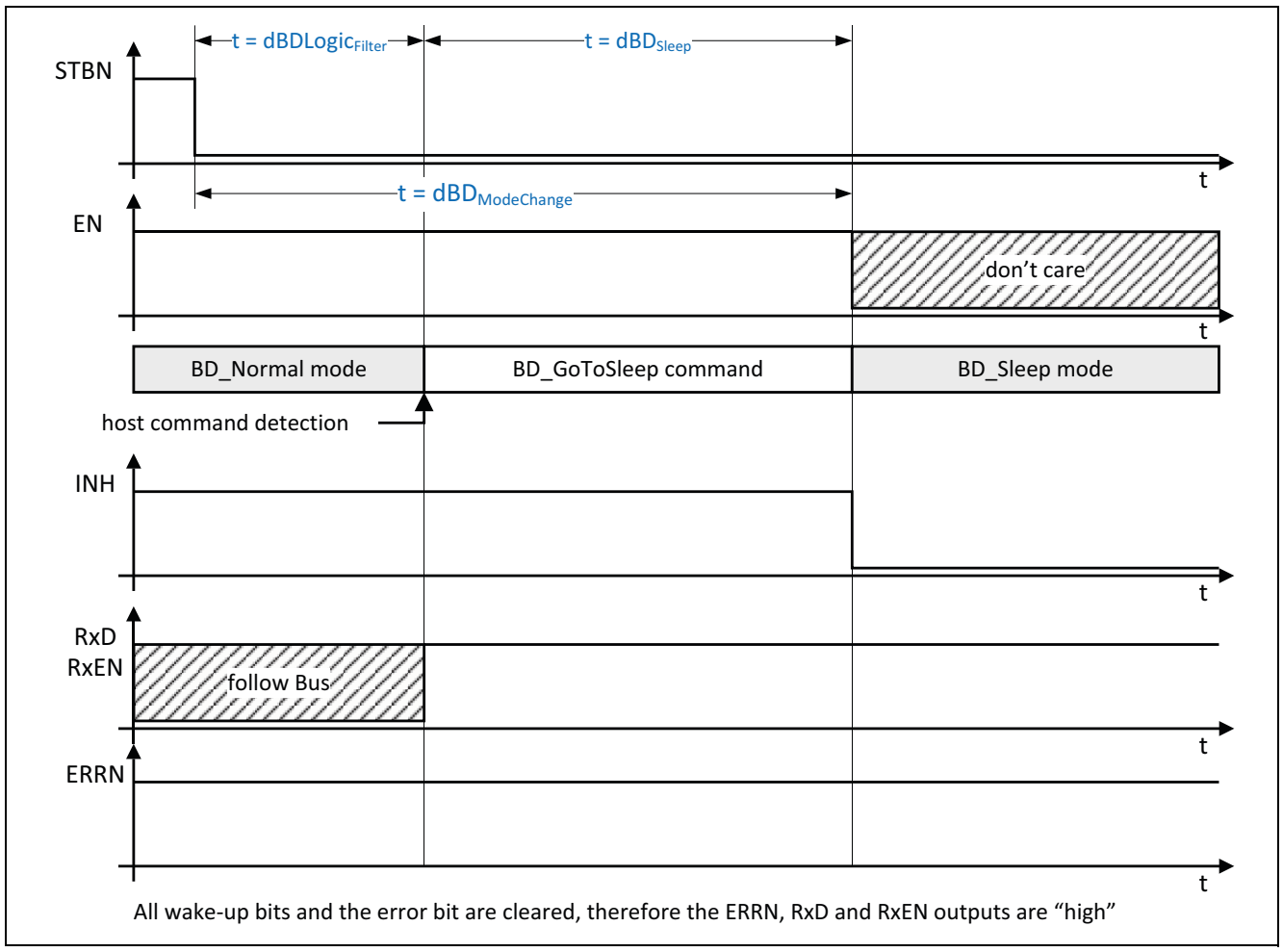


Figure 33 Entering BD_Sleep mode

The BD_GoToSleep command can be executed only when the wake-up flag is cleared. When the wake-up flag is cleared, the output pins RxD and RxEN are set to logical “high” in BD_Sleep mode and also during the execution of the “BD_GoToSleep command”.

In case the changeover to BD_Sleep mode is made by a host command, the EN input is disabled in BD_Sleep mode (see **Figure 32**, **Figure 33** and **Table 14**).

Applying the BD_GoToSleep host command to the TLE9221SX, while the wake-up flag is active, changes the operating mode directly to BD_Standby mode. The RxD and RxEN outputs are set to “low” and indicate a previous wake-up event (see **Figure 34** and **Table 14**).

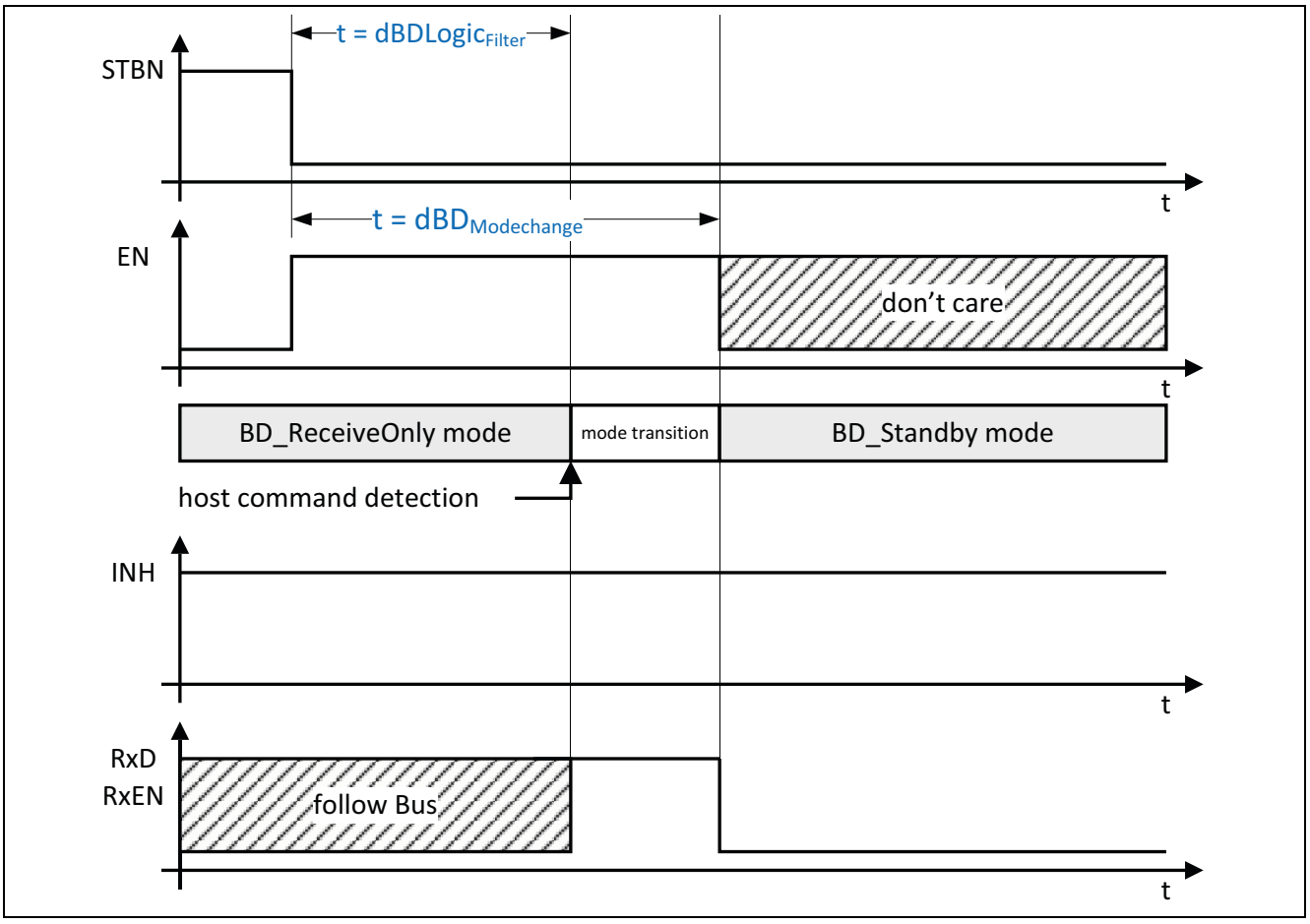


Figure 34 Changing over to BD_Standby, with an active wake-up flag

9.2.2 Quitting BD_Sleep by Host Command

Changeover to BD_Sleep mode can be made by a host command or by an undervoltage event. In case changeover to BD_Sleep was made by a host command via the BD_GoToSleep command, the EN input pin gets disabled when the TLE9221SX changes over to BD_Sleep mode.
As long as the STBN input pin remains at logical "low", any signal change at the EN input is ignored and does not trigger any mode change. Signal change at the STBN input pin enables the EN input as well and a mode change is possible.

Via a host command, BD_Sleep mode can only change to BD_Normal mode or to BD_ReceiveOnly mode (see **Figure 32** and **Table 14**).

9.3 Operating Mode Changeover by Undervoltage Flag

Besides a valid host command, any changeovers in the operating mode may also be triggered by setting the undervoltage flag after the undervoltage detection timer has expired (compare with **Chapter 8.3.1**). Setting the uV_{IO} or the uV_{BAT} undervoltage flag changes the mode of operation to BD_Sleep, and setting the uV_{CC} undervoltage flag changes the mode of operation to BD_Standby.

If the transceiver TLE9221SX changes over to BD_Sleep mode by setting the uV_{IO} or uV_{BAT} undervoltage flag, the EN input pin remains active even in BD_Sleep mode.

In case any undervoltage flag becomes active, while the FlexRay transceiver TLE9221SX is executing the BD_GoToSleep command, the mode of operation changes directly to BD_Sleep (see **Table 15** and **Figure 35**).

Setting the undervoltage flag does not cause any change in the operating mode, if the transceiver is already in BD_Sleep mode.

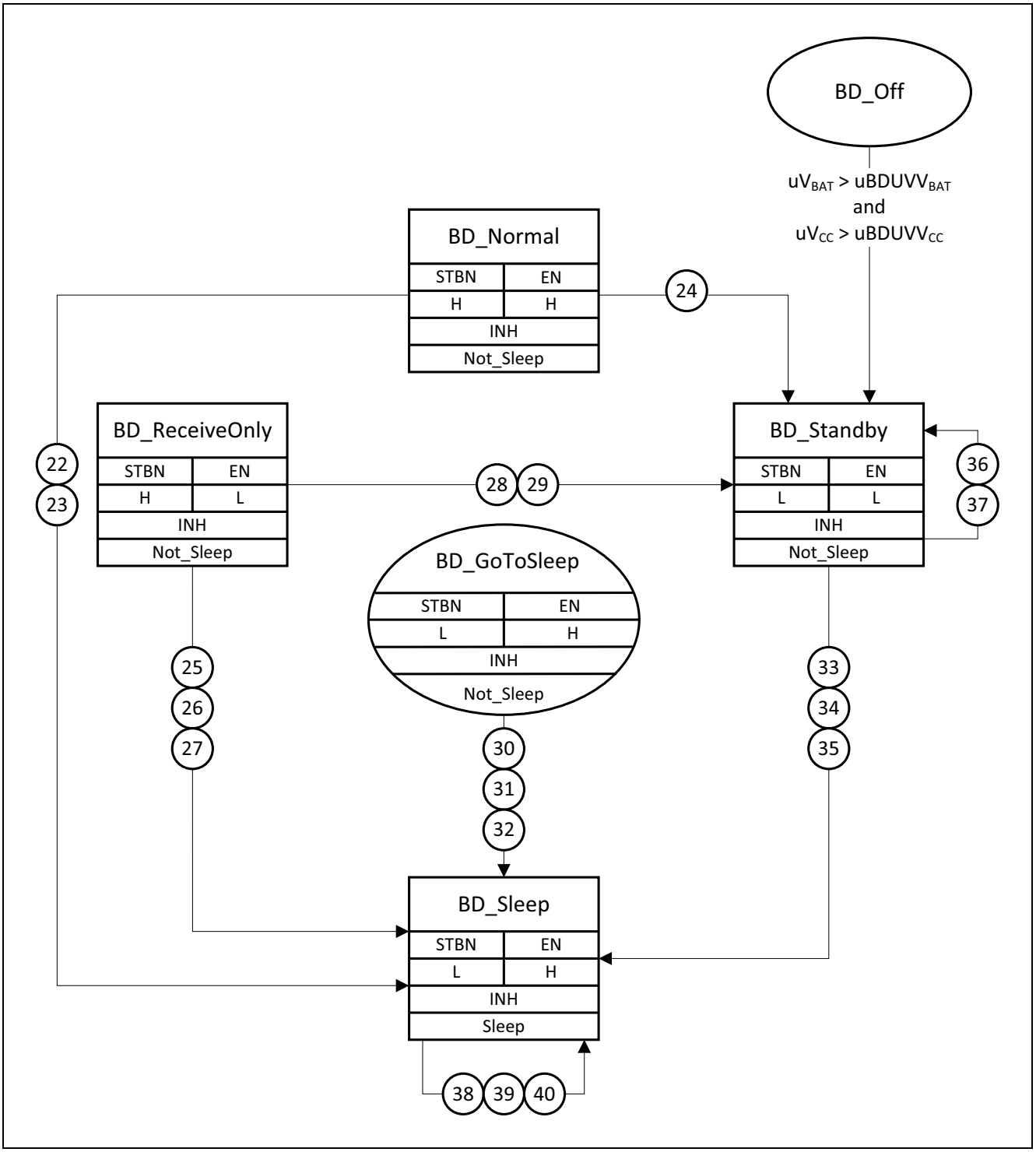


Figure 35 Operating mode changes by undervoltage flag

Table 15 Mode changes by setting the undervoltage flags [1) 2) 3) 4)]

No.	Primary Operating Mode	STBN	EN	Wake-up Flag	uV_{BAT} Flag	uV_{IO} Flag	uV_{CC} Flag	Secondary Operating Mode	ERRN[5)]	RxD[6)]	RxEN[6)]	INH	Remarks
BD_Normal Mode													
22	BD_Normal	H	H	H	set “L”	H	X	1 => BD_Sleep	1 => L	1 => H	1 => H	1 => Sleep	[7), 8)]
23	BD_Normal	X	X	H	X	set “L”	X	2 => BD_Sleep	1 => L	1 => L	1 => L	2 => Sleep	[7), 9), 10)]
24	BD_Normal	H	H	H	H	H	set “L”	1 => BD_Standby	1 => L	1 => H	1 => H	Not_Sleep	[7)]
BD_ReceiveOnly Mode													
25	BD_ReceiveOnly	H	L	H	set “L”	H	X	1 => BD_Sleep	1 => L	1 => H	1 => H	1 => Sleep	[8)]
26	BD_ReceiveOnly	H	L	L	set “L”	H	X	1 => BD_Sleep	H/L	1 => L	1 => L	1 => Sleep	[8), 11), 12)]
27	BD_ReceiveOnly	X	X	X	X	set “L”	X	2 => BD_Sleep	1 => L	1 => L	1 => L	2 => Sleep	[9), 10)]
28	BD_ReceiveOnly	H	L	H	H	H	set “L”	1 => BD_Standby	1 => L	1 => H	1 => H	Not_Sleep	–
29	BD_ReceiveOnly	H	L	L	H	H	set “L”	1 => BD_Standby	H/L	1 => L	1 => L	Not_Sleep	[11), 12)]
BD_GoToSleep Command													
30	BD_GoToSleep	L	H	H	set “L”	X	X	1 => BD_Sleep	H	H	H	1 => Sleep	[8), 13), 14)]
31	BD_GoToSleep	X	X	H	X	set “L”	X	1 => BD_Sleep	1 => L	1 => L	1 => L	1 => Sleep	[9), 13), 14)]
32	BD_GoToSleep	L	H	H	X	X	set “L”	1 => BD_Sleep	H	H	H	1 => Sleep	[13), 14)]
BD_Standby													
33	BD_Standby	L	L	H	set “L”	H	X	1 => BD_Sleep	H	H	H	1 => Sleep	[8)]
34	BD_Standby	L	L	L	set “L”	H	X	1 => BD_Sleep	L	L	L	1 => Sleep	[8), 11)]
35	BD_Standby	X	X	X	X	set “L”	X	1 => BD_Sleep	1 => L	1 => L	1 => L	1 => Sleep	[9)]
36	BD_Standby	L	L	H	H	H	set “L”	1 => BD_Standby	H	H	H	Not_Sleep	–
37	BD_Standby	L	L	L	H	H	set “L”	1 => BD_Standby	L	L	L	Not_Sleep	[11)]
BD_Sleep													
38	BD_Sleep	L	X	H	set “L”	X	X	1 => BD_Sleep	H	H	H	Sleep	[8)]
39	BD_Sleep	X	X	H	X	set “L”	X	1 => BD_Sleep	H	H	H	Sleep	[9)]
40	BD_Sleep	L	X	H	X	X	set “L”	1 => BD_Sleep	H	H	H	Sleep	–

1) The table describes the states and signals of flags, operating modes and output pins. This table does not contain any timing information. Time for mode changes or the response time of the digital outputs are specified in the electrical characteristics (compare with **Table 22**).
2) All flags are “low” active. “L” means the flag is set. “X” = “don’t care”.
   The color red stands for the event which triggered the mode transition.
   For example: set “L” or set “H”.
   The color blue stands for the consequence of the trigger event.
   The numbers, “1 =>”, “2 =>” indicate the order of the consequences.
   For example: “1=> BD_Normal” means the transceiver TLE9221SX changes over to BD_Normal mode.
   “2=> H” means the flag is cleared after the TLE9221SX has changed over to BD_Normal mode.
   “FB” stands for “Follow Bus” and means that depending on the signal on the FlexRay bus, the pins RxD and RxEN can either be “high” or “low”.
3) The wake-up flag stands for a detected wake-up event (compare with **Chapter 7.3** and **Table 10**).
   The uV_{BAT} flag is the same as the uV_{BAT} undervoltage flag, which is set after the uV_{BAT} undervoltage detection timer expires (compare with **Chapter 8.3.1**).
   The uV_{IO} flag is the same as the uV_{IO} undervoltage flag, which is set after the uV_{IO} undervoltage detection timer expires (compare with **Chapter 8.3.1**).
   The uV_{CC} flag is the same as the uV_{CC} undervoltage flag, which is set after the uV_{CC} undervoltage detection timer expires (compare with **Chapter 8.3.1**).
4) The ERRN output indicates the wake-up flag, the wake-up source bit and the error bit (compare with **Table 9**). The error bit is set only by the undervoltage bits, such as the uV_{BAT} undervoltage bit (bit 8), the uV_{CC} undervoltage bit (bit 9) and the uV_{IO} undervoltage bit (bit 10). All other possible sources setting the error bit, such as, for example a bus failure or an overtemperature event, are considered as not set in this table.
5) The signal at the ERRN output pin depends on the host command applied and not on the current operating mode (compare with **Chapter 6.3**).
6) The signals at the RxD and RxEN outputs depend on the current operation mode, and are independent of the host command applied (compare with **Table 5**).
7) While TLE9221SX changes over to BD_Normal mode, the wake-up flag is cleared. Moreover, the wake-up flag cannot be set in non-low power mode, and therefore the wake-up flag is always “high” in BD_Normal mode (see **Chapter 7.3**).
8) The uV_{BAT} undervoltage flag overrules the uV_{CC} undervoltage flag (see **Chapter 9.3.1**).
9) An undervoltage event at uV_{IO} blocks the Host Interface at once and sets all outputs to logical “low” (see **Chapter 8.3.4** and **Figure 28**). The transceiver TLE9221SX can not indicate the error bit and the wake-up flag.
10) The uV_{IO} undervoltage flag overrules the uV_{CC} undervoltage flag (see **Chapter 9.3.1**).
11) The wake-up flag was set during a previous wake-up event while the TLE9221SX was in low power mode.
12) If the host command BD_ReceiveOnly mode is applied, the ERRN indicates the wake-up source bit (see **Table 9**).
13) Since the BD_GoToSleep command can be executed only when the wake-up flag is cleared, the wake-up flag is always “high” while the TLE9221SX executes the BD_GoToSleep command.
14) The BD_GoToSleep command is considered as low power mode and the ERRN indicates the wake-up flag just as in the BD_Sleep or BD_Standby mode (see **Table 9**).

9.3.1 Priorities of Undervoltage Events

Even if there are undervoltage events on both power supplies uV_{BAT} and uV_{CC}, together with an undervoltage event on the reference supply uV_{IO}, the Central State Machine is operating and handles the undervoltage events.

An undervoltage event on uV_{IO} blocks the Host Interface at once and interrupts the communication before the uV_{IO} undervoltage timer expires. When the uV_{IO} undervoltage timer expires, the TLE9221SX changes the mode of operation to BD_Sleep. In case the uV_{CC} undervoltage flag is set, the uV_{IO} undervoltage flag overrules the uV_{CC} undervoltage flag.
If the uV_{CC} undervoltage flag was set before the uV_{IO} undervoltage flag, the mode of operation changes from BD_Standby to BD_Sleep mode.
If the uV_{IO} undervoltage flag was set before the uV_{CC} undervoltage flag, the mode of operation remains in BD_Sleep mode.

During an uV_{BAT} undervoltage event, the Host Interface and also the Communication Controller Interface continues to work until the undervoltage detection timer expires. The uV_{BAT} undervoltage flag also overrules a uV_{CC} undervoltage flag and the transceiver TLE9221SX ends up in BD_Sleep mode. Simultaneous undervoltage events at uV_{BAT} and uV_{IO}, additionally disable the Host Interface and the Communication Controller Interface in comparison to a single uV_{BAT} undervoltage event. After the undervoltage detection timer expires, the TLE9221SX changes over to BD_Sleep mode.

The least significant undervoltage flag is the uV_{CC} undervoltage flag. An active uV_{CC} undervoltage flag changes the mode of operation from non-low power mode to BD_Standby mode, when no other undervoltage flag is set. During an uV_{CC} undervoltage event the Transmitter is disabled.

9.4 Operating Mode Changes by Undervoltage Recovery

As stated in **Chapter 8.3**, any undervoltage flag causes a change in the operating mode and blocks the Host Interface and the Communication Controller Interface.

After recovering from the undervoltage condition, and after the undervoltage flags are cleared, the FlexRay transceiver TLE9221SX enables the Host Interface and also the Communication Controller Interface and the host command applied at the inputs STBN and EN changes the mode of operation (see **Figure 36** and **Table 16**).

9.4.1 BD_Sleep Mode Entry Flag

A special case is the undervoltage recovery from BD_Sleep mode while the host command BD_Standby is applied to the Host Interface.

The EN input pin will be disabled while the device is in BD_Sleep mode. A mode changeover via host command from BD_Sleep mode to BD_Standby mode is not permitted (compare with **Table 14**). The transceiver distinguishes the host command BD_Sleep from BD_Standby, after the transceiver recovers from an undervoltage event.
The BD_Sleep mode entry flag indicates, how the changeover to BD_Sleep mode occurred. If changeover to BD_Sleep mode took place by setting an undervoltage flag, the BDSME flag (BD_Sleep Mode Entry) is set to “low” and the EN input pin remains active. If changeover to BD_Sleep mode took place by a host command, the BDSME flag is set to logical “high” and the EN input pin gets disabled (see **Table 16**).

The BDSME is an internal flag and it is neither indicated at the ERRN output nor latched in the SIR.

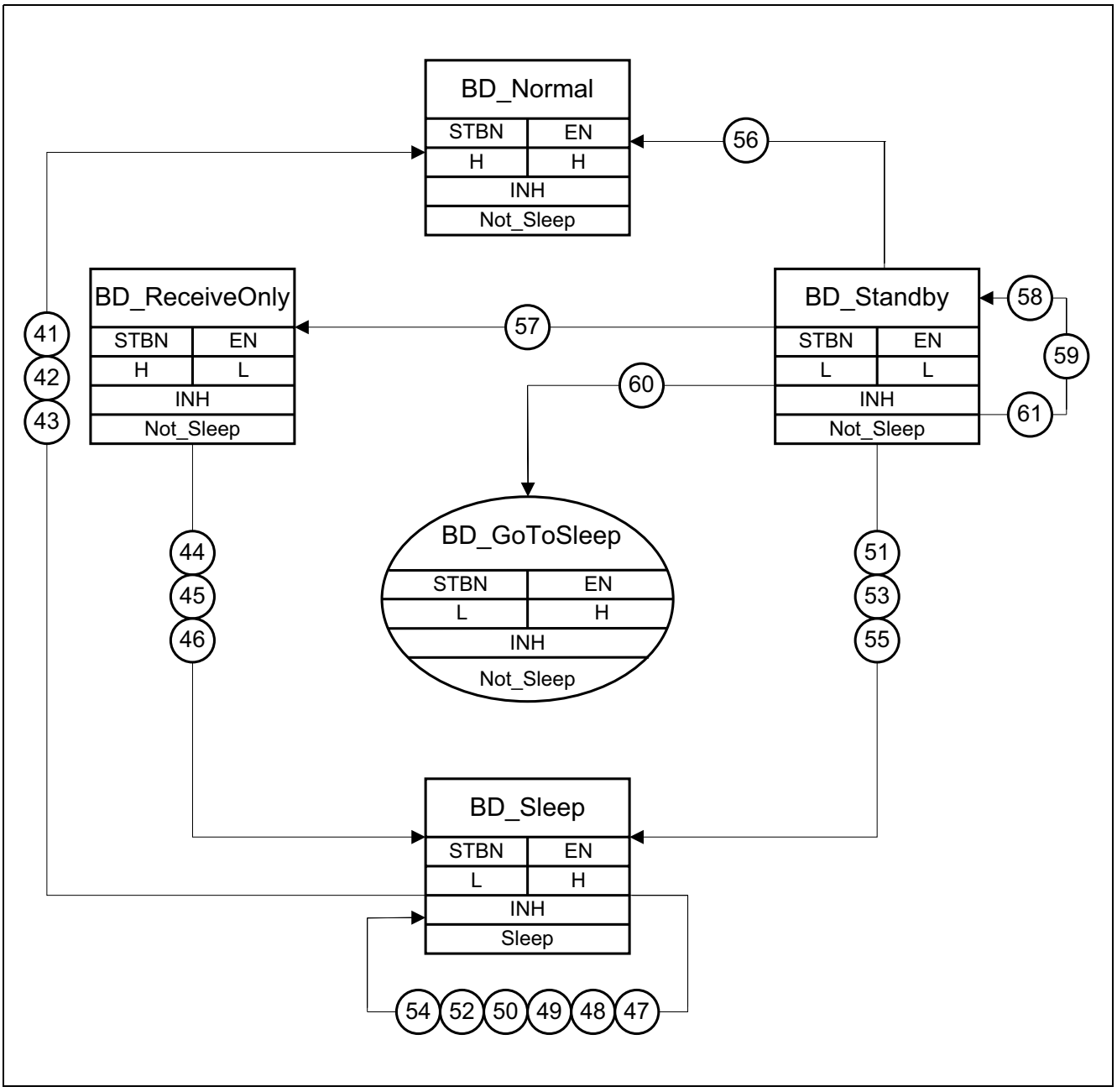


Figure 36 Change in the mode of operation by undervoltage recovery

Table 16 Mode changes via undervoltage recovery[1) 2) 3) 4)]

No.	Primary Operating Mode	STBN	EN	Wake-up Flag	BDSME Flag[5)]	uV_{BAT} Flag	uV_{IO} Flag	uV_{CC} Flag	Secondary Operating Mode	ERRN[6)]	RxD[7)]	RxEN[7)]	INH	Remarks
BD_Sleep -> Host Command BD_Normal														
41	BD_Sleep	H	H	2 => H	X	set “H”	H	H	1 => BD_Normal	2 => H	1=>FB	1=>FB	1 => Not_Sleep	[8)], [9)]
42	BD_Sleep	H	H	2 => H	X	H	set “H”	H	1 => BD_Normal	2 => H	1=>FB	1=>FB	1 => Not_Sleep	[8)], [9)]
43	BD_Sleep	H	H	2 => H	X	H	H	set “H”	1 => BD_Normal	2 => H	1=>FB	1=>FB	1 => Not_Sleep	[8)], [9)], [10)]
BD_Sleep -> Host Command BD_ReceiveOnly														
44	BD_Sleep	H	L	X	X	set “H”	H	H	1 => BD_ReceiveOnly	H/L	1=>FB	1=>FB	1 => Not_Sleep	[11)]
45	BD_Sleep	H	L	X	X	H	set “H”	H	1 => BD_ReceiveOnly	H/L	1=>FB	1=>FB	1 => Not_Sleep	[11)]
46	BD_Sleep	H	L	X	X	H	H	set “H”	1 => BD_ReceiveOnly	H/L	1=>FB	1=>FB	1 => Not_Sleep	[10)], [11)]
BD_Sleep -> Host Command BD_Sleep														
47	BD_Sleep	L	H	H	X	set “H”	H	H	BD_Sleep	H	H	H	Sleep	[12)]
48	BD_Sleep	L	H	H	X	H	set “H”	H	BD_Sleep	1 => H	1 => H	1 => H	Sleep	[12)]
49	BD_Sleep	L	H	H	X	H	H	set “H”	BD_Sleep	H	H	H	Sleep	[10)], [12)]
BD_Sleep -> Host Command BD_Standby														
50	BD_Sleep	L	L	H	H	set “H”	H	H	BD_Sleep	H	H	H	Sleep	[12)], [13)]
51	BD_Sleep	L	L	H	L	set “H”	H	H	1 => BD_Standby	H	H	H	1 => Not_Sleep	[12)], [14)]
52	BD_Sleep	L	L	H	H	H	set “H”	H	BD_Sleep	1 => H	1 => H	1 => H	Sleep	[12)], [13)]
53	BD_Sleep	L	L	H	L	H	set “H”	H	1 => BD_Standby	1 => H	1 => H	1 => H	1 => Not_Sleep	[12)], [14)]
54	BD_Sleep	L	L	H	H	H	H	set “H”	BD_Sleep	H	H	H	Sleep	[12)], [13)]
55	BD_Sleep	L	L	H	L	H	H	set “H”	1 => BD_Standby	H	H	H	1 => Not_Sleep	[12)], [14)]
BD_Standby														
56	BD_Standby	H	H	2 => H	X	H	H	set “H”	1 => BD_Normal	2 => H	1=>FB	1=>FB	Not_Sleep	[8)], [9)], [15)]

Table 16 Mode changes via undervoltage recovery[1) 2) 3) 4)]

No.	Primary Operating Mode	STBN	EN	Wake-up Flag	BDSME Flag[5)]	uV_{BAT} Flag	uV_{IO} Flag	uV_{CC} Flag	Secondary Operating Mode	ERRN[6)]	RxD[7)]	RxEN[7)]	INH	Remarks
57	BD_Standby	H	L	X	X	H	H	set “H”	1 => BD_ReceiveOnly	H/L	1=>FB	1=>FB	Not_Sleep	[11), 15), 16)]
58	BD_Standby	L	L	H	X	H	H	set “H”	BD_Standby	H	H	H	Not_Sleep	[15)]
59	BD_Standby	L	L	L	X	H	H	set “H”	BD_Standby	L	L	L	Not_Sleep	[15), 16)]
60	BD_Standby	L	H	H	X	H	H	set “H”	1 => BD_GoToSleep	H	H	H	Not_Sleep	[15)]
61	BD_Standby	L	H	L	X	H	H	set “H”	BD_Standby	L	L	L	Not_Sleep	[15), 16)]

1) The table describes the states and signals of flags, operating modes and output pins. This table does not contain any timing information. Time for mode changes or the response time of the digital outputs are specified in the electrical characteristics (compare with **Table 22**).

2) All flags are “low” active. “L” means the flag is set. “X” = “don’t care”.
The color red stands for the event which triggered the mode transition.
For example: set “L” or set “H”.
The color blue stands for the consequence of the trigger event.
The numbers, “1 =>”, “2 =>” indicate the order of the consequences.
For example: “1=> BD_Normal” means the transceiver TLE9221SX changes over to BD_Normal mode.
“2=> H” means the flag is cleared after the TLE9221SX has changed over to BD_Normal mode.
“FB” stands for “Follow Bus” and means that depending on the signal on the FlexRay bus, the pins RxD and RxEN can either be “high” or “low”.

3) The wake-up flag stands for a detected wake-up event (compare with **Chapter 7.3** and **Table 10**).
The uV_{BAT} flag is the same as the uV_{BAT} undervoltage flag, which is set after the uV_{BAT} undervoltage detection timer expires (compare with **Chapter 8.3.1**).
The uV_{IO} flag is the same as the uV_{IO} undervoltage flag, which is set after the uV_{IO} undervoltage detection timer expires (compare with **Chapter 8.3.1**).
The uV_{CC} flag is the same as the uV_{CC} undervoltage flag, which is set after the uV_{CC} undervoltage detection timer expires (compare with **Chapter 8.3.1**).

4) The ERRN output indicates the wake-up flag, the wake-up source bit and the error bit (compare with **Table 9**). The error bit is set only by the undervoltage bits, such as the uV_{BAT} undervoltage bit (bit 8), the uV_{CC} undervoltage bit (bit 9) and the uV_{IO} undervoltage bit (bit 10). All other possible sources setting the error bit, such as, for example, a bus failure or an overtemperature event, are considered as not set in this table.

5) BD_Sleep mode entry flag disables the EN input pin when set to logical “low” (see **Chapter 9.4.1**)

6) The signal at the ERRN output pin depends on the host command applied and not on the current operating mode (compare with **Chapter 6.3**).

7) The signals at the RxD and RxEN outputs depend on the current operating mode, and are independent of the host command applied (compare with **Table 5**).

8) While TLE9221SX changes over to BD_Normal mode the wake-up flag is cleared. Moreover, the wake-up flag cannot be set in non-low power mode, and therefore, the wake-up flag is always “high” in BD_Normal mode (see **Chapter 7.3**).

9) Changing over to BD_Normal mode clears the SIR, including the undervoltage bits and therefore sets the ERRN output to “high” (compare with **Chapter 6.3.1**).
10) BD_Sleep mode was either entered by a host command or by setting the uV_{BAT} or uV_{IO} undervoltage flag (see **Table 15**).
11) If the host command BD_ReceiveOnly mode is applied, the ERRN output indicates the wake-up source bit (see **Table 9**).
12) This assumes no wake-up event was detected and the wake-up flag is cleared.
13) The BDSME flag is cleared, changeover to BD_Sleep mode was made by a host command (see **Chapter 9.4.1**).
14) The BDSME flag is set, changeover to BD_Sleep mode was made by setting one or more undervoltage flags (see **Chapter 9.4.1**).
15) In BD_Standby mode, only the uV_{CC} undervoltage flag could be active, since any other active undervoltage flag would change the mode of operation to BD_Sleep mode (compare with **Table 15**).
16) A wake-up flag could have been set by a wake-up event while the transceiver was in BD_Standby mode.

9.5 Operation Mode Changes by the Wake-up Flag

Setting the wake-up flag triggers a mode change to BD_Standby mode, regardless of the transceiver being in BD_Sleep mode or in the BD_GoToSleep command. While the transceiver TLE9221SX remains in BD_Standby mode, a wake-up event sets the wake-up bit and the wake-up flag. The wake-up flag is indicated at the ERRN, RxD and RxEN outputs. No mode change by the wake-up event is applied (for details see **Figure 37** and **Table 17**).

The wake-up flag can be set only in BD_Sleep mode, BD Standby mode or while the BD_GoToSleep command is being executed (for details see **"Wake-up Flag and Wake-up Bits" on Page 29**).

While the wake-up flag is active, the FlexRay transceiver TLE9221SX cannot change over to BD_Sleep mode again (see **Figure 34**). To reset the wake-up flag, either change the operating mode of the TLE9221SX to BD_Normal mode or read out the SIR.

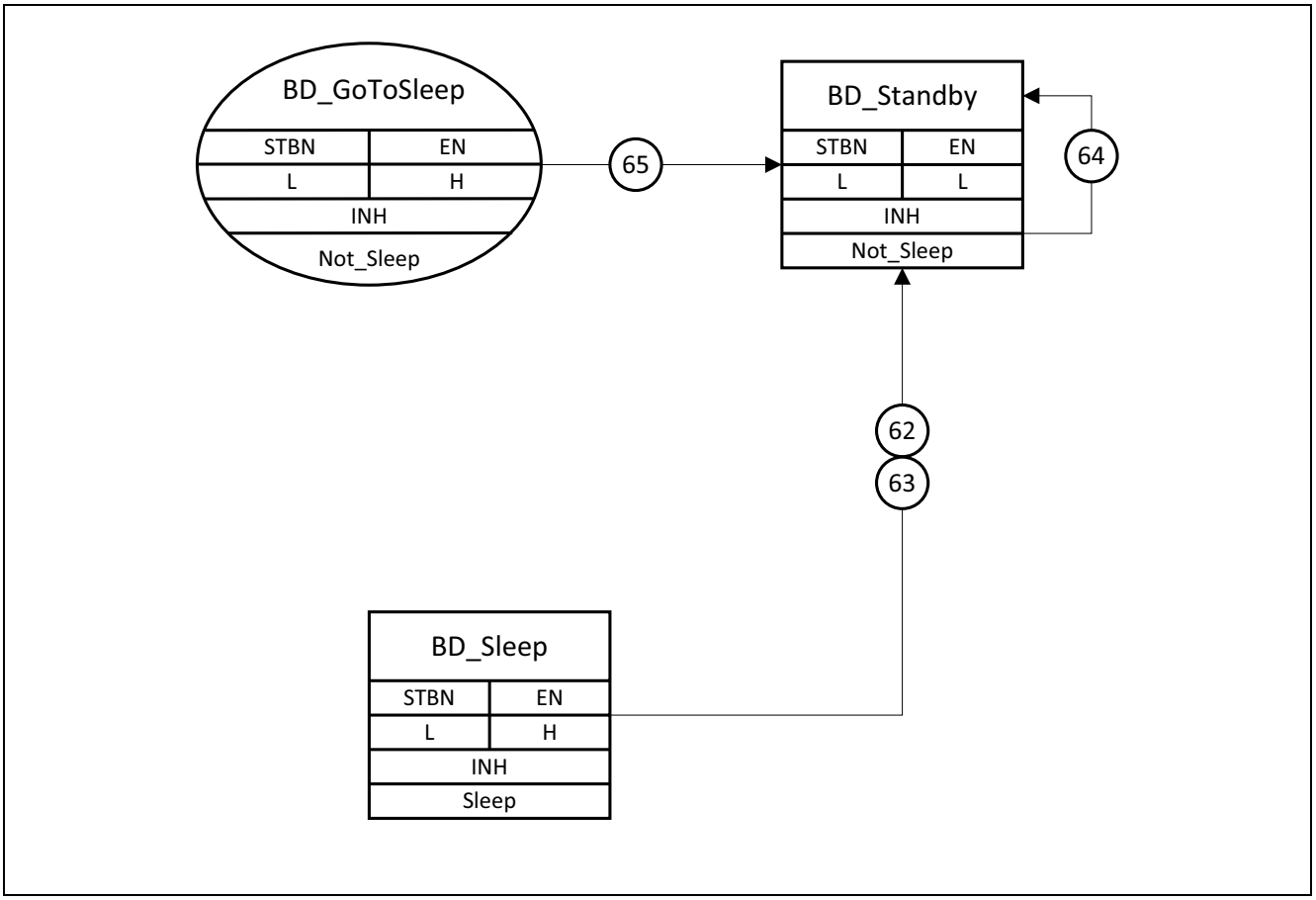


Figure 37 Operating mode change by wake-up flag

Setting the wake-up flag triggers not only a change in the operating mode, but also clears all undervoltage flags. The undervoltage bits available in the SIR remain active.

In case the undervoltage event remains present, setting the wake-up flag clears the undervoltage flag. The undervoltage detection timer is restarted and the undervoltage flag is set again when the undervoltage detection timer expires.

Note: Setting the wake-up flag clears only the undervoltage flag, not the undervoltage bit. The undervoltage bit remains active and is visible in the SIR.

Table 17 Mode changes by setting the wake-up flag [1) 2) 3) 4)]

No.	Primary Operating Mode	STBN	EN	Wake-up Flag	uV_{BAT} Flag	uV_{IO} Flag	uV_{CC} Flag	Secondary Operating Mode	ERRN[5)]	RxD[6)]	RxEN[6)]	INH	Remarks
BD_Sleep													
62	BD_Sleep	L	L	set “L”	2 => H	2 => H	2 => H	1 => BD_Standby	1 => L	1 => L	1 => L	1 => Not_Sleep	[7)]
63	BD_Sleep	L	H	set “L”	2 => H	2 => H	2 => H	1 => BD_Standby	1 => L	1 => L	1 => L	1 => Not_Sleep	[7)]
BD_Standby													
64	BD_Standby	L	L	set “L”	H	H	2 => H	BD_Standby	1 => L	1 => L	1 => L	Not_Sleep	[7), 8)]
BD_GoToSleep													
65	BD_GoToSleep	L	H	set “L”	2 => H	2 => H	2 => H	1 => BD_Standby	1 => L	1 => L	1 => L	1 => Not_Sleep	[7), 8)]

1) The table describes the states and signals of flags, operating modes and output pins. This table does not contain any timing information. Time for mode changes or the response time of the digital outputs are specified in the electrical characteristics (compare with **Table 22**).

2) All flags are “low” active. “L” means the flag is set. “X” = “don’t care”.
The color red stands for the event which triggered the mode transition.
For example: set “L” or set “H”.
The color blue stands for the consequence of the trigger event.
The numbers, “1 =>”, “2 =>” indicate the order of the consequences.
For example: “1=> BD_Normal” means the transceiver TLE9221SX changes over to BD_Normal mode.
“2=> H” means the flag is cleared after the TLE9221SX has changed over to BD_Normal mode.
“FB” stands for “Follow Bus” and means that depending on the signal on the FlexRay bus, the pins RxD and RxEN can either be “high” or “low”.

3) The wake-up flag stands for a detected wake-up event (compare with **Chapter 7.3** and **Table 10**).
The uV_{BAT} flag is the same as the uV_{BAT} undervoltage flag, which is set after the uV_{BAT} undervoltage detection timer expires (compare with **Chapter 8.3.1**).
The uV_{IO} flag is the same as the uV_{IO} undervoltage flag, which is set after the uV_{IO} undervoltage detection timer expires (compare with **Chapter 8.3.1**).
The uV_{CC} flag is the same as the uV_{CC} undervoltage flag, which is set after the uV_{CC} undervoltage detection timer expires (compare with **Chapter 8.3.1**).

4) The ERRN output indicates the wake-up flag, the wake-up source bit and the error bit (compare with **Table 9**). The error bit is set only by the undervoltage bits, such as the uV_{BAT} undervoltage bit (bit 8), the uV_{CC} undervoltage bit (bit 9) and the uV_{IO} undervoltage bit (bit 10). All other possible sources setting the error bit, such as, for example, a bus failure or an overtemperature event, are considered as not set in this table.

5) The signal at the ERRN output pin depends on the host command applied and not on the current operating mode (compare with **Chapter 6.3**).

6) The signals at the RxD and RxEN outputs depend on the current operation mode, and are independent of the host command applied (compare with **Table 5**).

7) Setting the wake-up flag also resets all undervoltage flags.
8) In BD_Standby mode, only the uV_{CC} undervoltage flag can be active (see **Table 15**).

10 Bus Error Indication

In case the TLE9221SX is not able to drive the correct data to the FlexRay bus, the transceiver sets the bus error bit (bit 4). The bus error bit indicates faulty data by setting the ERRN output to “low” (compare with **Table 9**). Therefore, three different detection mechanisms are implemented:

- uV_{CC} undervoltage detection
- RxD and TxD bit comparison
- Overcurrent detection

Just as any other SIR entry, the bus error bit is reset either by a SIR read-out or by changing over to BD_Normal mode (compare with **Chapter 6.3.1 “Reset the ERRN Output Pin”**).

Setting the bus error bit disables the Transmitter of the TLE9221SX in order to avoid corrupt data on the FlexRay bus. An active bus error bit does not trigger any change in the mode of operation.

10.1 Setting the Bus Error Bit by uV_{CC} Undervoltage

The Transmitter of the TLE9221SX is fed by the power supply uV_{CC} (compare with **Figure 2**). In case uV_{CC} is in undervoltage condition, the TLE9221SX cannot drive the correct bus levels to the FlexRay bus. Therefore, the transceiver sets the uV_{CC} undervoltage bit together with the bus error bit and the error bit.
In BD_Normal mode, the active uV_{CC} undervoltage bit and the active bus error bit disable the Transmitter. The uV_{CC} undervoltage bit starts the uV_{CC} undervoltage timer and if the timer expires, the undervoltage flag is set and a mode changeover is initiated (see also **Chapter 8.3.3 “Undervoltage Event at uVCC”**).

10.2 Setting the Bus Error Bit by RxD and TxD Comparison

The transceiver TLE9221SX compares the digital input signal at TxD with the signal received from the FlexRay bus at the RxD output. If the data transmit signal at the TxD input is different from the signal received at the RxD output, the TLE9221SX sets the bus error bit.

The RxD to TxD bit comparison is active only, when the transceiver TLE9221SX is in BD_Normal mode and the Transmitter is active (TxEN = “low”; BGE = “high”). Both, the rising and the falling edge at the TxD input signal trigger an internal comparator to compare the TxD signal with the RxD signal. The results are stored in an internal error counter. When the internal error counter exceeds 10 reported comparison failures, the bus error bit is set.

The error counter is reset when the Transmitter is reset.

10.3 Setting the Bus Error Bit by Overcurrent Detection

Four different current sensors monitor the output current and the input current at the pins BP and BM. In case the TLE9221SX detects an overcurrent caused by a bus short-circuit either to GND or to one of the power supplies, the TLE9221SX sets the bus error bit.

11 Overtemperature Protection

The Transmitter of TLE9221SX is protected against overheating with an internal temperature sensor (compare with **Figure 4**). The temperature sensor provides two temperature thresholds: $T_{J(Warning)}$ and $T_{J(Shut\_Down)}$. On exceeding the lower threshold $T_{J(Warning)}$, the transceiver sets the overtemperature warning bit (bit 6), indicating a “high” temperature situation. On exceeding the upper threshold $T_{J(Shut\_Down)}$, the transceiver TLE9221SX sets the overtemperature shut down bit (bit 5), indicating a critical temperature situation. On reaching the $T_{J(Shut\_Down)}$ threshold, the transceiver TLE9221SX also disables the Transmitter (see **Figure 38**). The overtemperature detection of the Transmitter is active only in BD_Normal mode. An overtemperature detection event does not trigger any change in the operating mode.

Both bits, the overtemperature shut down bit and the overtemperature warning bit set the error bit (bit 11) in the SIR. The error bit is indicated at the ERRN output (compare with **Chapter 6.3 “Status Information at the ERRN Output Pin”**).

The Transmitter can be enabled again after an overtemperature event by clearing the SIR (see also **Chapter 6.2.3 “Clearing Sequence of SIR”**).

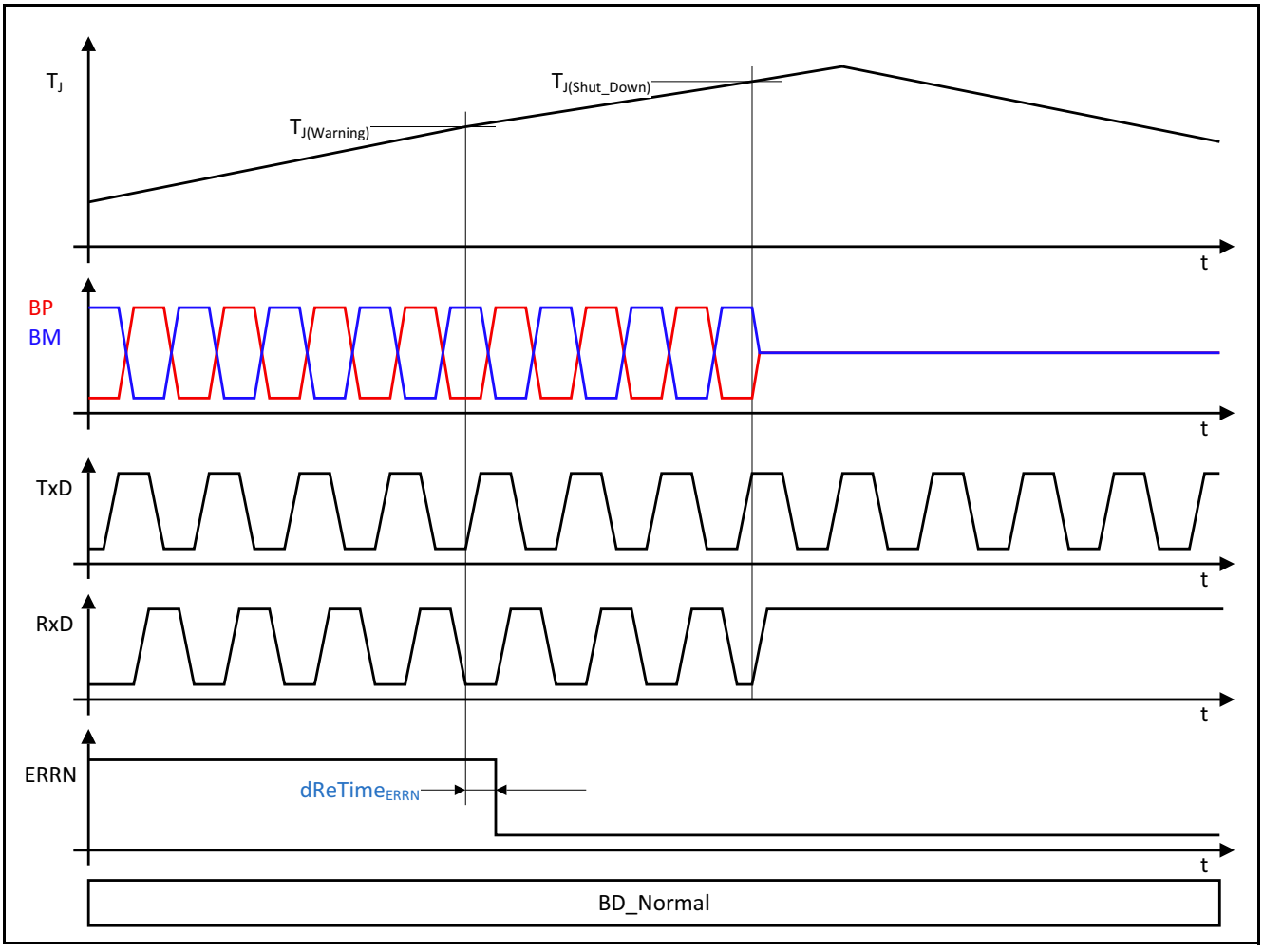


Figure 38 Overtemperature protection

12 Transmitter Time-out

To ensure that an active Transmitter blocks the FlexRay bus permanently, a time-out function is implemented within the TLE9221SX. In case the Transmitter is active for the time period t > dBDTxActiveMax, the Transmitter will be disabled automatically (see **Figure 39**). The Transmitter time-out sets the Transmitter time-out bit (bit 7) in the SIR and also the error bit. In BD_Normal mode, the Transmitter time-out is indicated at the ERRN output by a logical “low” signal. To reset the TxEN or BGE time-out, either change over again to BD_Normal mode or read out the SIR (see **Chapter 6.3.1 “Reset the ERRN Output Pin”**).

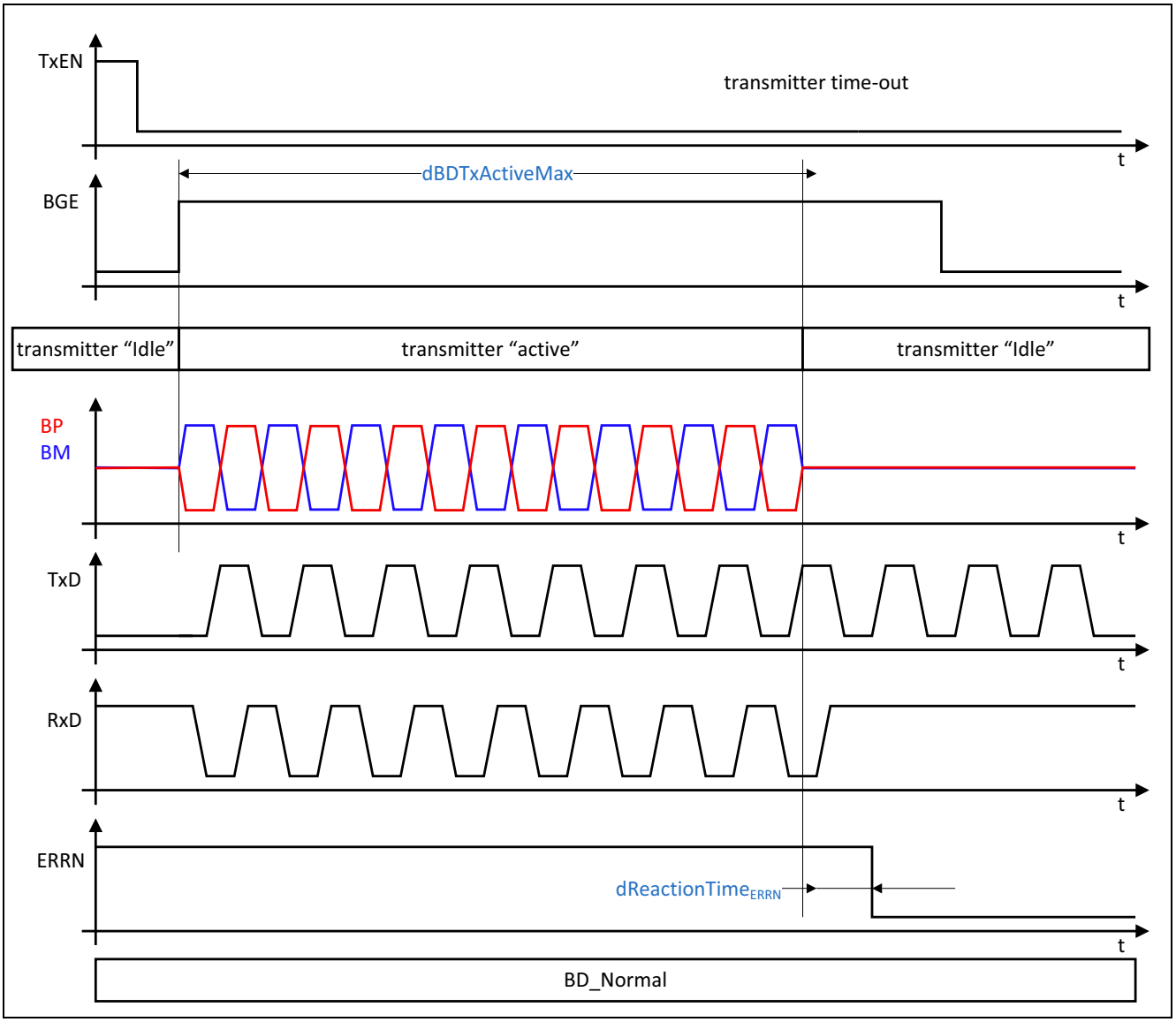


Figure 39 Transmitter time-out function

13 Mode Indication, Power-up and Parity Information

13.1 Power-up Bit

After switching on the power supplies uV_{CC} and uV_{BAT}, the FlexRay transceiver TLE9221SX sets the power-up bit (bit 3) in the SIR. The power-up bit is visible only by reading out the SIR and will be reset by clearing the SIR (see **Chapter 6.2.3 “Clearing Sequence of SIR”**).

13.2 Mode Indication Bit EN and Mode Indication Bit STBN

Two bits in the SIR are reserved for the indication of the operating mode. The SIR indicates the current mode of operation, regardless of whether the mode is selected via host command, undervoltage flag or wake-up flag. The mode indication bits have the same order as the host commands. Bit 13 of the SIR reflects the related host command at the EN pin of the actual mode of operation and bit 14 indicates the related host command at the STBN pin (compare with **Table 18**).

Table 18 Mode indication bits

Mode of Operation	Mode Indication Bit EN (bit 13)	Mode Indication Bit STBN (bit 14)
BD_Normal	“high”	“high”
BD_ReceiveOnly	“low”	“high”
BD_Standby	“low”	“low”
BD_Sleep	no read-out possible	no read-out possible
BD_GoToSleep	no read-out possible	no read-out possible

13.3 Even Parity Bit

The even parity bit (bit 15) can be used to check the transmission of the SIR. The even parity bit is set to logical “low” if the sum of all status bits is even, and it is logical “high” if the sum of all status bits is odd.

14 General Product Characteristics

14.1 Absolute Maximum Ratings

Table 19 Absolute maximum ratings voltages, currents and temperatures[1)]

All voltages with respect to ground; positive current flowing into the pin;
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage battery	uVBAT	-0.3	–	40	V	–	P_14.1.1
Supply voltage V_{CC}	uVCC	-0.3	–	6.0	V	–	P_14.1.2
Supply voltage V_{IO}	uVIO	-0.3	–	6.0	V	–	P_14.1.3
DC voltage versus GND on the pin BP	uBP	-40	–	40	V	–	P_14.1.4
DC voltage versus GND on the pin BM	uBM	-40	–	40	V	–	P_14.1.5
DC voltage versus GND on the pin INH	uINH	-0.3	–	uV_{BAT} + 0.3	V	–	P_14.1.6
DC voltage versus GND on the pin WAKE	uWAKE	-27	–	uV_{BAT} + 0.3	V	–	P_14.1.7
DC voltage versus GND on the pin STBN	uVSTBN	-0.3	–	V_{IO}	V	–	P_14.1.8
DC voltage versus GND on the pin EN	uVEN	-0.3	–	V_{IO}	V	–	P_14.1.9
DC voltage versus GND on the pin TxD	uVTxD	-0.3	–	V_{IO}	V	–	P_14.1.10
DC voltage versus GND on the pin TxEN	uVTxEN	-0.3	–	V_{IO}	V	–	P_14.1.11
DC voltage versus GND on the pin BGE	uVBGE	-0.3	–	V_{IO}	V	–	P_14.1.12
DC voltage versus GND on the pin RxD	uVRxD	-0.3	–	V_{IO}	V	–	P_14.1.13
DC voltage versus GND on the pin RxEN	uVRxEN	-0.3	–	V_{IO}	V	–	P_14.1.14
DC voltage versus GND on the pin ERRN	uVERRN	-0.3	–	V_{IO}	V	–	P_14.1.15
Currents							
Output current on the pin INH	iINH	-1	–	–	mA	–	P_14.1.16
Output current on the pin RxD	iRxD	-40	–	40	mA	–	P_14.1.17

Table 19 Absolute maximum ratings voltages, currents and temperatures[1)] (cont'd)

All voltages with respect to ground; positive current flowing into the pin;
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output current on the pin RxEN	iRxEN	-40	–	40	mA	–	P_14.1.18
Output Current on the pin ERRN	iERRN	-40	–	40	mA	–	P_14.1.19
Temperatures							
Junction temperature	TJunction	-40	–	150	°C	–	P_14.1.20
Storage temperature	TS	- 55	–	150	°C	–	P_14.1.21
ESD Immunity							
ESD immunity at BP, BM, V_{BAT}, WAKE versus GND	uESDEXT	-10	–	10	kV	HBM, (100 pF via 1.5 kΩ), [2)];	P_14.1.22
ESD immunity at all other pins	uESDINT	-2	–	2	kV	HBM, (100 pF via 1.5 kΩ), [2)];	P_14.1.23
ESD immunity to GND (all pins)	uESDCDM	-750	–	750	V	CDM, [3)];	P_14.1.24

1) Not subject to production test, specified by design.
2) ESD susceptibility, Human Body Model "HBM" according to ANSI/ESDA/JEDEC JS-001.
3) ESD susceptibility, Charged Device Model "CDM" according to EIA/JESD22-C101 or ESDA STM5.3.1

Note: Stresses beyond those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" the normal-operating range. Protection functions are not designed for continuous repetitive operation.

14.2 Functional Range

Table 20 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Transceiver supply voltage V_{BAT}	uV_{BAT}	5.5	–	18	V	1);	P_14.2.1
Transceiver supply voltage V_{BAT} extended supply range	uV_{BAT_EXT}	18	–	40	V	60 s, 2), 3);	P_14.2.2
Transceiver supply voltage V_{CC}	uV_{CC}	4.75	–	5.25	V	–	P_14.2.3
Transceiver supply voltage V_{IO}	uV_{IO}	3.0	–	5.25	V	–	P_14.2.4
Functional range V_{BAT} including local and remote wake-up functions	uV_{BAT_WAKE}	5.5	–	18	V	1);	P_14.2.5
Thermal Parameters							
Junction temperature	$T_{Junction}$	-40	–	150	°C	–	P_14.2.6

1) The TLE9221SX is fully functional, including the wake-up functions, in the specified uV_{BAT} range while uV_{CC} and uV_{IO} are also in their operating range.
2) Not subject to production test, specified by design
3) The extended supply range covers the load requirements according to ISO 16750-2 (load dump, jump start). This range is not qualified for continuous, repetitive operation.

Note: Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

14.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, please visit **www.jedec.org**.*

Table 21 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal Resistance							
Junction to ambient[1)]	R_{thJA}	–	100	–	K/W	[2)]	P_14.3.1
Thermal Shutdown Junction Temperature							
Thermal warning temperature	$T_{J(Warning)}$	150	160	170	°C	–	P_14.3.2
Thermal shut-down temperature	$T_{J(Shut\_Down)}$	170	180	190	°C	–	P_14.3.3
Temperature difference between warning temperature and shut-down temperature $\Delta T = T_{J(Shut\_Down)} - T_{J(Warning)}$	ΔT	10	20	25	°C	–	P_14.3.4

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The product (TLE9221SX) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu)

15 Electrical Characteristics

15.1 Functional Device Characteristics

Table 22 Electrical characteristics

5.5 V < uV_{BAT} < 18 V; 3.0 V < uV_{IO} < 5.25 V; 4.75 V < uV_{CC} < 5.25 V; R_{DCLOAD} = 45 Ω; C_{DCLOAD} = 100 pF;
-40 °C < $T_{Junction}$ < 150 °C;
All voltages with respect to ground; positive current flowing into the pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption uV_{BAT} Power Supply							
Current consumption uV_{BAT}, non-low power mode	iV_{BAT}	–	5.5	6.5	mA	BD_Normal, BD_ReceiveOnly, open load on INH, uV_{BAT} = 13.5 V;	P_15.1.1
Current consumption uV_{BAT} BD_Sleep	$iV_{BAT\_Sleep40}$	–	45	65	µA	uV_{BAT} = 13.5 V, uINH1 = 0 V, EN = “low”, STBN = “low”, $T_{Junction}$ = 40° C, uBDWake = 0 V;	P_15.1.4
Current consumption uV_{BAT} BD_Standby	iV_{BAT_Stb}	–	70	180	µA	uV_{BAT} = 13.5 V, open load on INH, uBDWake = 0 V;	P_15.1.5
Current Consumption uV_{CC} Power Supply							
Current consumption uV_{CC} BD_Normal	iV_{CC}	–	25	40	mA	Transmitter = “Data_0” or “Data 1”;	P_15.1.10
Current consumption uV_{CC} BD_Normal	$iV_{CC\_Tx\_Idle}$	–	0.07	1	mA	Transmitter = “Idle”, uV_{BAT} = 13.5 V;	P_15.1.11
Current consumption uV_{CC} BD_ReceiveOnly	iV_{CC_ROM}	–	0.05	0.5	mA	uV_{BAT} = 13.5 V;	P_15.1.12
Current consumption uV_{CC}BD_Sleep	$iV_{CC\_Sleep40}$	–	0.5	2	µA	uV_{CC} = 5 V, uV_{BAT} = 13.5 V, $T_{Junction}$ = 40°C;	P_15.1.15
Current consumption uV_{CC}BD_Standby	iV_{CC_Stb}	–	2	8	µA	uV_{CC} = 5 V, uV_{BAT} = 13.5 V;	P_15.1.16

Table 22 Electrical characteristics (cont'd)

5.5 V < uV_{BAT} < 18 V; 3.0 V < uV_{IO} < 5.25 V; 4.75 V < uV_{CC} < 5.25 V; R_{DCLOAD} = 45 Ω; C_{DCLOAD} = 100 pF;
-40 °C < $T_{Junction}$ < 150 °C;
All voltages with respect to ground; positive current flowing into the pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption uV_{IO} Power Supply							
Current consumption uV_{IO}, non-low power mode	iV_{IO}	–	0.15	0.5	mA	BD_Normal, BD_ReceiveOnly;	P_15.1.20
Current consumption uV_{IO} BD_Sleep	$iV_{IO\_Sleep40}$	–	2	3	µA	uV_{IO} = 5 V, TxEN = uV_{IO}, BGE = TxD = "low", $T_{Junction}$ = 40 °C;	P_15.1.23
Current consumption uV_{IO} BD_Standby	iV_{IO_Stb}	–	2	40	µA	uV_{IO} = 5 V, TxEN = uV_{IO}, BGE = TxD = "low";	P_15.1.24

Table 22 Electrical characteristics (cont'd)

5.5 V < uV_{BAT} < 18 V; 3.0 V < uV_{IO} < 5.25 V; 4.75 V < uV_{CC} < 5.25 V; R_{DCLOAD} = 45 Ω; C_{DCLOAD} = 100 pF;
-40 °C < $T_{Junction}$ < 150 °C;
All voltages with respect to ground; positive current flowing into the pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Undervoltage Detection uV_{BAT} Power Supply							
Undervoltage detection threshold uV_{BAT}	$uBDUVV_{BAT}$	4.0	4.8	5.5	V	falling edge;	P_15.1.30
Undervoltage detection hysteresis uV_{BAT}	$uBDUVV_{BAT\_Hys}$	–	100	–	mV	1);	P_15.1.31
Power-down threshold uV_{BAT}	$uBDPDV_{BAT}$	2.0	2.8	3.5	V	1);	P_15.1.32
V_{Bat} undervoltage filter time	$dBDUVV_{BAT\_Blk}$	50	–	500	µs	1), uV_{BAT} = 13.5 V to $uBDUVV_{BAT}$(min), (see **Figure 26**);	P_15.1.33
Response time for uV_{BAT} undervoltage detection	$dBDUVV_{BAT}$	–	550	650	ms	1), (see **Figure 26**);	P_15.1.35
Response time for uV_{BAT} undervoltage recovery	$dBDRV_{BAT}$	–	6	10	ms	1), (see **Figure 26**);	P_15.1.36
Undervoltage Detection uV_{CC} Power Supply							
Undervoltage detection threshold uV_{CC}	$uBDUVV_{CC}$	4.0	4.25	4.75	V	falling edge;	P_15.1.40
Undervoltage detection hysteresis uV_{CC}	$uBDUVV_{CC\_Hys}$	–	100	–	mV	1);	P_15.1.41
Power-down threshold uV_{CC}	$uBDPDV_{CC}$	1.5	2.25	3.5	V	1);	P_15.1.42
uV_{CC} undervoltage filter time	$dBDUVV_{CC\_Blk}$	3	–	25	µs	uV_{CC} = 4.75 V to $uBDUVV_{CC}$(min), (see **Figure 27**);	P_15.1.43
Response time for uV_{CC} undervoltage detection	$dBDUVV_{CC}$	–	550	650	ms	1), (see **Figure 27**);	P_15.1.45
Response time for uV_{CC} undervoltage recovery	$dBDRV_{CC}$	–	6	10	ms	1), (see **Figure 27**);	P_15.1.46

Table 22 Electrical characteristics (cont'd)

5.5 V < uV_{BAT} < 18 V; 3.0 V < uV_{IO} < 5.25 V; 4.75 V < uV_{CC} < 5.25 V; R_{DCLOAD} = 45 Ω; C_{DCLOAD} = 100 pF;
-40 °C < $T_{Junction}$ < 150 °C;
All voltages with respect to ground; positive current flowing into the pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Undervoltage Detection uV_{IO} Power Supply							
Undervoltage detection threshold uV_{IO}	uUV_{IO}	2.0	2.65	3.0	V	falling edge;	P_15.1.50
Undervoltage detection hysteresis uV_{IO}	uUV_{IO_Hys}	–	50	–	mV	[1];	P_15.1.51
uV_{IO} undervoltage filter time	$dBDUVV_{IO\_Blk}$	3	–	25	µs	uV_{IO} = 3 V to $uBDUVV_{IO}$(min), (see **Figure 28**);	P_15.1.52
Response time for uV_{IO} undervoltage detection	$dBDUVV_{IO}$	–	550	650	ms	[1], (see **Figure 28**);	P_15.1.54
Response time for uV_{IO} undervoltage recovery	$dBDRV_{IO}$	–	6	10	ms	[1], (see **Figure 28**);	P_15.1.55

Table 22 Electrical characteristics (cont'd)

5.5 V < uV_{BAT} < 18 V; 3.0 V < uV_{IO} < 5.25 V; 4.75 V < uV_{CC} < 5.25 V; R_{DCLOAD} = 45 Ω; C_{DCLOAD} = 100 pF;
-40 °C < $T_{Junction}$ < 150 °C;
All voltages with respect to ground; positive current flowing into the pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Digital Output RxD							
"high" level output voltage	$uV_{Dig\_Out\_High\_RxD}$	0.8 x uV_{IO}	–	1.0 x uV_{IO}	V	$iRxD_H$ = - 2 mA, [2];	P_15.1.60
"low" level output voltage	$uV_{Dig\_Out\_Low\_RxD}$	–	–	0.2 x uV_{IO}	V	$iRxD_L$ = 2 mA, [2];	P_15.1.61
Output voltage, uV_{IO} undervoltage	$uV_{Dig\_Out\_UV\_RxD}$	–	–	250	mV	R_BDRxD = 100 kΩ, [3];	P_15.1.62
Output voltage, BD_Off state	$uV_{Dig\_Out\_OFF\_RxD}$	–	–	100	mV	R_BDRxD = 100 kΩ, [4];	P_15.1.63
Rise time, 15 pF load	$dBDRxD_{R15}$	–	1	4	ns	[1], 20% - 80% of uV_{IO}, C_BDRxD = 15 pF;	P_15.1.64
Fall time, 15 pF load	$dBDRxD_{F15}$	–	1	4	ns	[1], 80% - 20% of uV_{IO}, C_BDRxD = 15 pF;	P_15.1.65
Rise time, 25 pF load	$dBDRxD_{R25}$	–	2	6	ns	20% - 80% of uV_{IO}, C_BDRxD = 25 pF;	P_15.1.66
Fall time, 25 pF load	$dBDRxD_{F25}$	–	2	6	ns	80% - 20% of uV_{IO}, C_BDRxD = 25 pF;	P_15.1.67
Sum of rise and fall time, 15 pF load	$dBDRxD_{R15}$ + $dBDRxD_{F15}$	–	2	8	ns	[1], C_BDRxD = 15 pF;	P_15.1.68
Difference of rise and fall time, 15 pF load	$\lvert dBDRxD_{R15} - dBDRxD_{F15} \rvert$	–	0.5	2.5	ns	[1], C_BDRxD = 15 pF;	P_15.1.69
Sum of rise and fall time, 25 pF load	$dBDRxD_{R25}$ + $dBDRxD_{F25}$	–	4	12	ns	C_BDRxD = 25 pF;	P_15.1.70
Difference of rise and fall time, 25 pF load	$\lvert dBDRxD_{R25} - dBDRxD_{F25} \rvert$	–	0.5	2.5	ns	C_BDRxD = 25 pF;	P_15.1.71
Digital Output RxEN							
"high" level output voltage	$uV_{Dig\_Out\_High\_RxEN}$	0.8 x uV_{IO}	–	1.0 x uV_{IO}	V	$iRxD_H$ = - 2 mA, [2];	P_15.1.80
"low" level output voltage	$uV_{Dig\_Out\_Low\_RxEN}$	–	–	0.2 x uV_{IO}	V	$iRxD_L$ = 2 mA, [2];	P_15.1.81
Output voltage, uV_{IO} undervoltage	$uV_{Dig\_Out\_UV\_RxEN}$	–	–	250	mV	R_BDRxEN = 100 kΩ, [3];	P_15.1.82
Output voltage, BD_Off state	$uV_{Dig\_Out\_OFF\_RxEN}$	–	–	100	mV	R_BDRxEN = 100 kΩ, [4];	P_15.1.83

Table 22 Electrical characteristics (cont'd)

5.5 V < uV_{BAT} < 18 V; 3.0 V < uV_{IO} < 5.25 V; 4.75 V < uV_{CC} < 5.25 V; R_{DCLOAD} = 45 Ω; C_{DCLOAD} = 100 pF;
-40 °C < $T_{Junction}$ < 150 °C;
All voltages with respect to ground; positive current flowing into the pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Rise time, 25 pF load	$dBDRxEN_{R25}$	–	2	6	ns	[1], 20% - 80% of uV_{IO}, C_BDRxEN = 25 pF;	P_15.1.84
Fall time, 25 pF load	$dBDRxEN_{F25}$	–	2	6	ns	[1], 80% - 20% of uV_{IO}, C_BDRxEN = 25 pF;	P_15.1.85

Table 22 Electrical characteristics (cont'd)

5.5 V < uV_{BAT} < 18 V; 3.0 V < uV_{IO} < 5.25 V; 4.75 V < uV_{CC} < 5.25 V; R_{DCLOAD} = 45 Ω; C_{DCLOAD} = 100 pF;
-40 °C < $T_{Junction}$ < 150 °C;
All voltages with respect to ground; positive current flowing into the pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Digital Output ERRN							
"high" level output voltage	$uV_{Dig\_Out\_High\_ERRN}$	0.8 x uV_{IO}	–	1.0 x uV_{IO}	V	$iERRN_H$ = - 2 mA, [2];	P_15.1.90
"low" level output voltage	$uV_{Dig\_Out\_Low\_ERRN}$	–	–	0.2 x uV_{IO}	V	$iERRN_L$ = 2 mA, [2];	P_15.1.91
Output voltage, uV_{IO} undervoltage	$uV_{Dig\_Out\_UV\_ERRN}$	–	–	250	mV	R_BDERRN = 100 kΩ, [3];	P_15.1.92
Output voltage, BD_Off state	$uV_{Dig\_Out\_OFF\_ERRN}$	–	–	100	mV	R_BDERRN = 100 kΩ, [4];	P_15.1.93
Rise time, 25 pF load	$dBDERRN_{R25}$	–	2	6	ns	[1], 20% - 80% of uV_{IO}, C_BDERRN = 25 pF;	P_15.1.94
Fall time, 25 pF load	$dBDERRN_{F25}$	–	2	6	ns	[1], 80% - 20% of uV_{IO}, C_BDERRN = 25 pF;	P_15.1.95
Response time	$dReaction\ Time_{ERRN}$	–	–	100	µs	[1], (see **Figure 13**);	P_15.1.96
Digital Input TxD							
"high" level input voltage	uBDLogic_1	0.6 x uV_{IO}	–	uV_{IO}	V	[2];	P_15.1.100
"low" level input voltage	uBDLogic_0	-0.3	–	0.4 x uV_{IO}	V	[2];	P_15.1.101
"high" level input current	iBDLogic_1	20		200	µA	–	P_15.1.102
"low" level input current	iBDLogic_0	–	–	1	µA	[1];	P_15.1.103
Input capacitance	C_BDTxD	–	–	5	pF	[1];	P_15.1.104

Table 22 Electrical characteristics (cont'd)

5.5 V < uV_{BAT} < 18 V; 3.0 V < uV_{IO} < 5.25 V; 4.75 V < uV_{CC} < 5.25 V; R_{DCLOAD} = 45 Ω; C_{DCLOAD} = 100 pF;
-40 °C < $T_{Junction}$ < 150 °C;
All voltages with respect to ground; positive current flowing into the pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Digital Input BGE							
"high" level input voltage	$uV_{Dig\_In\_High\_BGE}$	0.7 x uV_{IO}	–	uV_{IO}	V	[2];	P_15.1.110
"low" level input voltage	$uV_{Dig\_In\_Low\_BGE}$	-0.3	–	0.3 x uV_{IO}	V	[2];	P_15.1.111
"high" level input current	$i_{Dig\_In\_High\_BGE}$	20		200	µA	–	P_15.1.112
"low" level input current	$i_{Dig\_In\_Low\_BGE}$	-1	–	1	µA	–[1]	P_15.1.113
Input capacitance	C_BDBGE	–	–	5	pF	[1]	P_15.1.114
Digital Input STBN							
"high" level input voltage	$uV_{Dig\_In\_High\_STBN}$	0.7 x uV_{IO}	–	uV_{IO}	V	[2];	P_15.1.120
"low" level input voltage	$uV_{Dig\_In\_Low\_STBN}$	-0.3	–	0.3 x uV_{IO}	V	[2];	P_15.1.121
"high" level input current	$i_{Dig\_In\_High\_STBN}$	20		200	µA	–	P_15.1.122
"low" level input current	$i_{Dig\_In\_Low\_STBN}$	-1	–	1	µA	[1]	P_15.1.123
Input capacitance	C_BDSTBN	–	–	5	pF	[1]	P_15.1.124
Digital Input EN							
"high" level input voltage	$uV_{Dig\_In\_High\_EN}$	0.7 x uV_{IO}	–	uV_{IO}	V	[2];	P_15.1.130
"low" level input voltage	$uV_{Dig\_In\_Low\_EN}$	-0.3	–	0.3 x uV_{IO}	V	[2];	P_15.1.131
"high" level input current	$i_{Dig\_In\_High\_EN}$	20		200	µA	–	P_15.1.132
"low" level input current	$i_{Dig\_In\_Low\_EN}$	-1	–	1	µA	[1]	P_15.1.133
Input capacitance	C_BDEN	–	–	5	pF	[1]	P_15.1.134

Table 22 Electrical characteristics (cont'd)

5.5 V < uV_{BAT} < 18 V; 3.0 V < uV_{IO} < 5.25 V; 4.75 V < uV_{CC} < 5.25 V; R_{DCLOAD} = 45 Ω; C_{DCLOAD} = 100 pF;
-40 °C < $T_{Junction}$ < 150 °C;
All voltages with respect to ground; positive current flowing into the pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Tx Enable Input: TxEN							
"high" level input voltage	$uV_{Dig\_In\_High\_TxEN}$	0.7 x uV_{IO}	–	uV_{IO}	V	2);	P_15.1.140
"low" level input voltage	$uV_{Dig\_In\_Low\_TxEN}$	-0.3	–	0.3 x uV_{IO}	V	2);	P_15.1.141
"high" level input current	$i_{Dig\_In\_High\_TxEN}$	-1	–	1	µA	1);	P_15.1.142
"low" level input current	$i_{Dig\_In\_Low\_TxEN}$	-200	–	-20	µA	–	P_15.1.143
Input capacitance	C_BDTxEN	–	–	5	pF	1);	P_15.1.144
Maximum time of Transmitter activation via TxEN	dBDTxActive Max	1500	–	2600	µs	–	P_15.1.145

Table 22 Electrical characteristics (cont'd)

5.5 V < uV_{BAT} < 18 V; 3.0 V < uV_{IO} < 5.25 V; 4.75 V < uV_{CC} < 5.25 V; R_{DCLOAD} = 45 Ω; C_{DCLOAD} = 100 pF;
-40 °C < $T_{Junction}$ < 150 °C;
All voltages with respect to ground; positive current flowing into the pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Analog Output INH							
Output voltage; Not_Sleep	$uINH1_{Not-Sleep}$	uV_{BAT} - 0.8	–	–	V	iINH1 = -0.2 mA, uV_{BAT} > 5.5 V;	P_15.1.150
Absolute leakage current; BD_Sleep	$\|iINH1_{Leak}\|$	–	–	5	µA	uINH1 = 0 V;	P_15.1.151
Local Wake-up Input WAKE							
Wake-up detection threshold	$uBDWake_{Thr}$	0.35 x uV_{BAT}	0.5 x uV_{BAT}	0.65 x uV_{BAT}	V	–	P_15.1.160
Hysteresis on pin Wake	$uBDWake_{Hys}$	0.01 x uV_{BAT}	0.04 x uV_{BAT}	0.12 x uV_{BAT}	V	–	P_15.1.161
High level input current (pull-up)	$iBDWake_{H}$	-20	-9	-2	µA	uBDWAKE = $uBDWake_{Thr}$ + 50 mV, (see **Figure 14**), [5];	P_15.1.162
Low level input current (pull-down)	$iBDWake_{L}$	2	9	20	µA	uBDWAKE = $uBDWake_{Thr}$ - 50 mV, (see **Figure 14**), [5];	P_15.1.163
Wake pulse filter time	dBDWake PulseFilter	10	–	40	µs	(see **Figure 16**);	P_15.1.164
Response time to indicate the wake-up	$dBDWakeup Reaction_{local}$	–	–	100	µs	(see **Figure 16**);	P_15.1.165

Table 22 Electrical characteristics (cont'd)

5.5 V < uV_{BAT} < 18 V; 3.0 V < uV_{IO} < 5.25 V; 4.75 V < uV_{CC} < 5.25 V; R_{DCLOAD} = 45 Ω; C_{DCLOAD} = 100 pF;
-40 °C < $T_{Junction}$ < 150 °C;
All voltages with respect to ground; positive current flowing into the pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Bus Transmitter: BP, BM							
Differential output voltage; ("Data_0", "Data_1"), BD_Normal	$uBDTx_{active}$	0.6	–	2.0	V	40 Ω < R_{DCLOAD} < 55 Ω, [6];	P_15.1.170
Differential output voltage; "Data_0", BD_Normal	$uBDTx_{active\_D0}$	-2.0	–	-0.6	V	TxD = "low", TxEN = "low", 40 Ω < R_{DCLOAD} < 55 Ω;	P_15.1.171
Matching between differential output voltages at "Data_0" and "Data_1"	$uBDTx_{active\_Diff}$	-200	–	200	mV	BD_Normal, TxEN = "low", 40 Ω < R_{DCLOAD} < 55 Ω, $uBDTx_{active\_Diff}$ = $uBDTx_{active}$ - $uBDTx_{active\_D0}$;	P_15.1.172
BP absolute maximum output current, BP shorted to GND, no time limit	$iBP_{GNDShortMax}$	–	22	60	mA	–	P_15.1.180
BP absolute maximum output current, BP shorted to = -5 V, no time limit	$iBP_{-5VShortMax}$	–	43	60	mA	–	P_15.1.181
BP absolute maximum output current, BP shorted to = 27 V, no time limit	$iBP_{BAT27ShortMax}$	–	37	60	mA	–	P_15.1.182
BP absolute maximum output current, Short to BM	$iBP_{BMShortMax}$	–	30	60	mA	–	P_15.1.183
BM absolute maximum output current, BM shorted to GND, no time limit	$iBM_{GNDShortMax}$	–	22	60	mA	–	P_15.1.184
BM absolute maximum output current, BM shorted to = -5 V, no time limit	$iBM_{-5VShortMax}$	–	43	60	mA	–	P_15.1.185
BM absolute maximum output current, BM shorted to = 27 V, no time limit	$iBM_{BAT27ShortMax}$	–	37	60	mA	–	P_15.1.186

Table 22 Electrical characteristics (cont'd)

5.5 V < uV_{BAT} < 18 V; 3.0 V < uV_{IO} < 5.25 V; 4.75 V < uV_{CC} < 5.25 V; R_{DCLOAD} = 45 Ω; C_{DCLOAD} = 100 pF;
-40 °C < $T_{Junction}$ < 150 °C;
All voltages with respect to ground; positive current flowing into the pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
BM absolute maximum output current, Short to BP	$iBM_{BPShortMax}$	–	30	60	mA	–	P_15.1.187
Transmitter delay negative voltage	dBDTx10	–	31	50	ns	R_{DCLOAD} = 40 Ω, [6], [7], (see **Figure 41**);	P_15.1.200
Transmitter delay positive voltage	dBDTx01	–	31	50	ns	R_{DCLOAD} = 40 Ω, [6], [7], (see **Figure 41**);	P_15.1.201
Transmitter delay mismatch dBDTxAsym = |dBDTx10 -dBDTx01|	dBDTxAsym	–	–	4	ns	R_{DCLOAD} = 40 Ω, [6], [7], [8], (see **Figure 41**);	P_15.1.203
Fall time differential bus voltage, (80% -> 20%)	dBusTx10	6	12	18.75	ns	R_{DCLOAD} = 40 Ω, [6], (see **Figure 41**);	P_15.1.204
Rise time differential bus voltage, (20% -> 80%)	dBusTx01	6	12	18.75	ns	R_{DCLOAD} = 40 Ω, [6], (see **Figure 41**);	P_15.1.205
Difference between differential bus voltage rise time and fall time dBusTxDiff= |dBusTx01 - dBusTx10|	dBusTxDiff	–	–	3	ns	R_{DCLOAD} = 40 Ω, (see **Figure 41**);	P_15.1.206
Transmitter delay Idle -> active	dBDTxia	–	55	75	ns	R_{DCLOAD} = 40 Ω, (see **Figure 42**);	P_15.1.210
Transmitter delay Active -> idle	dBDTxai	–	55	75	ns	R_{DCLOAD} = 40 Ω, (see **Figure 42**);	P_15.1.211
Transmitter delay mismatch dBDTxDM = dBDTxai - dBDTxia	dBDTxDM	-30	–	30	ns	R_{DCLOAD} = 40 Ω, (see **Figure 42**);	P_15.1.212
Transition time Idle -> active	dBusTxia	–	15	30	ns	R_{DCLOAD} = 40 Ω, (see **Figure 42**);	P_15.1.213
Transition time Active -> idle	dBusTxai	–	15	30	ns	R_{DCLOAD} = 40 Ω, (see **Figure 42**);	P_15.1.214
Transmitter delay BGE Idle -> active	dBDBGEia	–	55	75	ns	R_{DCLOAD} = 40 Ω, (see **Figure 43**);	P_15.1.215
Transmitter delay BGE Active -> idle	dBDBGEai	–	55	75	ns	R_{DCLOAD} = 40 Ω, (see **Figure 43**);	P_15.1.216

Table 22 Electrical characteristics (cont'd)

5.5 V < uV_{BAT} < 18 V; 3.0 V < uV_{IO} < 5.25 V; 4.75 V < uV_{CC} < 5.25 V; R_{DCLOAD} = 45 Ω; C_{DCLOAD} = 100 pF;
-40 °C < $T_{Junction}$ < 150 °C;
All voltages with respect to ground; positive current flowing into the pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Bus Receiver: BP, BM							
Receiver threshold for detecting "Data_1"	uData1	150	–	300	mV	-10 V < uCM < 15 V, [9];	P_15.1.220
Receiver threshold for detecting "Data_0"	uData0	-300	–	-150	mV	-10 V < uCM < 15 V, [9];	P_15.1.221
Mismatch of Receiver thresholds	uData1-|uData0|	-30	–	30	mV	uCM = (uBP+uBM)/2 = 2.5 V;	P_15.1.222
Common mode voltage range	uCM	-10	–	15	V	[10];	P_15.1.230
Filter time for bus idle detection	dBDIdle Detection	50	–	200	ns	uBus = 900 mV -> 30 mV;	P_15.1.231
Filter time for bus active detection	dBDActivity Detection	100	–	250	ns	uBus = 30 mV -> 900 mV;	P_15.1.232
Receiver common mode input resistance	R_{CM1}, R_{CM2}	10	–	40	kΩ	Bus = "Idle", open load, uV_{CC} = 5 V;	P_15.1.233
Receiver differential input resistance	R_{CM1} + R_{CM2}	20	–	80	kΩ	Bus = "Idle", open load;	P_15.1.234
Absolute differential bus "Idle" voltage, All modes	$uBDTx_{Idle}$	–	–	30	mV	TxEN = "high", 40 Ω < R_{DCLOAD} < 55 Ω;	P_15.1.235
"Idle" voltage on BP and BM, non-low power mode	uBias non-low power	1.8	2.4	3.2	V	TxEN = "high", bus = "Idle", uV_{CC} = 5 V, 40 Ω < R_{DCLOAD} < 55 Ω;	P_15.1.240
"Idle" voltage on BP and BM, BD_Sleep, BD_Standby, BD_GoToSleep	uBias low power	-100	–	100	mV	TxEN = "high", bus = "Idle", uV_{CC} = 5 V, 40 Ω < R_{DCLOAD} < 55 Ω;	P_15.1.241
Absolute leakage current on BP, when Transmitter off	iBP_{Leak}	–	7	15	µA	uBP = uBM = 5 V, all other pins connected to GND;	P_15.1.250
Absolute leakage current on BM, when Transmitter off	iBM_{Leak}	–	7	15	µA	uBP = uBM = 5 V, all other pins connected to GND;	P_15.1.251
Absolute leakage current loss to GND on BP	$iBP_{LeakGND}$	–	500	1600	µA	uBP = uBM = 0 V, all other pins connected to 16 V via 0 Ohm;	P_15.1.252
Absolute leakage current loss to GND on BM	$iBM_{LeakGND}$	–	500	1600	µA	uBP = uBM = 0 V, all other pins connected to 16 V via 0 Ohm;	P_15.1.253

Table 22 Electrical characteristics (cont'd)

5.5 V < uV_{BAT} < 18 V; 3.0 V < uV_{IO} < 5.25 V; 4.75 V < uV_{CC} < 5.25 V; R_{DCLOAD} = 45 Ω; C_{DCLOAD} = 100 pF;
-40 °C < $T_{Junction}$ < 150 °C;
All voltages with respect to ground; positive current flowing into the pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Receiver delay, falling edge	dBDRx10	–	65	75	ns	C_BDRxD = 25 pF, $dBUSRx0_{BD}$ = $dBUSRx1_{BD}$ > t_{Bit} = 60 ns, (see **Figure 44**);	P_15.1.260
Receiver delay, rising edge	dBDRx01	–	65	75	ns	C_BDRxD = 25 pF, $dBUSRx0_{BD}$ = $dBUSRx1_{BD}$ > t_{Bit} = 60 ns, (see **Figure 44**);	P_15.1.261
Receiver delay mismatch dBDRxAsym = |dBDRx10 -dBDRx01|	dBDRxAsym	–	–	5	ns	C_BDRxD = 25 pF, [8], $dBUSRx0_{BD}$ = $dBUSRx1_{BD}$ > t_{Bit} = 60 ns, (see **Figure 44**);	P_15.1.262
Bus driver idle response time	dBDRxai	50	–	250	ns	C_BDRxEN = 25 pF, (see **Figure 45**);	P_15.1.263
Bus driver activity response time	dBDRxia	100	–	300	ns	C_BDRxEN = 25 pF, (see **Figure 45**);	P_15.1.264
Idle-Loop delay dBDTxRxai = dBDRxai+dBDTxai	dBDTxRxai	–	–	325	ns	C_BDRxEN = 25 pF;	P_15.1.265
BP output current, bus "Idle"	iBP_{Idle}	–	–	5.0	mA	-27 V < BP < 27 V;	P_15.1.270
BM output current, bus "Idle"	iBM_{Idle}	–	–	5.0	mA	-27 V < BM < 27 V;	P_15.1.271
Input capacitance at pin BP	C_BDBP	–	–	30	pF	[1];	P_15.1.272
Input capacitance at pin BM	C_BDBM	–	–	30	pF	[1];	P_15.1.273
Differential input capacitance between BP and BM	C_BDBus	–	–	20	pF	[1];	P_15.1.274

Table 22 Electrical characteristics (cont'd)

5.5 V < uV_{BAT} < 18 V; 3.0 V < uV_{IO} < 5.25 V; 4.75 V < uV_{CC} < 5.25 V; R_{DCLOAD} = 45 Ω; C_{DCLOAD} = 100 pF;
-40 °C < $T_{Junction}$ < 150 °C;
All voltages with respect to ground; positive current flowing into the pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Remote Wake-up Detection: BP, BM							
Low-power Receiver threshold for detecting "Data_0"	uData0_LP	-400	–	-100	mV	(see **Figure 18**);	P_15.1.280
Acceptance time-out of a "Data_0" phase in the wake-up pattern	$dWU_{0Detect}$	1	–	4	µs	(see **Figure 18**);	P_15.1.281
Acceptance time-out of an "Idle" or "Data 1" phase in the wake-up pattern	$dWU_{IdleDetect}$	1	–	4	µs	(see **Figure 18**);	P_15.1.282
Acceptance time-out for wake-up pattern recognition	$dWU_{Timeout}$	48	–	140	µs	(see **Figure 18**);	P_15.1.283
Acceptance time-out for interruptions	$dWU_{Interrupt}$	0.13	–	1	µs	(see **Figure 20**), [1], [11];	P_15.1.284
Response time after wake-up	$dBDWakeupReaction_{remote}$	–	–	100	µs	(see **Figure 18**);	P_15.1.285
Host Commands and SIR							
Mode transition time after applying the host command	$dBD_{ModeChange}$	–	–	100	µs	(see **Figure 10**), $iNH1_{Leak}$ > 0.2 mA, all mode changes;	P_15.1.290
Mode transition time to BD_Standby after power-up	$dBD_{PowerUp}$	–	–	100	µs	V_{BAT} > $uBDUVV_{BAT}$, V_{CC} > $uBDUVV_{CC}$, (see **Figure 30**);	P_15.1.291
Filter time for detection of the host commands at the pins EN and STBN	$dBDLogic_{Filter}$	10	–	30	µs	(see **Figure 10**);	P_15.1.292
Time for mode selection via the EN pin within the Go-To-Sleep command	dBD_{Sleep}	25	–	50	µs	(see **Figure 33**);	P_15.1.293
Timing window for EN pin to clock out the SIR	dEN_{Clock}	3	5	8	µs	(see **Figure 11**);	P_15.1.294
Time-out at the EN pin for the SIR read-out	$dEN_{Timeout}$	10	–	30	µs	(see **Figure 11**);	P_15.1.295

1) Not part of production test, specified by design.
2) No undervoltage at uV_{IO} and either uV_{CC} or uV_{BAT} with supply.
3) Undervoltage at uV_{IO} and either uV_{CC} or uV_{BAT} with supply.

4) BD_Off state uV_{CC} and uV_{BAT} are without supply (see also **Chapter 8.4.1**).
5) Currents not tested at full uV_{BAT} range in production, they are specified by design.
6) TxD signal is constant from 100 ns up to 4400 ns before the first edge. The parameter is valid for both polarities.
7) Sum of TxD signal rise and fall time (20% - 80% V_{IO}) of up to 9 ns.
8) Guaranteed for +/- 300 mV as well as for +/- 150 mV level of uBus.
9) Activity detected previously for uBus up to +/- 3000 mV
10) Tested on a receiving bus driver. The sending bus driver has a ground offset voltage in the range of -12.5 V to +12.5 V and sends a 50/50 test pattern.
11) The minimum value is only guaranteed when the phase that is interrupted was continuously present for at least 870 ns.

15.2 Diagrams

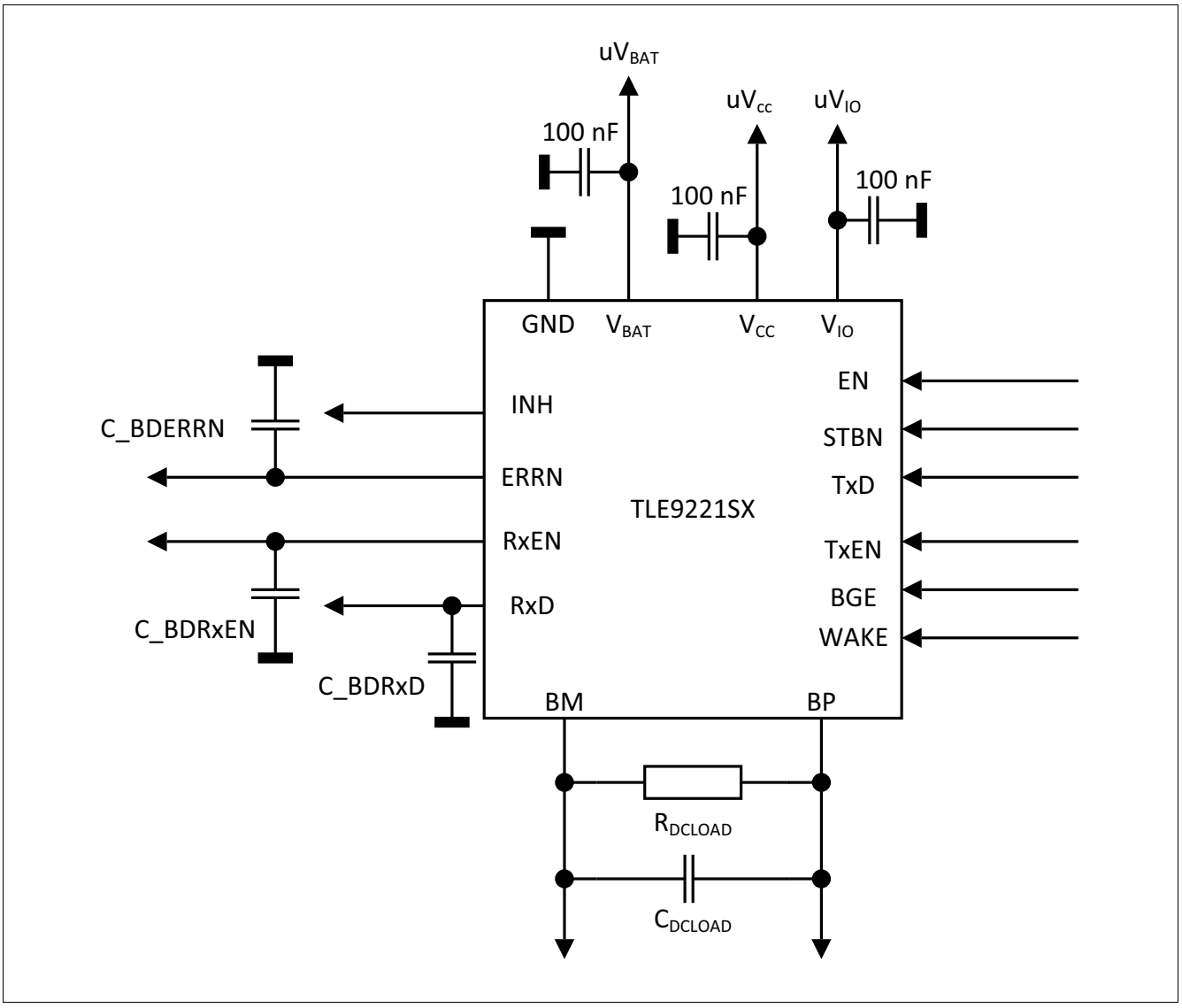


Figure 40 Simplified test circuit

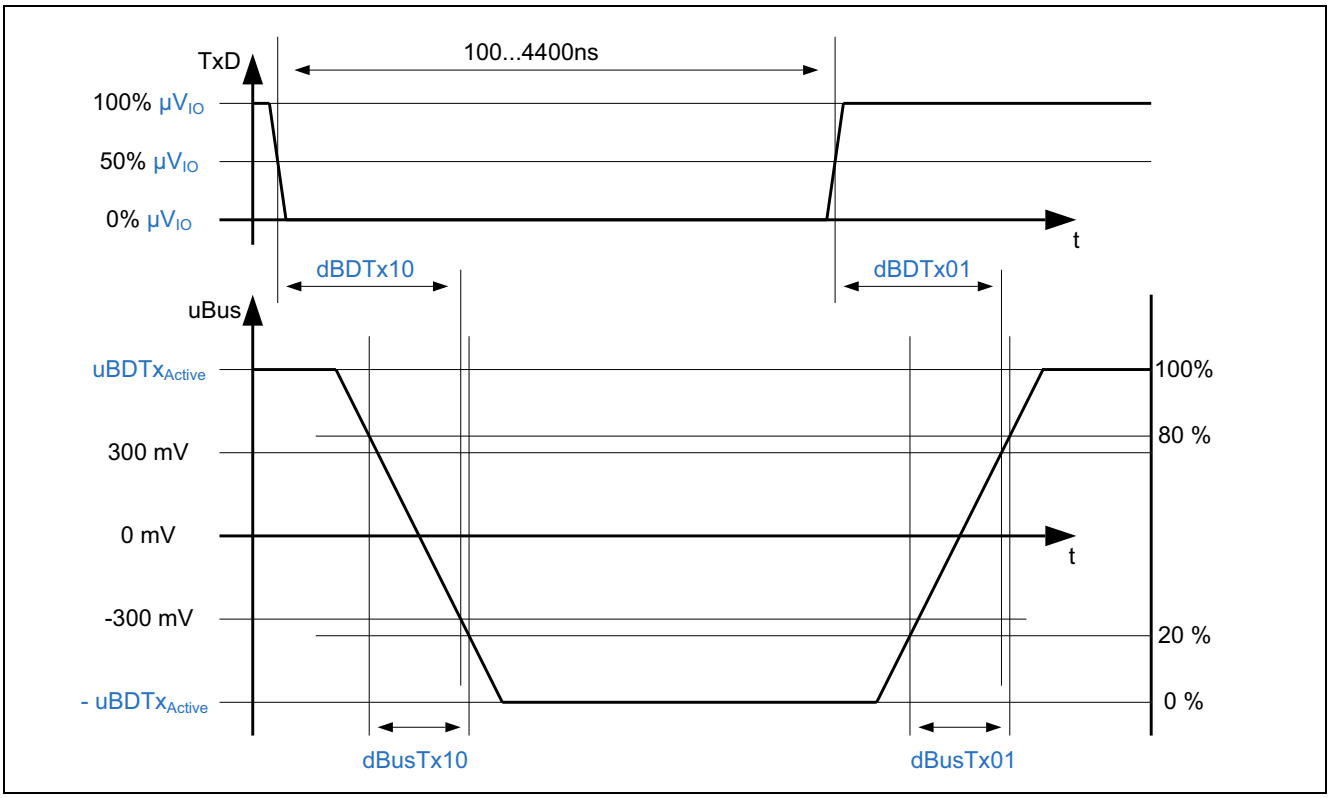


Figure 41 Transmitter characteristics

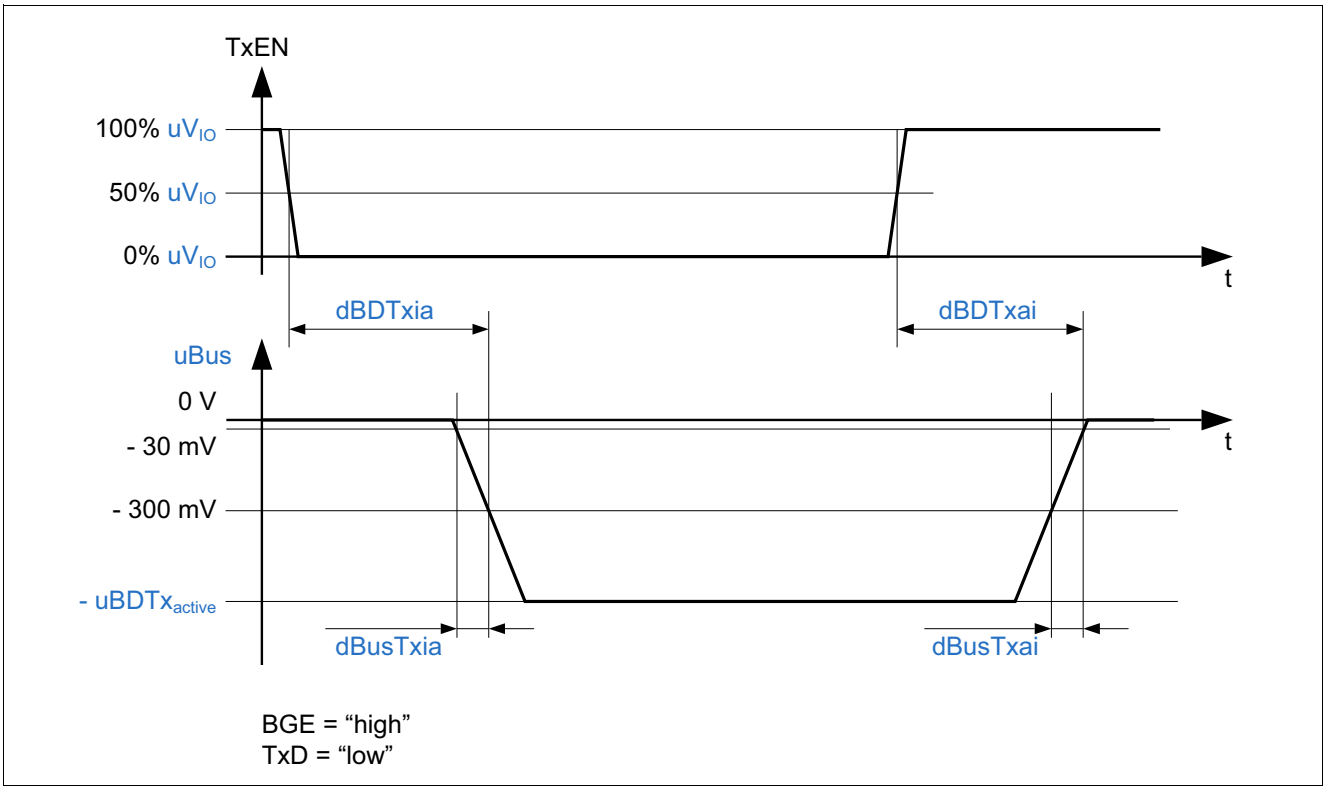


Figure 42 Transmitter characteristics from “Idle” to “active” and vice versa

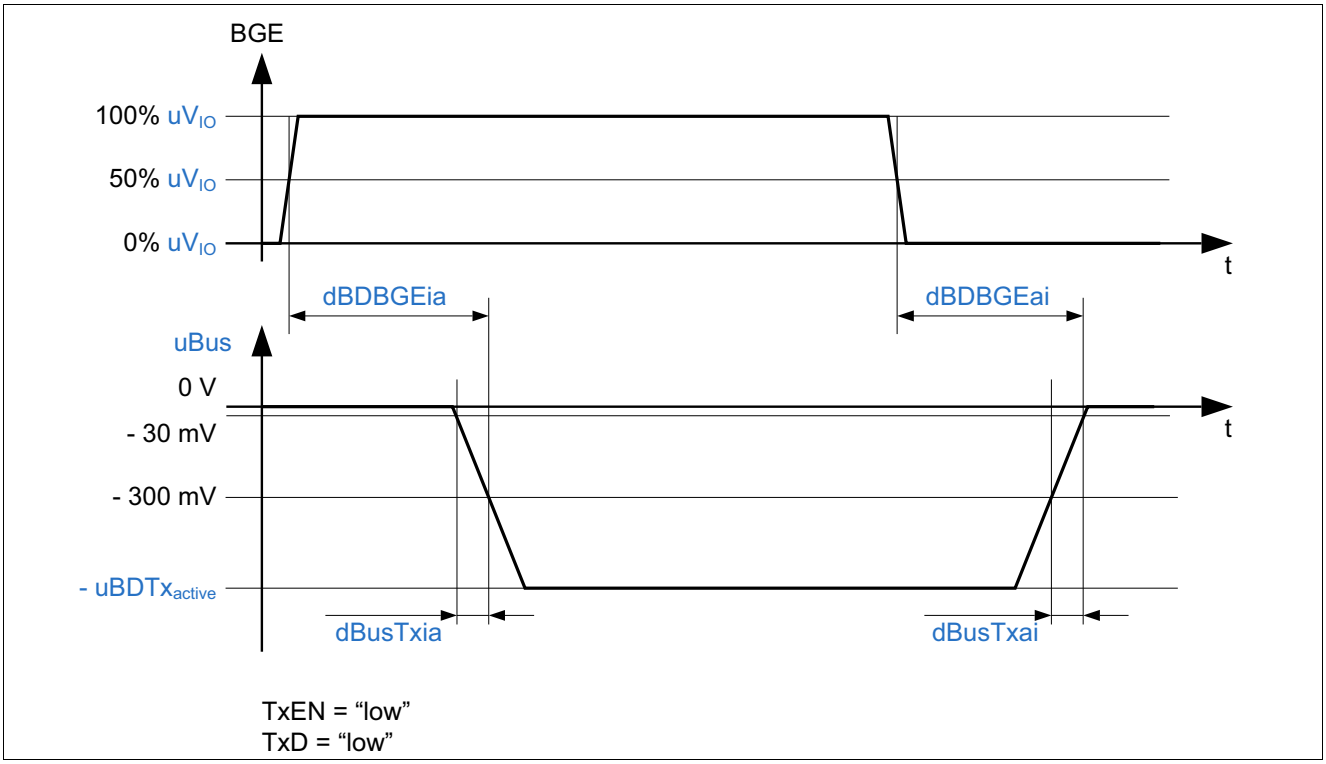


Figure 43 Transmitter characteristics with bus guardian enable

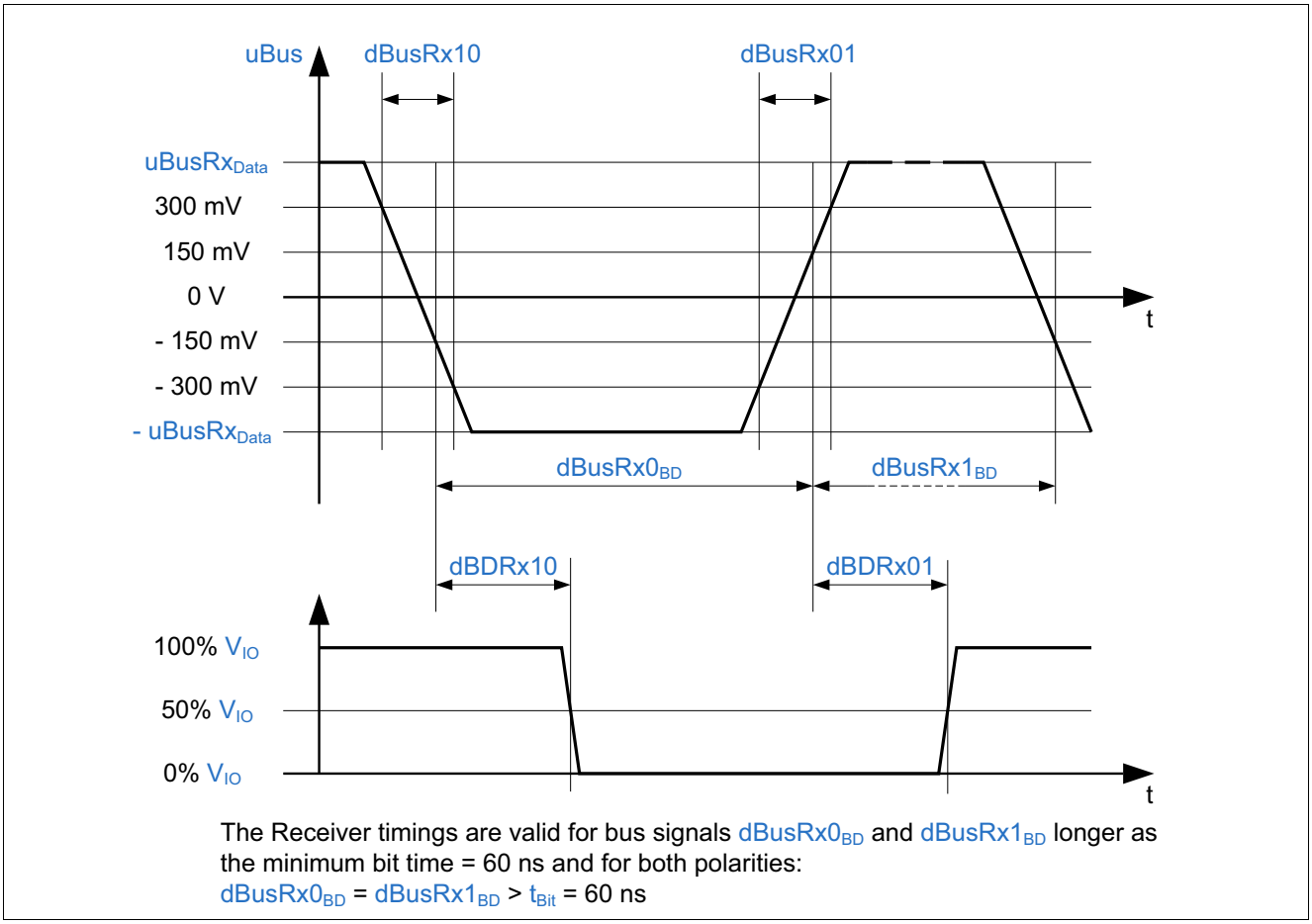
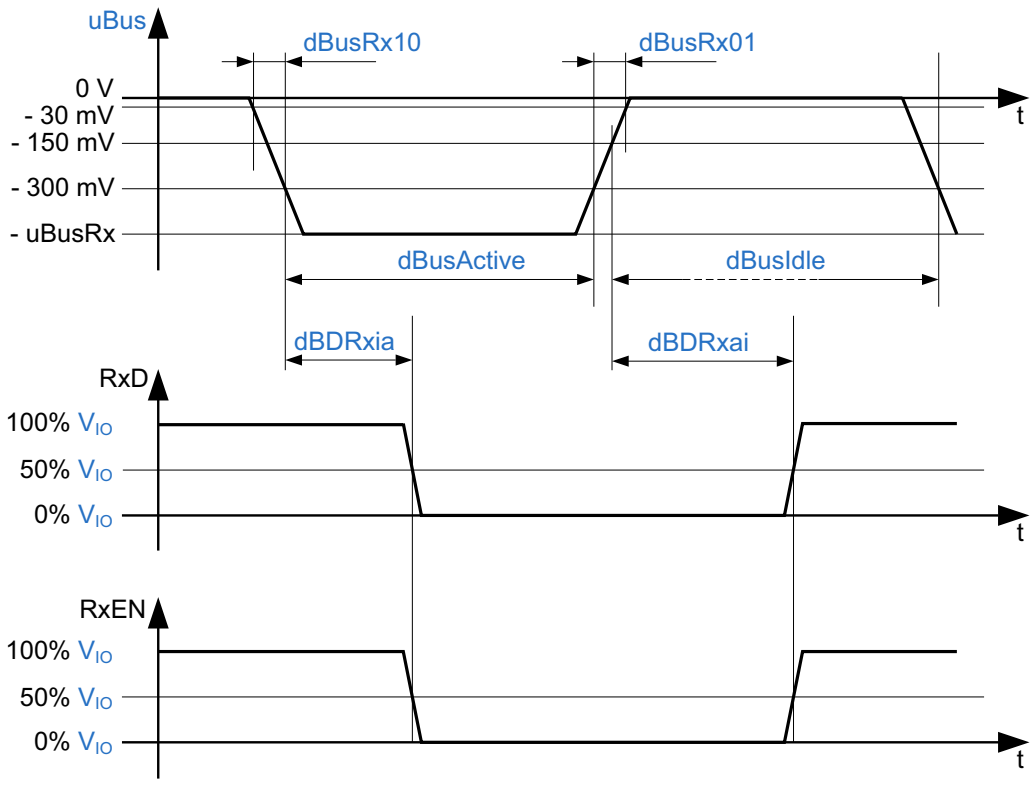


Figure 44 Receiver timing characteristics



The signals on the pins RxD and RxEN switch within a delay < 10 ns

Figure 45 Receiver transition from “Idle” to “active” and vice versa

16 Application Information

16.1 ESD Robustness according to IEC61000-4-2

Tests for ESD robustness according to IEC61000-4-2 “Gun test” (150 pF, 330 Ω) have been performed. The results and test conditions are available in a separate test report.

Table 23 ESD robustness according to IEC61000-4-2

Performed Test	Symbol	Result	Unit	Remarks
Electrostatic discharge voltage at pin BM, BP and WAKE versus GND	$uESD_{IEC}$	≥ +11	kV	[1], [2] Positive pulse
Electrostatic discharge voltage at pin BM, BP and WAKE versus GND	$uESD_{IEC}$	≤ -11	kV	[1], [2] Negative pulse

1)ESD susceptibility “ESD GUN IEC61000-4-2”.
Tested by external test facility (IBEE Zwickau, EMC test report no.: 22-02-13).
2) Test result without any external bus filter network, e.g. common mode choke.

16.2 Bus Interface Simulation Model Parameter

The simulated value $R_{BDTransmitter}$ describes the equivalent bus driver output impedance.

$$R_{BDTransmitter} = 50\Omega \times (uBus_{100} - uBus_{40}) / (2.5 \times uBus_{40} - uBus_{100})$$

$uBus_{100}$ = differential output voltage on a 100Ω||100pF load, while driving “Data_1” to the bus. Value based on simulation.

$uBus_{40}$ = differential output voltage on a 40Ω||100pF load, while driving “Data_1” to the bus. Value based on simulation.

Figure 46 Bus driver output resistance

Table 24 Bus driver simulation resistor

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Bus driver interface simulation resistor	$RD_{BDTransmitter}$	30	100	500	Ω	1)

1) Simulated value for reference purposes only.

16.3 Typical RxD Output Signals

The simulated RxD output behavior describe the rise and fall times of the RxD pin on a 50 Ohm, 10 pF load at the end of a standard lossless transmission line with 1 ns propagation delay (see **Table 25**, **Figure 47** and **Figure 48**).

Table 25 RxD output signal (simulated values),

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Sum of rise and fall time on the RxD output	$dBDRxD_{R10}$+ $dBDRxD_{F10}$	–	–	16.5	ns	C_BDRxD = 10 pF, 1) R_CBDRxD = 50 Ω
Difference of rise and fall time on the RxD output	$\lvert dBDRxD_{R10}$ - $dBDRxD_{F10}\rvert$	–	–	5	ns	C_BDRxD = 10 pF, 1) R_CBDRxD = 50 Ω

1) Simulated value for reference purposes only.

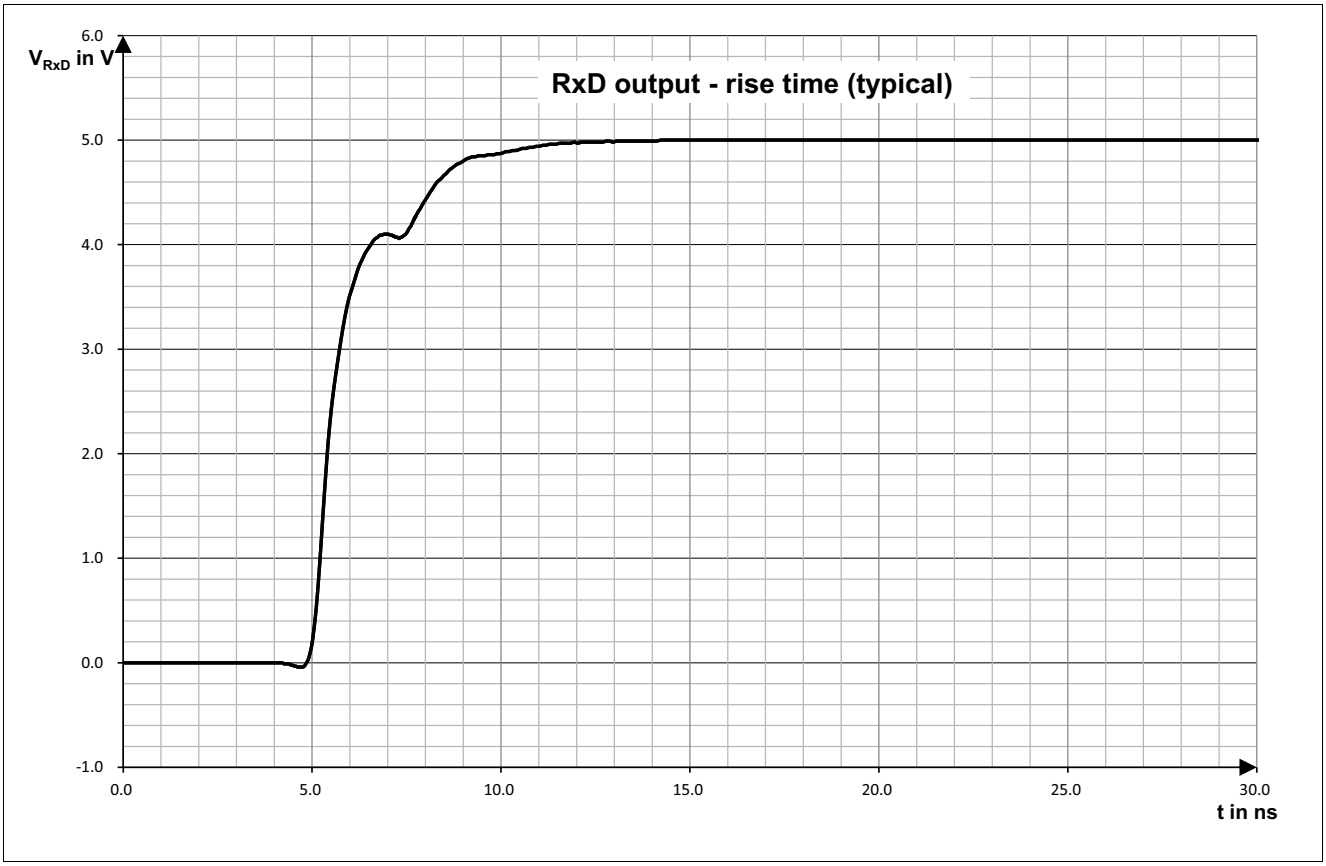


Figure 47 RxD output rise time (typical simulation value)

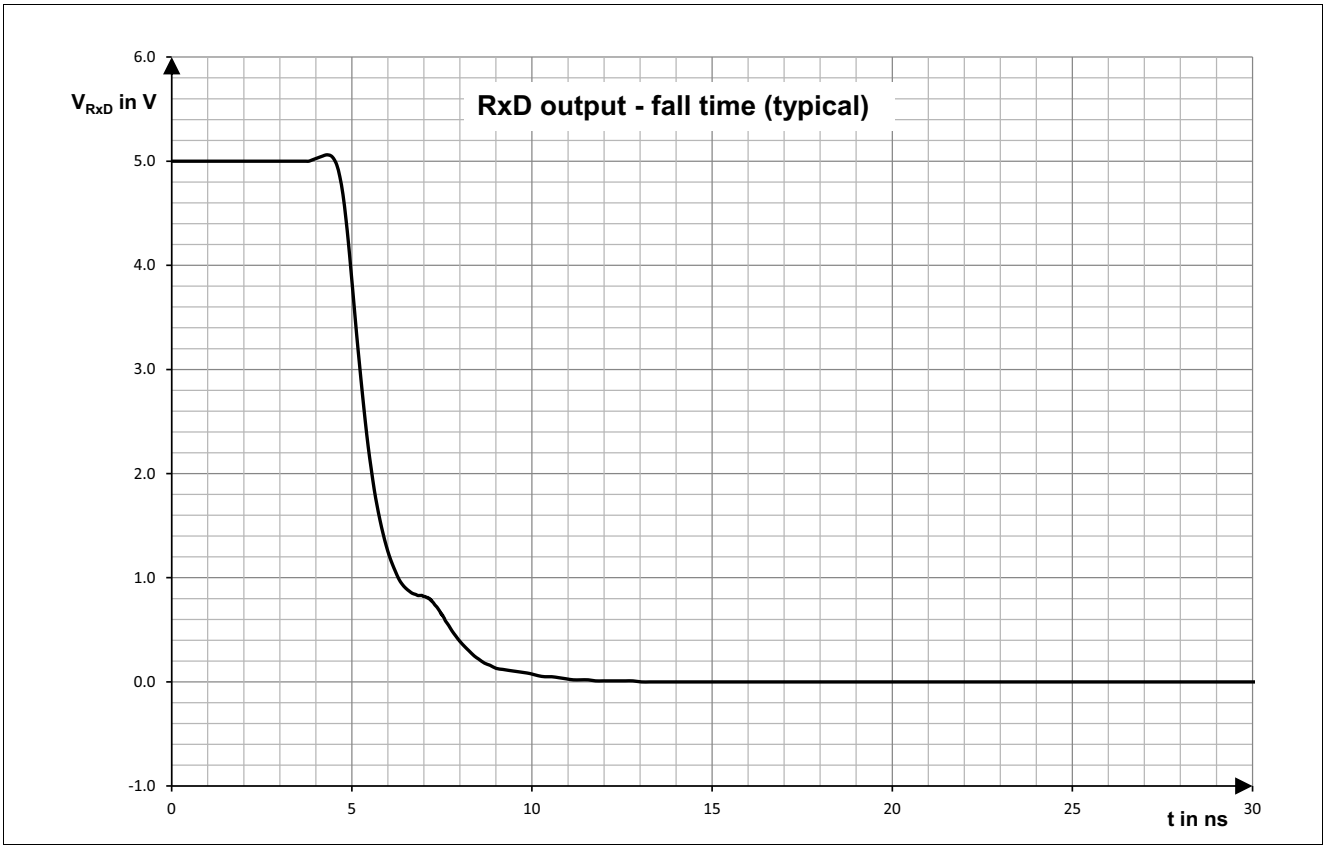


Figure 48 RxD output fall time (typical simulation value)

16.4 Operating Temperature

The FlexRay transceiver TLE9221SX is qualified for temperature Grade 1 (-40°C to +125°C ambient operating temperature) according to AEC - Q100. Grade 1 according AEC - Q100 is equivalent to the ambient temperature for class 1 T_{AMB_Class1} .

Infineon specifies for the electrical characteristics (see **Table 21**) the junction temperature $T_{Junction}$. The ambient temperature can be calculated with the power dissipation and the thermal resistance R_{thJA} (see **Figure 49**).

$$T_J = T_A + R_{thJA} \times P_d$$

$$T_A = T_J - R_{thJA} \times P_d$$

with:

T_A	= ambient temperature
T_J	= junction temperature
P_d	= power dissipation of the FlexRay transceiver
R_{thJA}	= thermal resistance junction to ambient

Figure 49 Ambient temperature T_A calculation

16.5 Application Example

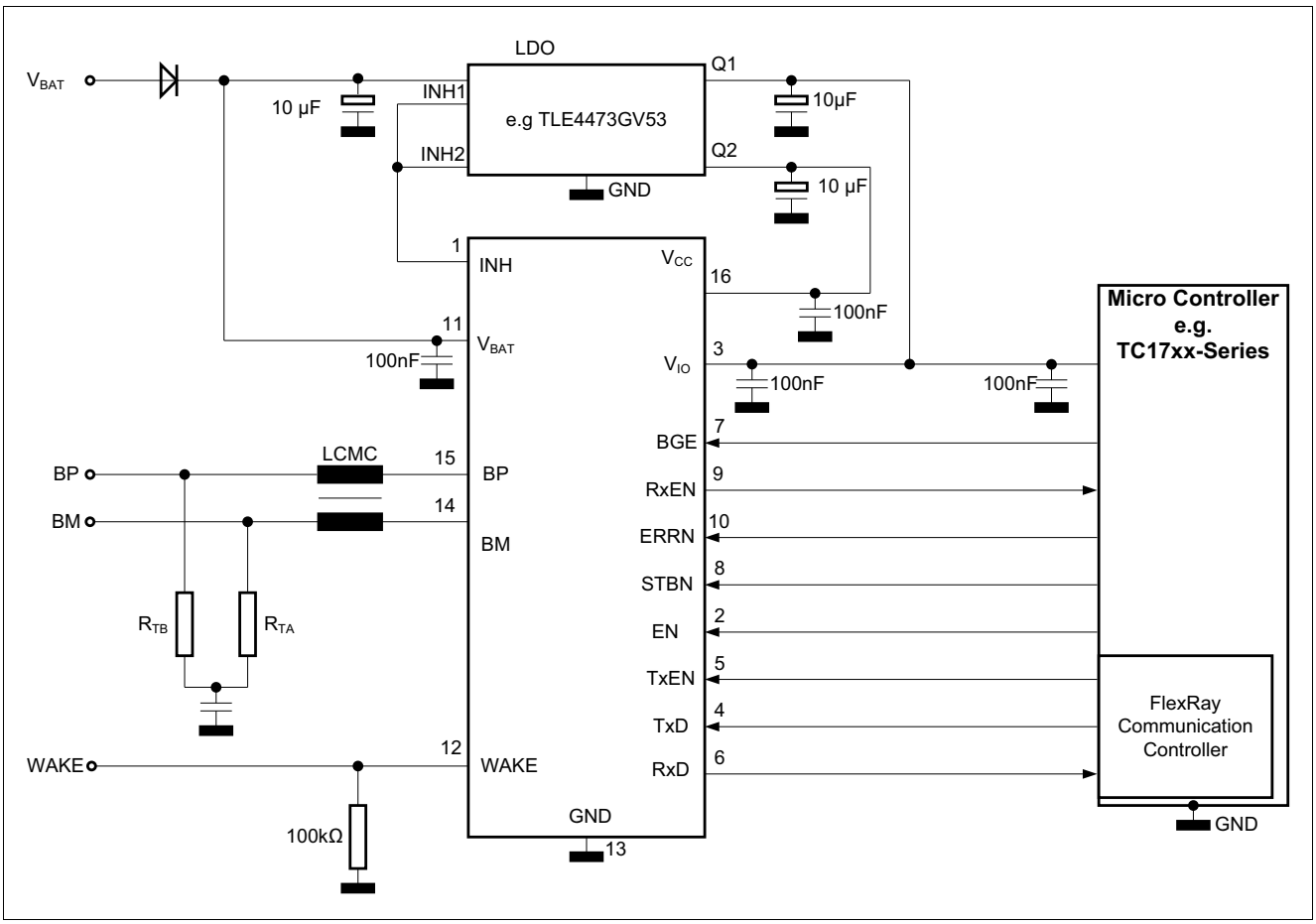


Figure 50 Simplified application example for the TLE9221SX

16.6 Further Application Information

- Please contact us for information regarding the pin FMEA.
- For further information you may visit: **http://www.infineon.com**

17 Package information

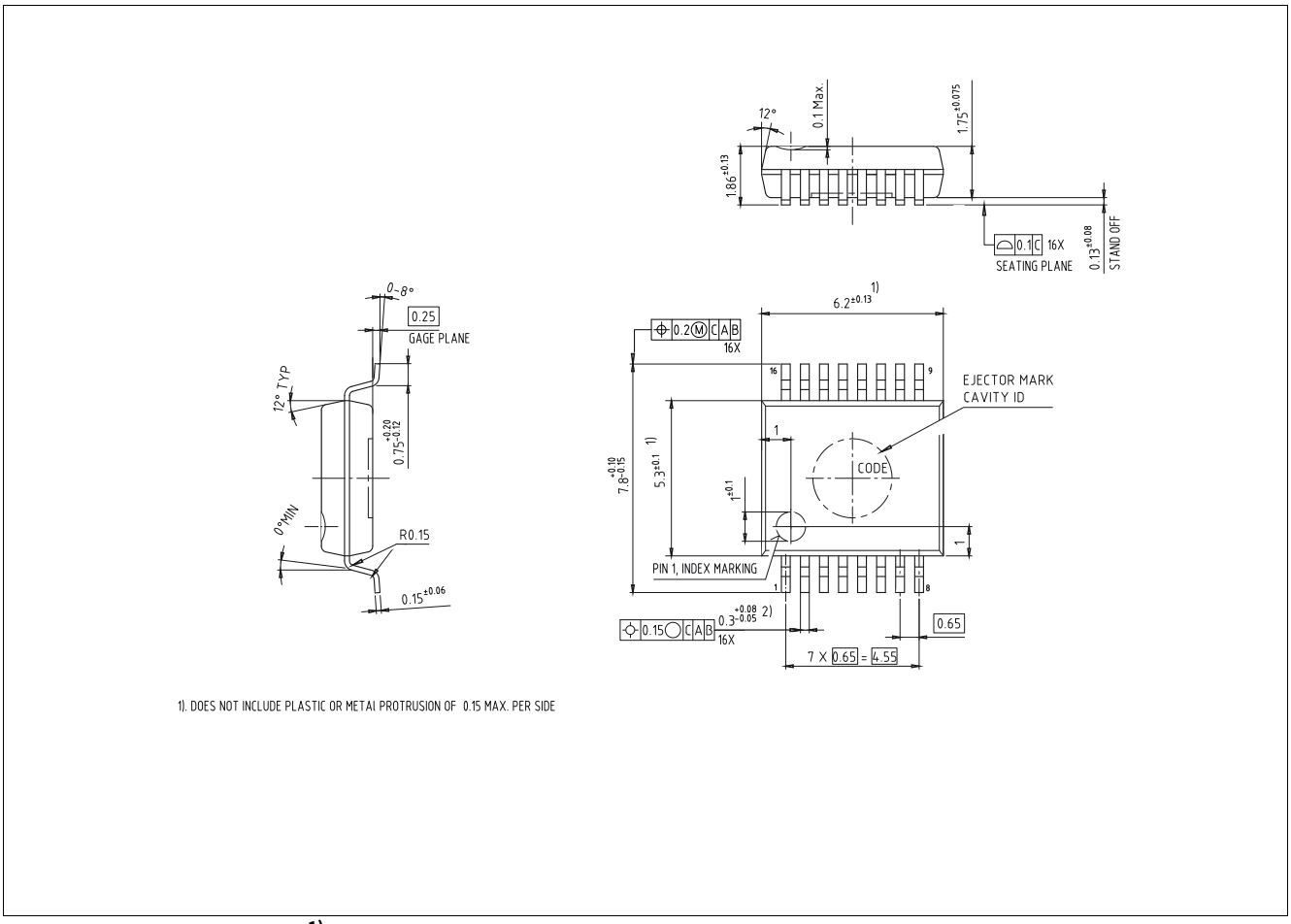


Figure 51 PG-SSOP-16 [1)]

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

18 Revision History

Revision	Date	Changes
1.31	2019-02-06	Update Layout style, editorial changes
1.3	2015-08-18	Data Sheet updated based on Data Sheet Rev. 1.2: Package name changed to PG-SSOP-16: • All Pages Paragraph on FlexRay Consortium removed: • **Page 6, Description** “ISO 17458” added: • **Page 5, Features** • **Page 6, Description** Reference to FlexRay EPL removed: • **Page 5, Features** • **Page 6, Description** • **Page 9, Functional Description** • **Page 16, Host Interface** • **Page 17, Power Supply Interface** • **Page 23, Reset the ERRN Output Pin** • **Page 24, Wake-up Detector** • **Page 32, INH Output** • **Page 42, Operating Mode Description** • **Page 53, BD_Sleep Mode Entry Flag** “CT index ...” removed: • **Table 19, Absolute maximum ratings voltages, currents and temperatures** • **Table 20, Functional range** • **Table 22, Electrical characteristics** • **Table 23, ESD robustness according to IEC61000-4-2** • **Table 24, Bus driver simulation resistor** • **Table 25, RxD output signal (simulated values),** • **Chapter 16.4, Operating Temperature**

Revision History

Revision	Date	Changes
1.2	2015-03-11	Data Sheet updated based on Data Sheet Rev. 1.1: • All pages: Changed package name to PG-SSOP16-1 • **Page 10**, **Table 2** Footnote updated • **Page 67**, **Table 20** Max. limit of the extended functional range for uV_{BAT_EXT} (P_14.2.2) updated.
1.1	2013-07-15	Data Sheet updated based on Data Sheet Rev. 1.0: • **Page 67**, **Table 20**: New parameter for the supply uV_{BAT} added: Extended functional range for uV_{BAT_EXT} (P_14.2.2).
1.0	2013-05-17	Data Sheet created.

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Edition 2019-02-06
Published by
Infineon Technologies AG
81726 Munich, Germany

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Document reference
Z8F54046603

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