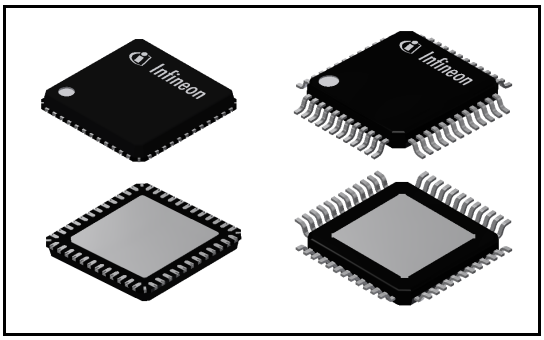
TLD5542-1

H-Bridge DC/DC Controller with SPI Interface

Infineon® LITIX™ Power Flex

AEC Qualified RoHS

Package	PG-VQFN-48	PG-TQFP-48
Marking	TLD55421QV	TLD55421QU
Sales Name	TLD5542-1QV	TLD5542-1QU



1 Overview

Features

- Single inductor high power Buck-Boost controller
- Wide LED forward voltage range (2 V up to 55 V)
- Wide VIN range (IC 4.5 V to 40 V, power 4.5 V to 55 V)
- Switching frequency range from 200 kHz to 700 kHz
- SPI for diagnostics and control
- Maximum efficiency in every condition (up to 96%)
- Constant current (LED) and constant voltage regulation
- Drives multiple loads with a single IC thanks to the Fast Output Discharge operation
- Limp Home function (fail safe mode)
- EMC optimized device: features an Auto Spread Spectrum
- LED and input current sense with dedicated monitor outputs
- Advanced protection features for device and load
- Enhanced dimming features: Analog and PWM dimming
- LED current accuracy +/- 3%
- Available in a small thermally enhanced PG-VQFN-48 or PG-TQFP-48 package
- Automotive AEC Qualified

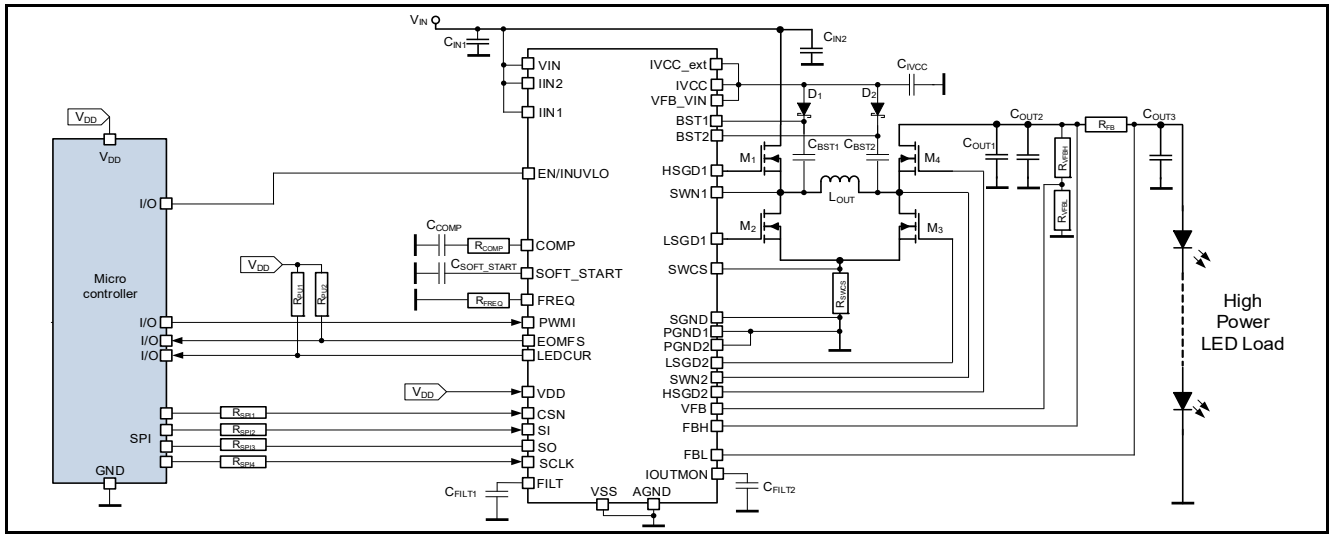


Figure 1 Application Drawing - TLD5542-1 as current regulator

Overview

Description

The TLD5542-1 is a synchronous MOSFET H-Bridge DC/DC controller with built in protection features and SPI interface. This concept is beneficial for driving high power LEDs with maximum system efficiency and minimum number of external components. The TLD5542-1 offers both analog and digital (PWM) dimming.The switching frequency is adjustable in the range of 200 kHz to 700 kHz. It can be synchronized to an external clock source. A built in programable Spread Spectrum switching frequency modulation and the forced continuous current regulation mode improve the overall EMC behavior. Furthermore the current mode regulation scheme provides a stable regulation loop maintained by small external compensation components. The adjustable soft start feature limits the current peak as well as voltage overshoot at start-up. The TLD5542-1 is suitable for use in the harsh automotive environment.

Table 1 Product Summary

Power Stage input voltage range	V_{POW}	4.5 V … 55 V
Device Input supply voltage range	V_{VIN}	4.5 V … 40 V
Maximum output voltage (depending by the application conditions)	$V_{OUT(max)}$	55 V as LED Driver Boost Mode 50 V as LED Driver Buck Mode 50 V as Voltage regulator
Switching Frequency range	f_{SW}	200 kHz... 700 kHz
Typical NMOS driver on-state resistance at T_j = 25°C (Gate Pull Up)	$R_{DS(ON\_PU)}$	2.3 Ω
Typical NMOS driver on-state resistance at T_j = 25°C (Gate Pull Down)	$R_{DS(ON\_PD)}$	1.2 Ω
SPI clock frequency	$f_{SCLK(MAX)}$	5 MHz

Protective Functions

- Over load protection of external MOSFETs
- Shorted load, output overvoltage protection
- Input undervoltage protection
- Thermal shutdown of device with autorestart behavior
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Latched diagnostic information via SPI
- Device Overtemperature shutdown and Temperature Prewarning
- Smart monitoring and advanced functions provide I_{LED} and I_{IN} information

Limp Home Function

- Limp Home activation via LHI pin

Applications

- Especially designed for driving multiple high power LED functions (I.E. Low Beam, High Beam, DRL)
- Automotive Exterior Lighting: full LED headlamp assemblies
- General purpose DC/DC voltage regulator

2 Block Diagram

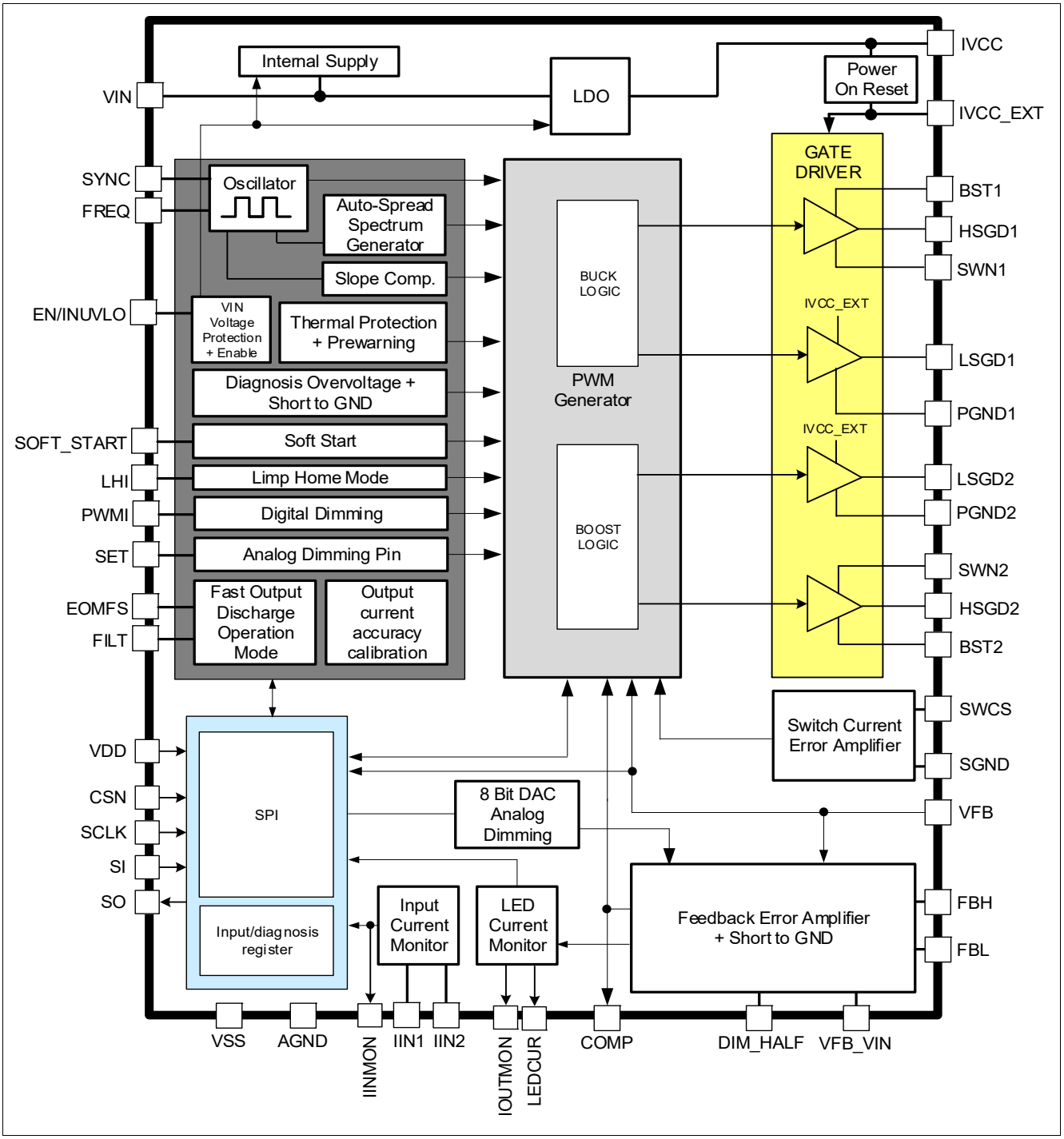


Figure 2 Block Diagram - TLD5542-1

3 Pin Configuration

3.1 Pin Assignment

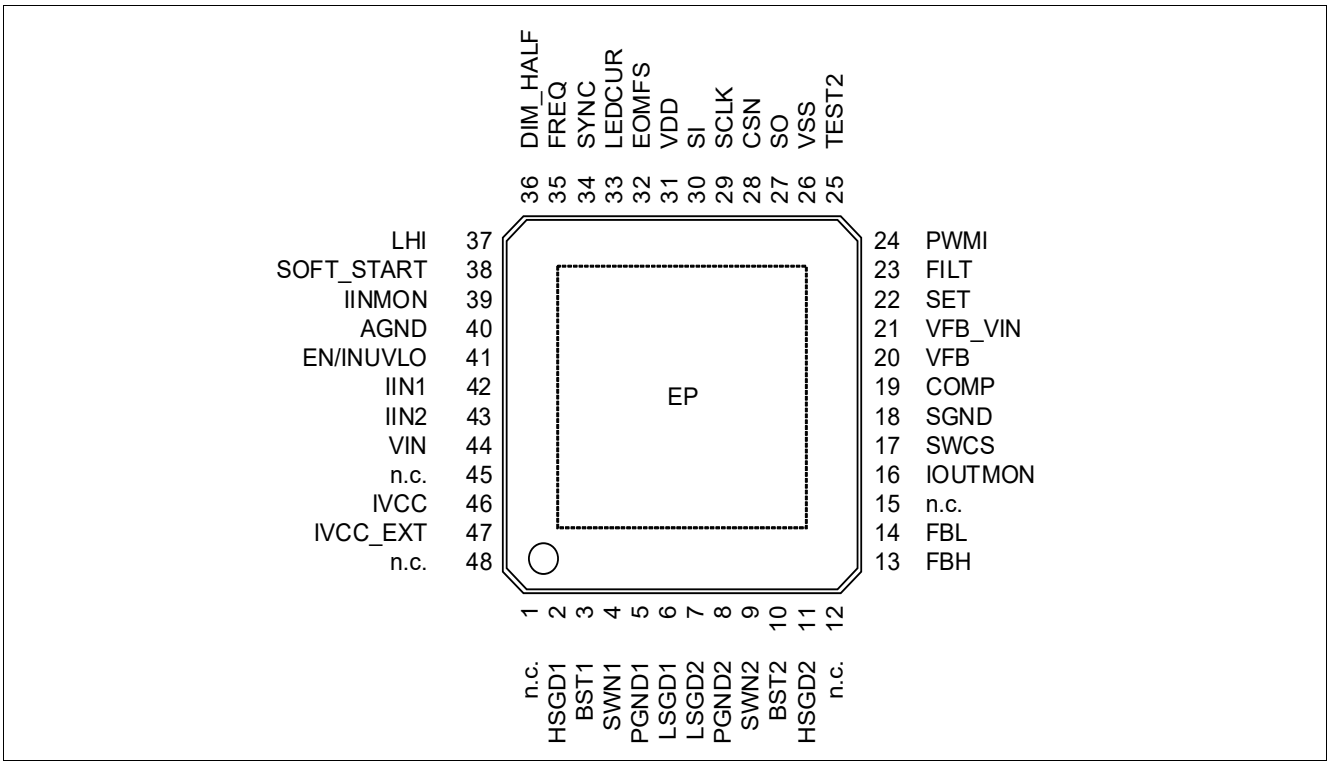


Figure 3 Pin Configuration - TLD5542-1

3.2 Pin Definitions and Functions

Table 2 Pin Definitions and Functions

Pin	Symbol	I/O [1]		Function
Power Supply				
1, 12, 15, 45, 48	n.c.	-		**Not connected, tie to AGND on the Layout;**
44	VIN	-		**Power Supply Voltage;** Supply for internal biasing.
31	VDD	-		**Digital GPIO Supply Voltage;** Connect to reverse voltage protected 5 V or 3.3 V supply.
47	IVCC_EXT	I	PD	**External LDO input;** Input to alternatively supply internal Gate Drivers via an external LDO. Connect to IVCC pin to use internal LDO to supply gate drivers. Must not be left open.
5, 8	PGND1, 2	-		**Power Ground;** Ground for power potential. Connect externally close to the chip.
26	VSS	-		**Digital GPIO Ground;** Ground for GPIO pins.
40	AGND	-		**Analog Ground;** Ground Reference
-	EP	-		**Exposed Pad;** Connect to external heatspreading Cu area (e.g. inner GND layer of multilayer PCB with thermal vias).
Gate Driver Stages				
2	HSGD1	O		**Highside Gate Driver Output 1;** Drives the top n-channel MOSFET with a voltage equal to V_{IVCC_EXT} superimposed on the switch node voltage SWN1. Connect to gate of external switching MOSFET.
11	HSGD2	O		**Highside Gate Driver Output 2;** Drives the top n-channel MOSFET with a voltage equal to V_{IVCC_EXT} superimposed on the switch node voltage SWN2. Connect to gate of external switching MOSFET.
6	LSGD1	O		**Lowside Gate Driver Output 1;** Drives the lowside n-channel MOSFET between GND and V_{IVCC_EXT}. Connect to gate of external switching MOSFET.
7	LSGD2	O		**Lowside Gate Driver Output 2;** Drives the lowside n-channel MOSFET between GND and V_{IVCC_EXT}. Connect to gate of external switching MOSFET.
4	SWN1	IO		**Switch Node 1;** SWN1 pin swings from a diode voltage drop below ground up to V_{IN}.
9	SWN2	IO		**Switch Node 2;** SWN2 pin swings from ground up to a diode voltage drop above V_{OUT}.

Table 2 Pin Definitions and Functions

Pin	Symbol	I/O [1]		Function
46	IVCC	O		**Internal LDO output;** Used for internal biasing and gate driver supply. Bypass with external capacitor close to the pin. Pin must not be left open.
Inputs and Outputs				
37	LHI	I	PD	**Limp Home Input Pin;** Used to enter in Limp Home state during Fail Safe condition.
23	FILT	-		**MFS Filter;** Connect with a 220pF capacitor to GND to filter MFS reference Voltage.
25	TEST2	-		**Test Pin;** Used for Infineon end of line test, connect to GND in application.
41	EN/INUVLO	I	PD	**Enable/Input Under Voltage Lock Out;** Used to put the device in a low current consumption mode, with additional capability to fix an undervoltage threshold via external components. Pin must not be left open.
35	FREQ	I		**Frequency Select Input;** Connect external resistor to GND to set frequency.
34	SYNC	I	PD	**Synchronization Input;** Apply external clock signal for synchronization.
24	PWMI	I	PD	**Control Input;** Digital input 5 V or 3.3 V.
13	FBH	I		**Output current Feedback Positive;** Non inverting Input (+).
14	FBL	I		**Output current Feedback Negative;** Inverting Input (-).
3	BST1	IO		**Bootstrap capacitor;** Used for internal biasing and to drive the Highside Switch HSGD1. Bypass to SWN1 with external capacitor close to the pin. Pin must not be left open.
10	BST2	IO		**Bootstrap capacitor;** Used for internal biasing and to drive the Highside Switch HSGD2. Bypass to SWN2 with external capacitor close to the pin. Pin must not be left open.
17	SWCS	I		**Current Sense Input;** Inductor current measurement - Non Inverting Input (+).
18	SGND	I		**Current Sense Ground;** Inductor current sense - Inverting Input (-). Route as Differential net with SWCS on the Layout.
42	IIN1	I		**Input Current Monitor Positive;** Non Inverting Input (+), connect to VIN if input current monitor is not needed.
43	IIN2	I		**Input Current Monitor Negative;** Inverting Input (-), connect to VIN if input current monitor is not needed.
19	COMP	O		**Compensation Network Pin;** Connect R and C network to pin for stability phase margin adjustment.

Pin Configuration

Table 2 Pin Definitions and Functions

Pin	Symbol	I/O [1]		Function
38	SOFT_START	O		**Softstart configuration Pin;** Connect a capacitor C_{SOFT_START} to GND to fix a soft start ramp default time.
21	VFB_VIN	I		**Input Voltage Feedback for analog dimming compensation;** Connect with a Resistor divider to Vin. If not used , short to IVCC
36	DIM_HALF	I		**Dual Range Output Current;** Double the analog dimming compensation when High.
20	VFB	I		**Voltage Loop Feedback Pin;** VFB is intended to set output overvoltage protection and F.D. output voltage sensing.
22	SET	I		**Analog current sense adjustment Pin;**
39	IINMON	O		**Input current monitor output;** Monitor pin that produces a voltage proportional to $V_{IN1-IN2}$. Typical IINMON will be equal 1 V when V_{IIN1}-V_{IIN2} = 50 mV.
16	IOUTMON	O		**Output current monitor output;** Monitor pin that produces a voltage proportional to $V_{FBH-FBL}$ plus an offset. Connect with a bypass capacitor to ground
33	LEDCUR	O		**LED current Flag;** An open drain output used to detect the presence of load current on MFS topologies
32	EOMFS	O		**End of MFS routine Flag;** An open drain output which is pulled to LOW when MFS routine is ongoing, released to high when complete.
SPI				
30	SI	I	PD	**Serial data in;** Digital input 5 V or 3.3 V.
29	SCLK	I	PD	**Serial clock;** Digital input 5 V or 3.3 V.
28	CSN	I	PU	**SPI chip select;** Digital input 5 V or 3.3 V. Active LOW.
27	SO	O		**Serial data out;** Digital output, referenced to V_{DD}.

1) O: Output, I: Input,
PD: pull-down circuit integrated,
PU: pull-up circuit integrated

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings[1)]
T_J = -40°C to +150°C; all voltages with respect to AGND, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
VIN Supply Input	V_{VIN}	-0.3	–	60	V	–	P_4.1.1
VDD Digital supply voltage	V_{VDD}	-0.3	–	6	V	–	P_4.1.2
IVCC Internal Linear Voltage Regulator Output voltage	V_{IVCC}	-0.3	–	6	V	–	P_4.1.3
IVCC_EXT External Linear Voltage Regulator Input voltage	V_{IVCC_EXT}	-0.3	–	6	V	–	P_4.1.4
Gate Driver Stages							
LSGD1,2 - PGND1,2 Lowside Gatedriver voltage	$V_{LSGD1,2-PGND1,2}$	-0.3	–	5.5	V	–	P_4.1.54
HSGD1,2 - SWN1,2 Highside Gatedriver voltage	$V_{HSGD1,2-SWN1,2}$	-0.3	–	5.5	V	2)	P_4.1.55
SWN1, SWN2 switching node voltage	$V_{SWN1,2}$	-1	–	60	V	–	P_4.1.6
(BST1-SWN1), (BST2-SWN2) Boostrap voltage	$V_{BST1,2-SWN1,2}$	-0.3	–	6	V	2)	P_4.1.7
BST1, BST2 Boostrap voltage related to GND	$V_{BST1,2}$	-0.3	–	65	V	–	P_4.1.8
SWCS Switch Current Sense Input voltage	V_{SWCS}	-0.3	–	0.3	V	–	P_4.1.9
SGND Switch Current Sense GND voltage	V_{SGND}	-0.3	–	0.3	V	–	P_4.1.10
SWCS-SGND Switch Current Sense differential voltage	$V_{SWCS-SGND}$	-0.5	–	0.5	V	–	P_4.1.11
PGND1,2 Power GND voltage	$V_{PGND1,2}$	-0.3	–	0.3	V	–	P_4.1.28
High voltage Pins							
IIN1, IIN2 Input Current monitor voltage	$V_{IIN1,2}$	-0.3	–	60	V	–	P_4.1.12

Table 3 Absolute Maximum Ratings[1)] (cont'd)
***T_J* = -40°C to +150°C; all voltages with respect to AGND, (unless otherwise specified)**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IIN1-IIN2 Input Current monitor differential voltage	$V_{IIN1-IIN2}$	-0.5	–	0.5	V	2)	P_4.1.13
FBH, FBL Feedback Error Amplifier voltage	$V_{FBH, FBL}$	-0.3	–	60	V	–	P_4.1.14
FBH-FBL Feedback Error Amplifier differential voltage	$V_{FBH-FBL}$	-0.5	–	0.5	V	2)	P_4.1.15
EN/INUVLO Device enable/input undervoltage lockout	$V_{EN/INUVLO}$	-0.3	–	60	V	–	P_4.1.16
Digital (I/O) Pins							
PWMI Digital Input voltage	V_{PWMI}	-0.3	–	5.5	V	–	P_4.1.17
CSN Voltage at Chip Select pin	V_{CSN}	-0.3	–	5.5	V	–	P_4.1.18
SCLK Voltage at Serial Clock pin	V_{SCLK}	-0.3	–	5.5	V	–	P_4.1.19
SI Voltage at Serial Input pin	V_{SI}	-0.3	–	5.5	V	–	P_4.1.20
SO Voltage at Serial Output pin	V_{SO}	-0.3	–	5.5	V	–	P_4.1.21
SYNC Synchronization Input voltage	V_{SYNC}	-0.3	–	5.5	V	–	P_4.1.22
LHI Limp Home Input Voltage	V_{LHI}	-0.3	–	5.5	V	–	P_4.1.58
Analog Pins							
VFB, VFB_VIN Output and Input Voltage feedback pins	V_{VFB}, V_{VFB_VIN}	-0.3	–	5.5	V	–	P_4.1.25
DIM_HALF Dual Range Output Current	V_{DIM_HALF}	-0.3	–	5.5	V	–	P_4.1.26
FILT MFS Filter pin voltage	V_{FILT}	-0.3	–	3	V	–	P_4.1.62
EOMFS, LEDCUR Flags output voltage	V_{FLAGS}	-0.3	–	5.5	V	–	P_4.1.61
SET Analog dimming Input voltage	V_{SET}	-0.3	–	5.5	V	–	P_4.1.29
COMP Compensation Input voltage	V_{COMP}	-0.3	–	3.6	V	–	P_4.1.30

Table 3 Absolute Maximum Ratings[1)] (cont'd)
***T_J* = -40°C to +150°C; all voltages with respect to AGND, (unless otherwise specified)**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SOFT_START Softstart Voltage	V_{SOFT_START}	-0.3	–	3.6	V	–	P_4.1.31
FREQ Voltage at frequency selection pin	V_{FREQ}	-0.3	–	3.6	V	–	P_4.1.32
IINMON Voltage at input monitor pin	V_{IINMON}	-0.3	–	3.6	V	–	P_4.1.33
IOUTMON Voltage at output monitor pin	$V_{IOUTMON}$	-0.3	–	5.5	V	–	P_4.1.34
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_4.1.35
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.36
ESD Susceptibility							
ESD Resistivity of all Pins	$V_{ESD,HBM}$	-2	–	2	kV	HBM[3)]	P_4.1.37
ESD Resistivity to GND	$V_{ESD,CDM}$	-500	–	500	V	CDM[4)]	P_4.1.38
ESD Resistivity of corner Pins to GND	V_{ESD,CDM_corner}	-750	–	750	V	CDM[4)]	P_4.1.39

1) Not subject to production test, specified by design.
2) Does not refer to GND
3) ESD susceptibility, Human Body Model "HBM" according to AEC Q100-002
4) ESD susceptibility, Charged Device Model "CDM" AECQ100-011 Rev. D

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Table 4 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Device Extended Supply Voltage Range	V_{VIN}	4.5	–	40	V	1) (parameter deviations possible)	P_4.2.1
Device Nominal Supply Voltage Range	V_{VIN}	8	–	36	V	–	P_4.2.2
Power Stage Voltage Range	V_{POW}	4.5	–	55	V	1)	P_4.2.5

Table 4 Functional Range (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Digital Supply Voltage	V_{DD}	3	–	5.5	V	–	P_4.2.3
Junction Temperature	T_j	-40	–	150	°C	–	P_4.2.4

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 5

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	0.9	–	K/W	1) 2)	P_4.3.1
Junction to Ambient	R_{thJA}	–	25	–	K/W	3) 2s2p	P_4.3.2

1) Not subject to production test, specified by design.

2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and the exposed pad are fixed to ambient temperature). Ta = 25°C; The IC is dissipating 1 W.

3) Specified R_{thJA} value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board; The device was simulated on a 76.2 x 114.3 x 1.5 mm board. The 2s2p board has 2 outer copper layers (2 x 70 µm Cu) and 2 inner copper layers (2 x 35 µm Cu). A thermal via (diameter = 0.3 mm and 25 µm plating) array was applied under the exposed pad and connected the first outer layer (top) to the first inner layer and second outer layer (bottom) of the JEDEC PCB. Ta = 25°C; The IC is dissipating 1 W.

5 Power Supply

The TLD5542-1 is supplied by the following pins:

- VIN (main supply voltage)
- VDD (digital supply voltage)
- IVCC_EXT (supply for internal gate driver stages)

The VIN supply, in combination with the VDD supply, provides internal supply voltages for the analog and digital blocks. In situations where VIN voltage drops below VDD voltage, an increased current consumption may be observed at the VDD pin.

The SPI and IO interfaces are supplied by the VDD pin.

IVCC_EXT is the supply for the low side driver stages, which is also used to charge, by means of external Schottky diodes, the bootstrap capacitors. These capacitors provide power to the high side driver stages. If no external voltage is available, IVCC_EXT pin must be shorted to IVCC, which is the output of an internal 5 V LDO.

The supply pins VIN, VDD and IVCC_EXT have undervoltage detections.

Undervoltage on VDD prevents the activation of the gate driver stages and any SPI communication (the SPI registers are reset). Undervoltage on IVCC_EXT or IVCC pins forces a deactivation of the driver stages, thus stopping the switching activity, but has no effect on the SPI register settings.

Moreover the double function pin EN/INUVLO can be used as an input undervoltage protection by placing a resistor divider from VIN to GND (refer to **Chapter 10.3**).

If EN/INUVLO undervoltage is detected, it will turn-off the IVCC voltage regulator, stop switching, stop communications and reset all the registers.

Figure 4 shows a basic concept drawing of the supply domains and interactions among pins VIN, VDD and IVCC/IVCC_EXT.

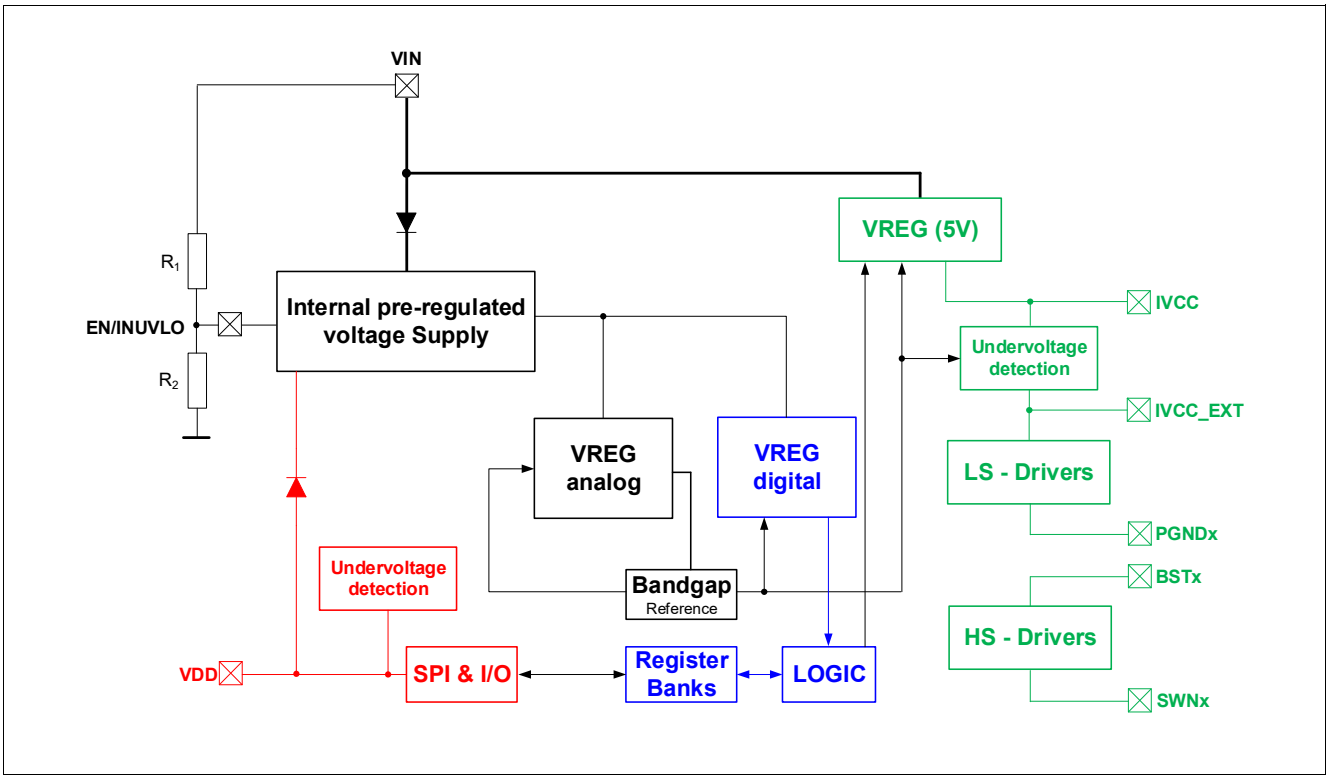


Figure 4 Power Supply Concept Drawing

Usage of EN/INUVLO pin in different applications

The pin EN/INUVLO is a double function pin and can be used to put the device into a low current consumption mode. An undervoltage threshold is fixed by placing an external resistor divider (A) in order to avoid low voltage operating conditions. This pin can be driven by a µC-port as shown in (B) (C).

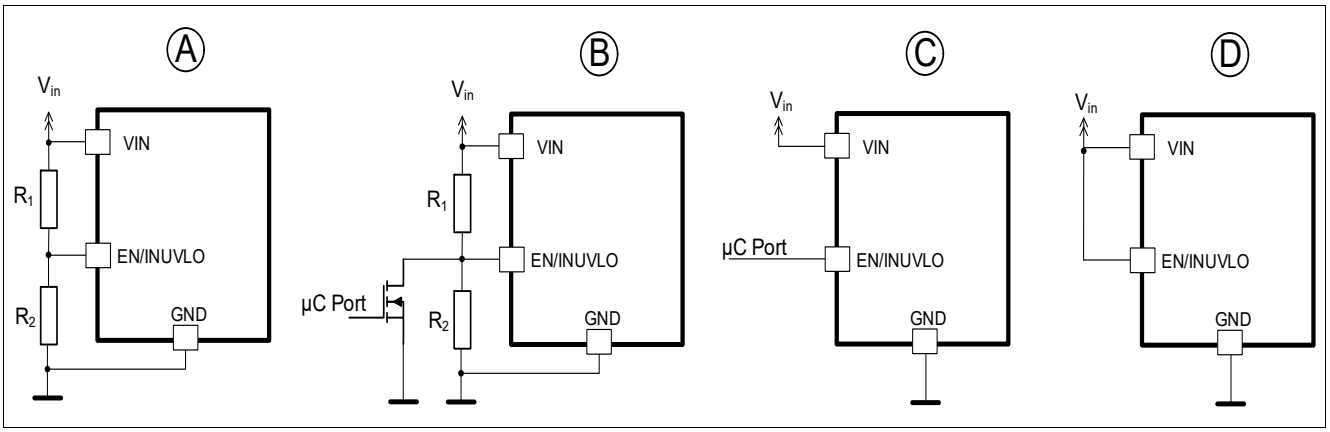


Figure 5 Usage of EN/INUVLO pin in different applications

5.1 Different Power States

TLD5542-1 has the following power states:

- SLEEP state
- IDLE state
- LIMP HOME state
- ACTIVE state

The transition between the power states is determined according to these variables after a filter time of max. 3 clock cycles:

- VIN level
- EN/INUVLO level
- IVCC level
- IVCC_EXT level
- VDD level
- LHI level
- `DVCCTRL.IDLE` bit state

The state diagram including the possible transitions is shown in **Figure 6**.

The Power-up condition is entered when the supply voltage V_{VIN} exceed its minimum supply voltage threshold $V_{VIN(ON)}$.

SLEEP

When the device is powered it enters the SLEEP state, all outputs are OFF and the SPI registers are reset, independently from the supply voltages at the pins VIN , VDD, IVCC, and IVCC_EXT. The current consumption is low. Refer to parameters: $I_{VDD(SLEEP)}$, and $I_{VIN(SLEEP)}$.

The transition from SLEEP to ACTIVE state requires a specified time: t_{ACTIVE}.

IDLE

In IDLE state, the current consumption of the device can reach the limits given by parameter I_{VDD} (P_5.3.4). The internal voltage regulator and IVCC linear regulator are working. Not all diagnosis functions are available (refer to **Chapter 10** for additional informations). In this state there is no switching activity, independently from the supply voltages V_{IN}, V_{DD}, IVCC and IVCC_EXT. When V_{DD} is available, the SPI registers are working and SPI communication is possible.

Limp Home

The Limp Home state is beneficial to fulfill system safety requirements and provides the possibility to maintain a defined current/voltage level on the output via a backup control circuitry. The backup control circuitry turns on required loads during a malfunction of the µC. For detailed info, refer to **Chapter 8**.

When Limp Home state is entered, SPI registers are reset to their default values and SPI communication is possible but only in read mode (SPI registers can be read but cannot be written). In order to regulate the output current/voltage, it is necessary that V_{IN} and IVCC_EXT are present and above their undervoltage threshold.

ACTIVE

In active state the device will start switching activity to provide power at the output only when PWMI = HIGH. To start the Highside gate drivers HSGD1,2 the voltage level $V_{BST1,2}$ - $V_{SWN1,2}$ needs to be above the threshold

$V_{BST1,2}$ - $V_{SWN1,2\_UVth}$. In ACTIVE state the device current consumption via V_{IN} and V_{DD} is dependent on the external MOSFET used and the switching frequency f_{SW}.

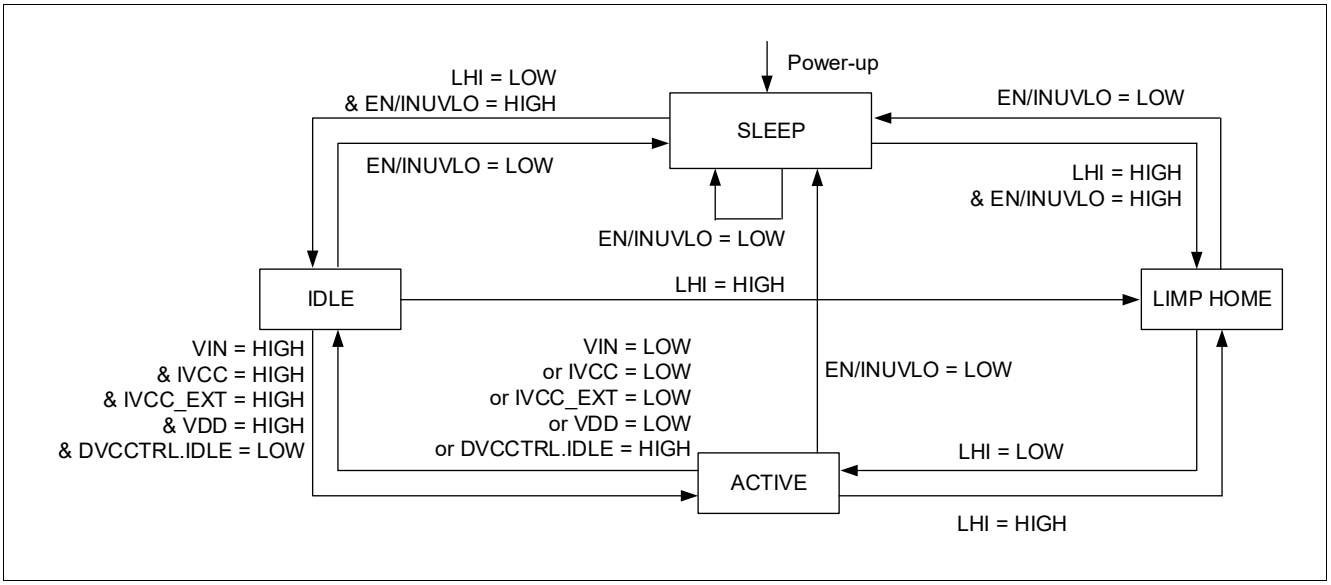


Figure 6 Simplified State Diagram

5.2 Different Possibilities to RESET the device

There are several reset triggers implemented in the device.

After any kind of reset, the Transmission Error Flag (`TER`) is set to HIGH.

Under Voltage Reset:

EN/INUVLO: When EN/INUVLO is below $V_{EN/INUVLOth}$ (P_5.3.7), the SPI interface is not working and all the registers are reset to their default values. In addition, the device enters SLEEP mode and the current consumption is minimized.

VDD: When V_{VDD} is below $V_{VDD(UV)}$ (P_5.3.6), the SPI interface is not working and all the registers are reset to their default values.

Reset via SPI command:

There is a command (`DVCCTRL.SWRST` = HIGH) available to RESET all writeable registers with the exception of MUXCTRL, to their default values. Note that the result coming from the Calibration routine, which is readable by the SPI when `DVCCTRL.ENCAL` = HIGH, is not reset by the SWRST.

Reset via Limp Home:

When Limp Home state is detected the registers are reset to the default values.

5.3 Electrical Characteristics

Table 6 EC Power Supply

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power Supply V_{IN}							
Input Voltage Startup	$V_{VIN(ON)}$	–	–	4.7	V	V_{IN} increasing; $V_{EN/INUVLO}$ = HIGH; V_{DD} = 5 V; IVCC = IVCC_EXT = 10 mA;	P_5.3.1
Input Undervoltage switch OFF	$V_{VIN(OFF)}$	–	–	4.5	V	V_{IN} decreasing; $V_{EN/INUVLO}$ = HIGH; V_{DD} = 5 V; IVCC = IVCC_EXT = 10 mA;	P_5.3.14
Device operating current	$I_{VIN(ACTIVE)}$	–	5	7	mA	[1)]ACTIVE mode; V_{PWMI} = 0 V; V_{VFB_VIN} = 1/(51+1)*V_{VIN}; V_{VFB}=0.7V	P_5.3.2
V_{IN} Sleep mode supply current	$I_{VIN(SLEEP)}$	–	–	1.5	µA	$V_{EN/INUVLO}$ = 0 V; V_{CSN} = V_{DD} = 5 V; V_{IN} = 13.5 V; V_{IVCC} = V_{IVCC_EXT}= 0 V;	P_5.3.3
Digital Power Supply V_{DD}							
Digital supply current	I_{VDD}	–	–	0.5	mA	V_{IN} = 13.5 V; f_{SCLK} = 0 Hz; V_{PWMI} = 0 V; V_{EN} =V_{CSN} = V_{DD} = 5 V;	P_5.3.4
Digital Supply Sleep mode current	$I_{VDD(SLEEP)}$	–	–	1.5	µA	$V_{EN/INUVLO}$ = 0 V; V_{CSN} = V_{DD} = 5 V; V_{IN} = 13.5 V; V_{IVCC} = V_{IVCC_EXT} = 0 V;	P_5.3.5
Undervoltage shutdown threshold voltage	$V_{VDD(UV)}$	1	–	3	V	V_{CSN} = V_{DD}; V_{SI} = V_{SCLK} = 0 V; SO from LOW to HIGH impedance;	P_5.3.6
EN/INUVLO Pin characteristics							
Input Undervoltage falling Threshold	$V_{EN/INUVLOth}$	1.6	1.75	1.9	V	–	P_5.3.7

Table 6 EC Power Supply (cont'd)

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
EN/INUVLO Rising Hysteresis	$V_{EN/INUVLO(hyst)}$	–	90	–	mV	1)	P_5.3.8
EN/INUVLO input Current LOW	$I_{EN/INUVLO(LOW)}$	0.45	0.89	1.34	µA	$V_{EN/INUVLO}$ = 0.8 V;	P_5.3.9
EN/INUVLO input Current HIGH	$I_{EN/INUVLO(HIGH)}$	1.1	2.2	3.3	µA	$V_{EN/INUVLO}$ = 2 V;	P_5.3.10
LHI Pin characteristics							
LOW level	$V_{LHI(L)}$	0	-	0.8	V	–	P_5.3.16
HIGH level	$V_{LHI(H)}$	2.0	-	5.5	V	–	P_5.3.17
L-Input pull-down current	$I_{LHI(L)}$	6	12	18	µA	V_{LHI} = 0.8 V;	P_5.3.18
H-Input pull-down current	$I_{LHI(H)}$	15	30	45	µA	V_{LHI} = 2.0 V;	P_5.3.19
Timings							
SLEEP mode to ACTIVE time	t_{ACTIVE}	–	–	0.7	ms	1) $V_{IVCC} = V_{IVCC\_EXT}$; C_{IVCC} = 10 µF; V_{IN} = 13.5 V; V_{DD} = 5 V;	P_5.3.11

1) Not subject to production test, specified by design.

6 Regulator Description

The TLD5542-1 includes all of the functions necessary to provide constant current to the output as usually required to drive LEDs. A voltage mode regulation can also be implemented (Refer to **Chapter 6.6**).

It is designed to control 4 gate driver outputs in a H-Bridge topology by using only one inductor and 4 external MOSFETs. This topology is able to operate in high power Boost, Buck-Boost and Buck mode applications with maximum efficiency.

The transition between the different regulation modes is done automatically by the device itself, with respect to the application boundary conditions.

The Buck-Boost to Boost transition can be smoothed by mean of BB_BST_CMP bitfield.

A SPI flag provides mode feedback to the µC (refer to SPI bits `REGUSETMON.REGUMODFB`).

6.1 Regulator Diagram Description

The analog current control loop (A5, A6 with complessive gain = $IFBx_{gm}$) connected to the sensing pins FBL, FBH regulates the output current.

The regulator function is implemented by a pulse width modulated (PWM) current mode controller. The error in the output current loop is used to determine the appropriate duty cycle to get a constant output current.

An external compensation network (R_{COMP}, C_{COMP}) is used to adjust the control loop to various application boundary conditions.

The inductor current for the current mode loop is sensed by the R_{SWCS} resistor.

R_{SWCS} is used also to limit the maximum external switches / inductor current.

If the Voltage across R_{SWCS} exceeds its overcurrent threshold (V_{SWCS_buck} or V_{SWCS_boost} for buck or boost operation respectively) the device reduces the duty cycle in order to bring the switches current below the imposed limit.

The current mode controller has a built-in slope compensation as well to prevent sub-harmonic oscillations.

The control loop logic block (LOGIC) provides a PWM signal to four internal gate drivers. The gate drivers (HSGD1,2 and LSGD1,2) are used to drive external MOSFETs in an H-Bridge setup . Once the soft start expires a forced CCM regulation mode is performed.

The control loop block diagram displayed in **Figure 7** shows a typical constant current application. The voltage across R_{FB} sets the output current.

The output current is adjusted via the SPI register `LEDCURRADIM.ADIMVAL` plus an offset trimming on `LEDCURRCAL.CALIBVAL` register. Refer to **Chapter 8.1** for more details.

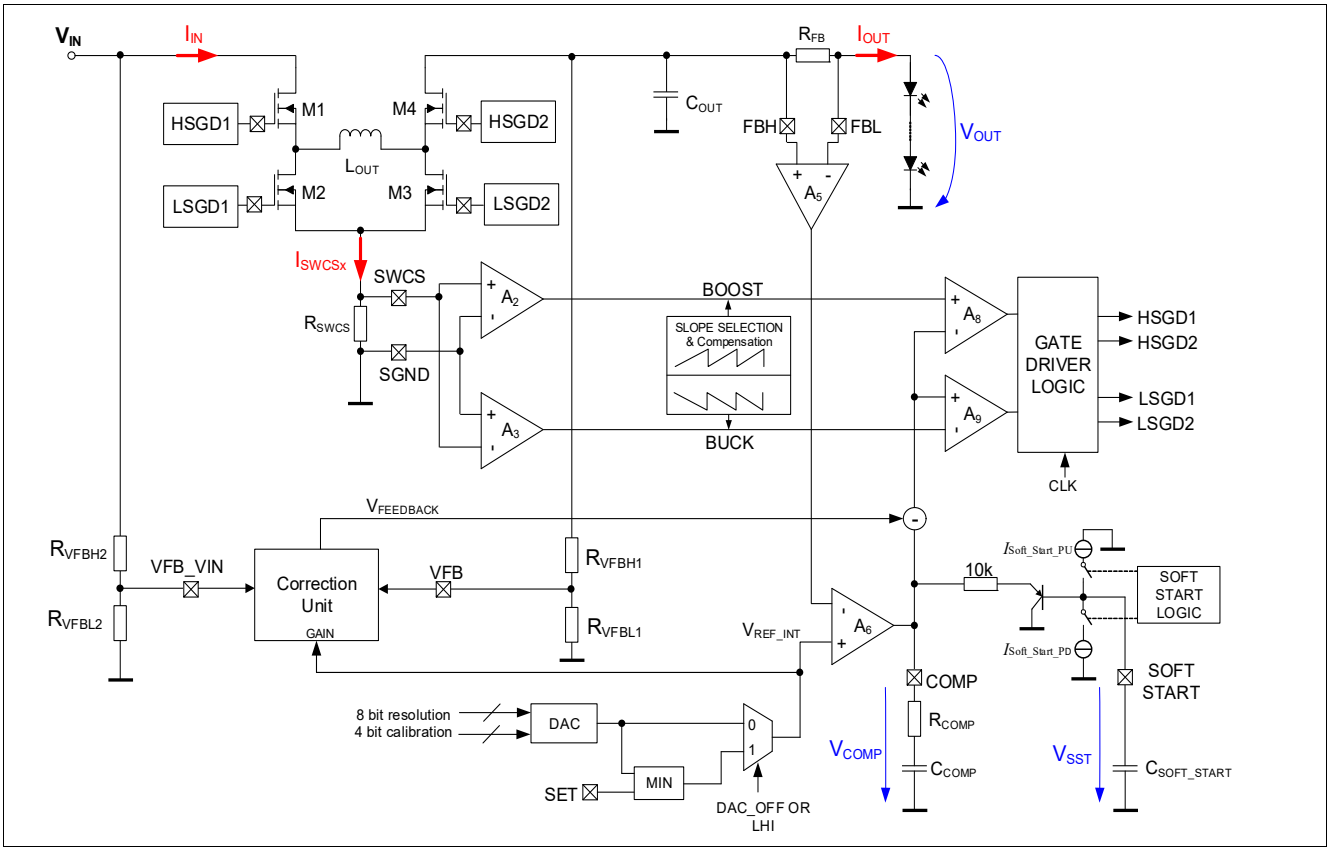


Figure 7 Regulator Block Diagram - TLD5542-1

An Infineon proprietary correction unit (see **Figure 7**) ensures optimum performance on MFS architecture, minimizing dependency of comp voltage by the analog dimming value, and reduces overshoots during load jump up.

The correction unit provides an input voltage feedback to the regulator loop, proportional to Vout/Vin through the VFB/VFB_VIN signals. Therefore, the 2 voltage dividers at VFB and VIN_VFB are related to each other, and their ratio is setting the feedback amount. Correction unit feedback can be disabled by setting SWTMOD.VFB_VIN_OFF bitfield.

The negative feedback applied to V_{COMP} is also proportional to the analog dimming value. The smaller the analog dimming value, the larger is the feedback voltage:

$$V_{FEEDBACK} \approx 0.05 \cdot \frac{V_{VFB}}{V_{VFB_{VIN}}} \cdot (100\% - ADIM[\%]) \quad [V] \tag{6.1}$$

In order to ensure good accuracy on VFB_VIN reading, the total resistance on the divider should be less than 100kΩ. It is recommended to have VFB_VIN / VFB voltage dividers ratio equal to 1 / 1.5 (I.E. RVFBH2=RVFBH1=51kΩ , RVFBL2=1kΩ , RVFBL1 =1.5kΩ).

If the input voltage feedback is too high (I.E. RVFBL2 is too low), V_{COMP} may saturate toward the operating range limit (2V) and the output current regulation would be affected. Minimum temperature, maximum Vout/Vin ratio and minimum ADIM value shall be considered as worst case condition when checking for V_{COMP} dynamic operating range.

6.2 Adjustable Soft Start Ramp

The soft start routine has 2 functionalities:

- Fault management: fault mask and wait-before-retry time (**Figure 8** and chapter **Chapter 10.2**)
- Limit input inrush current and output overshoots by limiting Vcomp (**Figure 7**) in boost mode

The soft start routine is applied in two cases:

- At startup (first PWM rise after IDLE to ACTIVE transition)
- After output short to GND detection

The soft start routine is active during the rising and falling edges of the VSST. The soft start timing is defined by a capacitor placed at the SOFT_START pin and the pull-up and pull down current sources ($I_{Soft\_Start\_PU}$, $I_{Soft\_Start\_PD}$).

Minimum value for soft start capacitor has to be designed such that, at startup, the output voltage exceeds the short to ground threshold (VFBH_S2G_inc), before the soft start voltage reaches $V_{SOFT\_START\_LOFF}$. Minimum temperature and minimum input voltage shall be considered as worst case condition for previously mentioned dimensioning.

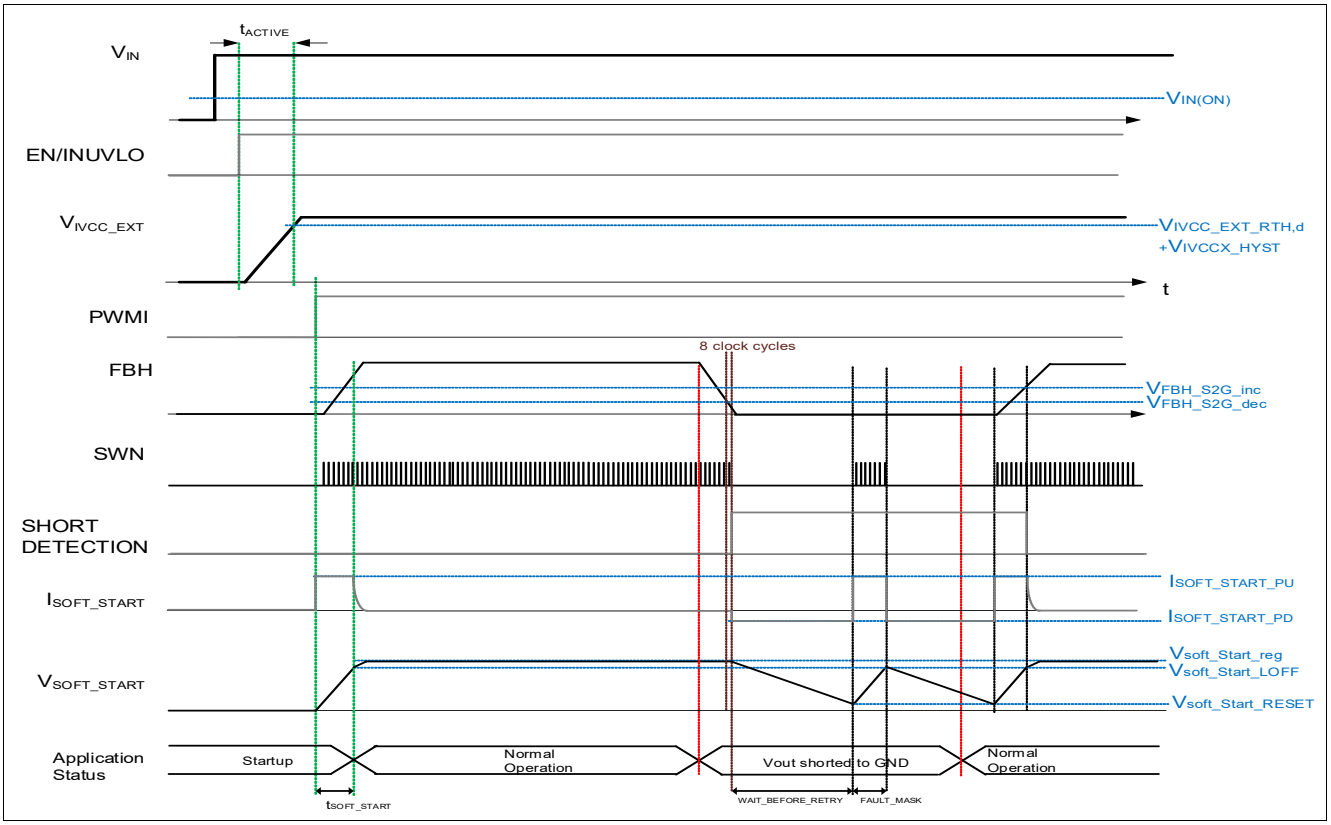


Figure 8 Soft Start timing diagram on a short to ground detected by the FBH pin

Soft Start rising edge time is aproximately:

$$t_{SOFT\_START} = V_{Soft\_Start\_LOFF} \cdot \frac{C_{Soft\_Start}}{I_{Soft\_Start\_PU}} \quad (6.2)$$

The Soft Start routine limits the inrush current during boost mode by clamping the COMP pin through a buffer as in **Figure 7**. Therefore this functionality is effective only when Soft Start capacitor is sufficiently larger than the comp capacitor.

If the inductor current is low during the soft start rising edge, DCM is enabled and MOSFET M4 is disabled. If the inductor current increases then M4 may get enabled.

After the soft start has been completed (V_{SOFT_START} > $V_{SOFT\_START\_LOFF}$) CCM is forced and M4 is permanently enabled, independently from the inductor current level.

To avoid overshoot at startup on voltage regulators, may be useful to keep CCM forced also during soft start by setting CCM_4EVER bitfield.

If a short circuit on the output is detected, a pull-down current source $I_{SOFT\_START\_PD}$ (P_6.4.20) is activated. This current brings down the V_{SOFT_START} until $V_{SOFT\_START\_RESET}$ (P_6.4.22) is reached. Afterwards the pull-up current source $I_{SOFT\_START\_PU}$ (P_6.4.19) turns on again. If the fault condition hasn't been removed until $V_{SOFT\_START\_LOFF}$ (P_6.4.21) is reached, the pull-down current source turns back on again, initiating a new cycle. This will continue until the fault is removed.

If a low duty cycle PWMI is applied at startup, the output voltage may be still below the short to ground threshold once the soft start fault mask is expired. Therefore the TLD5542-1 has a special feature in order to prevent short to ground in case of startup with low duty cycle PWM.

At first PWMI rise after IDLE to ACTIVE transition, the internal PWM signal is extended if the following conditions are met:

- A capacitor is connected to the IOUTMON pin (suggested 220pF)
- IDLE mode is kept for less than 10ms
- PWMI rise is provided within 10ms from IDLE to ACTIVE transition

The PWMI extension last until one of the two following conditions is reached:

- Until V_{SOFT_START} exceeds $V_{Soft\_Start\_LOFF}$
- Until $V_{FBH\text{-}FBL}$ exceeds $V_{FBH\_FBL\_IN}$

6.3 Switching Frequency setup

The switching frequency can be set from 200 kHz to 700 kHz by an external resistor connected from the FREQ pin to GND or by supplying a sync signal as specified in chapter **Chapter 11.2**. Select the switching frequency with an external resistor according to the graph in **Figure 9** or the following approximate formulas.

$$f_{SW}[kHz] = 5375 * (R_{FREQ}[k\Omega])^{-0.8} \quad (6.3)$$

$$R_{FREQ}[k\Omega] = 46023 * (f_{SW}[kHz])^{-1.25} \quad (6.4)$$

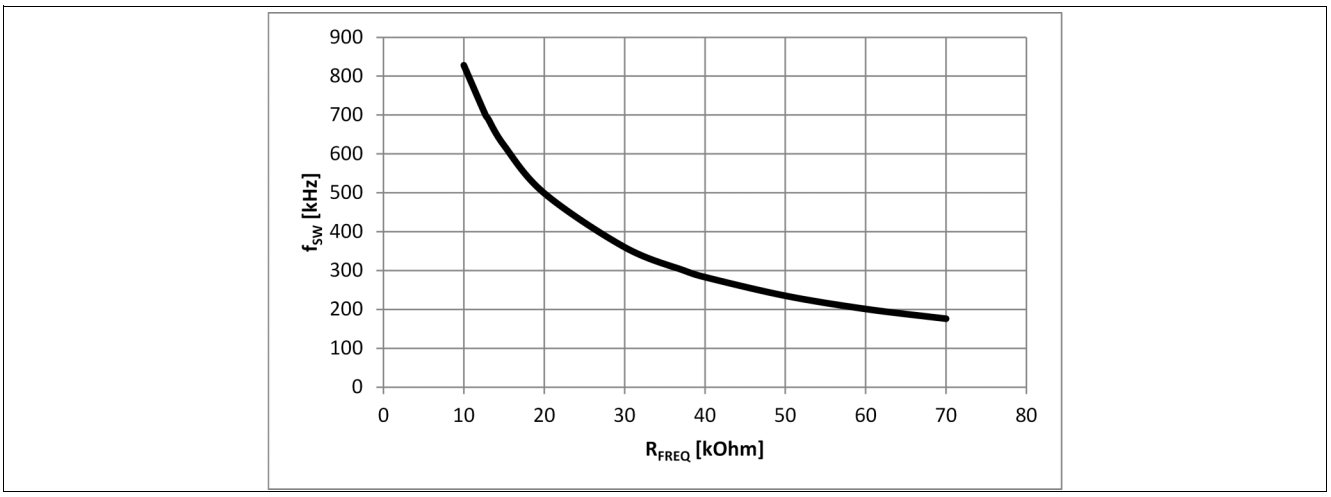


Figure 9 Switching Frequency f_{SW} versus Frequency Select Resistor to GND R_{FREQ}

6.4 Operation of 4 switches H-Bridge architecture

Inductor L_{OUT} connects in an H-Bridge configuration with 4 external N channel MOSFETs (M1, M2, M3 & M4)

	BOOST MODE	BUCK-BOOST MODE	BUCK MODE
M1	ON	PWM	PWM
M2	OFF	PWM	PWM
M3	PWM	PWM	OFF
M4	PWM	PWM	ON

Figure 10 4 switches H-Bridge architecture Transistor Status summary

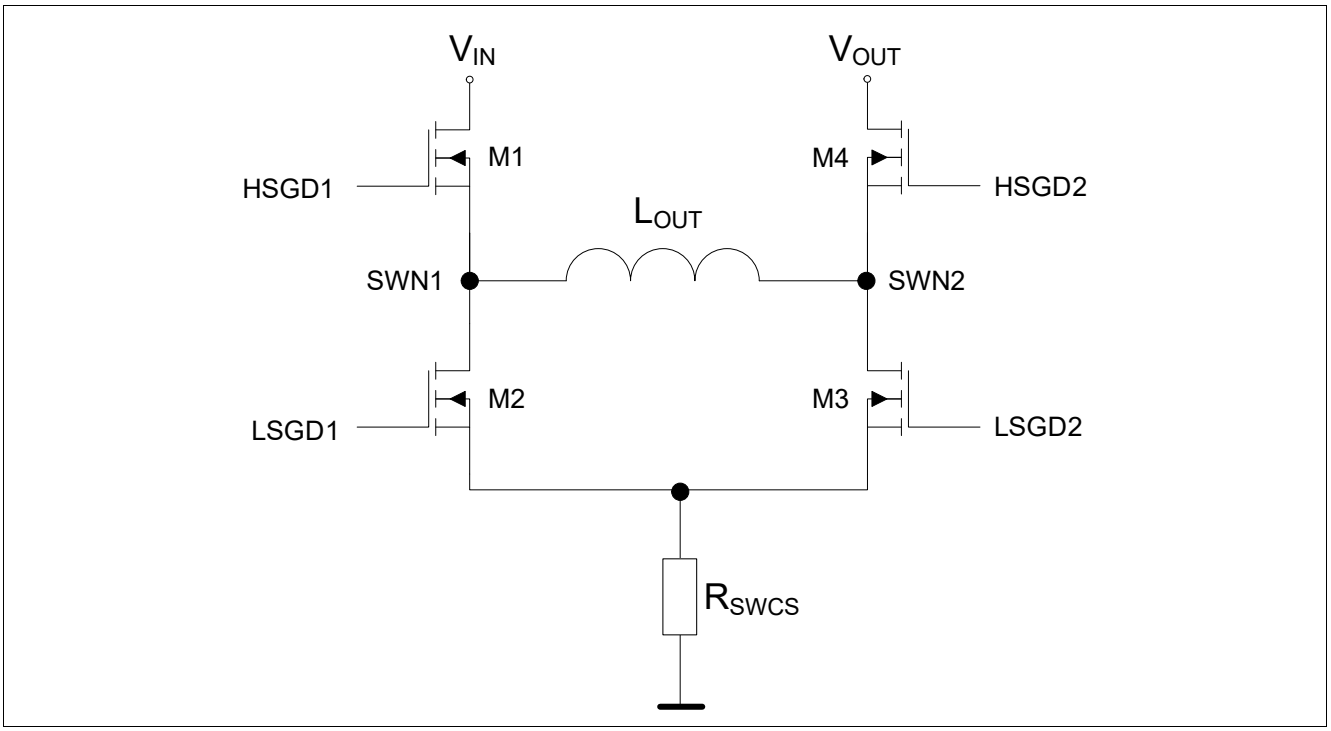


Figure 11 4 switches H-Bridge architecture overview

6.4.1 Boost mode ($V_{IN} < V_{OUT}$)

- M1 is always ON, M2 is always OFF
- Every cycle M3 turns ON first and inductor current is sensed (peak current control)
- M3 stays ON until the upper reference threshold is reached across R_{SWCS} (Energizing)
- M3 turns OFF, M4 turns ON until the end of the cycle (Recirculation)
- Switches M3 and M4 alternate, behaving like a typical synchronous boost Regulator (see **Figure 12**)

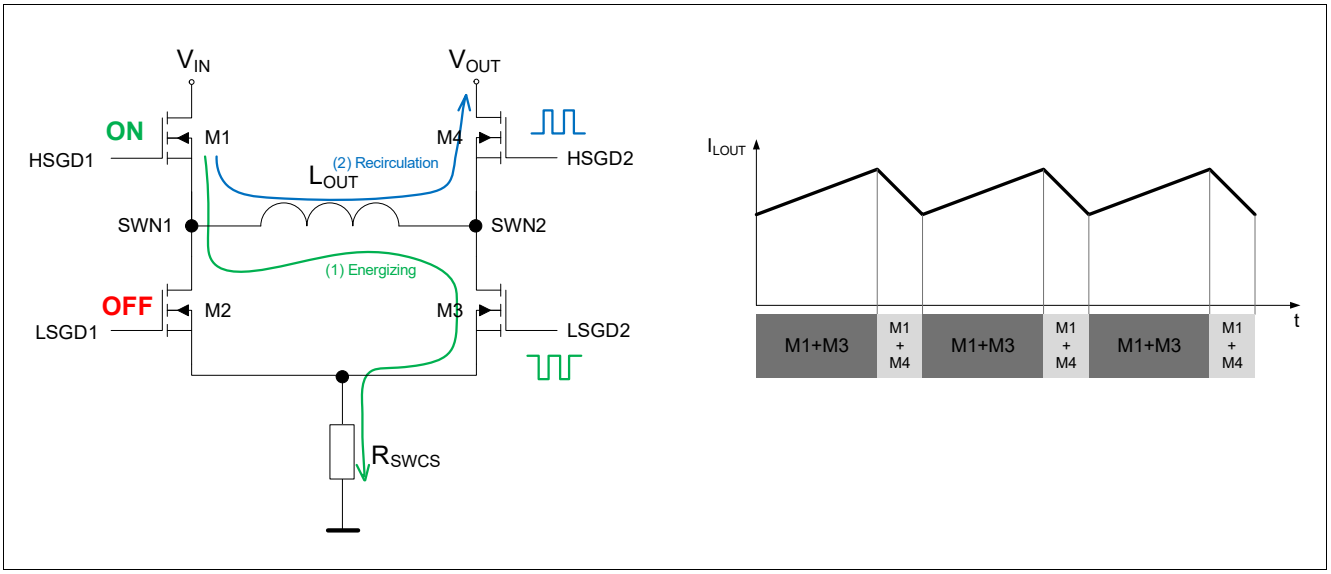


Figure 12 4 switches H-Bridge architecture in BOOST mode

Simplified comparison of 4 switches H-Bridge architecture to traditional asynchronous Boost approach.

- M2 is always OFF in this mode (open)
- M1 is always ON in this mode (closed connection of inductor to V_{IN})
- M4 acts as a synchronous diode, with significantly lower conduction power losses (I^2 x R_{DSON} vs. 0.7 V x I)

Note: Diode is source of losses and lower system efficiency!

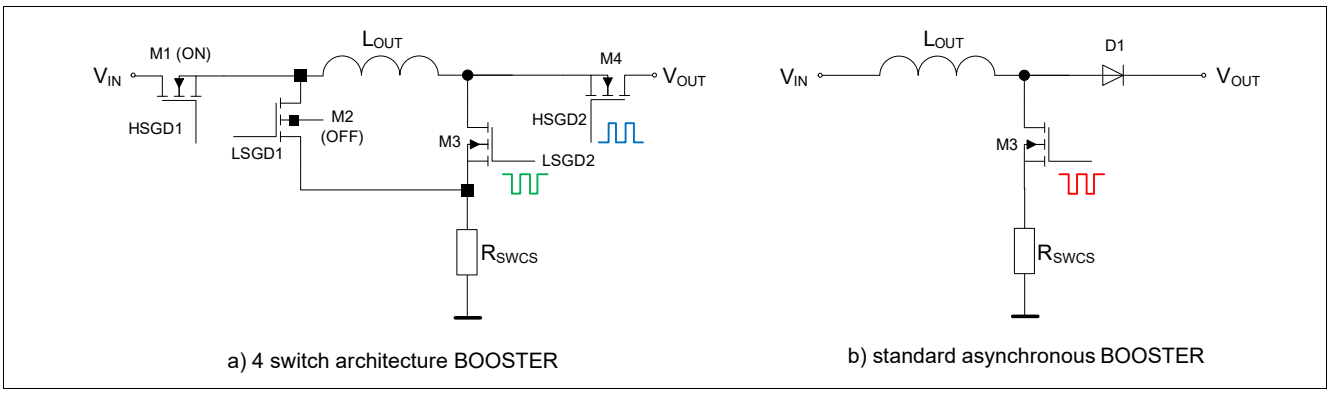


Figure 13 4 switches H-Bridge architecture in BOOST mode compared to standard async Booster

6.4.2 Buck mode (V_{IN} > V_{OUT})

- M4 is always ON, M3 is always OFF
- Every cycle M2 turns ON and inductor current is sensed (valley current control)
- M2 stays ON until the lower reference threshold is reached across R_{SWCS} (Recirculation)
- M2 turns OFF, M1 turns ON until the end of the cycle (Energizing)
- Switches M1 and M2 alternate, behaving like a typical synchronous BUCK Regulator (see **Figure 14**)

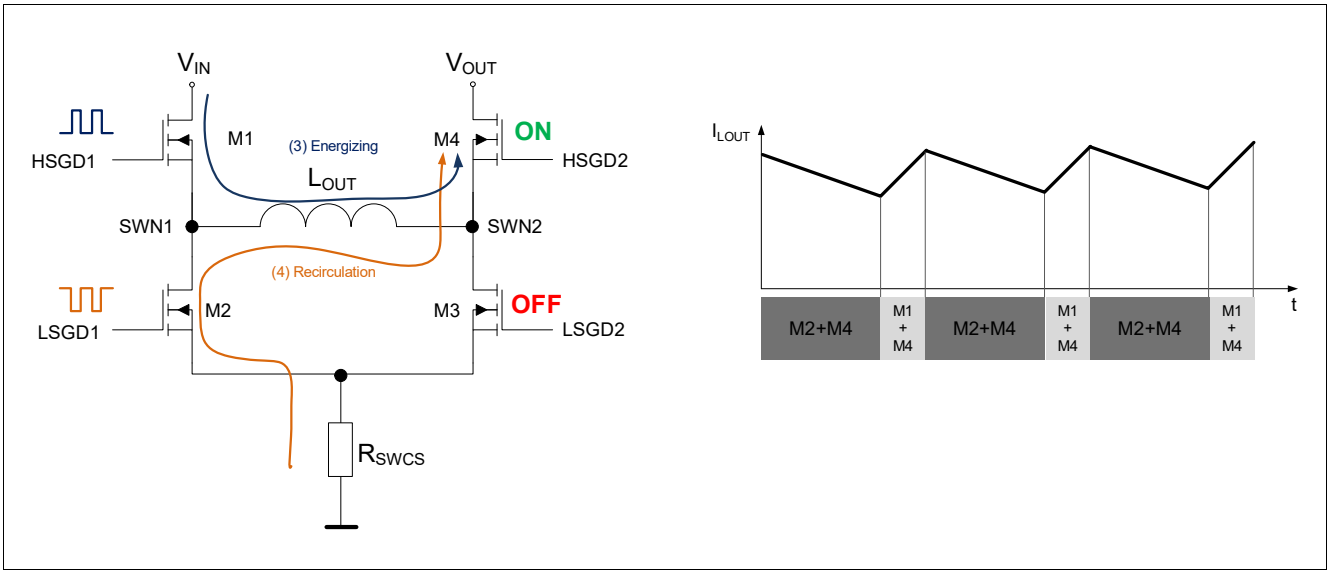


Figure 14 4 switches H-Bridge architecture in BUCK mode

Simplified comparison of 4 switches architecture to traditional asynchronous Buck approach.

- M3 is always OFF in this mode (open).
- M4 is always ON in this mode (closed connection inductor to V_{OUT}).
- M2 acts as a synchronous diode, with significantly lower conduction losses (I^2 x R_{DSON} vs. 0.7 V x I)

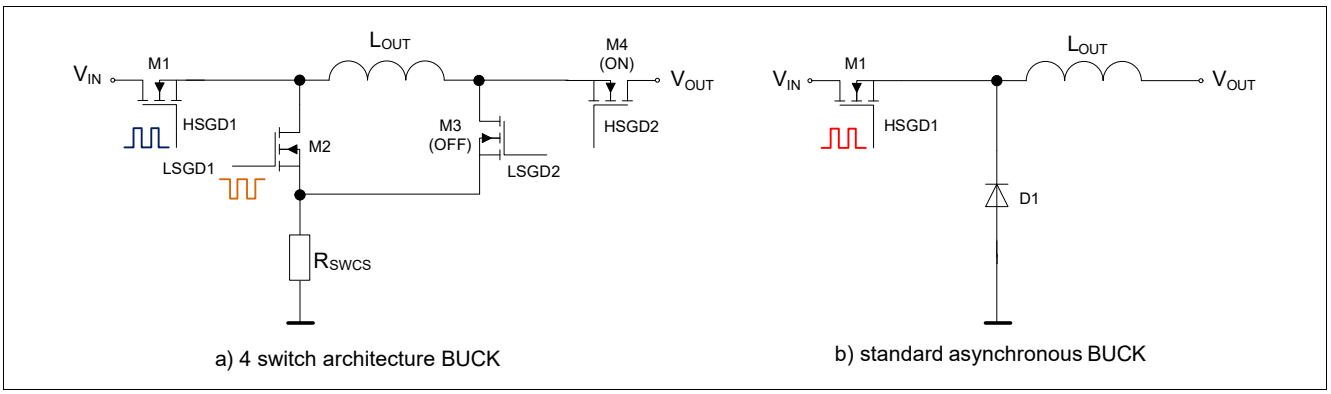


Figure 15 4 switches H-Bridge architecture in BUCK mode compared to standard async BUCK

6.4.3 Buck-Boost mode (V_{IN} ~ V_{OUT})

- When V_{IN} is close to V_{OUT} the controller is in Buck-Boost operation
- All switches are switching in buck-boost operation. The direct energy transfer from the Input to the output (M1+M4 = ON) is beneficial to reduce ripple current and improves the energy efficiency of the Buck-Boost control scheme
- The two buck boost waveforms and switching behaviors are displayed in **Figure 16** below

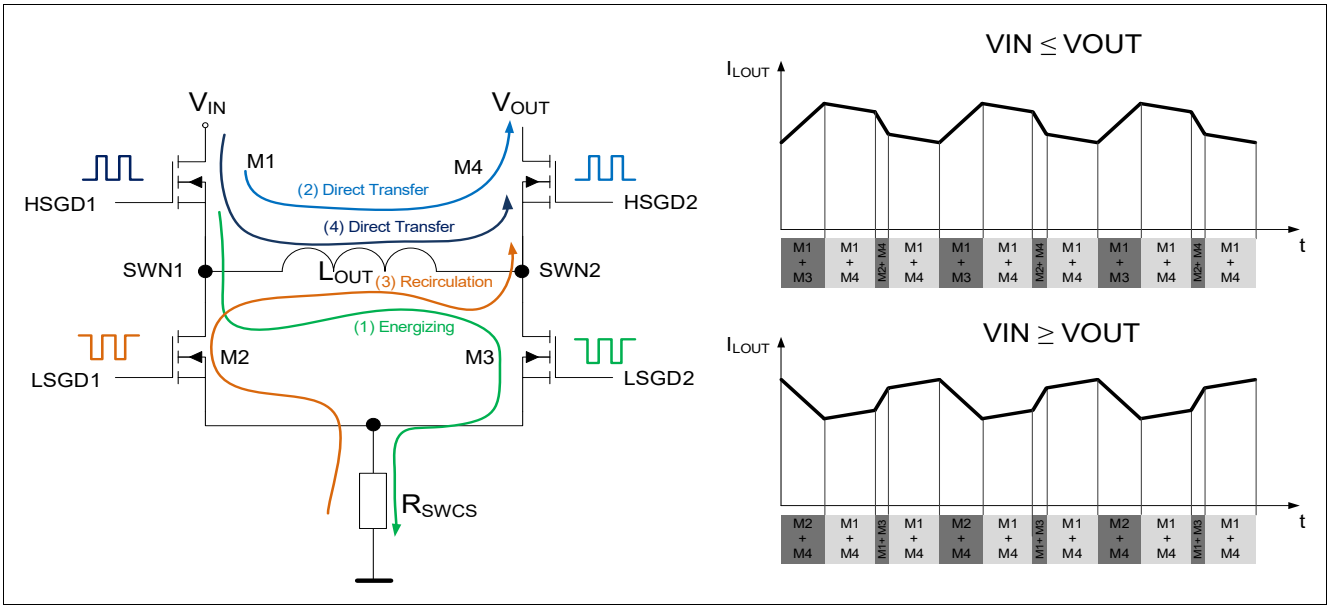


Figure 16 4 switches H-Bridge architecture in BUCK-BOOST mode

6.5 Fast Output Discharge Operation Mode - Multi Floating Switches Topology

Multiple light functions can be driven by a single DC/DC converter adopting a Multi Floating Switch (MFS) topology. In a MFS topology, each LED Function is connected in series and can be independently turned off via a bypass switch. Because of the series connections, all the functions are driven with the same current (except for Loads with complementary duty cycle I.E. DRL, LB). Different brightness can be achieved with individual PWM duty cycles.

In order to drive different LED functions in this topology, a Buck Boost converter is probably needed. A single stage buck boost topology has high efficiency buts requires several µF of output capacitance (C_{OUT}). The extra voltage present on this capacitor, when shorting one function to turn it off, may create a current spike in the LEDs that have to remain on.

The TLD5542-1 has a dedicated state machine which controls a fast discharge of the output cap to a desired fraction of the initial output voltage. This Fast Output Discharge feature (F.D.), if carefully configured, limits the current spike during load jump events preventing LED damage.

An Example of the Multi Floating Switch topology architecture and operation are shown in **Figure 17**

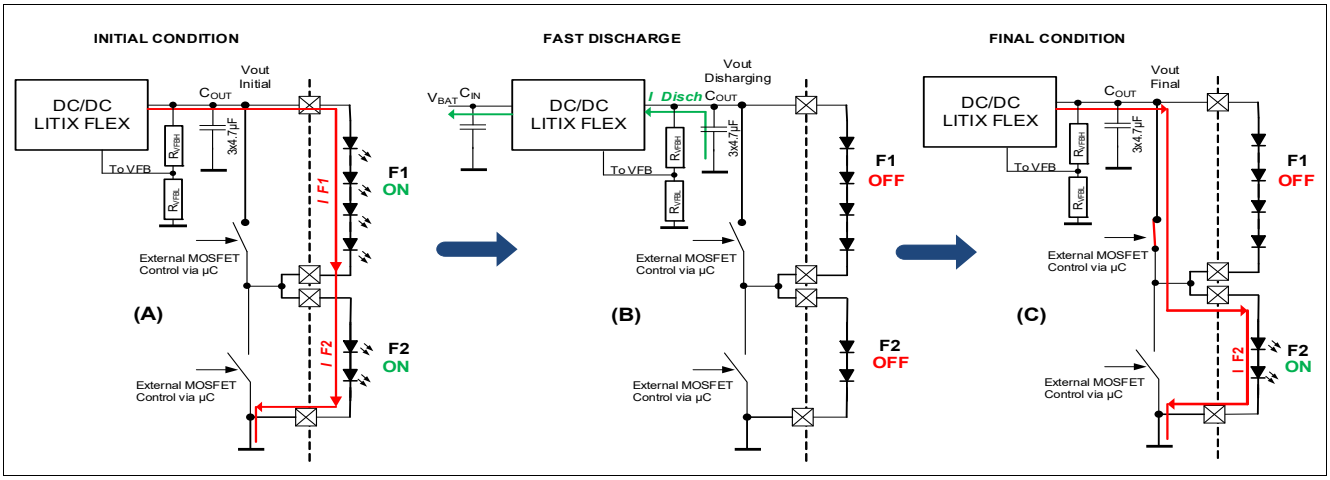


Figure 17 Multi Floating Switch topology: operation sequence on 2 Functions: (F1+F2) to (F2)

The F.D. operation consists of discharging the capacitor C_{OUT} to the final load voltage (**Figure 17**-B) before the bypass switch closure. The external Microcontroller Software has to take care of the synchronization between the TLD5542-1 F.D. operation and the bypass Switches activation.

The discharged energy from C_{OUT} is recovered back to the Input capacitor C_{IN} which could cause a small overshoot on the C_{IN} itself. This feature allows high efficiency designs also when PWM operation with repetitive Load Jumps is needed.

The F.D. feature is needed when a negative V_{OUT} step is performed, so when one or more LED functions are switched off. If additional LED functions are turned on, increasing the output voltage, the F.D. does not have to be used.

In case analog dimming is performed during a load Jump (I.E. from 1A LB to 300mA DRL), even with a positive V_{OUT} step, a discharge of the COMP capacitor could be necessary.

In MFS topologies, a short interruption of the current is observed during the Load Transitions (either positive or negative) in all the functions, until V_{OUT} is stable and the device control loop is able to provide the target output current.

We will refer to any Voltage-Current or Load configuration just before the Load Jump as "Initial" (**Figure 17**-A), while we will refer to any value after the system is in the new Load configuration as "Final" (**Figure 17**-C).

Set the Target C_{OUT} discharge voltage

The Target output voltage ($V_{OUTFinal}$) of an F.D. operation is communicated to the TLD5542-1 as a fraction of the V_{OUT} at the beginning of the Jump ($V_{OUTInitial}$), and not as an absolute Value.

In order to F.D. the output Capacitor to a desired Ratio of the initial voltage, two SPI commands have to be sent to the TLD5542-1 register MFSSETUP1.

- The first is to write in the MFSSETUP1.LEDCHAIN the Ratio Denominator
- The second is to write in the MFSSETUP1 register the Ratio Numerator and the Start Of Multi Floating Switch, respectively in the LEDCHAIN and SOMFS bitfields

The time interval between the Ratio Denominator and Numerator SPI commands, needs to be long enough to sample the Initial Voltage of the F.D. in the FILT capacitor.

After the second command, as soon as the Chip select is raised the F.D. begins. The final output voltage of the F.D. operation, after a MFS routine is correctly performed, will be approximately:

$$V_{OUTFinal} = \frac{RatioNumerator}{RatioDenominator} \cdot V_{OUTInitial} \quad (6.5)$$

If RatioNumerator is bigger than RatioDenominator, the output voltage remains constant, but the COMP capacitor is discharged during all the TPREP

F.D. operation will exit if the output voltage reaches $V_{FBH\_S2G\_dec}$.

Example:

In order to jump from 6LED (18 V) to 2LEDs (6 V), the Ratio is 1/3 of initial voltage.

So the 2 SPI commands that have to be sent are:

Spi command 1: set MFSSETUP1 to 0x06 (Ratio Denominator = 6)

Spi command 2: set MFSSETUP1 to 0x22 (Ratio Numerator+SOMFS = 0x02+0x20)

Preparation Time t_{prep}:

The TLD5542-1 enables the user to set a period t_{prep} on the load jump, where C_{COMP} is discharged continuously with a constant current (IEA_neg).

The Preparation Time has to be sufficient for the capacitor C_{COMP} to be discharged the desired value.

$$t_{DischComp} = Dvcomp\frac{C_{COMP}}{I_{EA\_neg}} = t_{prep} \quad (6.6)$$

In order to set a preparation time on the TLD5542-1, a SPI command has to be sent to the register `MFSSETUP2.MFSDLY`).

The **Equation (6.7)** below describes the relationship between the switching frequency f_{SW} and the MFSSETUP2.MFSDLY register value.

$$t_{prep} = \frac{1}{f_{SW}} \cdot \left[2 + (MFSDLY)_{dec}\right] \quad (6.7)$$

For SPI command details refer to **Chapter 12.6**.

The F.D. procedure is automatically extended until Cout capacitor is discharged to the target value, and Tprep is expired. If there is the need to do not discharge the CCOMP, but Discharge only the Vout , is possible to set MFSSETUP2.MFSDLY to 0 on a F.D. routine, Cout will be anyway discharged to the target voltage.

Fast Discharge Phase

After programming the desired output voltage Ratio via SPI , the right Preparation Time and activating the state machine (`MFSSETUP1.SOMFS` = HIGH) the TLD5542-1 inverts the inductor current I_L and keeps its negative peak at a reduced switch current limit I_{SwLim} until the V_{OUT} reaches the desired target.

$$I_{SwLim} \approx \frac{V_{SWCS\_boost}}{R_{SWCS}} \cdot \frac{2}{3} \quad (6.8)$$

Figure 18 displays the relation of inductor current I_L and the output voltage V_{OUT} during a fast output discharge operation mode.

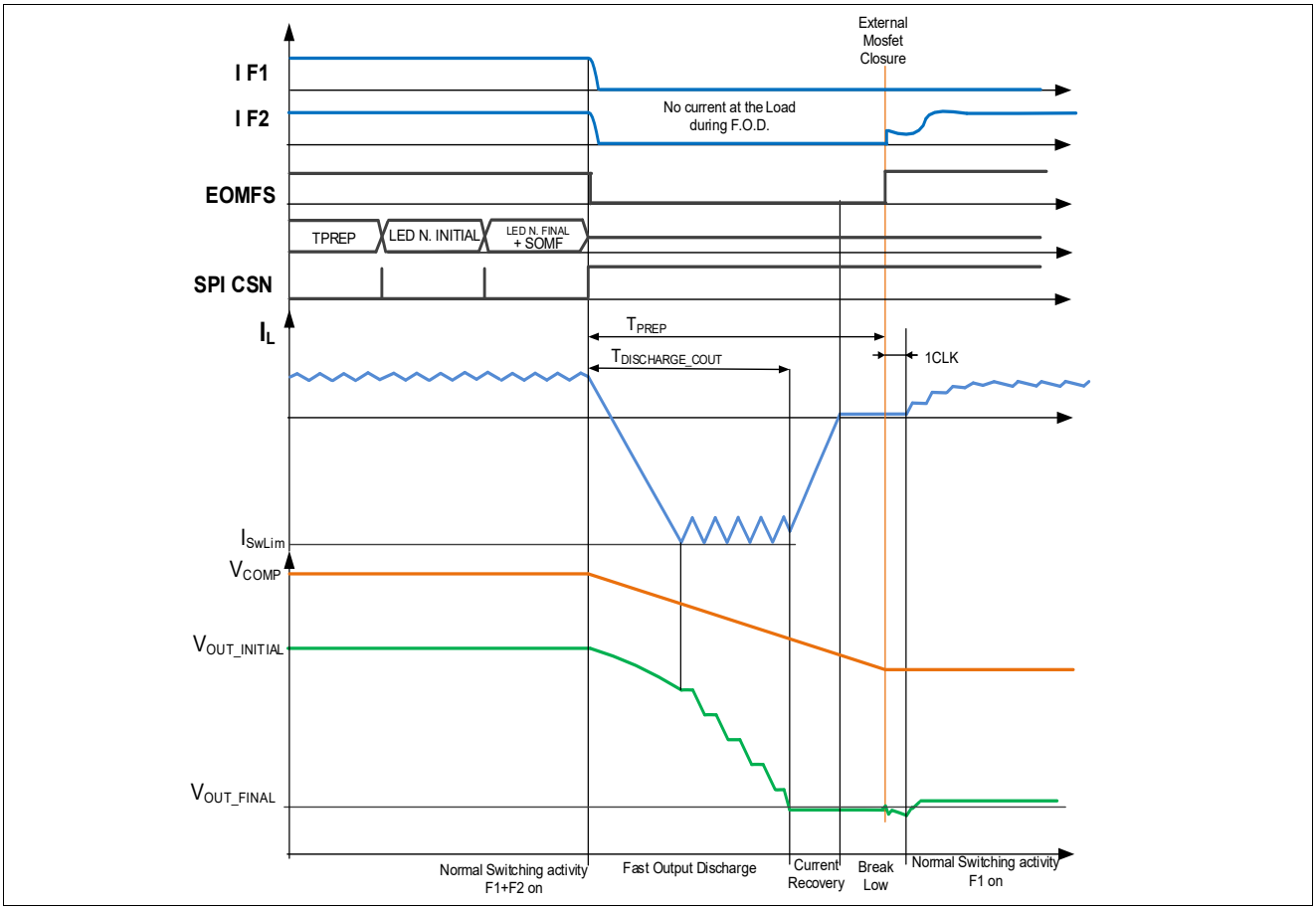


Figure 18 Fast Output Discharge timing diagram

If the discharge current limit I_{SwLim} needs to be reduced further , the `MFSSETUP1.ILIM_HALF_MFS` bit can be used to reduce it to the **Equation (6.9)** (only during the F.D. phase and not in normal operation), see SPI Chapter for further details **Chapter 12.6**.

$$I_{SwLim} \approx \frac{V_{SWCS\_boost}}{R_{SWCS}} \cdot \frac{1}{2} \tag{6.9}$$

Setting the EA_IOUT_MFS bit will reduce (only during the F.D. phase) the saturation current of the error amplifier A6 (IEA_neg) that discharges the Comp capacitor.

Once V_{OUT} reaches the desired target, the current recovery phase brings I_L from a negative value back to 0 A and the device stays in “Brake-Low condition” (both Lowside gatedrivers = ON) until the programmed preparation time (`MFSSETUP2.MFSDLY`) expires.

Only when both the current recovery phase has ended and t_{prep} is expired an SPI flag(STD bit EOMFS) and the pin EOMFS are set to HIGH. One clock cycle after EOMFS is asserted, the TLD5542-1 starts automatically switching again.

Figure 18 displays one Fast Output Discharge cycle.

Sequence of operations to perform a Fast Output Discharge

In order to perform a F.D .operation, the user has to :

- Send via SPI to `MFSSETUP1.LEDCHAIN` the Ratio Denominator.
- Set via SPI an adequate Preparation Time
- Send via SPI to `MFSSETUP1.LEDCHAIN` the Ration Numerator + SOMFS

- Wait until preparation time is expired and Vout has reached the target value (EOMFS is asserted)
- Adjust the Floating switches to the new configuration

In case of short to GND the routine is not executed or it is aborted.

At startup (after EN = High), if PWM has never been set to HIGH, F.D. routine can not be executed.

If a F.D. is needed just after device enable (for instance to lower the output voltage after a low battery reset), PWMI has to be set to 1 before the SOMFS command, and the F.D. procedure will be executed only once the SS is expired.

Other than for the 2 above exceptions, it is always possible to perform F.D. independently from PWM signal and output overvoltage condition.

6.6 Programming Output Voltage (Constant Voltage Regulation)

For a voltage regulator, the output voltage can be set by selecting the values R_{FB1}, R_{FB2} according to the following **Equation (6.10)**:

$$V_{OUT} = \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \cdot V_{FBH-FBL} \tag{6.10}$$

Refer to the voltage regulator application drawing on **Figure 45**.

After the output voltage is fixed via the resistor divider, the value can be changed via the Analog Dimming bits `ADIMVAL`.

6.7 Electrical Characteristics

Table 7 EC Regulator

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Regulator:							
$V_{FBH-FBL\_REF}$ reference voltage	$V_{FBH-FBL\_REF}$	145.5	150	154.5	mV	ADIMVAL = *240;*	P_6.4.1
$V_{FBH-FBL\_REF}$ reference voltage	$V_{FBH-FBL\_REF}$	12	15	18	mV	ADIMVAL =*24;* Calibration Procedure not performed	P_6.4.5
FBH Bias current @ highside sensing setup	I_{FBH_HSS}	65	110	155	µA	1) V_{FBL} = 7 V; $V_{FBH - FBL}$ = 150 mV;	P_6.4.8
FBL Bias current @ highside sensing setup	I_{FBL_HSS}	17	30	43	µA	1) V_{FBL} = 7 V; $V_{FBH - FBL}$ = 150 mV;	P_6.4.9
A6 sense Amp +sat current	I_{EA_pos}	25	29	33	µA	1) VCOMP = 1V; ADIMVAL = 240; $V_{FBH - FBL}$ = 0 mV	P_6.10.2
A6 sense Amp -sat current	I_{EA_neg}	-63	-56	-49	µA	1) VCOMP = 1V; ADIMVAL = 240; $V_{FBH - FBL}$ = 500 mV	P_6.10.3
A5A6 sense Amp g_m	$IFBx_{gm}$	–	890	–	µS	1) EA_GM=0	P_6.4.10
Output Monitor Voltage	$V_{IOUTMON}$	1.33	1.4	1.47	V	$V_{FBH - FBL}$ = 150 mV;	P_6.4.11
Maximum BOOST Duty Cycle	D_{BOOST_MAX}	89	91	93	%	1) f_{sw} = 300 kHZ;	P_6.4.12
Input current Monitor Voltage	V_{IINMON}	0.95	1	1.05	V	1) $V_{IIN1 - IIN2}$ = 50 mV; V_{IIN1} = $V_{VIN(ON)}$ to 55 V;	P_6.4.15
Switch Peak Over Current Threshold - BOOST	V_{SWCS_boost}	70	76	82	mV	1)	P_10.8.15
Switch Peak Over Current Threshold - BUCK	V_{SWCS_buck}	-60	-50	-40	mV	1)	P_10.8.16
Soft Start							
Soft Start pull up current	$I_{Soft\_Start\_PU}$	22	26	32	µA	V_{Soft_Start} = 1 V;	P_6.4.19
Soft Start pull down current	$I_{Soft\_Start\_PD}$	2.2	2.6	3.2	µA	V_{Soft_Start} = 1 V;	P_6.4.20
Soft Start Latch-OFF Threshold	$V_{Soft\_Start\_LOFF}$	1.65	1.75	1.85	V	–	P_6.4.21
Soft Start Reset Threshold	$V_{Soft\_Start\_RESET}$	0.1	0.2	0.3	V	–	P_6.4.22

Table 7 EC Regulator (cont'd)

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Soft Start Voltage during regulation	$V_{Soft\_Start\_reg}$	1.9	2	2.1	V	1)No Faults	P_6.9.3
Output Current init reference Voltage $V_{FBH-FBL}$	$V_{FBH\_FBL\_IN}$	11	17.5	24	mV	V_{FB} = 1.4 V;	P_10.8.10
Output Current EA_GM boost reference Voltage $V_{FBH-FBL}$	$V_{FBH\_FBL\_EA}$	–	120	-	mV	1)V_{FB} = 1.4 V; ADIMVAL =240;	P_6.10.4
Oscillator							
Switching Frequency	f_{SW}	285	300	315	kHz	T_j = 25°C; R_{FREQ}= 37.4 kΩ;	P_6.4.23
SYNC Frequency	f_{SYNC}	200	–	700	kHz	–	P_6.4.24
SYNC Turn On Threshold	$V_{SYNC,ON}$	2	–	–	V	–	P_6.4.25
SYNC Turn Off Threshold	$V_{SYNC,OFF}$	–	–	0.8	V	–	P_6.4.26
SYNC High Input Current	$I_{SYNC,H}$	15	30	45	µA	V_{SYNC} = 2.0 V;	P_6.4.62
SYNC Low Input Current	$I_{SYNC,L}$	6	12	18	µA	V_{SYNC} = 0.8 V;	P_6.4.63
Gate Driver for external Switch							
Gate Driver undervoltage threshold VBST1,2-VSWN1,2_UVth	$V_{BST1,2}$-$V_{SWN1,2\_UVth}$	3.4	–	4	V	$V_{BST1,2}$ - $V_{SWN1,2}$ decreasing;	P_6.4.64
HSGD1,2 NMOS driver on-state resistance (Gate Pull Up)	$R_{DS(ON\_PU)HS}$	1.4	2.3	3.7	Ω	$V_{BST1,2}$ - $V_{SWN1,2}$ = 5 V; I_{source} = 100 mA;	P_6.4.28
HSGD1,2 NMOS driver on-state resistance (Gate Pull Down)	$R_{DS(ON\_PD)HS}$	0.6	1.2	2.2	Ω	$V_{BST1,2}$ - $V_{SWN1,2}$ = 5 V; I_{sink} = 100 mA;	P_6.4.29
LSGD1,2 NMOS driver on-state resistance (Gate Pull Up)	$R_{DS(ON\_PU)LS}$	1.4	2.3	3.7	Ω	V_{IVCC_EXT} = 5 V; I_{source} = 100 mA;	P_6.4.30
LSGD1,2 NMOS driver on-state resistance (Gate Pull Down)	$R_{DS(ON\_PD)LS}$	0.4	1.2	1.8	Ω	V_{IVCC_EXT} = 5 V; I_{sink} = 100 mA;	P_6.4.31
HSGD1,2 Gate Driver peak sourcing current	$I_{HSGD1,2\_SRC}$	380	–	–	mA	1) $V_{HSGD1,2}$ - $V_{SWN1,2}$ = 1 V to 4 V; $V_{BST1,2}$ - $V_{SWN1,2}$ = 5 V	P_6.4.32
HSGD1,2 Gate Driver peak sinking current	$I_{HSGD1,2\_SNK}$	410	–	–	mA	1) $V_{HSGD1,2}$ - $V_{SWN1,2}$ = 4 V to 1 V; $V_{BST1,2}$ - $V_{SWN1,2}$ = 5 V	P_6.4.33

Table 7 EC Regulator (cont'd)

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
LSGD1,2 Gate Driver peak sourcing current	$I_{LSGD1,2\_SRC}$	370	–	–	mA	1) $V_{LSGD1,2}$ = 1 V to 4 V; V_{IVCC_EXT} = 5 V;	P_6.4.34
LSGD1,2 Gate Driver peak sinking current	$I_{LSGD1,2\_SNK}$	550	–	–	mA	1) $V_{LSGD1,2}$ = 4 V to 1 V; V_{IVCC_EXT} = 5 V;	P_6.4.35
LSGD1,2 OFF to HSGD1,2 ON delay	$t_{LSOFF-HSON\_delay}$	15	30	40	ns	1)	P_6.4.36
HSGD1,2 OFF to LSGD1,2 ON delay	$t_{HSOFF-LSON\_delay}$	35	60	75	ns	1)	P_6.4.37

1) Not subject to production test, specified by design

7 Digital Dimming Function

PWM dimming is adopted to vary LEDs brightness with greatly reduced chromaticity shift. PWM dimming achieves brightness reduction by varying the duty cycle of a constant current in the LED string.

7.1 Description

A PWM signal can be transmitted to the TLD5542-1 as described below.

PWM via direct interface

The PWMI pin can be fed with a pulse width modulated (PWM) signals, this enables when HIGH and disables when LOW the gate drivers of the main switches.

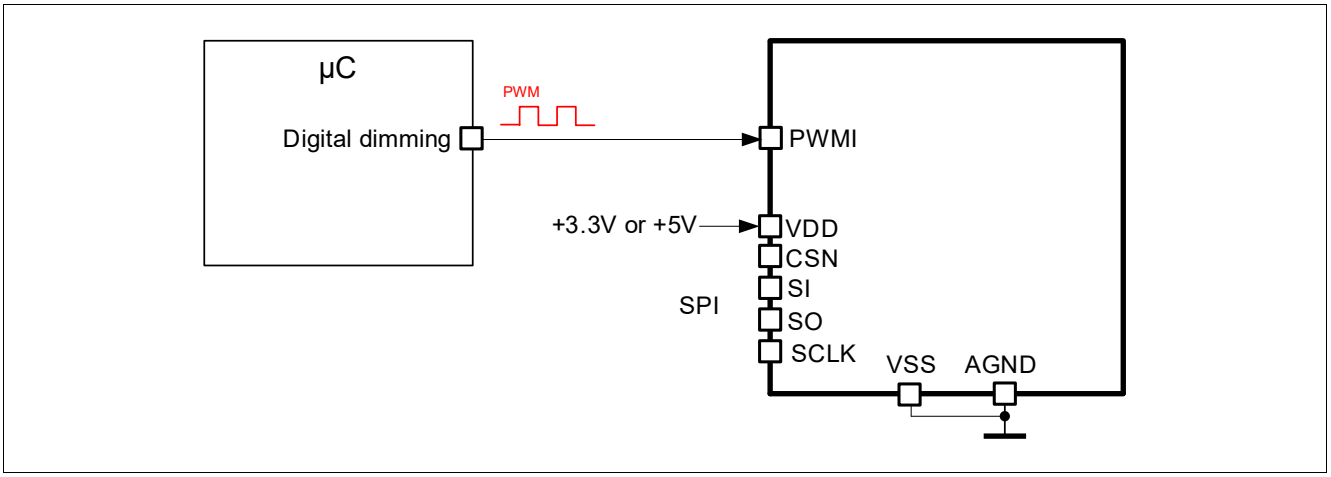


Figure 19 Digital Dimming Overview

Note: In Register `REGUSETMON.REGUMODFB` *the regulation mode can be read. During PWMI = LOW the SPI will always deliver the Regulation mode which was present at PWMI = HIGH as actual regulation mode, instead of "no Regulation".*

To avoid unwanted output overshoots due to not soft start assisted startups, PWM dimming in LOW state should not be used to suspend the output current for long time intervals. To stop in a safe manner DVCCTRL.IDLE=HIGH or EN/INUVLO=LOW can be used.

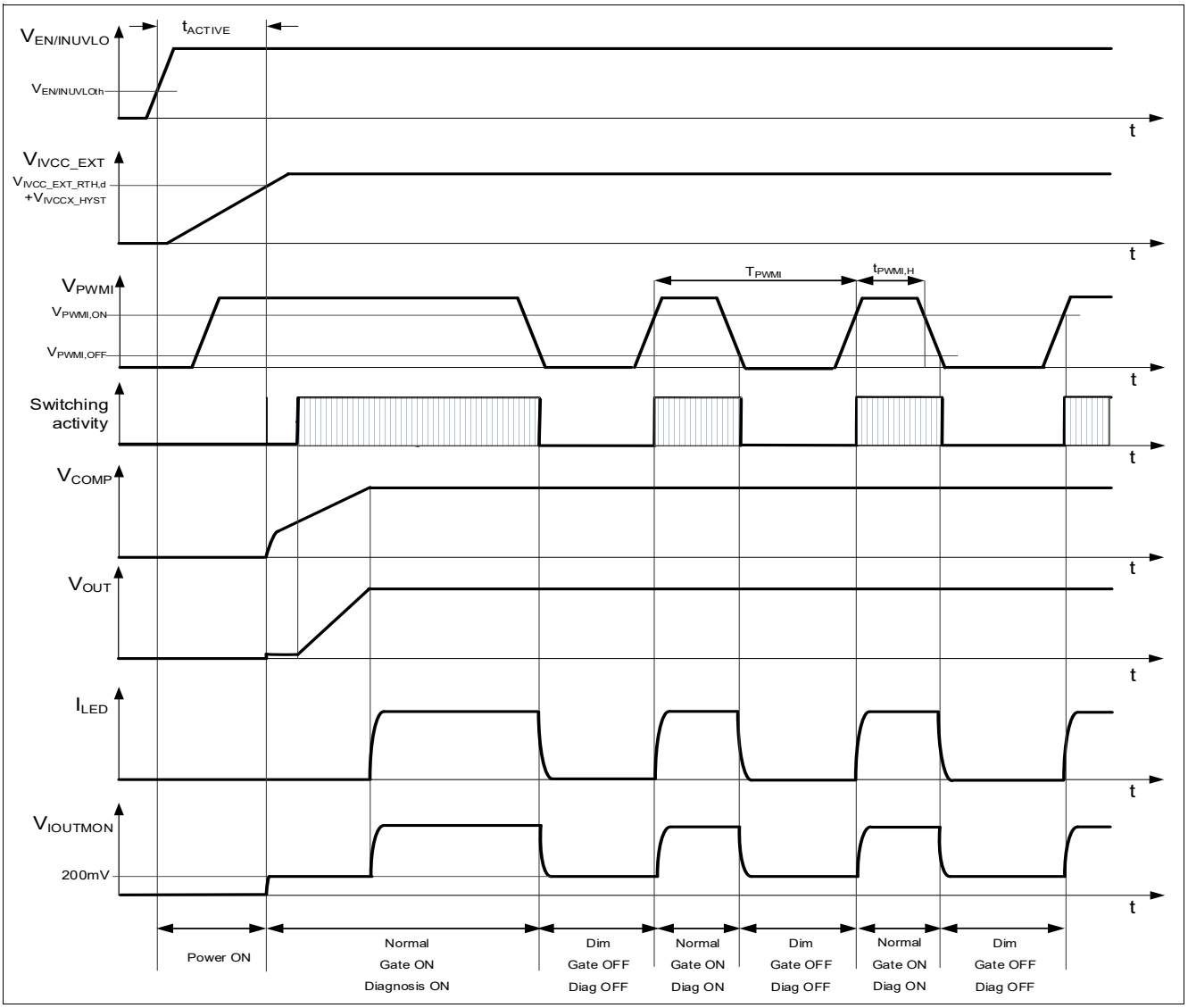


Figure 20 Timing Diagram LED Dimming and Start up behavior example (V_{VDD} and V_{VIN} stable in the functional range and not during startup)

7.2 Electrical Characteristics

Table 8 EC Digital Dimming

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PWMI Input:							
PWMI Turn On Threshold	$V_{PWMI,ON}$	2	–	–	V	–	P_7.2.1
PWMI Turn Off Threshold	$V_{PWMI,OFF}$	–	–	0.8	V	–	P_7.2.2
PWMI High Input Current	$I_{PWMI,H}$	15	30	45	µA	V_{PWMI} = 2.0 V;	P_7.2.4
PWMI Low Input Current	$I_{PWMI,L}$	6	12	18	µA	V_{PWMI} = 0.8 V;	P_7.2.5

8 Analog Dimming and Limp Home

If the TLD5542-1 is used as current regulator, the analog dimming feature allows control of the LED peak current level from the default maximum value. If the device is used as voltage regulator, then the analog dimming can be used to reduce the output voltage. In this chapter the assumption is to have it as a current regulator.

8.1 Description

For the calculation of the output current I_{OUT} the following **Equation (8.1)** is used:

$$I_{OUT} = \frac{V_{FBH} - V_{FBL}}{R_{FB}} \quad (8.1)$$

The analog dimming feature is adjusting the average LED current level via the control of the feedback error amplifier reference voltage $V_{FBH\text{-}FBL\_REF}$.

In the default state (DAC_OFF=0 and LHI=LOW), the current adjustment is done via a 8BIT SPI parameter (`LEDCURRADIM.ADIMVAL`) as shown on **Figure 21** .

If DAC_OFF = 1 then the error amplifier reference voltage is the minimum between SET pin and DAC value. Therefore, in order to have a full scale dimming via SET pin , ADIMVAL has to be set to 240.

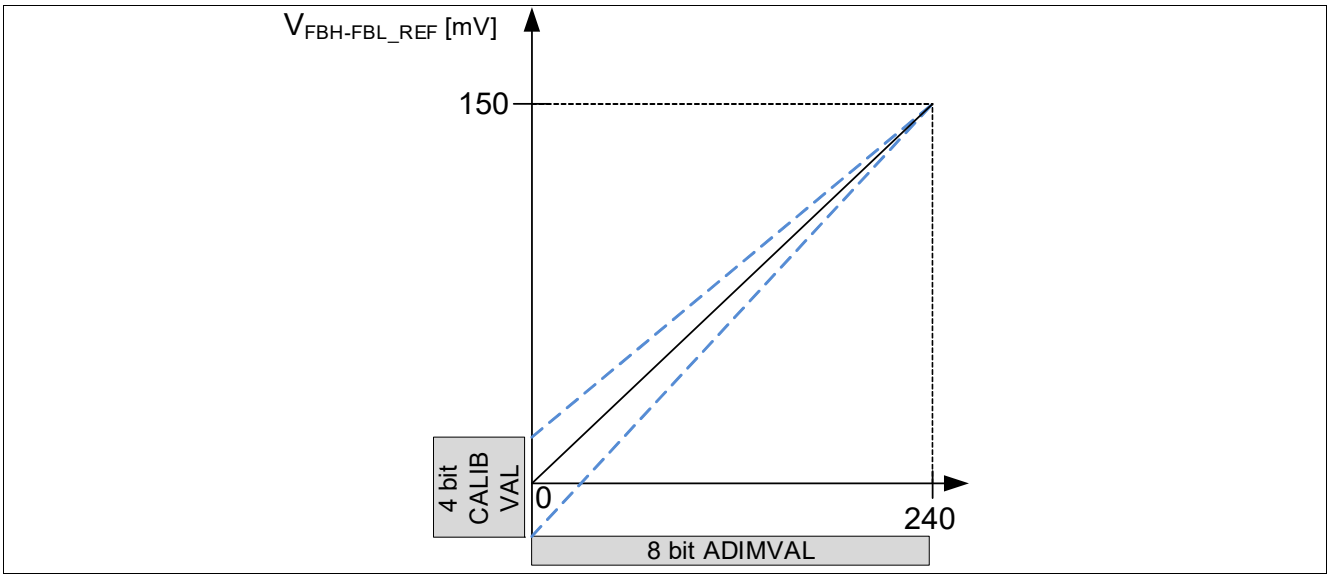


Figure 21 Analog Dimming Overview

Analog dimming adjustment during Limp Home state:

To enter in Limp Home state the LHI pin must be HIGH.

Note: If the PWMI and the EN/INUVLO are not set to HIGH, it is not possible to enable switching, even during Limp Home state.

In Limp Home state, or if DAC_OFF=1, the analog dimming control is done via the SET pin. A resistor divider between IVCC/IVCC_EXT, SET and GND can be used to fix a load current/voltage value (refer to below).

When Limp Home is entered, the device will discharge the output capacitor with a F.D. Routine down to $V_{FBH\_S2G\_dec}$ (MFSDLY set to the default Value). At the end of the F.D. routine, if the PWMI is kept HIGH, the device will start regulating with the analog dimming level provided by the SET pin.

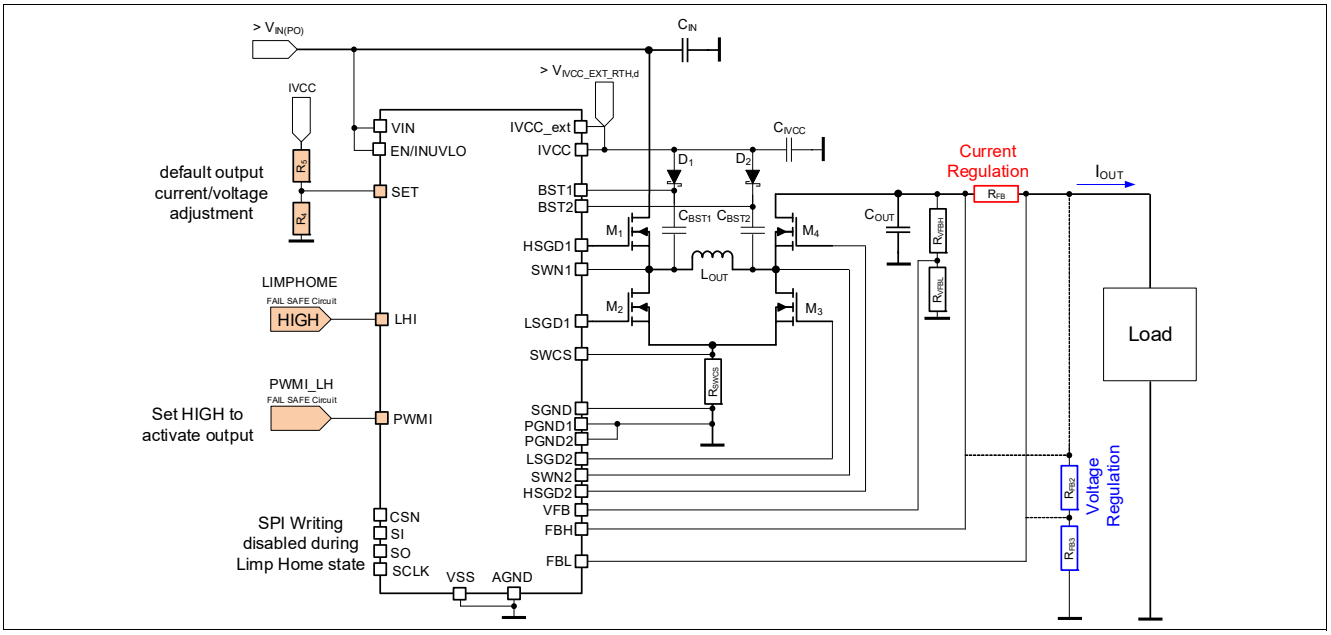


Figure 22 Limp Home state schematic overview

Using the SET pin to adjust the output current:

During Limp Home state or if DAC_OFF = 1, the average I_{OUT} can be adjusted by controlling the voltage at the SET pin (V_{SET}) between 0.2 V and 1.4 V. The typical I_{OUT} behaviour is described by **Equation (8.2)** below:

$$I_{OUT} = \frac{V_{SET} - 200\ mV}{R_{FB} \cdot 8} \tag{8.2}$$

If V_{SET} is 200 mV (typ.) the LED current is only determined by the internal offset voltages of the comparators. To assure the switching activity is stopped and $I_{OUT} = 0$, V_{SET} has to be < 100 mV, see **Figure 23**.

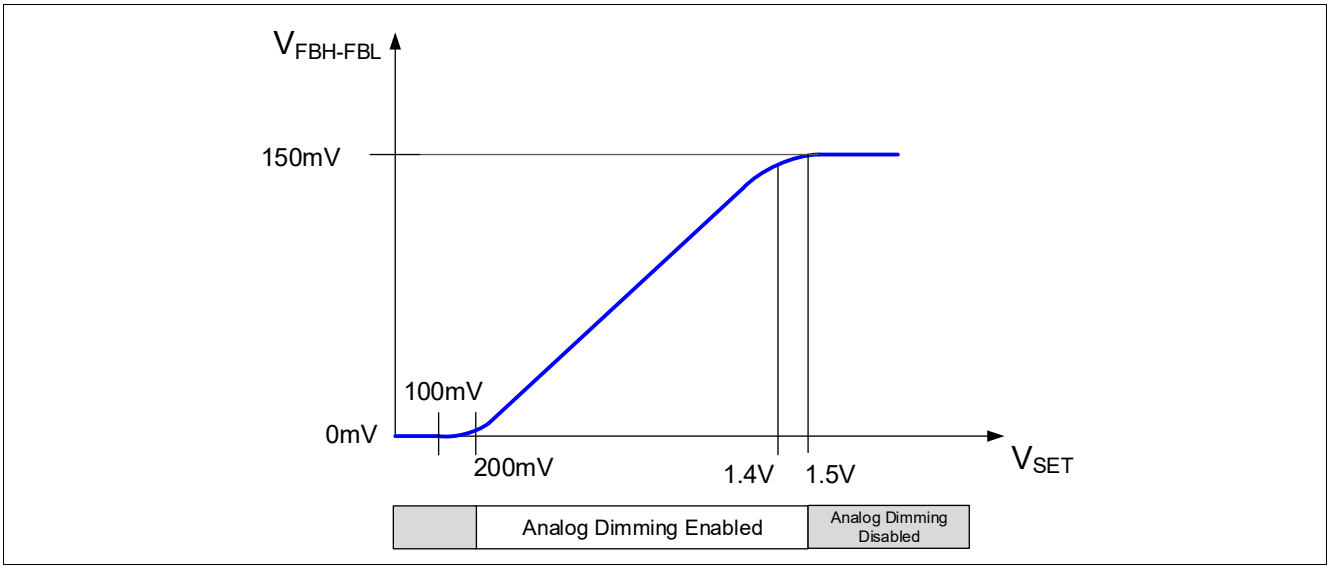


Figure 23 Analog Dimming Overview

8.2 LED current calibration procedure

The LED current calibration procedure improves the accuracy during analog dimming. In order to be most effective, this routine has to be performed in the application, when the TLD5542-1 temperature and the output

voltage are the ones in which the driver has to be accurate. The output current must be 0 during the procedure run. The optimum should be to re-calibrate the output periodically every time the application has PWMI=LOW for a sufficent long time .

Current calibration procedure:

- Power the load with a low analog dimming value (for example 10%)
- Set PWMI = LOW and disconnect the Load at the same time (to avoid Vout drifts from operating conditions and bring the output current to 0)
- Quickly (to avoid Vout drifts) µC enables the calibration routine: `DVCCTRL.ENCAL` = HIGH
- Quickly (to avoid Vout drifts) µC starts the calibration: `LEDCURRCAL.SOCAL` = HIGH
- Waiting time (needed to internally perform the calibration routine) → aprox. 200 µs
- TLD5542-1 will set the FLAG: `LEDCURRCAL.EOCAL` = HIGH, when calibration routine has finished
- Reconnect the load
- The output current is automatically adjusted to a low offset and more accurate analog dimming value

Once the calibration routine is correctly performed, the output current accuracy with analog dimming = 10% (`LEDCURRADIM.ADIMVAL` = 24) is 10%.

The Calibration routine is not affecting the accuracy at 100% analog dimming.

The ENCAL Bits affect both device operation and CALIBVAL reading result:

- ENCAL = HIGH: the calibration result coming from the routine is used by internal circuitry and can be read back from CALIBVAL
- ENCAL = LOW: SPI value written in CALIBVAL is used by internal circuitry and can be read back; calibration routine start is inhibited

As a result, µC can use a stored result from a previously performed calibration to directly impose the desired value without waiting for a new routine to finish.

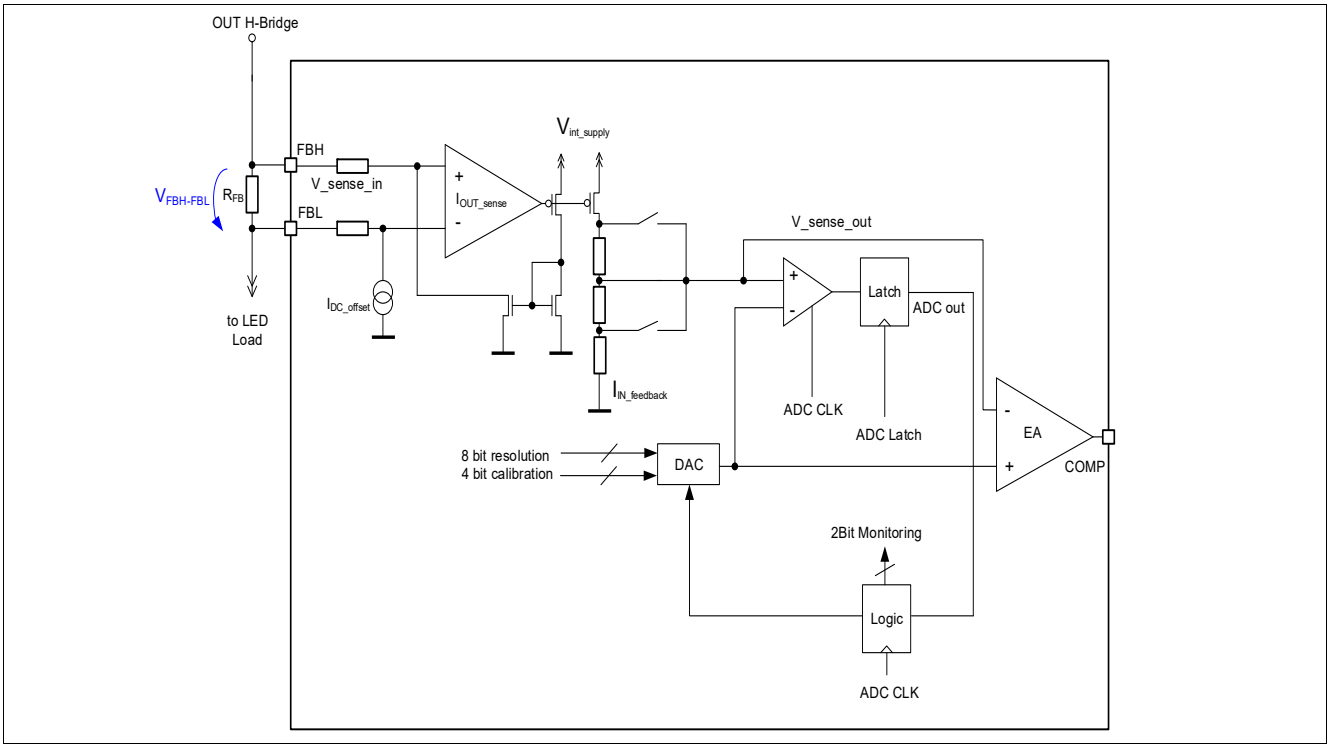


Figure 24 LED current accuracy calibration overview

8.3 Electrical Characteristics

Table 9 EC Analog Dimming

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Source current on SET Pin	I_{SET_source}	–	–	1	µA	[1] V_{SET} = 0.2 V to 1.4 V;	P_8.3.4

1) Specified by design: not subject to production test.

9 Linear Regulator

The TLD5542-1 features an integrated voltage regulator for the supply of the internal gate driver stages. Furthermore an external voltage regulator can be connected to the IVCC_EXT pin to achieve an alternative gate driver supply if required.

9.1 IVCC Description

When the IVCC pin is connected to the IVCC_EXT pin, the internal linear voltage regulator supplies the internal gate drivers with a typical voltage of 5 V and current up to I_{LIM} (P_9.2.2). An external output capacitor with low ESR is required on pin IVCC for stability and buffering transient load currents. During normal operation the external MOSFET switches will draw transient currents from the linear regulator and its output capacitor (**Figure 25**, drawing A). Proper sizing of the output capacitor must be considered to supply sufficient peak current to the gate of the external MOSFET switches. A minimum capacitance value is given in parameter C_{IVCC} (P_9.2.4).

Alternative IVCC_EXT Supply Concept:

The IVCC_EXT pin can be used for an external voltage supply to alternatively supply the MOSFET Gate drivers. This concept is beneficial in the high input voltage range to avoid power losses in the IC (**Figure 25**, drawing B).

Integrated undervoltage protection for the external switching MOSFET:

An integrated undervoltage reset threshold circuit monitors the linear regulator output voltage. This undervoltage reset threshold circuit will turn OFF the gate drivers in case the IVCC or IVCC_EXT voltage falls below their undervoltage Reset switch OFF Thresholds $V_{IVCC\_RTH,d}$ (P_9.2.9) and $V_{IVCC\_EXT\_RTH,d}$ (P_9.2.5).

In Limp Home state the Undervoltage Reset switch OFF threshold for the IVCC has no impact on the switching activity.

The Undervoltage Reset threshold for the IVCC and the IVCC_EXT pins help to protect the external switches from excessive power dissipation by ensuring the gate drive voltage is sufficient to enhance the gate of the external logic level N-channel MOSFETs.

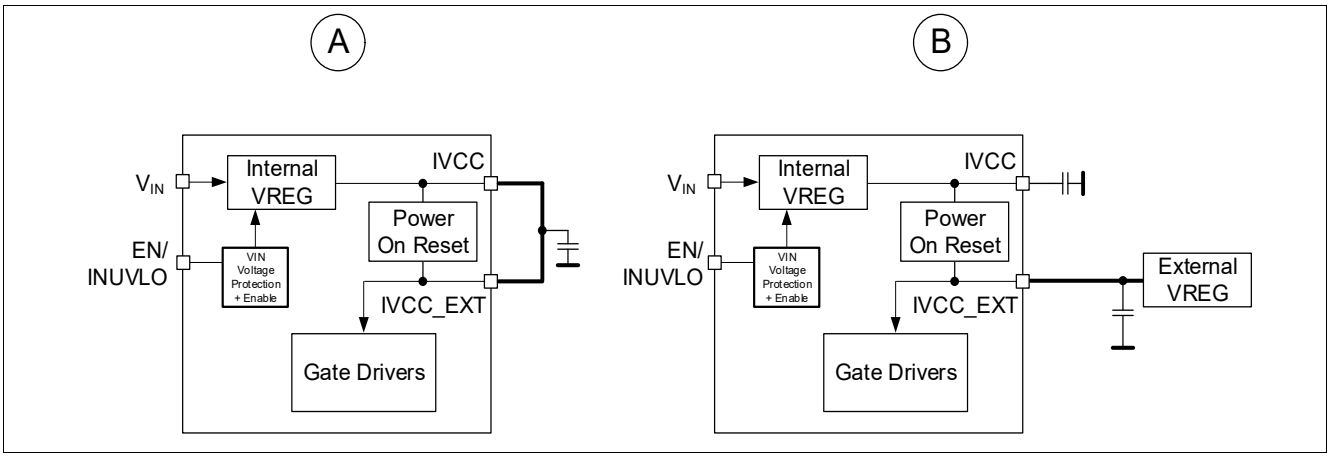


Figure 25 Voltage Regulator Configurations

9.2 Electrical Characteristics

Table 10 EC Line Regulator

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IVCC							
Output Voltage	V_{IVCC}	4.8	5	5.2	V	V_{IN}= 13.5 V; 0.1 mA ≤ I_{IVCC} ≤ 50 mA;	P_9.2.1
Output Current Limitation	I_{LIM}	70	90	110	mA	1) V_{IVCC} = 4 V;	P_9.2.2
Drop out Voltage (V_{IN} - V_{IVCC})	V_{DR}	–	200	350	mV	V_{IN} = 5 V; I_{IVCC} = 10 mA;	P_9.2.3
IVCC Buffer Capacitor	C_{IVCC}	10	–	–	µF	1) 2)	P_9.2.4
IVCC_EXT Undervoltage Reset switch OFF Threshold	$V_{IVCC\_EXT\_RTH,d}$	3.6	3.8	4.0	V	3) V_{IVCC_EXT} decreasing;	P_9.2.5
IVCC Undervoltage Reset switch OFF Threshold	$V_{IVCC\_RTH,d}$	3.6	3.8	4.0	V	3) V_{IVCC} decreasing;	P_9.2.9
IVCC and IVCC_EXT Undervoltage Hysterisis	V_{IVCCX_HYST}	0.315	0.365	0.395	V	V_{IVCC} increasing; V_{IVCC_EXT} increasing;	P_9.2.6

1) Not subject to production test, specified by design

2) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum. Use capacitors with LOW ESR.

3) Selection of external switching MOSFET is crucial. $V_{IVCC\_EXT\_RTH,d}$ and $V_{IVCC\_RTH,d}$ min. as worst case V_{GS} must be considered.

10 Protection and Diagnostic Functions

10.1 Description

The TLD5542-1 has integrated circuits to diagnose and protect against overvoltage, short circuits of the load and overtemperature faults. Furthermore, the device provides a 2 Bit information of I_{LED}, I_{IN} by the SPI to the µC.

In IDLE state, only the overtemperature Shut Down, overtemperature warning, IVCC or IVCC_EXT undervoltage monitor, V_{DD} or $V_{EN/INUVLO}$ undervoltage monitor are reported according to specifications.

In a summary of the protection, diagnostic and monitor functions is displayed.

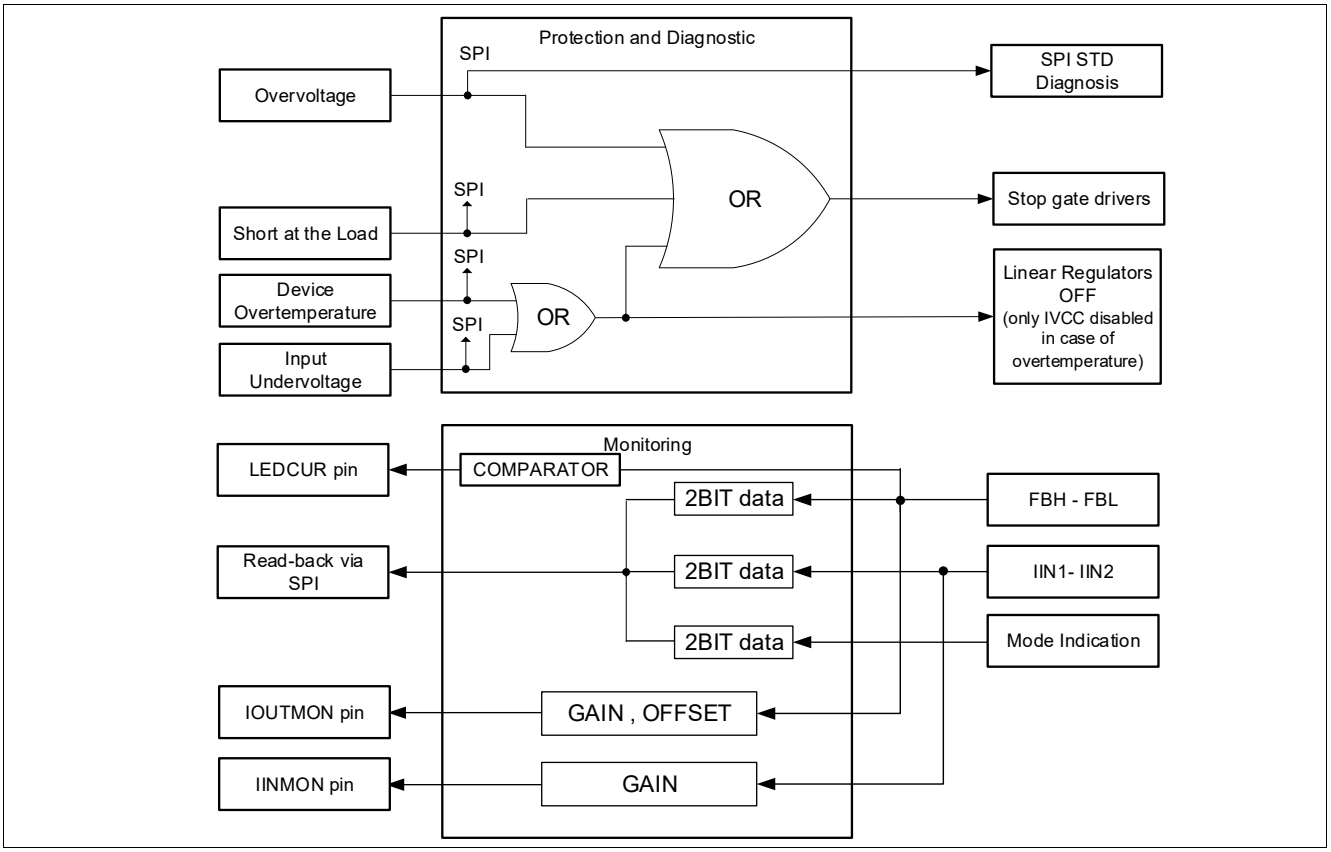


Figure 26 Protection, Diagnostic and Monitoring Overview - TLD5542-1

Note: A device Overtemperature event overrules all other fault events!

10.2 Output Overvoltage, Short circuit protection

The VFB pin measures the voltage on the application output and in accordance with the populated resistor divider overvoltage thresholds is set.

The Short to GND at the output is detected by a fixed threshold on the FBH pin

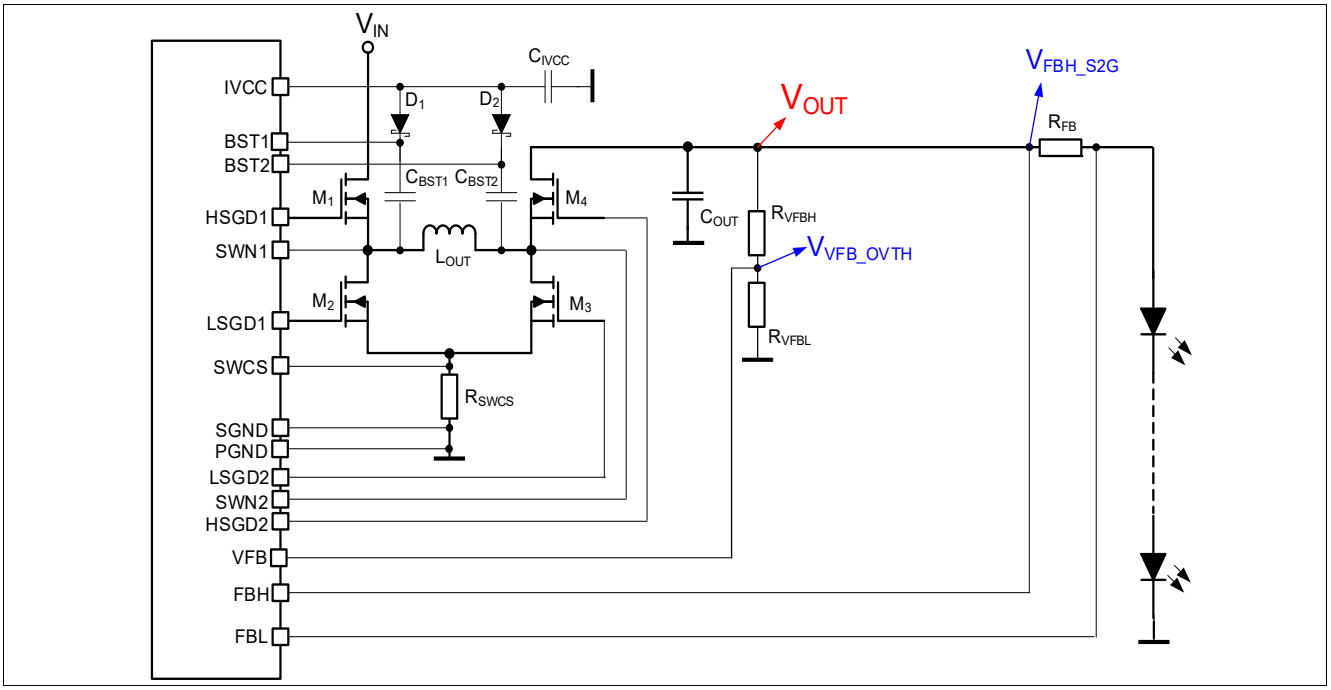


Figure 27 Over Voltage and Short to grond Protection Pins - Overview

10.2.1 Short Circuit protection

The device detects a short circuit at the output if this condition is verified:

- The pin FBH falls below the threshold voltage $V_{FBH\_S2G\_dec}$ for at least 8 clock cycles

It is possible to disable short circuit protection by setting SWTMOD.S2G_OFF to 1, this could be useful for high output voltage swing applications (like MFS topology) . In case of short to GND, the device will simply regulate the pre-fixed current to GND, without endangering the application.

During the rising edge of the Soft Start the short circuit detection is ignored until $V_{SOFT\_START\_LOFF}$ (see **Figure 8**).

After a short circuit detection, the SPI flag (SHRTLED) in the STD diagnosis register is set to HIGH and the gate drivers stop delivering output current (Brake-Low condition, both LS MOSFETs ON). The Device will auto restart with the soft start routine described in **Chapter 6.2**. The dedicated diagnosis flag (SHRTLED) will be cleared after the next reading cycle of the STD diagnosis.

To prevent false S2G tripping after startup, a large enough soft-start capacitor must be used to allow the output voltage to get above the S2G condition.

*Note: If the short circuit condition disappears, the device will re-start with the soft start routine as described in **Chapter 6.2**.*

10.2.2 Overvoltage Protection

A voltage divider between V_{OUT}, VFB pin and AGND is used to adjust V_{OUT} overvoltage protection threshold (V_{OUT_OV}), refer to **Figure 27** and **Equation (10.1)**:

$$V_{OUT\_OV} = V_{VFB\_OVTH} \cdot \frac{R_{VFBH} + R_{VFBL}}{R_{VFBL}} \quad (10.1)$$

If V_{VFB} gets higher than its overvoltage threshold V_{VFB_OVTH} , the SPI flag (OUTOV) in the STD diagnosis set to HIGH and the gate drivers stop switching for output regulation (Brake-Low condition both LS MOSFETs ON). When V_{VFB_OVTH}- $V_{VFB\_OVTH,HYS}$ threshold is reached the device will auto restart. The dedicated diagnosis flag (OUTOV) will be cleared after the next reading cycle of the STD diagnosis.

If the overvoltage threshold V_{OUT_OV} is set below the maximum V_{IN} application operating range, then attention needs to be paid to the overvoltage behavior.

If load current persists during overvoltage event, repetitive overvoltage triggering may occur with a high frequency. This prevents inductor current regulation and the output current may even increase. To avoid this condition, proper sizing of the external components is needed (i.e. increase the output capacitance or the overvoltage threshold in order to delay the overvoltage trigger).

10.3 Input voltage monitoring, protection

Input undervoltage shutdown level can be defined through an external resistor divider, as shown in .

EN/INUVLO pin voltages are internally compared to their respective thresholds by means of hysteretic comparators.

Neglecting the hysteresis, the following equations hold:

$$UV_{th} = \frac{R_1 + R_2}{R_2} \cdot EN/INUVLO_{th} \quad (10.2)$$

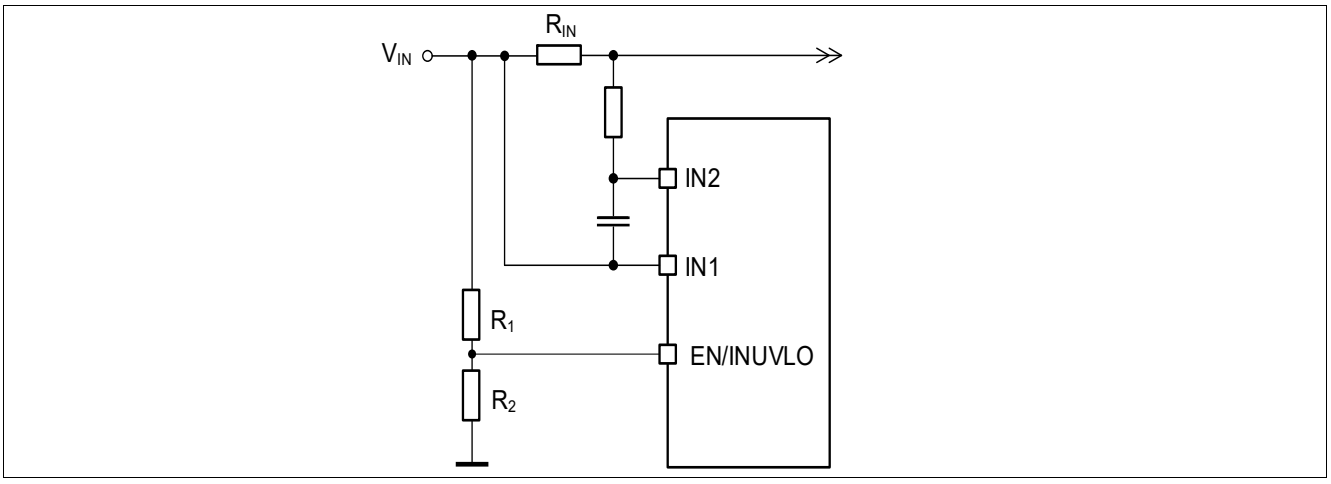


Figure 28 Input Voltage Protection

10.4 Input current Monitoring

The two inputs (IIN1, IIN2) can be used to monitor the Input current.

The input current, measured via IIN1 and IIN2 pins, can be monitored through an analog output pin and an SPI routine.

The IINMON pin provides a linear indication of the current flowing through the input. The following **Equation (10.3)** is applicable:

$$V_{IINMON} = I_{IN} \cdot R_{IN} \cdot 20 \quad (10.3)$$

Purpose of the input current monitoring routine is to verify if the input current level is in the range of the Input Current Sense threshold $V_{IIN1-IIN2}$.

- The output of the Input Current Sense is compared to the internal precise reference voltage
- The comparator works like a 2 bit window ADC referred to the internal precise reference voltage

To execute the current monitor routine the CURRMON.SOMON bit has to be set HIGH and the result is ready when CURRMON.EOMON is read HIGH.

The result of the input monitor routine is reported on the CURRMON.INCURR bit.

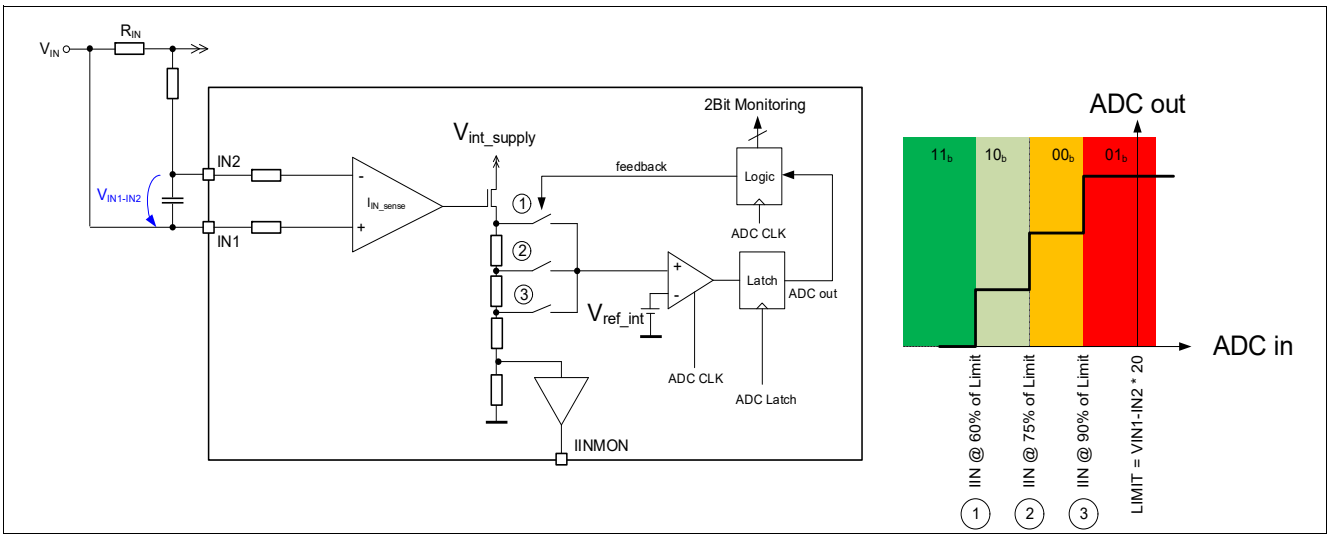


Figure 29 Input Current Monitoring General Overview

10.5 Output current Monitoring

The output current can be monitored through an analog output pin, an open drain flag, an SPI routine and a STD diagnosis bit.

LEDCUR is an open drain output, signaling LED current detected in MFS topologies.

The corresponding detection threshold is defined by k_{LEDC_INC} and k_{LEDC_DEC}.

LEDCUR pin voltage raises to HIGH when $V_{FBH-FBL}/V_{FBH-FBL\_REF} > k_{LEDC\_INC}$, and is pulled LOW when $V_{FBH-FBL}/V_{FBH-FBL\_REF} < k_{LEDC\_DEC}$. Both k_{LEDC_INC} and k_{LEDC_DEC} are depending on analog dimming value, as shown on .

The same information is also present on the STD diagosis via SPI , in the LEDCUR bit.

For a less immediate, but more detailed information about the output current, the SPI current monitor routine can be used:

- The output of the Led Current Sense is compared to the output of the Analog Dimming DAC
- The comparator works like a 2 bit window ADC around 8 bit DAC output

To execute the current monitor routine the CURRMON.SOMON bit has to be set HIGH and the result is ready when CURRMON.EOMON is read HIGH.

When CURRMON.SOMON bit is set to HIGH both input and output current monitor routines are executed in parallel.

The result of the monitor routine is reported on the CURRMON.LEDCURR bit.

The IOUTMON pin provides a linear indication of the current flowing through the LEDs. The typical IOUTMON behaviour follows **Equation (10.4)** :

$$V_{IOUTMON} = 200\ mV + I_{OUT} \cdot R_{FB} \cdot 8 \tag{10.4}$$

The typical output impedance of the IOUTMON is 24k Ohm.

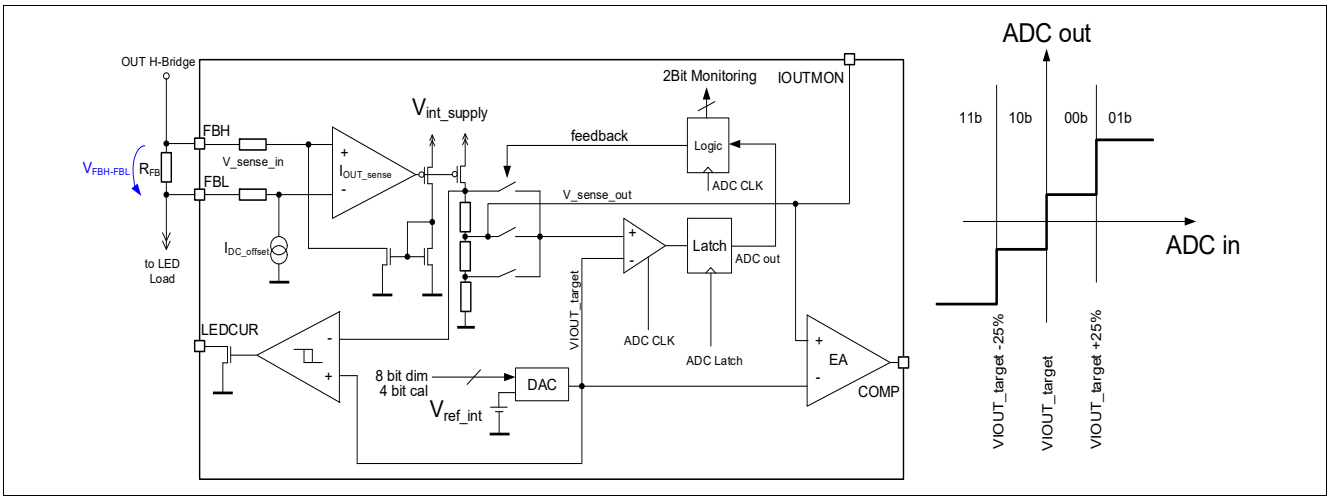


Figure 30 Output Current Monitoring General Overview

10.6 Device Temperature Monitoring

A temperature sensor is integrated on the chip. The temperature monitoring circuit compares the measured temperature to the warning and shutdown thresholds. If the internal temperature sensor reaches the warning temperature, the temperature warning bit TW is set to HIGH. This bit is not latched (i.e. if the temperature falls below the warning threshold (with hysteresis), the TW bit is reset to LOW again).

If the internal temperature sensor reaches the shut-down temperature, the Gate Drivers plus the IVCC regulator are shut down as described in **Figure 31** and the temperature shut-down bit: TSD is set to HIGH. The TSD bit is latched while the Gate Drivers plus the IVCC regulator have an auto restart behavior.

Note: The Device will start up with a soft start routine after a TSD condition disappear.

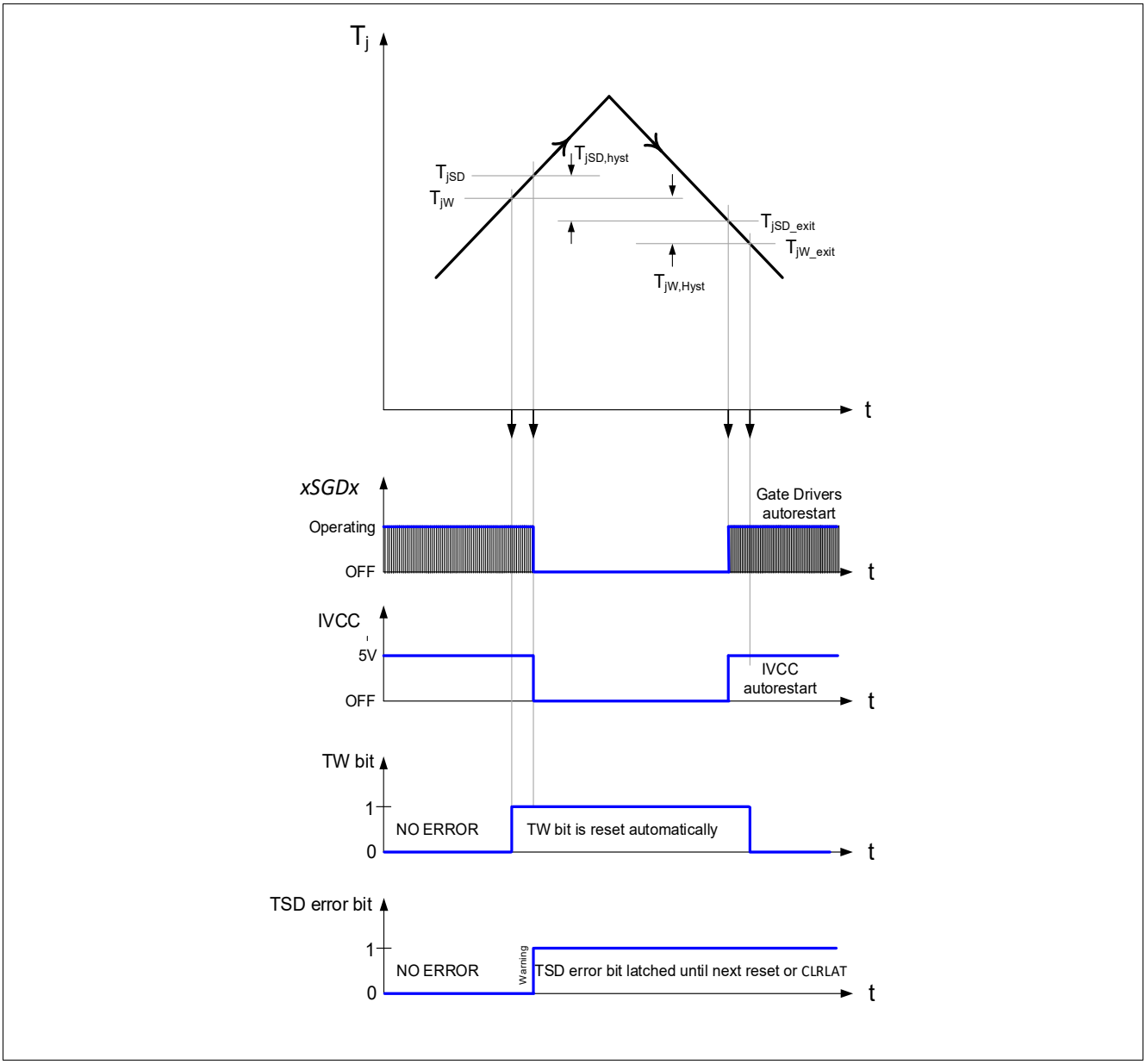


Figure 31 Device Overtemperature Protection Behavior

10.7 Electrical Characteristics

Table 11 EC Protection and Diagnosis

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Short Circuit Protection							
Short to GND exit threshold	$V_{FBH\_S2G\_inc}$	1.95	2.05	2.15	V	1) V_{FBH} increasing;	P_6.9.1
Short to GND entry threshold	$V_{FBH\_S2G\_dec}$	1.65	1.75	1.85	V	1) V_{FBH} decreasing;	P_6.9.2
LEDCUR detect threshold increasing	k_{LEDC_INC}	60	70	80	%	1) ADIMVAL = 240 $V_{FBH-FBL}$ increasing;	P_10.7.1
LEDCUR detect threshold increasing	k_{LEDC_INC}	45	55	65	%	1) ADIMVAL = 48 $V_{FBH-FBL}$ increasing;	P_10.7.2
LEDCUR detect threshold decreasing	k_{LEDC_DEC}	50	60	70	%	1) ADIMVAL = 240 $V_{FBH-FBL}$ decreasing;	P_10.7.3
LEDCUR detect threshold decreasing	k_{LEDC_DEC}	30	40	50	%	1) ADIMVAL = 48 $V_{FBH-FBL}$ decreasing;	P_10.7.4
LEDCUR detect hysteresys	k_{LEDCUR_HYS}	-	12	-	%	1) ADIMVAL = 48 to 240	P_10.7.5
Temperature Protection:							
Thermal Warning junction temperature	$T_{j,W}$	125	140	155	°C	1)	P_10.8.2
Temperature warning Hysteresis	$T_{j,W,hyst}$	–	10	–	°C	1)	P_10.8.3
Over Temperature Shutdown	$T_{j,SD}$	160	175	190	°C	1)	P_10.8.4
Over Temperature Shutdown Hysteresis	$T_{j,SD,hyst}$	–	10	–	°C	1)	P_10.8.5
Overvoltage Protection:							
VFB Over Voltage Feedback Threshold	V_{VFB_OVTH}	1.42	1.46	1.50	V		P_10.8.6
Output Over Voltage Feedback Hysteresis	$V_{VFB\_OVTH,HYS}$	25	40	58	mV	Output Voltage decreasing;	P_10.8.7
Flags							
LEDCUR, EOMFS Pin Output Impedance	R_{F12}	–	2.1	–	kΩ	1) When Pull Down is active I=100uA	P_10.8.14

1) Specified by design; not subject to production test.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

11 Infineon FLAT SPECTRUM Feature set

11.1 Description

The Infineon FLAT SPECTRUM feature set has the target to minimize external additional filter circuits. The goal is to provide several beneficial concepts to provide easy adjustments for EMC improvements after the layout is already done and the HW designed.

11.2 Synchronization Function

The TLD5542-1 features a SYNC input pin which can be used by a µC pin to define an oscillator switching frequency. The µC is responsible to synchronize with various devices by applying appropriate SYNC signals to the dedicated DC/DC devices in the system. Refer to **Figure 32**

Note: The Synchronization function can not be used when the Spread Spectrum is active.

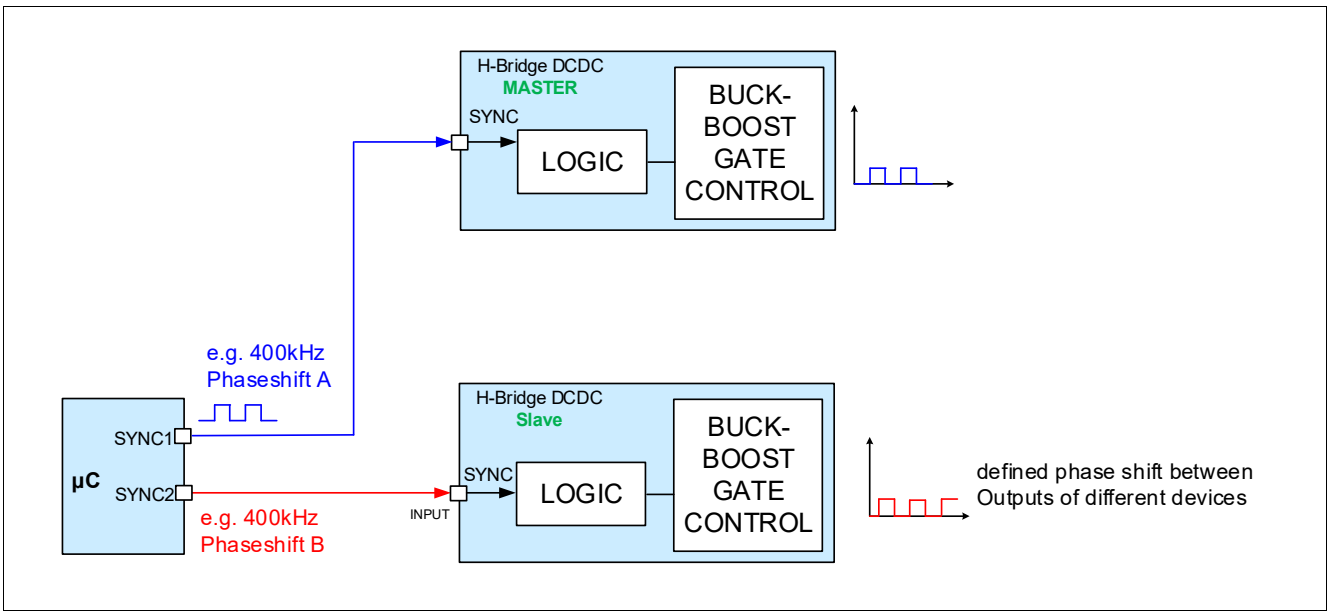


Figure 32 Synchronization Overview

11.3 Spread Spectrum

The Spread Spectrum modulation technique significantly improves the lower frequency range of the spectrum (f < 30 MHz).

By using the spread spectrum technique, it is possible to optimize the input filter only for the peak limits, and also pass the average limits (average emission limits are -20dB lower than the peak emission limits). By using spread spectrum, the need for low ESR input capacitors is relaxed because the input capacitor series resistor is important for the low frequency filter characteristic. This can be an economic benefit if there is a strong requirement for average limits.

The TLD5542-1 features a built in Spread Spectrum function which can be enabled (`SWTMOD.ENSPREAD`) and adjusted via the SPI interface. Dedicated SPI-Bits are used to adjust the modulation frequency f_{FM}, (P_11.6.3) and (P_11.6.4) (`SWTMOD.FMSPREAD`) and the deviation frequency f_{dev}, (P_11.6.1) and (P_11.6.2) (`SWTMOD.FDEVSPREAD`) accordingly to specific application needs. Refer to **Figure 33** for more details.

The following adjustments can be programmed when `SWTMOD.ENSPREAD` = HIGH:

`SWTMOD.FMSPREAD` = LOW: 12 kHz

`SWTMOD.FMSPREAD` = HIGH: 18 kHz

`SWTMOD.FDEVSPREAD` = HIGH: ±8% of f_{SW}

`SWTMOD.FDEVSPREAD` = LOW: ±16% of f_{SW}

Note: The Spread Spectrum function can not be used when the synchronization pin is used.

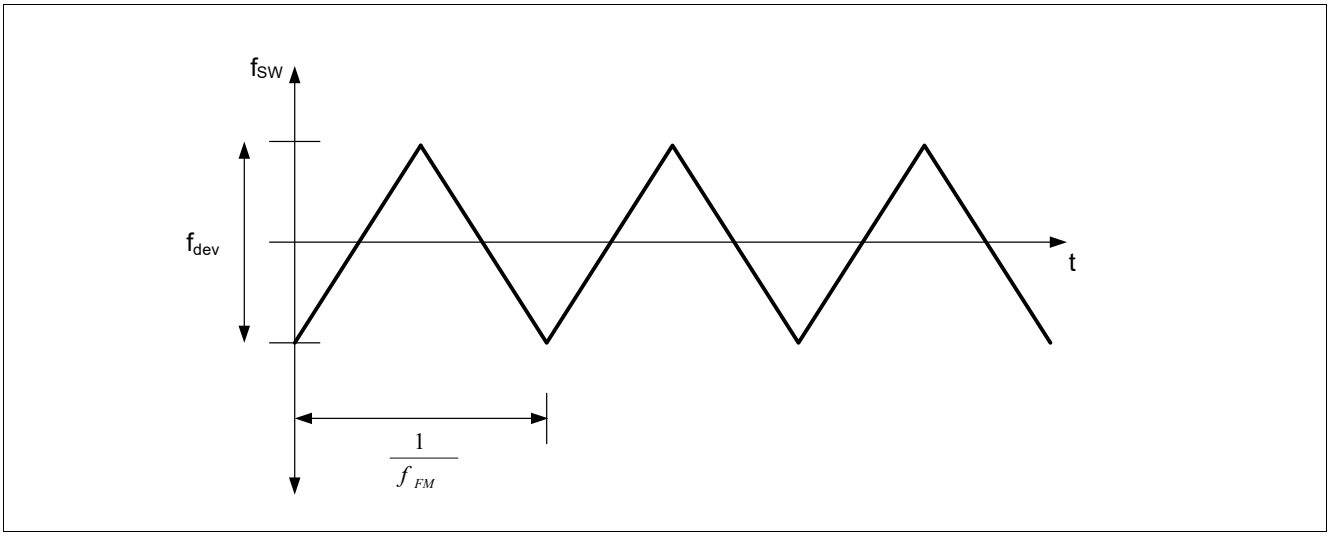


Figure 33 Spread Spectrum Overview

11.4 EMC optimized schematic

Figure 34 below displays the Application circuit with additional external components for improved EMC behavior.

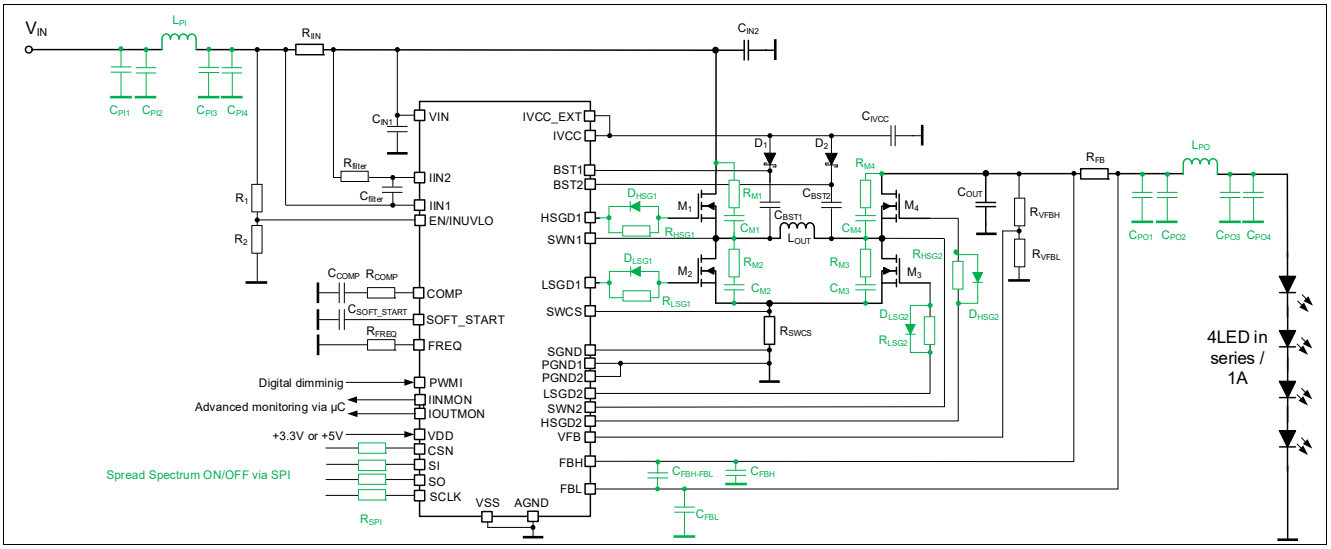


Figure 34 Application Drawing Including Additional Components for an Improved EMC Behavior

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

11.5 Electrical Characteristics

Table 12 EC Spread Spectrum

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Spread Spectrum Parameters							
Frequency Deviation	f_{dev}	–	±8	–	%	1) SWTMOD.FDEVSPREAD = HIGH;	P_11.6.1
Frequency Deviation	f_{dev}	–	±16	–	%	1) SWTMOD.FDEVSPREAD = LOW;	P_11.6.2
Frequency Modulation	f_{FM}	–	12	–	kHz	1) SWTMOD.FMSPREAD = LOW;	P_11.6.3
Frequency Modulation	f_{FM}	–	18	–	kHz	1) SWTMOD.FMSPREAD = HIGH;	P_11.6.4

1) Specified by design; not subject to production test.

12 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and CSN. Data is transferred by the lines SI and SO at the rate given by SCLK. The falling edge of CSN indicates the beginning of an access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of CSN. A modulo 8/16 counter ensures that data is taken only when a multiple of 8 bit has been transferred after the first 16 bits. Otherwise, a TER (i.e. Transmission Error) bit is asserted. In this way the interface provides daisy chain capability with 16 bit as well as with 8 bit SPI devices.

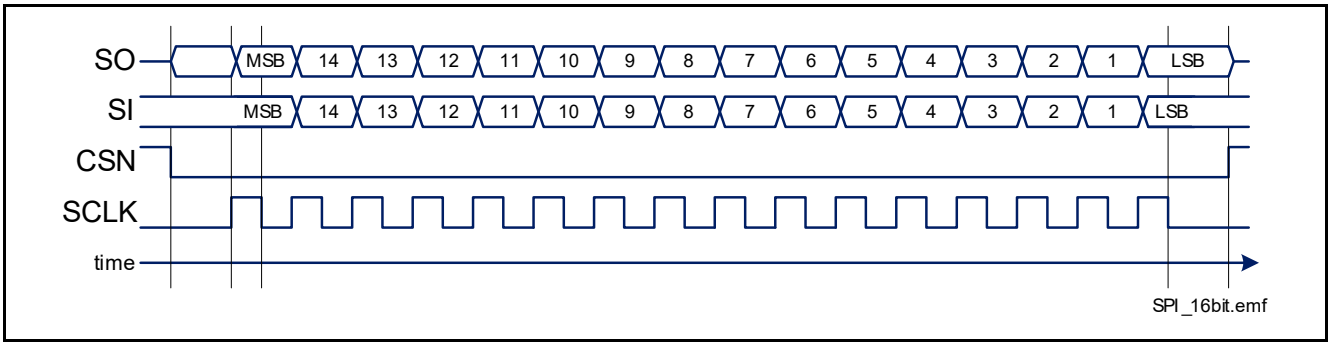


Figure 35 Serial Peripheral Interface

12.1 SPI Signal Description

CSN - Chip Select

The system microcontroller selects the TLD5542-1 by means of the CSN pin. Whenever the pin is in LOW state, data transfer can take place. When CSN is in HIGH state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

CSN HIGH to LOW Transition

- The requested information is transferred into the shift register.
- SO changes from high impedance state to HIGH or LOW state depending on the signal level at pin SI.
- If the device is in SLEEP mode, the SO pin remains in high impedance state and no SPI transmission will occur.
- TER Flag will set the Bit number 10 in the STD diagnosis Frame. This Bit is set to HIGH after an undervoltage contition, reset via SPI command, on Limp Home state entering or after an incorrect SPI transmission. TER Flag can be read also direcly on the SO line between the falling edge of the CSN and the first rising edge of the SCLK according to the **Figure 36**.

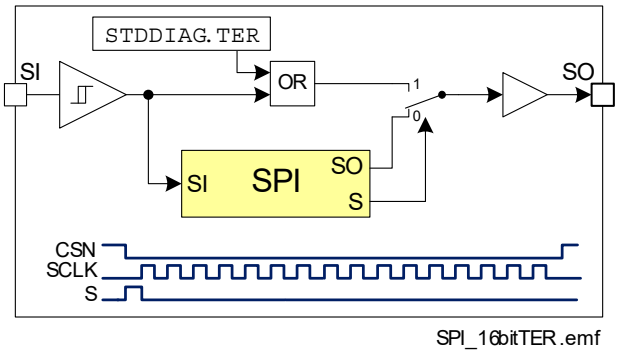


Figure 36 Combinatorial Logic for TER bit

CSN LOW to HIGH Transition

- Command decoding is only done, when after the falling edge of CSN exactly a multiple (0,1, 2, 3, …) of eight SCLK signals have been detected after the first 16 SCLK pulses. In case of faulty transmission, the transmission error bit (TER) is set and the command is ignored.
- Data from shift register is transferred into the addressed register.

SCLK - Serial Clock

This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in LOW state whenever chip select CSN makes any transition, otherwise the command may be not accepted.

SI - Serial Input

Serial input data bits are shift-in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The input data consists of two parts, control bits followed by data bits. Please refer to **Chapter 12.5** for further information.

SO Serial Output

Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the CSN pin goes to LOW state. New data will appear at the SO pin following the rising edge of SCLK.

Please refer to **Chapter 12.5** for further information.

12.2 Daisy Chain Capability

The SPI of the TLD5542-1 provides daisy chain capability. In this configuration several devices are activated by the same CSN signal MCSN. The SI line of one device is connected with the SO line of another device (see **Figure 37**), in order to build a chain. The end of the chain is connected to the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK which is connected to the SCLK line of each device in the chain.

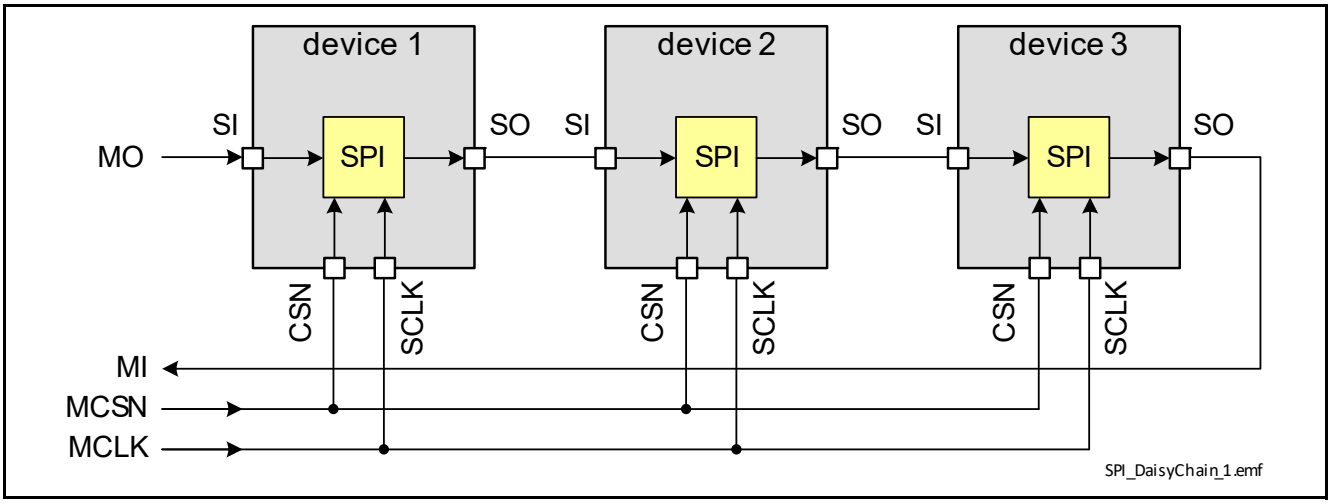


Figure 37 Daisy Chain Configuration

In the SPI block of each device, there is one shift register where each bit from the SI line is shifted in with each SCLK. The bit shifted out occurs at the SO pin. After sixteen SCLK cycles, the data transfer for one device is finished. In single chip configuration, the CSN line must turn HIGH to make the device acknowledge the transferred data. In daisy chain configuration, the data shifted out at device 1 has been shifted in to device 2. When using three devices in daisy chain, several multiples of 8 bits have to be shifted through the devices (depending on how many devices with 8 bit SPI and how many with 16 bit SPI). After that, the MCSN line must turn HIGH (see **Figure 38**).

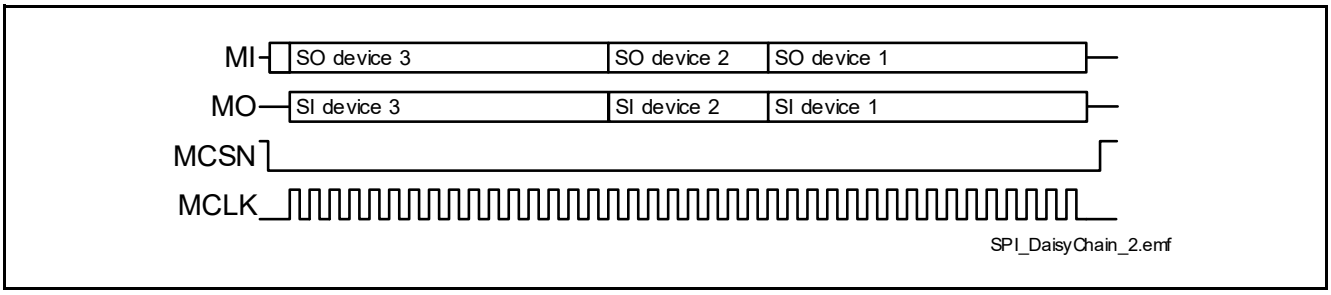


Figure 38 Data Transfer in Daisy Chain Configuration

12.3 Timing Diagrams

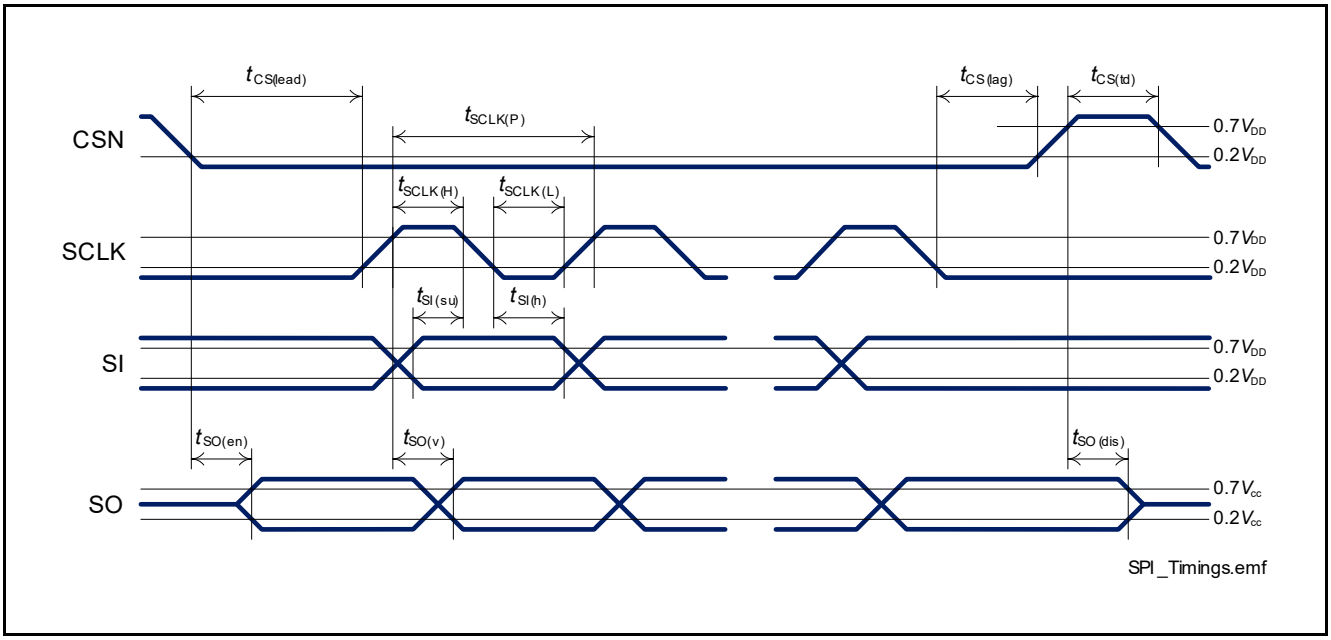


Figure 39 Timing Diagram SPI Access

12.4 Electrical Characteristics

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, V_{DD}= 3 V to 5.5 V, all voltages with respect to ground; (unless otherwise specified)

Table 13 EC Serial Peripheral Interface (SPI)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input Characteristics (CSN, SCLK, SI) - LOW level of pin							
CSN	$V_{CSN(L)}$	0	–	0.8	V	–	P_12.4.1
SCLK	$V_{SCLK(L)}$	0	–	0.8	V	–	P_12.4.2
SI	$V_{SI(L)}$	0	–	0.8	V	–	P_12.4.3
Input Characteristics (CSN, SCLK, SI) - HIGH level of pin							
CSN	$V_{CSN(H)}$	2	–	V_{DD}	V	–	P_12.4.4
SCLK	$V_{SCLK(H)}$	2	–	V_{DD}	V	–	P_12.4.5
SI	$V_{SI(H)}$	2	–	V_{DD}	V	–	P_12.4.6
L-input pull-up current at CSN pin	$-I_{CSN(L)}$	31	63	94	µA	V_{DD} = 5 V; V_{CSN} = 0.8 V;	P_12.4.7
H-input pull-up current at CSN pin	$-I_{CSN(H)}$	22	45	67	µA	V_{DD} = 5 V; V_{CSN} = 2 V;	P_12.4.8
L-Input Pull-Down Current at Pin							
SCLK	$I_{SCLK(L)}$	6	12	18	µA	V_{SCLK} = 0.8 V;	P_12.4.9
SI	$I_{SI(L)}$	6	12	18	µA	V_{SI} = 0.8 V;	P_12.4.10
H-Input Pull-Down Current at Pin							
SCLK	$I_{SCLK(H)}$	15	30	45	µA	V_{SCLK} = 2 V;	P_12.4.11
SI	$I_{SI(H)}$	15	30	45	µA	V_{SI} = 2 V;	P_12.4.12
Output Characteristics (SO)							
L level output voltage	$V_{SO(L)}$	0	–	0.4	V	I_{SO} = -2 mA;	P_12.4.13
H level output voltage	$V_{SO(H)}$	V_{DD} - 0.4 V	–	V_{DD}	V	I_{SO} = 2 mA; V_{DD} = 5 V;	P_12.4.14
Output tristate leakage current	$I_{SO(OFF)}$	-1	–	1	µA	V_{CSN} = V_{DD}; V_{SO} = 0 V or V_{SO} = V_{DD};	P_12.4.15
Timings							
Enable lead time (falling CSN to rising SCLK)	$t_{CSN(lead)}$	200	–	–	ns	1)	P_12.4.17
Enable lag time (falling SCLK to rising CSN)	$t_{CSN(lag)}$	200	–	–	ns	1)	P_12.4.18
Transfer delay time (rising CSN to falling CSN)	$t_{CSN(td)}$	250	–	–	ns	1)	P_12.4.19
Output enable time (falling CSN to SO valid)	$t_{SO(en)}$	–	–	200	ns	1) C_L = 20 pF at SO pin;	P_12.4.20

Table 13 EC Serial Peripheral Interface (SPI) (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output disable time (rising CSN to SO tristate)	$t_{SO(dis)}$	–	–	200	ns	1) C_L = 20 pF at SO pin;	P_12.4.21
Serial clock frequency	f_{SCLK}	–	–	5	MHz	1)	P_12.4.22
Serial clock period	$t_{SCLK(P)}$	200	–	–	ns	1)	P_12.4.24
Serial clock HIGH time	$t_{SCLK(H)}$	75	–	–	ns	1)	P_12.4.25
Serial clock LOW time	$t_{SCLK(L)}$	75	–	–	ns	1)	P_12.4.26
Data setup time (required time SI to falling SCLK)	$t_{SI(su)}$	20	–	–	ns	1)	P_12.4.27
Data hold time (falling SCLK to SI)	$t_{SI(h)}$	20	–	–	ns	1)	P_12.4.28
Output data valid time with capacitive load	$t_{SO(v)}$	–	–	100	ns	1) C_L = 20 pF;	P_12.4.29

1) Not subject to production test, specified by design

12.5 SPI Protocol

The relationship between SI and SO content during SPI communication is shown in **Figure 40**. The SI line represents the frame sent from the µC and the SO line is the answer provided by the TLD5542-1. The first SO response is the response from the previous command.

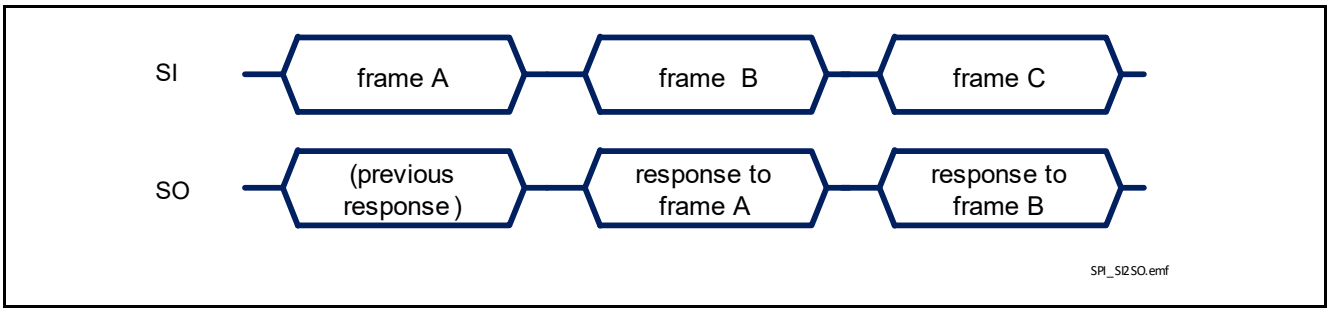


Figure 40 Relationship between SI and SO during SPI communication

The SPI protocol will provide the answer to a command frame only with the next transmission triggered by the µC. Although the biggest majority of commands and frames implemented in TLD5542-1 can be decoded without the knowledge of what happened before, it is advisable to consider what the µC sent in the previous transmission to decode TLD5542-1 response frame completely.

More in detail, the sequence of commands to “read” and “write” the content of a register will look as follows:

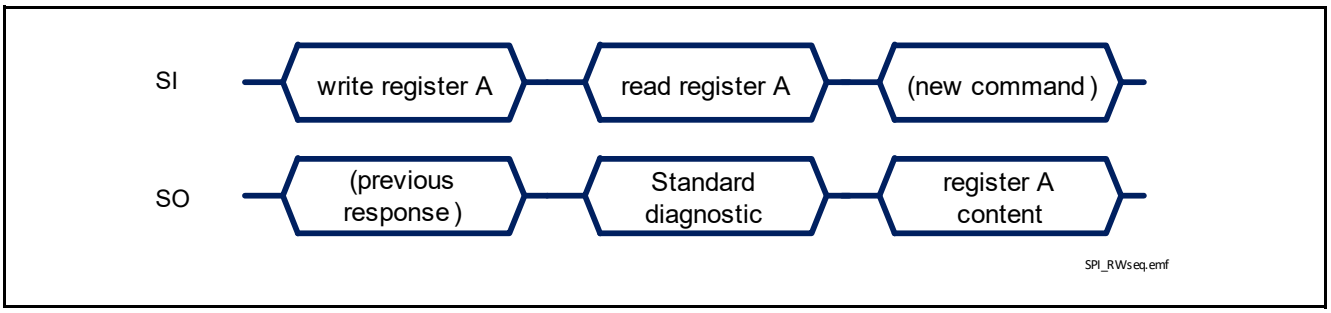


Figure 41 Register content sent back to µC

There are 3 special situations where the frame sent back to the µC doesn't depend on the previously received frame:

- in case an error in transmission happened during the previous frame (for instance, the clock pulses were not multiple of 8 with a minimum of 16 bits), shown in **Figure 42**
- when TLD5542-1 logic supply comes out of an Undervoltage reset condition ($V_{DD} < V_{DD(UV)}$ as shown in **Figure 43** or EN/INUVLO < $V_{EN/INUVLOth}$)
- in case of a read or write command for a “not used” or “reserved” register (in this case TLD5542-1 answers with Standard Diagnosis at the next SPI transmission)

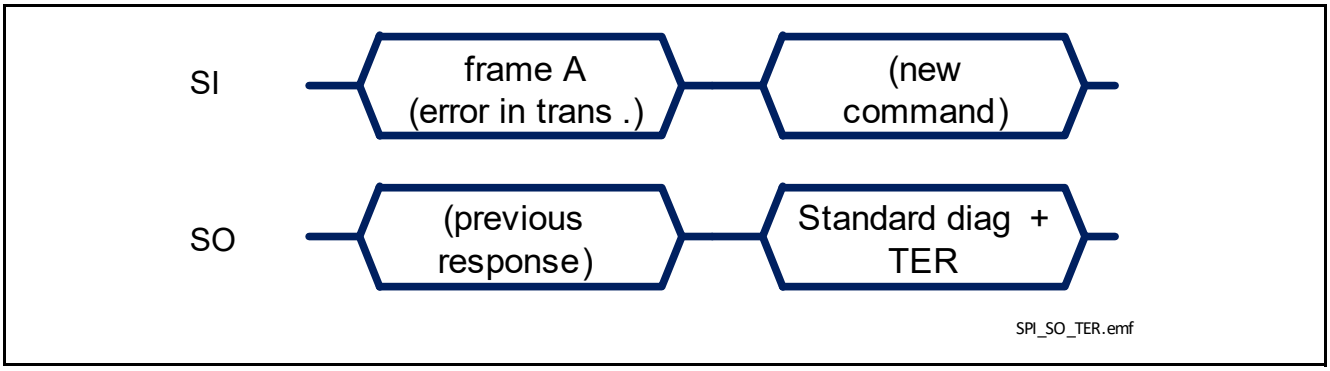


Figure 42 TLD5542-1 response after an error in transmission

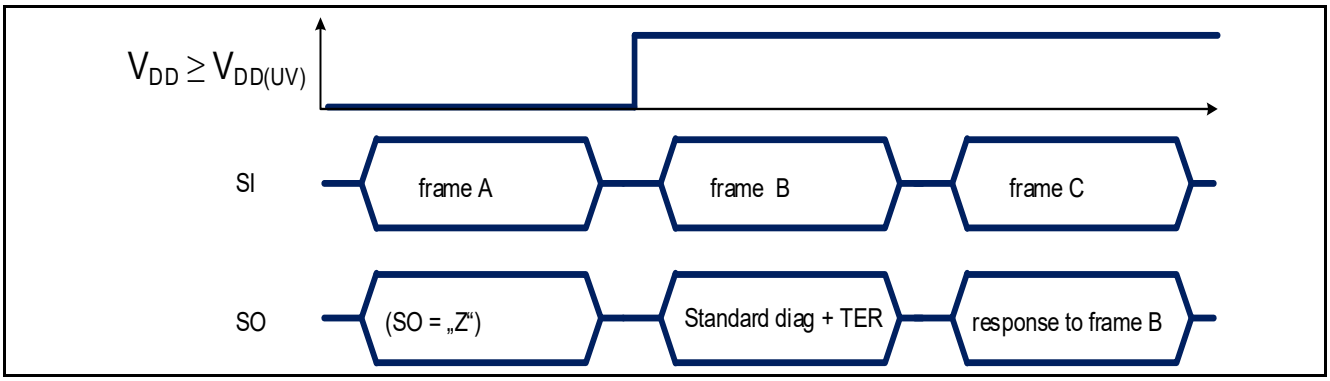


Figure 43 TLD5542-1 response after coming out of Power-On reset at V_{DD}

12.6 SPI Registers Overview

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Frame	W/R	RB	ADDR						Data							
	Write Register in bank 0															
SI	1	0	ADDR						Data							
	Read Register in bank 0															
SI	0	0	ADDR						x	x	x	x	x	x	x	0
	Read Standard Diagnosis															
SI	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1

Reading a register needs two SPI frames. In the first frame the read command is sent. In the second frame the output at SPI signal SO will contain the requested information. The MSB will be HIGH (while in case of standard diagnosis is LOW). A new command can be executed in the second frame.

12.6.1 Standard Diagnosis

The Standard Diagnosis reports several diagnostic informations and the status of the device and the utility routines.

The bits UVLORST, TER, OUTOV, IVCCUVLO and SHRTLED are latched and automatically cleared after a STD diagnosis reading.

A CLRLAT command resets the diagnostic Latched Flag TSD bit.

The TSD bit is always latched and clearable only via explicit CLRLAT command.

The STD bits which are real time status monitors or mirror of internal registers are not cleared after a STD diagnosis reading or via explicit CLRLAT command:

- The STATE bits and TW are real time status flags
- The bits EOMON, EOMFS and EOCAL are mirror of internal register
- The SWRST_BSTUV bit is the logic OR of:
  - latched SWRST flag after a DVCSTRL.SWRST command (clearable via STD Diagnosis reading)
  - real time monitor of gate driver undervolage (VBSTx-VSWNx_UVth)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SWRST_BSTUV	UVLORST	STATE		TER	EOMON	EOMFS	EOCAL	0	OUTOV	IVCCUVLO	LEDCUR	SHRTLED	TSD	TW

Field	Bits	Type	Description
SWRST_BSTUV	14	r	**SWRST OR VBSTx-VSWNx_UVth Monitor** 0_B , no SWRST or undervoltage on the Gate Drivers occured 1_B , there was at least one SWRST since last readout OR an undervoltage condition at the gate drivers is occurring
UVLORST	13	r	**V_{DD} OR $V_{EN/INUVLO}$ Undervoltage Monitor** 0_B , there was no V_{DD} OR $V_{EN/INUVLO}$ undervoltage since last readout 1_B , there was at least one V_{DD} undervoltage OR $V_{EN/INUVLO}$ undervoltage condition since last readout
STATE	12:11	r	**Operative State Monitor** 00_B , (reserved) 01_B , Limp Home Mode 10_B , Active Mode 11_B , Idle Mode
TER	10	r	**Transmission Error** 0_B , Previous transmission was successful (modulo 16 + n*8 clocks received, where n = 0, 1, 2...) 1_B , Previous transmission failed or first transmission after reset
EOMON	9	r	**End of LED/Input Current Monitor Routine Bit** 0_B , Current monitoring routine not completed, not successfully performed or never run. 1_B , Current Monitor routine successfully performed (is reset to 0_B when SOMON is set to 1_B)
EOMFS	8	r	**End of MFS Routine Bit** 0_B , MFS routine not completed, not successfully performed or never run. 1_B , MFS routine successfully performed (is reset to 0_B when SOMOFS is set to 1_B)
EOCAL	7	r	**End of Calibration Routine** 0_B , Calibration routine not completed, not successfully performed or never run. 1_B , Calibration routine successfully performed (is reset to 0_B when SOCAL is set to 1_B)
OUTOV	5	r	**Output overvoltage Monitor** 0_B , Output overvoltage not detected since last readout 1_B , Output overvoltage was detected since last readout
IVCCUVLO	4	r	**IVCC or IVCC_EXT Undervoltage Lockout Monitor** 0_B , IVCC and IVCC_EXT above $V_{IVCC\_RTH,d}$ or $V_{IVCC\_EXT\_RTH,d}$ threshold since last readout 1_B , Undervoltage on IVCC or IVCC_EXT occurred since last readout
LEDCUR	3	r	**LED Current Flag (see LEDCUR pin description Chapter 10.5)** 0_B , LED current not detected 1_B , LED current detected

Field	Bits	Type	Description
SHRTLED	2	r	**Shorted LED Diagnosis** 0_B , Short circuit condition not detected since last readout 1_B , Short circuit condition detected since last readout
TSD	1	r	**Over Temperature Shutdown** 0_B , T_j below temperature shutdown threshold 1_B , Overtemperature condition detected since last readout
TW	0	r	**Over Temperature Warning** 0_B , T_j below temperature warning threshold 1_B , T_j exceeds temperature warning threshold

12.6.2 Register structure

Table 15 describes in detail the available registers with their bit-fields function, size and position
Table 14 shows register addresses and summarize bit-field position inside each register

Table 14 Register Bank 0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**W/R**	**RB**	**ADDR**						**Data**							
LEDCURRADIM	W/R	0	0	0	0	0	0	0	ADIMVAL							
LEDCURRCAL	W/R	0	0	0	0	0	1	1	x	DAC_OFF	SOCAL	EOCAL	CALIBVAL			
SWTMOD	W/R	0	0	0	0	1	0	1	x	DCM_EN	CCM4EVER	VFB_VIN_OFF	S2G_OFF	ENSPREAD	FMSPREAD	FDEVSPREAD
DVCCTRL	W/R	0	0	0	0	1	1	0	EA_IOUT	EA_GM	SLOPE		ENCAL	CLRLAT	SWRST	IDLE
MFSSETUP1	W/R	0	0	0	1	0	0	1	EA_IOUT_MFS	ILIM_HALF_MFS	SOMFS	EOMFS	LEDCHAIN			
MFSSETUP2	W/R	0	0	0	1	0	1	0	MFSDLY							
CURRMON	W/R	0	0	0	1	1	0	0	x	x	SOMON	EOMON	INCURR		LEDCURR	
REGUSETMON	W/R	0	0	0	1	1	1	1	x	x	x		REGUMODFB		BB_BST_CMP	
MUXCTRL	W/R	1	1	1	1	1	1	0	MFS_REF	AMUX_EN	SO_MUX_SEL					

A write to a non existing address is ignored, a read to a non existing register is ignored and the STD Diagnosis Frame is send out.

Table 15 Register description

Register name	Field	Bits	Type	Purpose
LEDCURRADIM	ADIMVAL	7:0	r/w	**LED Current Configuration Register** 00000000_B, analog dimming @ 0% of LED current fixed via R_{FB} 11110000_B, (default) analog dimming @ 100% of LED current fixed via R_{FB}
LEDCURRCAL	CALIBVAL	3:0	r/w	**LED Current Accuracy Trimming Configuration Register** LED current calibration value definition, the first bit is the calibration sign: 0000_B, (default) Initial state in the middle of the range 0111_B, maximum calibration value positive 1111_B, maximum calibration value negative
	EOCAL	4	r	End of calibration routine signalling bit: 0_B , (default) calibration routine not completed, not successfully performed or never run. 1_B , calibration successfully performed (is reset to 0_B when SOCAL is set to 1_B)
	SOCAL	5	r/w	Start of calibration routine signalling bit: 0_B , (default) no calibration routine started 1_B , calibration routine start (autoclear)
	DAC_OFF	6	r/w	Switch OFF internal analog dimming DAC bit: 0_B , (default) internal DAC active 1_B , internal DAC inactive and analog dimming error amplifier mapped to SET pin

Table 15 Register description (cont'd)

Register name	Field	Bits	Type	Purpose
SWTMOD	FDEVSPREAD	0	r/w	**Switching Mode Configuration Register** Deviation Frequency f_{DEV} definition: 0_B , (default) ±16% of f_{SW} 1_B , ±8% of f_{SW}
	FMSPREAD	1	r/w	Frequency Modulation Frequency f_{FM} definition: 0_B , (default) 12 kHz 1_B , 18 kHz
	ENSPREAD	2	r/w	Enable Spread Spectrum feature: 0_B , (default) Spread Spectrum modulation disabled 1_B , Spread Spectrum modulation enabled
	S2G_OFF	3	r/w	Short to GND protection enable Bit 0_B , (default) Short to ground protection enabled 1_B , Short to ground protection disabled
	VFB_VIN_OFF	4	r/w	Vin Feedback Enable on VFB_VIN pin 0_B , (default) Enable Vin Feedback 1_B , Disable Vin Feedback
	CCM_4EVER	5	r/w	Forced Continuous Conduction Mode 0_B , (default) Forced CCM after soft start finish 1_B , Forced CCM even during soft start ramp up
	DCM_EN	6	r/w	Enable Bit to allow DCM regulation (MOSFET M4 control) 0_B , (default) DCM is disabled (M4 alternately switching), 1_B , DCM is enabled (M4 is permanently OFF)

Table 15 Register description (cont'd)

Register name	Field	Bits	Type	Purpose
DVCCTRL	IDLE	0	r/w	**Device Control Register** IDLE mode configuration bit: 0_B , ACTIVE mode (default) 1_B , IDLE mode
	SWRST	1	r/w	Software reset bit: 0_B , (default) normal operation 1_B , execute reset command
	CLRLAT	2	r/w	Clear Latch bit: 0_B , (default) normal operation 1_B , execute CLRLAT command
	ENCAL	3	r/w	Enable automatic output current calibration bit: 0_B , (default) DAC takes CALIBVAL from SPI registers 1_B , DAC takes CALIBVAL from last completed automatic calibration procedure; SOCAL Bit can be set.
	SLOPE	5:4	r/w	slope compensation strenght: 00_B , (default) Nominal 01_B , +25% 10_B , -50% 11_B , -25%
	EA_GM	6	r/w	Increase the gain of the error amplifier, active only when output current is below 80% of target (i.e. < VFBH_FBL_EA): 0_B , (default) inactive 1_B , $IFBx_{gm}$ boosted to 1420µS
	EA_IOUT	7	r/w	Bit to decrease the saturation current of the error amplifier in current mode control loop: 0_B , (default) inactive 1_B , active: error amplifier saturation current reduced to 10uA

Table 15 Register description (cont'd)

Register name	Field	Bits	Type	Purpose
MFSSETUP1	LEDCHAIN	3:0	r/w	**Multifloat Switch configuration Register** MFS ratio bits: set MFS jump ratio 0001_B, smallest Value 1 Step 0010_B, 2 Steps 1000_B, (default) 8 Steps 1111_B, 15 Steps 0000_B, largest Value 16 Steps
	EOMFS	4	r	End of MFS routine bit: 0_B , (default) MFS routine not completed, not successfully performed or never run. 1_B , MFS routine successfully performed (is reset to 0_B when SOMFS is set to 1_B).
	SOMFS	5	r/w	Start of MFS routine bit: 0_B , (default) MFS routine not activated 1_B , MFS routine activated
	ILIM_HALF	6	r/w	Bit to decrease the Switch Current Limit (I_{SwLim}) during F.D. operation: 0_B , (default)inactive I_{SwLim} = 2/3of default value 1_B , I_{SwLim} reduced to 1/2of default value
	EA_IOUT_MFS	7	r/w	Bit to decrease the saturation current of the error amplifier (A6) in current mode control loop only during MFS routine: 0_B , (default) inactive 1_B , active: error amplifier current reduced to 20%
MFSSETUP2	MFSDLY	7:0	r/w	**Multifloatswitch configuration register 2 (delay time programming)** 00000000_B, smallest delay time in respect to f_{SW} 11111111_B, largest delay time in respect to f_{SW} 10000000_B, (default) delay time in respect to f_{SW}

Table 15 Register description (cont'd)

Register name	Field	Bits	Type	Purpose
CURRMON	LEDCURR	1:0	r	**Current Monitor Register** Status of the LED Current bits: 00_B , (default) LED current between Target and +25% 01_B , LED current above +25% of Target 10_B , LED current between Target and -25% 11_B , LED current below -25% of Target
	INCURR	3:2	r	Status of the Input Current bits: 00_B , (default) Input current between 75% and 90% of Limit 01_B , Input current between 90% and the Limit 10_B , Input current between 60% and 75% of Limit 11_B , Input current below 60% of Limit
	EOMON	4	r	End of LED/Input Current Monitoring bit: 0_B , (default) Current monitoring routine not completed, not successfully performed or never run. 1_B , Current Monitor routine successfully performed (is reset to 0_B when SOMON is set to 1_B)
	SOMON	5	r/w	Start of LED/Input Current Monitoring bit: 0_B , (default) Current monitor routine not started 1_B , Start of the current monitor routine
REGUSETMON	REGUMODFB	3:2	r	**Regulation Setup And Monitor Register** Feedback of Regulation Mode bits: 01_B , (default) Buck 10_B , Boost 11_B , Buck-Boost
	BB_BST_CMP	1:0	r/w	Buck boost to Boost transition compensation level: 00_B , (default) Min compensation: useful when low switching frequencies are selected 01_B , Low compensation: I.E. adopted @f_{SW}=250kHz 10_B , Mid compensation: I.E. adopted @f_{SW}=400kHz 11_B , Max compensation: useful when high switching frequencies are selected I.E. @f_{SW}=500kHz
MUXCTRL	SO_MUX_SEL	5:0	r/w	**Internal Muxes Configuration Register** Digital Multiplexer selector, output on SO pin: 000000_B, (default) SO pin configured as normal SPI output 000100_B, as default with in addition internal oscillator clock available when CS_N is high
	AMUX_EN	6	r/w	Analog Mux enable, output on FILT pin: 0_B , (default) Analog Mux disabled 1_B , Analog Mux enabled
	MFS_REF	7	r/w	MFS reference to FILT pin Path Enable: 0_B , (default) path disabled 1_B , Path Enabled

13 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

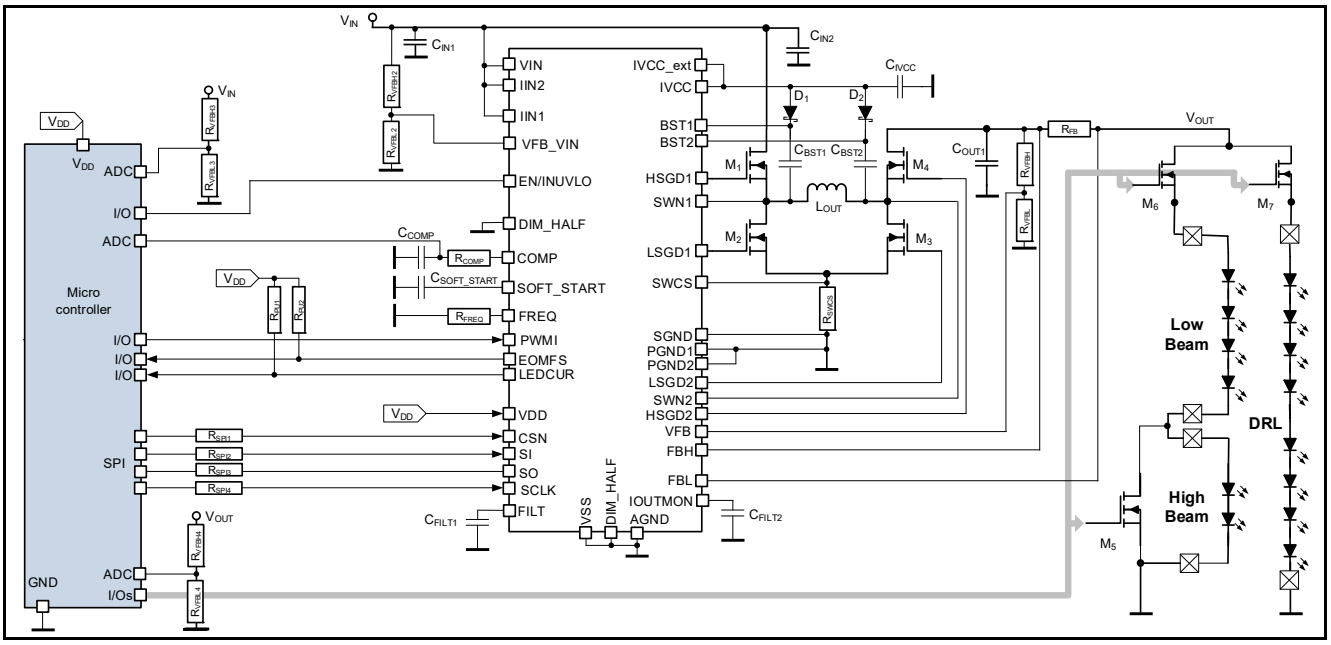


Figure 44 Application Drawing - TLD5542-1 on a 3 functions LED Driver Module

Table 16 BOM - TLD5542-1 as current regulator (I_{OUT} = 1 A, f_{SW} = 300 kHz)

Reference Designator	Value	Manufacturer	Part Number	Type
D_1 , D_2	BAT46WJ	--	BAT46WJ	Diode
C_{IN1}	10 µF, 50 V	TDK	X7R	Capacitor
C_{IN2}	4.7 µF, 50 V	TDK	X7R	Capacitor
$C_{FILT1,2}$	220 pF, 10 V	TDK	X7R	Capacitor
C_{COMP}	15 nF, 16 V	TDK	X7R	Capacitor
C_{SOFT_START}	15 nF, 16 V	TDK	X7R	Capacitor
C_{OUT1}	3x3.3 µF, 100 V	TDK	X7R	Capacitor
C_{IVCC}	10 µF, 16 V	TDK	X7R	Capacitor
C_{BST1} , C_{BST2}	100 nF, 16 V	TDK	X7R	Capacitor
IC_1	--	Infineon	TLD5542-1	IC
L_{OUT}	10 µH	TDK	SPM10065VT-100M	Inductor
R_{FB}	0.100 Ω, 1%	Panasonic	--	Resistor
R_1 , R_2 , R_3 , R_{PD} , R_{EN} , R_{PWMI} , R_{Sense1} , R_{Sense2} , R_{SYNC} , R_{SCLK} , R_{SI} , R_{SO} , R_{CSN}	xx kΩ, 1%	Panasonic	--	Resistor
R_{VFBL} , R_{VFBH}	1k5Ω, 51kΩ, 1%	Panasonic	--	Resistor
R_{VFBL2} , R_{VFBH2}	1kΩ, 51kΩ, 1%	Panasonic	--	Resistor

Table 16 BOM - TLD5542-1 as current regulator (I_{OUT} = 1 A, f_{SW} = 300 kHz)

Reference Designator	Value	Manufacturer	Part Number	Type
R_{COMP}	1k Ω, 1%	Panasonic	--	Resistor
R_{FREQ}	24 kΩ, 1%	Panasonic	--	Resistor
R_{SWCS}	0.007 Ω, 1%	Panasonic	ERJB1CFR05U	Resistor
M_1 , M_2 , M_3 , M_4, M_5, M_6, M_7	Dual MOSFET: 60V / 26 mΩ N-ch	Infineon	IPG20N10S4L-26	Transistor

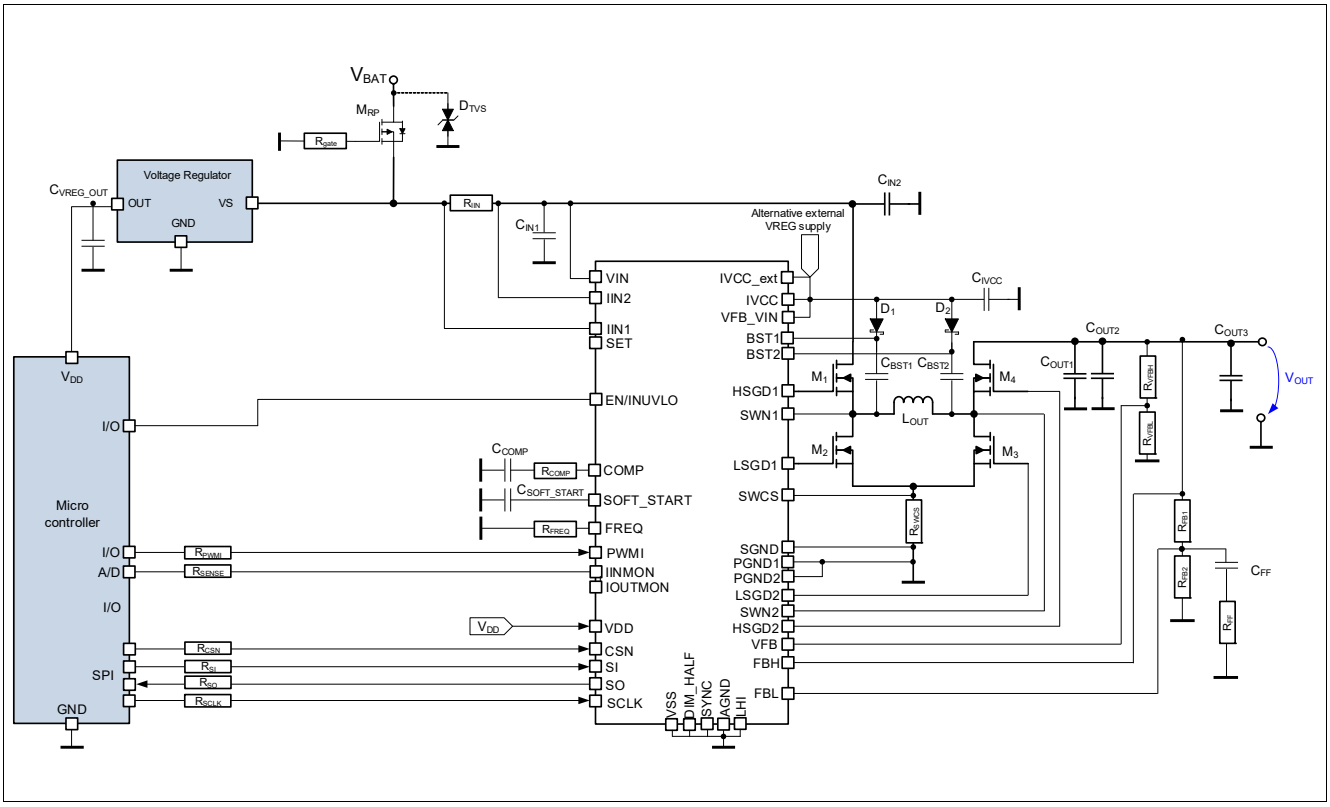


Figure 45 Application Drawing - TLD5542-1 as adjustable voltage regulator

Table 17 BOM - TLD5542-1 as voltage regulator

Reference Designator	Value	Manufacturer	Part Number	Type
D_1 , D_2	BAT46WJ	--	BAT46WJ	Diode
C_{IN1}	1 µF, 100 V	TDK	X7R	Capacitor
C_{IN2}	4.7 µF, 100 V	TDK	X7R	Capacitor
C_{COMP}	22 nF, 16 V	TDK	X7R	Capacitor
C_{FF}	10 nF, 50 V	TDK	X7R	Capacitor
C_{SOFT_START}	22 nF, 16 V	TDK	X7R	Capacitor
C_{OUT1}	3x4.7 µF, 100 V	TDK	X7R	Capacitor
C_{OUT2} , C_{OUT3}	100 nF, 100 V	TDK	X7R	Capacitor
C_{IVCC}	10 µF, 16 V	TDK	X7R	Capacitor
C_{BST1} , C_{BST2}	100 nF, 16 V	TDK	X7R	Capacitor
IC_1	--	Infineon	TLD5542-1	IC

Table 17 BOM - TLD5542-1 as voltage regulator

Reference Designator	Value	Manufacturer	Part Number	Type
L_{OUT}	10 µH	Coilcraft	XAL1010-103MEC	Inductor
R_{FF}	1.5 kΩ, 1%	Panasonic	--	Resistor
R_{FB1} , R_{FB2}	150Ω, 20.5kΩ, 1%	Panasonic	--	Resistor
R_{IN}	0.005 Ω, 1%	Panasonic	--	Resistor
R_{PWMI} , R_{Sense1} , R_{Sense2} , R_{SYNC} , R_{SCLK} , R_{SI} , R_{SO} , R_{CSN}	xx kΩ, 1%	Panasonic	--	Resistor
R_{VFBL} , R_{VFBH}	1.5 kΩ, 24 kΩ, 1%	Panasonic	--	Resistor
R_{COMP}	0 Ω, 1%	Panasonic	--	Resistor
R_{FREQ}	37.4 kΩ, 1%	Panasonic	--	Resistor
R_{SWCS}	0.007 Ω, 2%	--	--	Resistor
M_1 , M_2 , M_3 , M_4	Dual MOSFET: 100 V / 35 mΩ N-ch	Infineon	IPG20N10S4L-35	Transistor

13.1 Further Application Information

Typical Performance Characteristics of Device

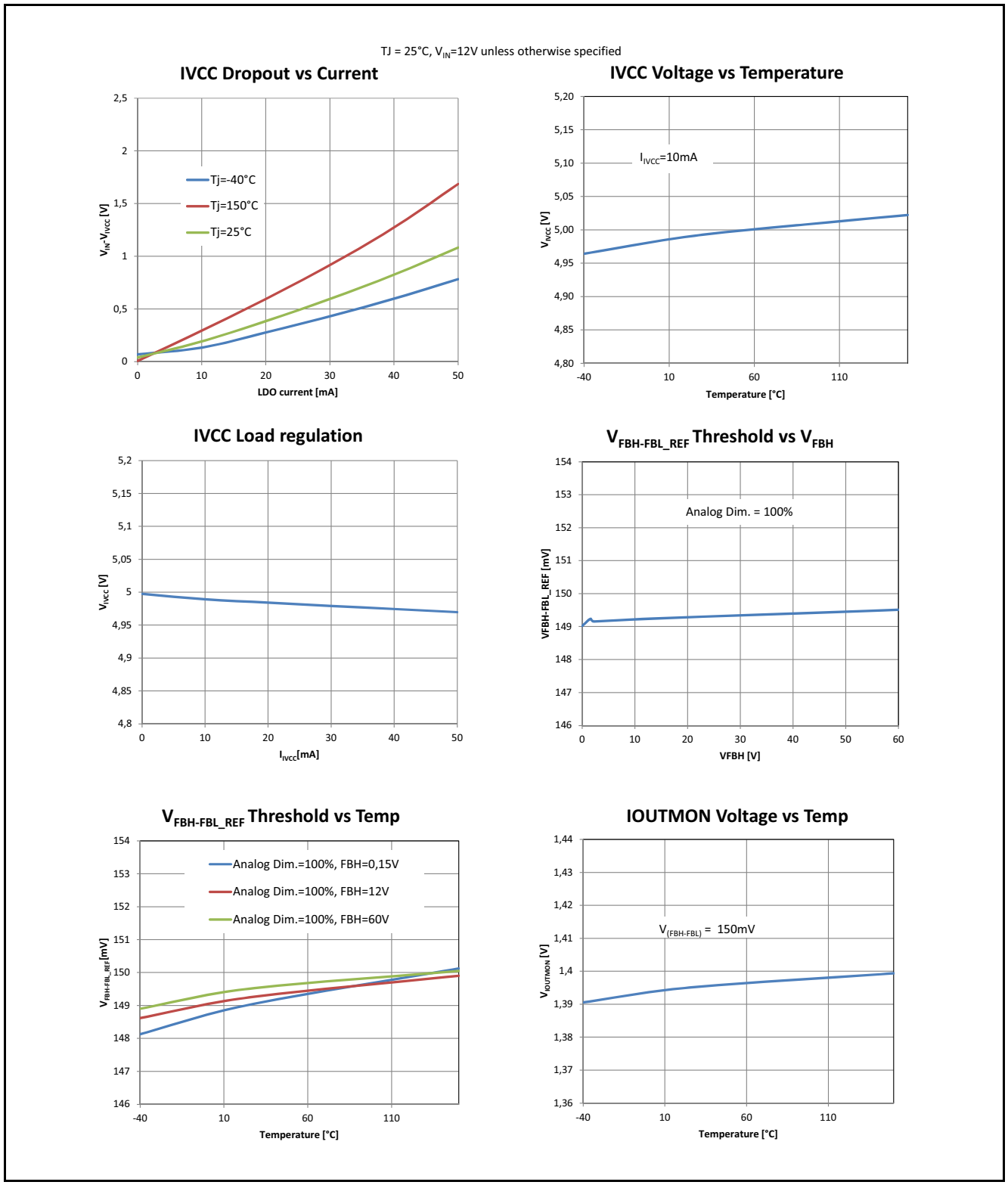


Figure 46 Characterization Diagrams 1

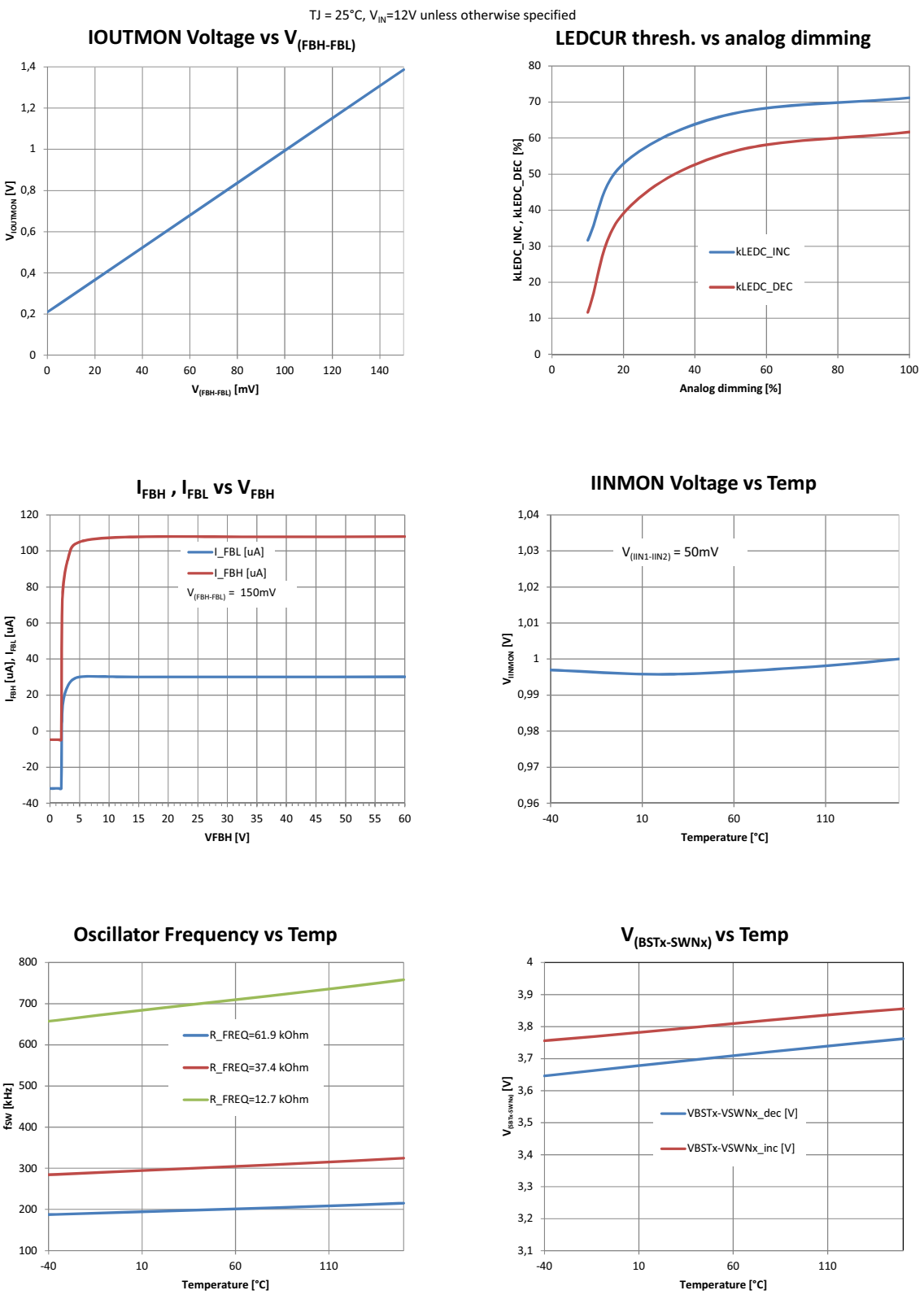


Figure 47 Characterization Diagrams 2

- For further information you may contact **http://www.infineon.com/**

14 Package Outlines

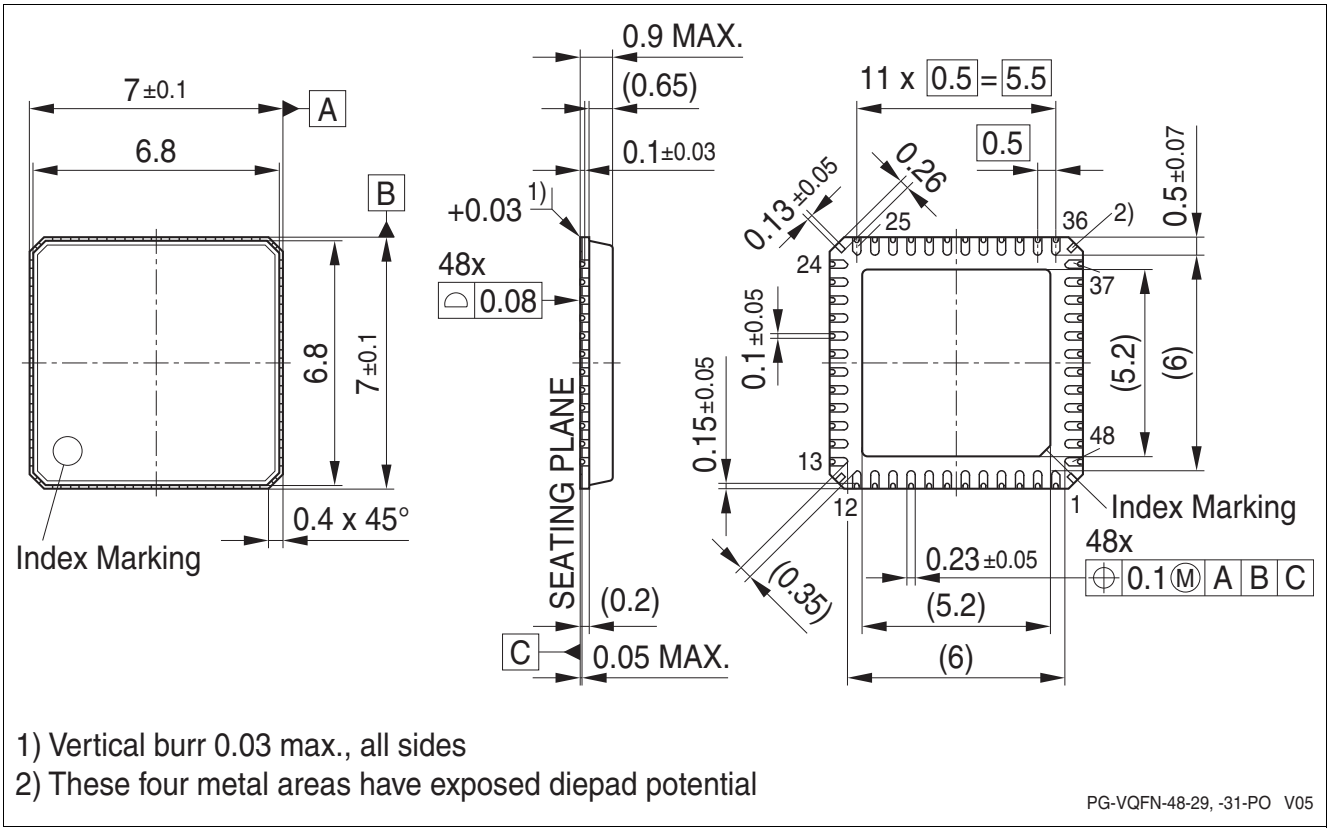


Figure 48 PG-VQFN-48 (with LTI)

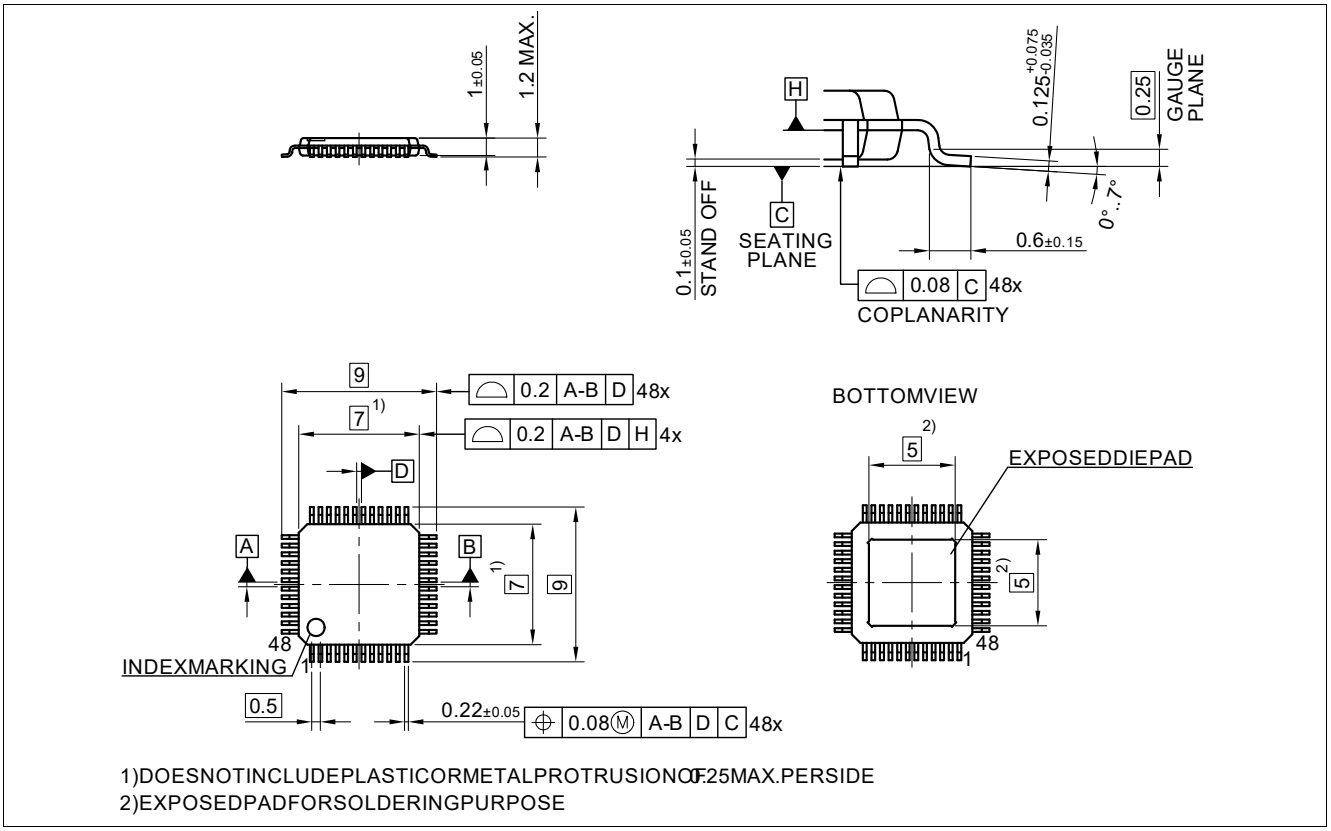


Figure 49 PG-TQFP-48

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

15 Revision History

Table 18 Revision History

Revision	Date	Changes
Rev. 1.0	2019-11-21	Released datasheet
Rev. 1.10	2019-12-11	changed ESD in to “CDM” AECQ100-011 including revision : Rev. D
Rev. 1.10	2019-12-11	Updated Vout Overvoltage description **Chapter 10.2**

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Edition 2019-12-11
Published by
Infineon Technologies AG
81726 Munich, Germany

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Document reference
TLD5542-1

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