

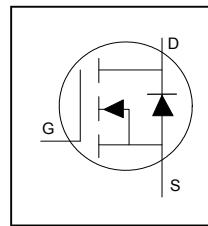
### Application

- Brushed motor drive applications
- BLDC motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC inverters

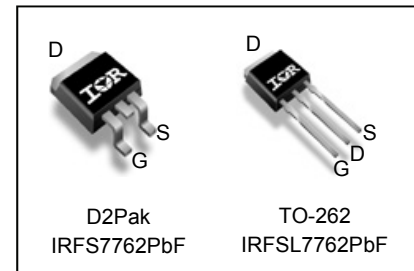
### Benefits

- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche SOA
- Enhanced body diode dV/dt and dI/dt capability
- Lead-free, RoHS compliant

HEXFET® Power MOSFET

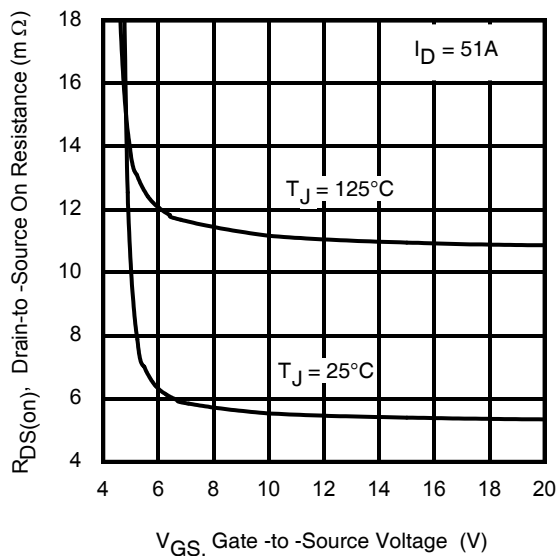


<b>V<sub>DSS</sub></b>	<b>75V</b>
<b>R<sub>DS(on)</sub> typ.</b>	<b>5.6mΩ</b>
	<b>6.7mΩ</b>
<b>I<sub>D</sub></b>	<b>85A</b>

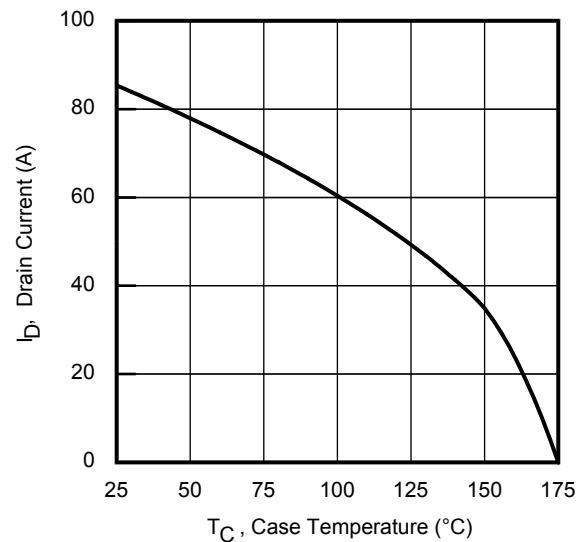


<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFSL7762PbF	TO-262	Tube	50	IRFSL7762PbF
IRFS7762PbF	D <sup>2</sup> -Pak	Tube	50	IRFS7762PbF
		Tape and Reel Left	800	IRFS7762TRLpF



**Fig 1.** Typical On-Resistance vs. Gate Voltage



**Fig 2.** Maximum Drain Current vs. Case Temperature

**Absolute Maximum Rating**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	85	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	60	
$I_{DM}$	Pulsed Drain Current ①	335	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	140	W
	Linear Derating Factor	0.95	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

**Avalanche Characteristics**

Symbol	Parameter	Max.	Units
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ③	160	mJ
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ⑧	243	
$I_{AR}$	Avalanche Current ①	See Fig 15, 16, 23a, 23b	A
$E_{AR}$	Repetitive Avalanche Energy ①		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦	—	1.05	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑨	—	40	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	58	—	mV/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	5.6	6.7	mΩ	$V_{GS} = 10\text{V}, I_D = 51\text{A}$
		—	6.6	—		$V_{GS} = 6.0\text{V}, I_D = 26\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	2.1	—	3.7	V	$V_{DS} = V_{GS}, I_D = 100\mu\text{A}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 75\text{V}, V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 75\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
$R_G$	Gate Resistance	—	2.5	—	Ω	

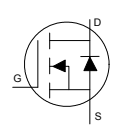
**Notes:**

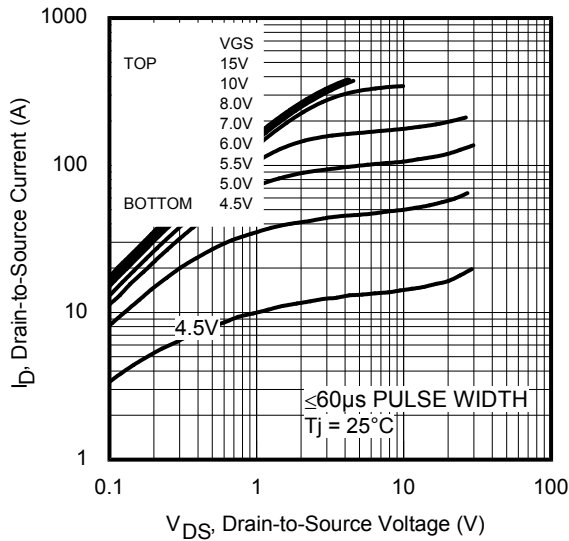
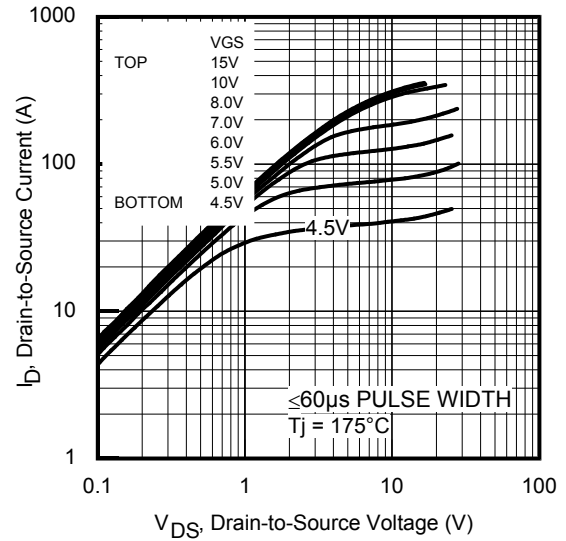
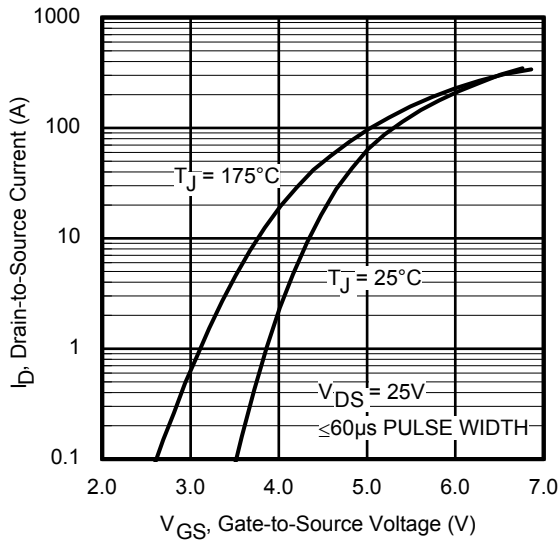
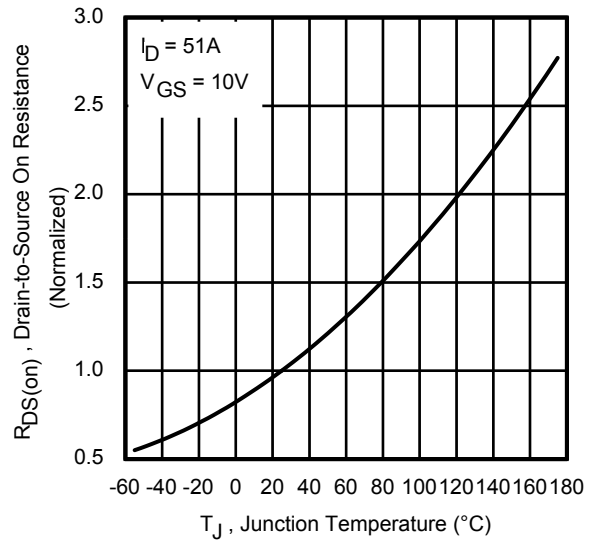
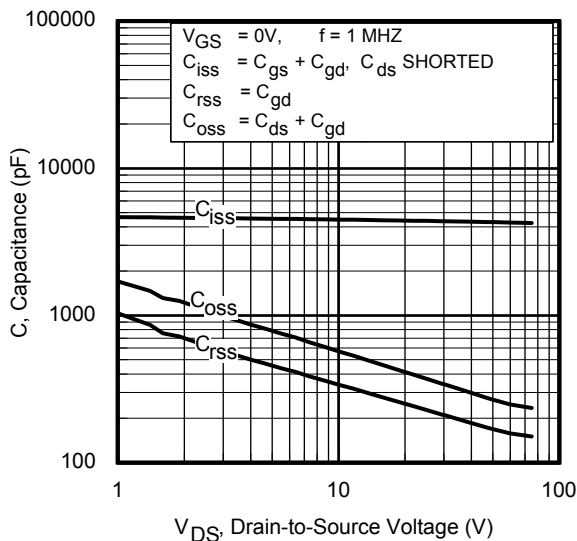
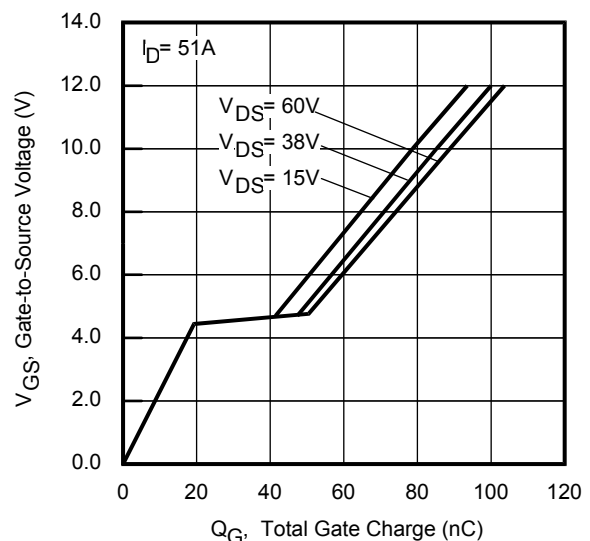
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 120\mu\text{H}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 51\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ③  $I_{SD} \leq 51\text{A}$ ,  $di/dt \leq 735\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $R_{\theta}$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑧ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 22\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ⑨ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994: <http://www.irf.com/technical-info/appnotes/an-994.pdf>

**Dynamic Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	180	—	—	S	$V_{DS} = 10\text{V}, I_D = 51\text{A}$
$Q_g$	Total Gate Charge	—	85	130	nC	$I_D = 51\text{A}$ $V_{DS} = 38\text{V}$ $V_{GS} = 10\text{V}$
$Q_{gs}$	Gate-to-Source Charge	—	21	—		
$Q_{gd}$	Gate-to-Drain Charge	—	26	—		
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	60	—		
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	$V_{DD} = 38\text{V}$ $I_D = 51\text{A}$ $R_G = 2.7\Omega$ $V_{GS} = 10\text{V}$ ④
$t_r$	Rise Time	—	49	—		
$t_{d(off)}$	Turn-Off Delay Time	—	57	—		
$t_f$	Fall Time	—	40	—		
$C_{iss}$	Input Capacitance	—	4440	—	pF	$V_{GS} = 0\text{V}$ $V_{DS} = 25\text{V}$ $f = 1.0\text{MHz}$ , See Fig.7 $V_{GS} = 0\text{V}, V_{DS} = 0\text{V to } 60\text{V}$ ⑥ $V_{GS} = 0\text{V}, V_{DS} = 0\text{V to } 60\text{V}$ ⑤
$C_{oss}$	Output Capacitance	—	370	—		
$C_{rss}$	Reverse Transfer Capacitance	—	230	—		
$C_{oss\ eff. (ER)}$	Effective Output Capacitance (Energy Related)	—	330	—		
$C_{oss\ eff. (TR)}$	Output Capacitance (Time Related)	—	430	—		

**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	85	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	335		
$V_{SD}$	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 51\text{A}, V_{GS} = 0\text{V}$ ④
$dv/dt$	Peak Diode Recovery $dv/dt$	—	13	—	V/ns	$T_J = 175^\circ\text{C}, I_S = 51\text{A}, V_{DS} = 75\text{V}$ ③
$t_{rr}$	Reverse Recovery Time	—	34	—	ns	$T_J = 25^\circ\text{C}$ $V_{DD} = 64\text{V}$ $T_J = 125^\circ\text{C}$ $I_F = 51\text{A}$ , $di/dt = 100\text{A}/\mu\text{s}$ ④
		—	46	—		
$Q_{rr}$	Reverse Recovery Charge	—	54	—	nC	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$
		—	69	—		
$I_{RRM}$	Reverse Recovery Current	—	2.7	—	A	$T_J = 25^\circ\text{C}$


**Fig 3. Typical Output Characteristics**

**Fig 4. Typical Output Characteristics**

**Fig 5. Typical Transfer Characteristics**

**Fig 6. Normalized On-Resistance vs. Temperature**

**Fig 7. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage**

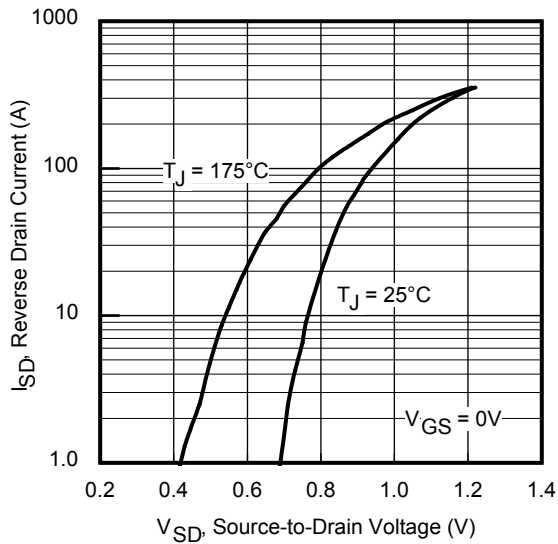


Fig 9. Typical Source-Drain Diode Forward Voltage

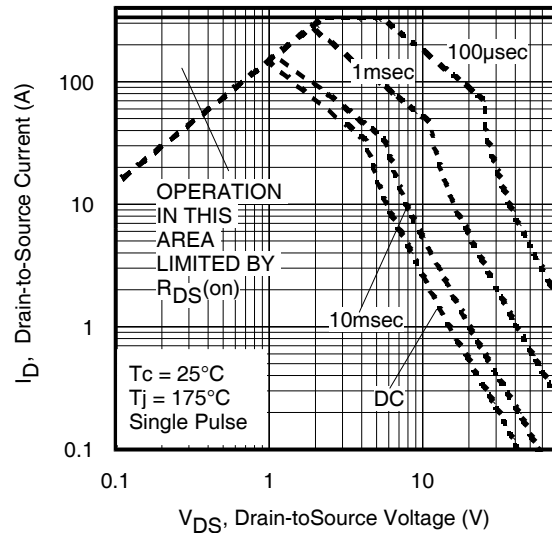


Fig 10. Maximum Safe Operating Area

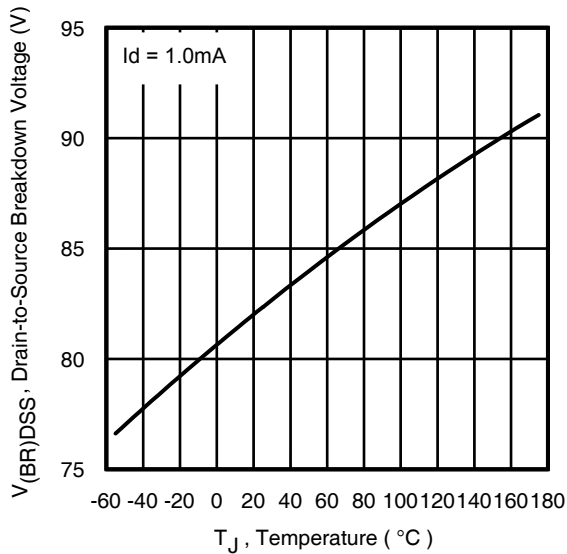


Fig 11. Drain-to-Source Breakdown Voltage

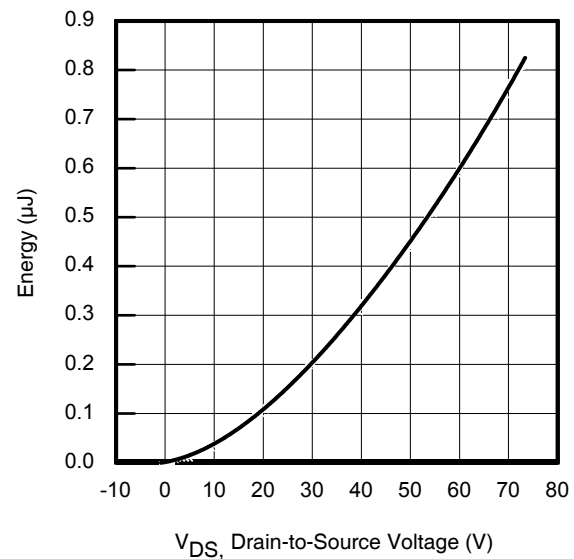


Fig 12. Typical  $C_{oss}$  Stored Energy

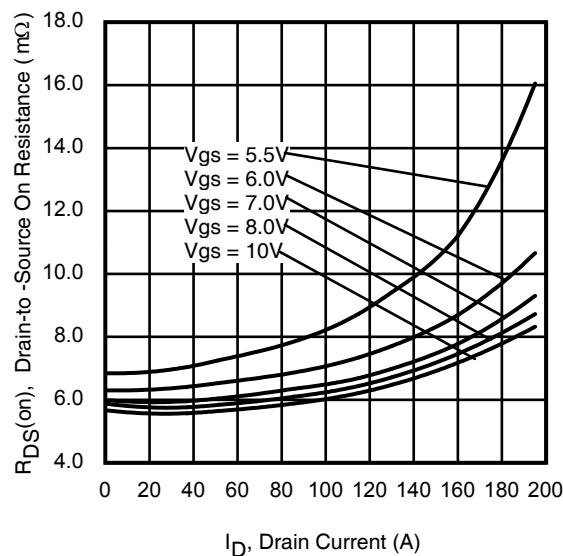
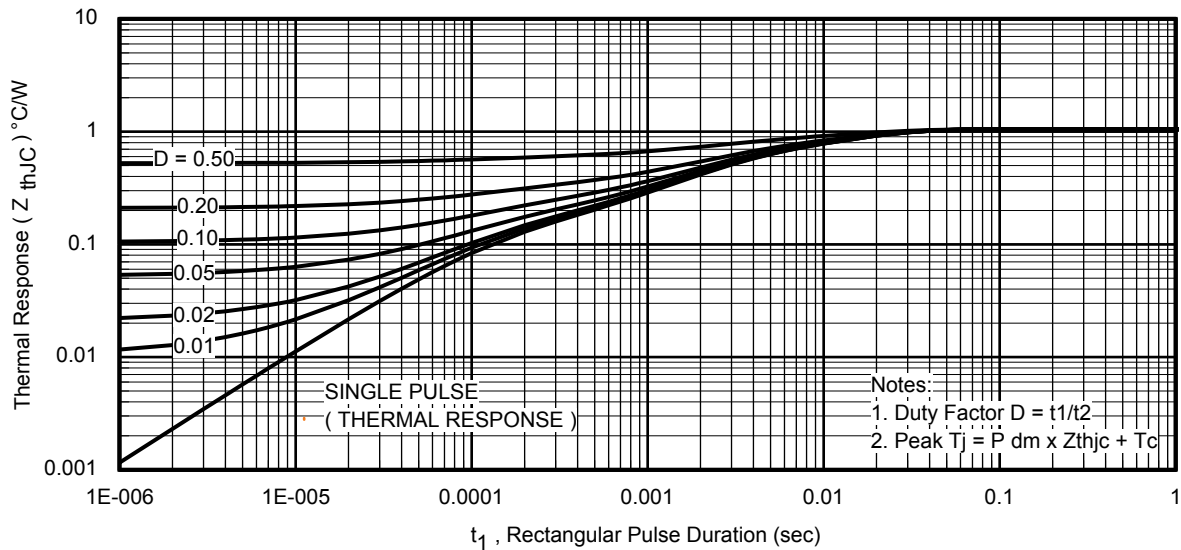
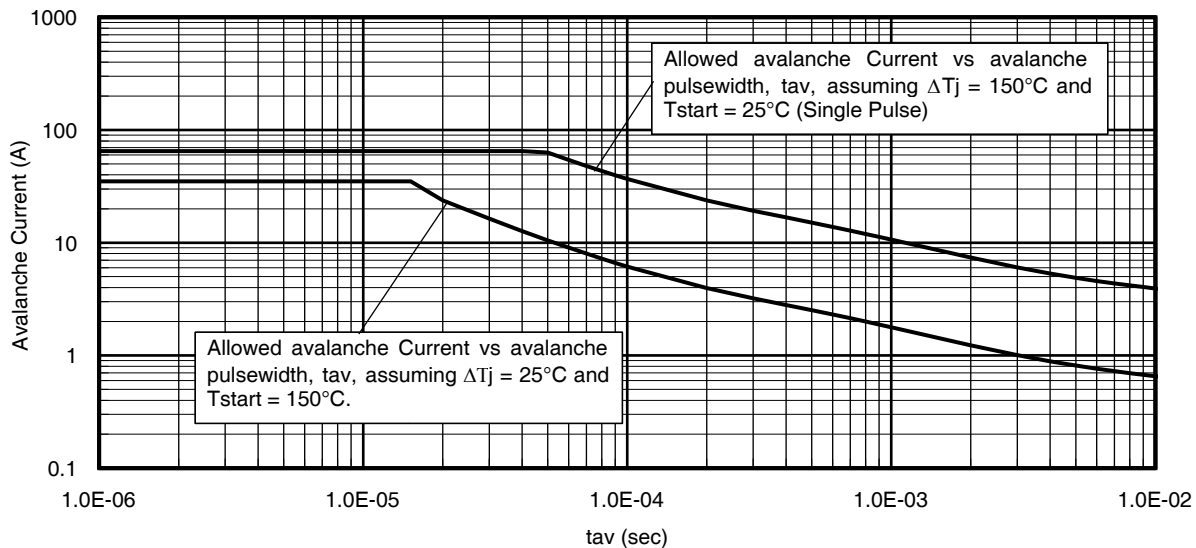
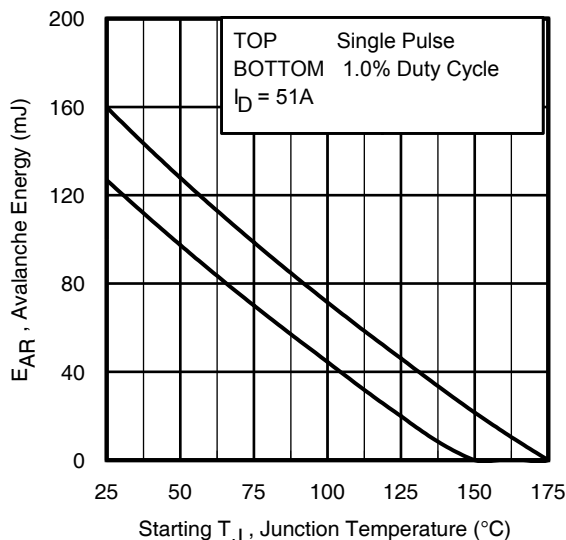


Fig 13. Typical On-Resistance vs. Drain Current


**Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 15. Avalanche Current vs. Pulse Width**

**Fig 16. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves , Figures 15, 16:  
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)  
 $P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$   
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$   
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$

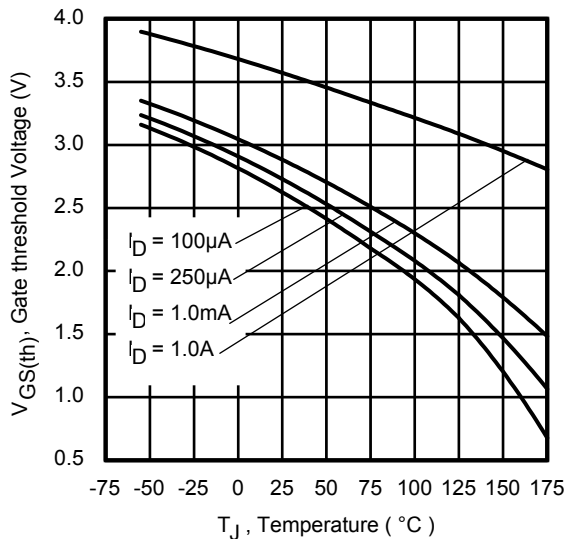


Fig 17. Threshold Voltage vs. Temperature

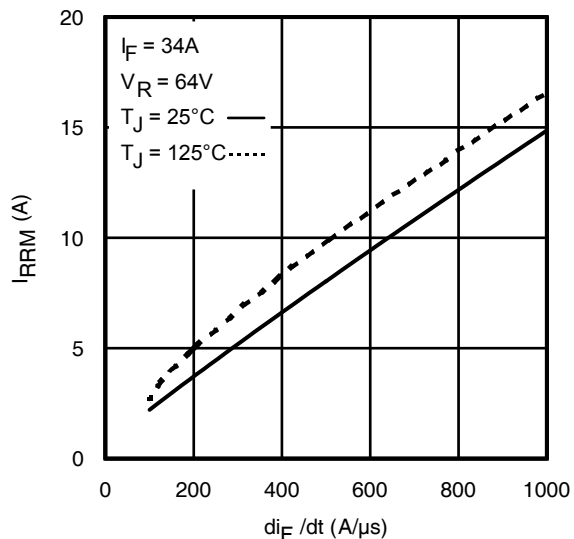


Fig 18. Typical Recovery Current vs. di/dt

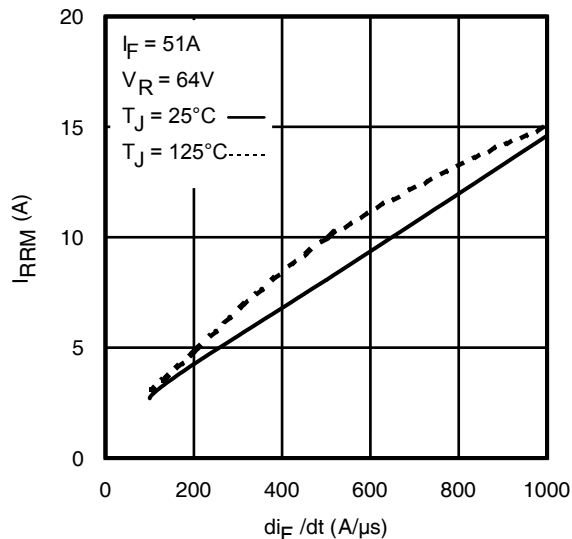


Fig 19. Typical Recovery Current vs. di/dt

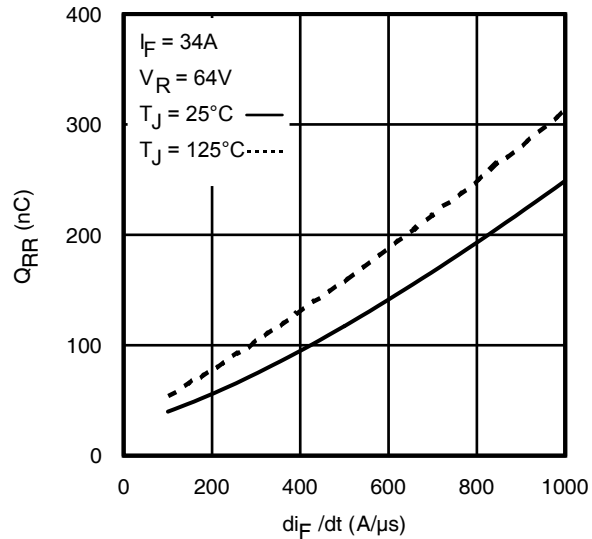


Fig 20. Typical Stored Charge vs. di/dt

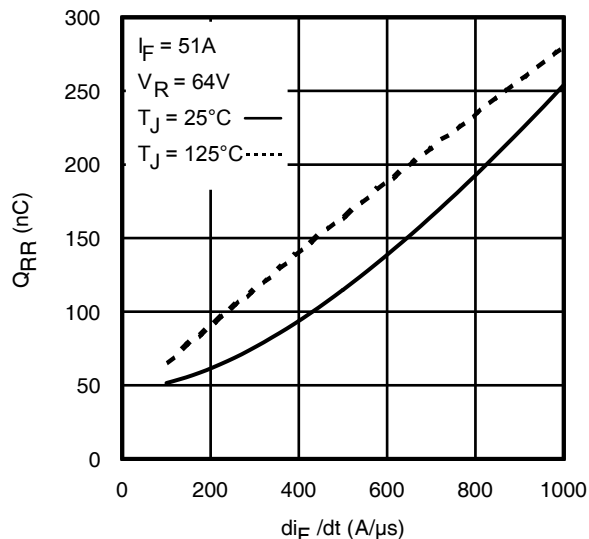
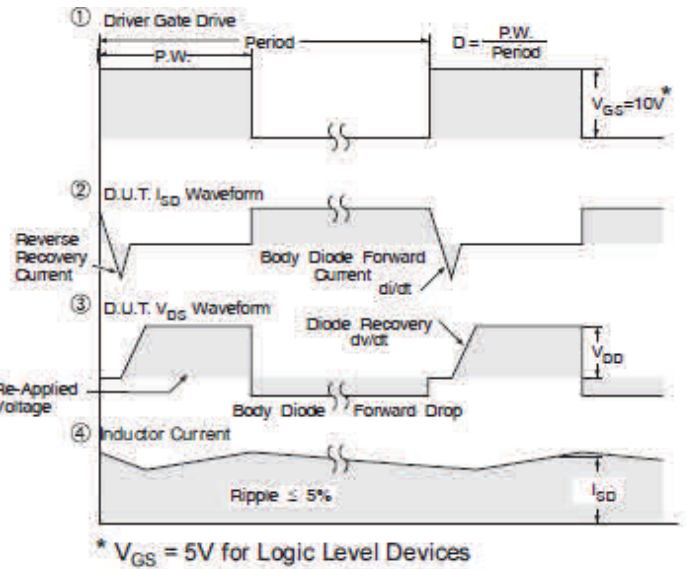
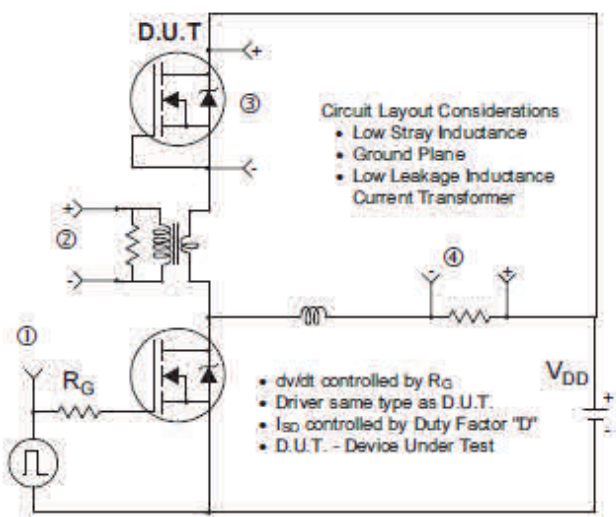
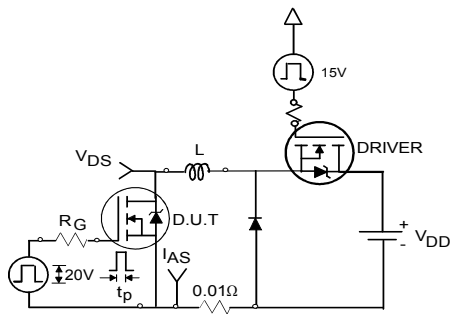


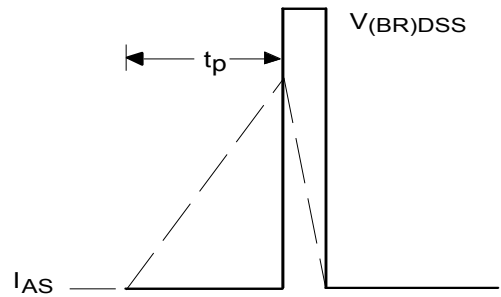
Fig 21. Typical Stored Charge vs. di/dt



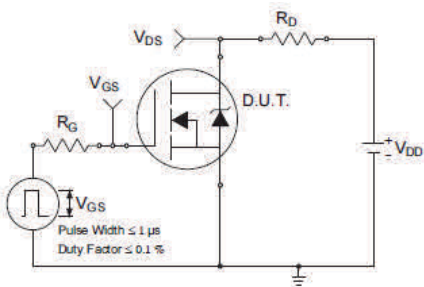
**Fig 22.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs



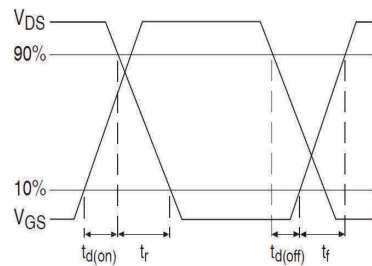
**Fig 23a.** Unclamped Inductive Test Circuit



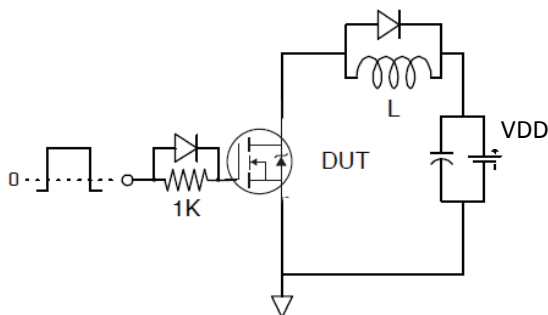
**Fig 23b.** Unclamped Inductive Waveforms



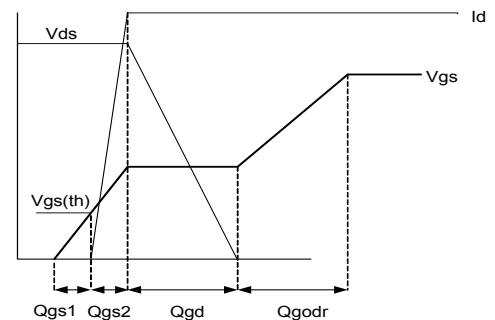
**Fig 24a.** Switching Time Test Circuit



**Fig 24b.** Switching Time Waveforms



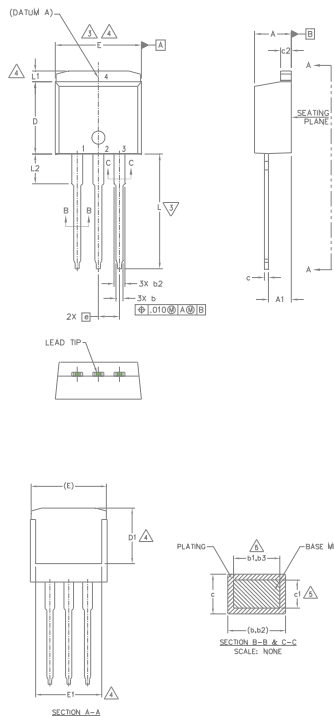
**Fig 25a.** Gate Charge Test Circuit



**Fig 25b.** Gate Charge Waveform



TO-262 Package Outline (Dimensions are shown in millimeters (inches))



SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.06	4.83	.160	.190	5	
A1	2.03	3.02	.080	.119		
b	0.51	0.99	.020	.039		
b1	0.51	0.89	.020	.035		
b2	1.14	1.78	.045	.070		
b3	1.14	1.73	.045	.068		
c	0.38	0.74	.015	.029		
c1	0.38	0.58	.015	.023		5
c2	1.14	1.65	.045	.065		
D	8.38	9.65	.330	.380		3
D1	6.86	-	.270	-	4	
E	9.65	10.67	.380	.420	3,4	
E1	6.22	-	.245	-	4	
e	2.54	BSC	.100	BSC		
L	13.46	14.10	.530	.555	4	
L1	-	1.65	-	.065		
L2	3.56	3.71	.140	.146		

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
  5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  6. CONTROLLING DIMENSION: INCH.
  7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

- IGBTs, CoPACK
- 1.- GATE
  - 2.- COLLECTOR
  - 3.- EMITTER
  - 4.- COLLECTOR

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

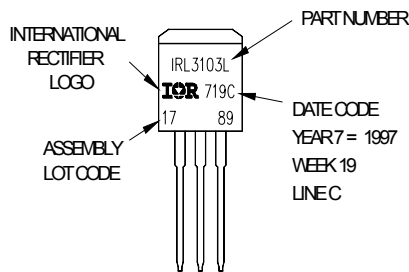
DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE

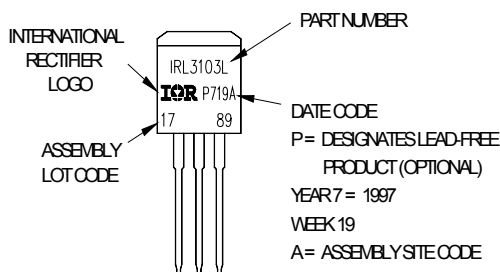
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON VVV19, 1997  
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"

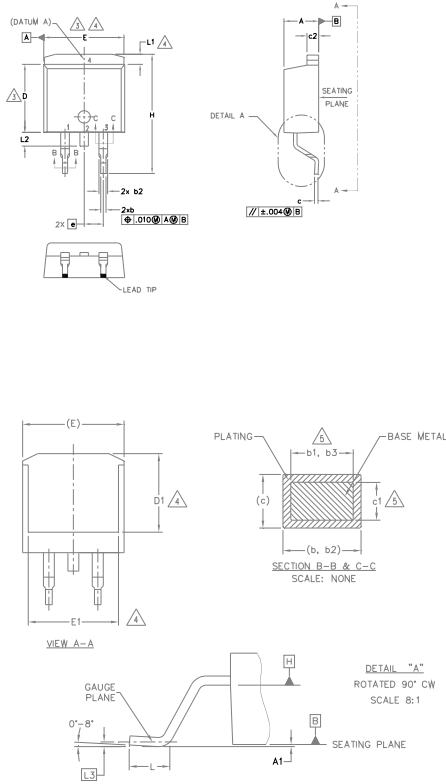


OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**D<sup>2</sup>Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))**



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	
E1	6.22	-	.245	-	4
e	2.54	BSC	.100	BSC	
H	14.61	15.88	.575	.625	4
L	1.78	2.79	.070	.110	
L1	-	1.68	-	.066	
L2	-	1.78	-	.070	
L3	0.25	BSC	.010	BSC	

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
  4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
  5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
  6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
  7. CONTROLLING DIMENSION: INCH.
  8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

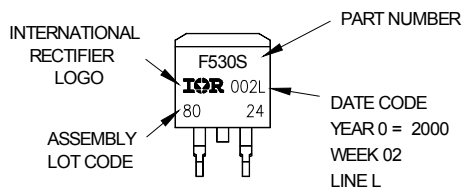
LEAD ASSIGNMENTS

- DIODES
- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
  - 2, 4.- CATHODE
  - 3.- ANODE
- HEXFET
- 1.- GATE
  - 2, 4.- DRAIN
  - 3.- SOURCE
- IGBTs, CoPACK
- 1.- GATE
  - 2, 4.- COLLECTOR
  - 3.- EMITTER

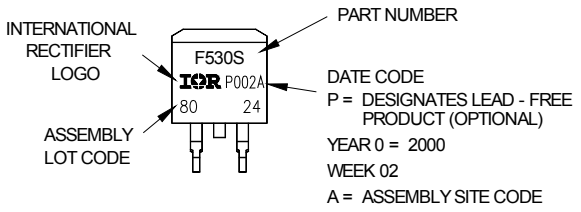
**D<sup>2</sup>Pak (TO-263AB) Part Marking Information**

EXAMPLE: THIS IS AN IRF530S WITH LOT CODE 8024 ASSEMBLED ON VWV 02, 2000 IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead - Free"

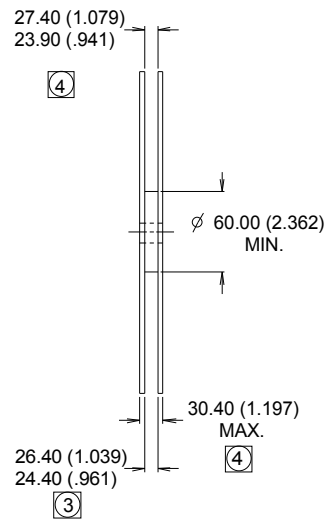
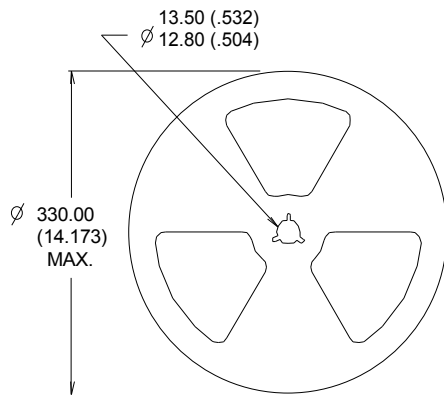
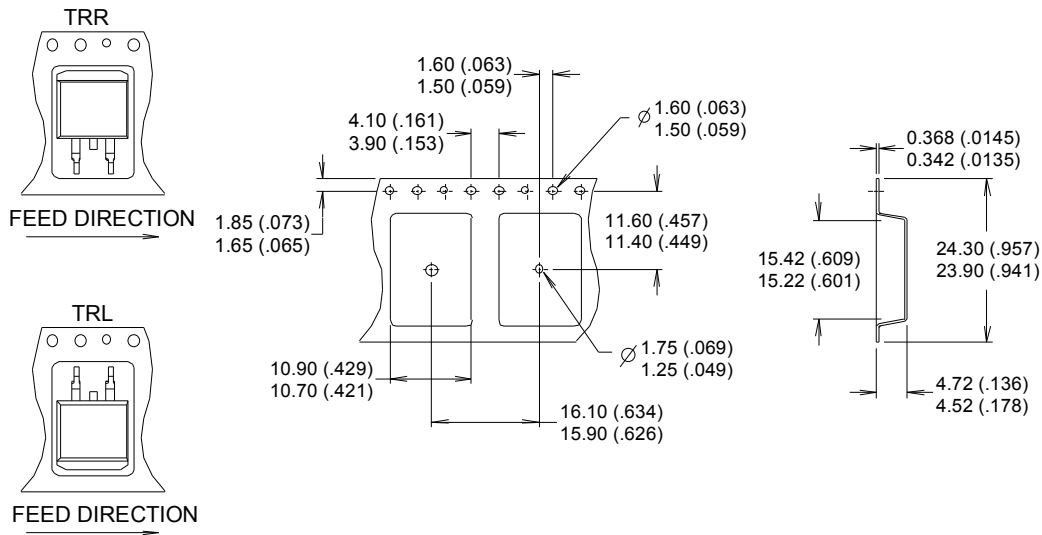


OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

D<sup>2</sup>Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))



- NOTES :
1. COMFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  - ③ DIMENSION MEASURED @ HUB.
  - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information†**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F) ††	
<b>Moisture Sensitivity Level</b>	D <sup>2</sup> Pak	MSL1
	TO-262	
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier’s web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comments
2/19/2015	<ul style="list-style-type: none"> <li>Updated <math>E_{AS (L=1mH)} = 243mJ</math> on page 2</li> <li>Updated note 8 “Limited by <math>T_{Jmax}</math>, starting <math>T_J = 25^{\circ}C</math>, <math>L = 1mH</math>, <math>R_G = 50\Omega</math>, <math>I_{AS} = 22A</math>, <math>V_{GS} = 10V</math>” on page 2</li> </ul>

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