OptiMOS™ Power Stage

TDA21490

1 Description

- High frequency, low profile dc-dc converters
- Voltage Regulators for CPUs, GPUs, and high current rails

The TDA21490 power stage contains a low quiescent-current synchronous buck gate-driver IC co-packaged with high-side and low-side MOSFETs. The package is optimized for PCB layout, heat transfer, driver/MOSFET control timing, and minimal switch node ringing when layout guidelines are followed. The gate driver and MOSFET combination enables higher efficiency at the lower output voltages required by cutting edge CPU, GPU and DDR memory designs.

The TDA21490 internal MOSFET current sense algorithm with temperature compensation achieves superior current sense accuracy versus best-in-class controller-based inductor DCR sense methods. Protection includes cycle-by-cycle over-current protection with programmable threshold, VCC/VDRV UVLO protection, bootstrap capacitor under-voltage protection, phase fault detection, IC temperature reporting and thermal shutdown. The TDA21490 also features auto-replenishment of the bootstrap capacitor to prevent over-discharging. The TDA21490 features a deep-sleep power saving mode, which greatly reduces the power consumption when the multiphase system enters PS3/PS4 mode.

Operation at switching frequency as high as 1.5 MHz enables high performance transient response, allowing reduction of output inductance and output capacitance values while maintaining industry leading efficiency.

The TDA21490 is optimized for CPU core power delivery in server applications. The ability to meet the stringent requirements of the server market also makes the TDA21490 ideally suited for powering GPU and DDR memory designs.

2 Features

- Co-packaged driver, high-side and low-side MOSFETs
- 5-mV/A on-chip MOSFET current sensing with temperature compensated reporting
- Input voltage (VIN) range of 4.25 V to 16 V
- VCC and VDRV supply of 4.25 V to 5.5 V
- Output voltage range from 0.25 V up to 5.5 V
- Output peak current capability of 90 A
- Output DC current capability of 70 A
- Operation up to 1.5 MHz
- VCC/VDRV under-voltage lockout (UVLO)
- Bootstrap capacitor under-voltage protection
- 8-mV/°C temperature analog output
- Thermal shutdown and fault flag
- Cycle-by-cycle over-current protection with programmable threshold and fault flag
- MOSFET phase fault detection and flag
- Auto-replenishment of bootstrap capacitor
- Deep-sleep mode for power saving

Pinout

- Compatible with 3.3-V tri-state PWM input
- Body-Braking load transient support
- Small 5 mm x 6 mm x 1 mm PQFN package
- Lead free RoHS compliant package

Table 1 Product Identification

Base Part Number	Temp Range	Package	Orderable Part Number
TDA21490	-40 °C to 125 °C	PQFN 5 mm x 6 mm	TDA21490AUMA1

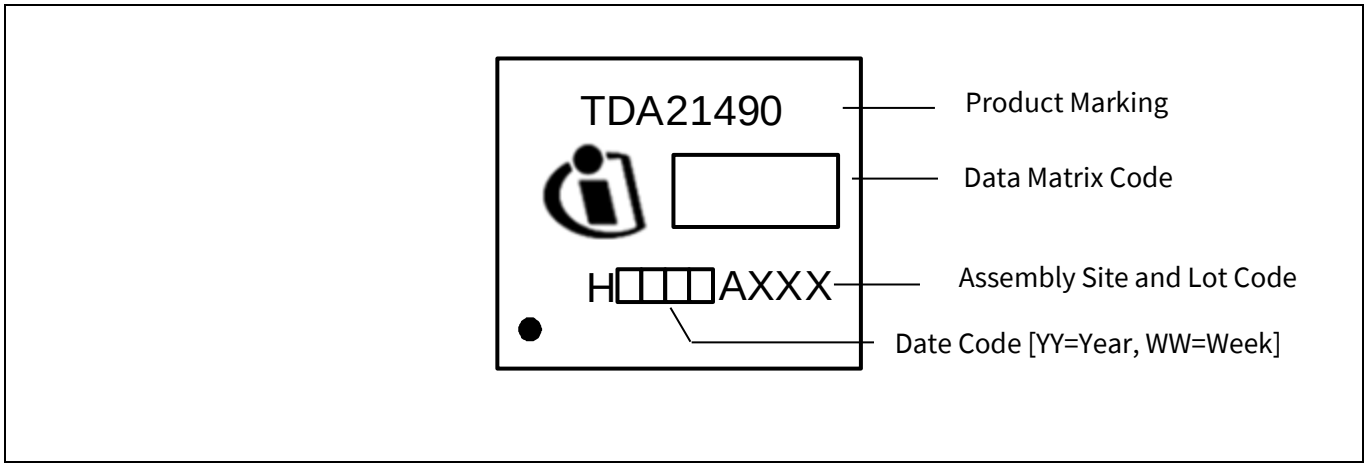

Figure 1 Picture of the Product

3 Pinout

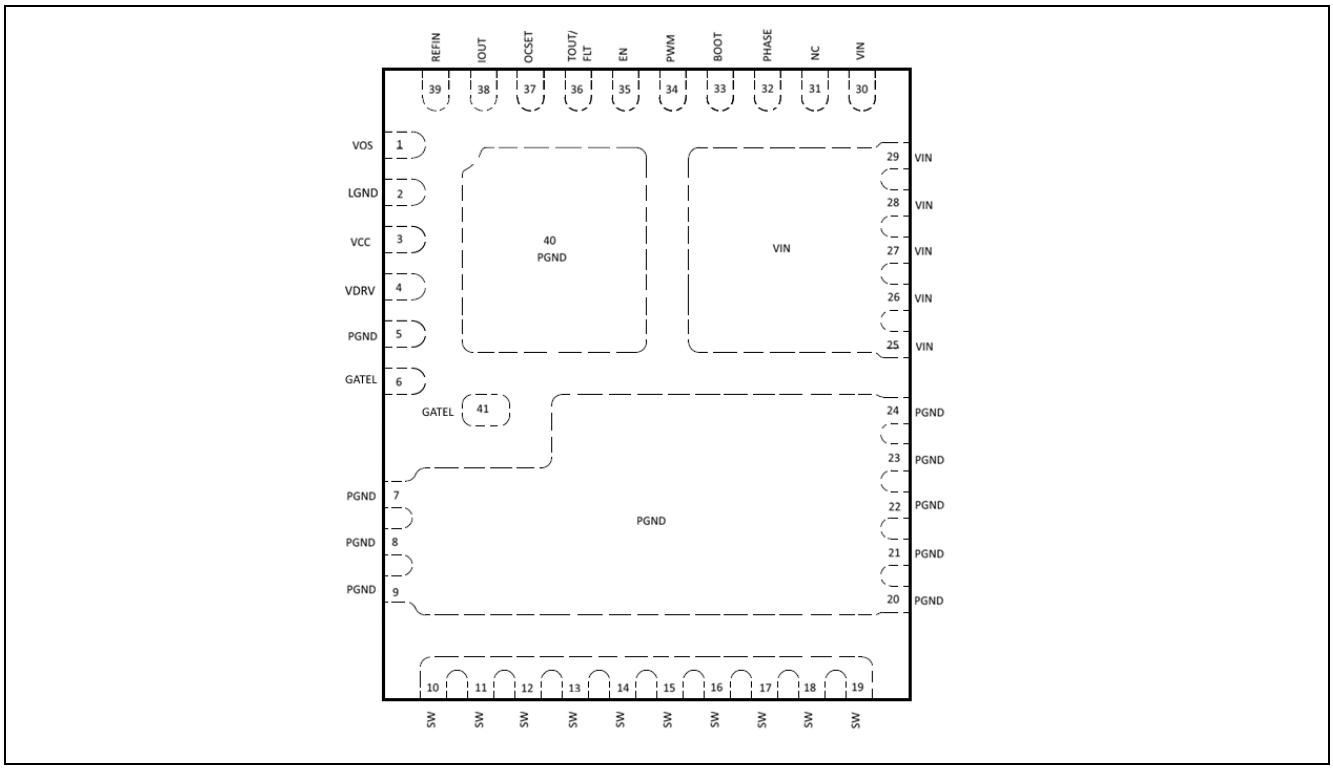

Figure 2 Pinout, Numbering and Name of Pins (transparent top view)

4 Block Diagram

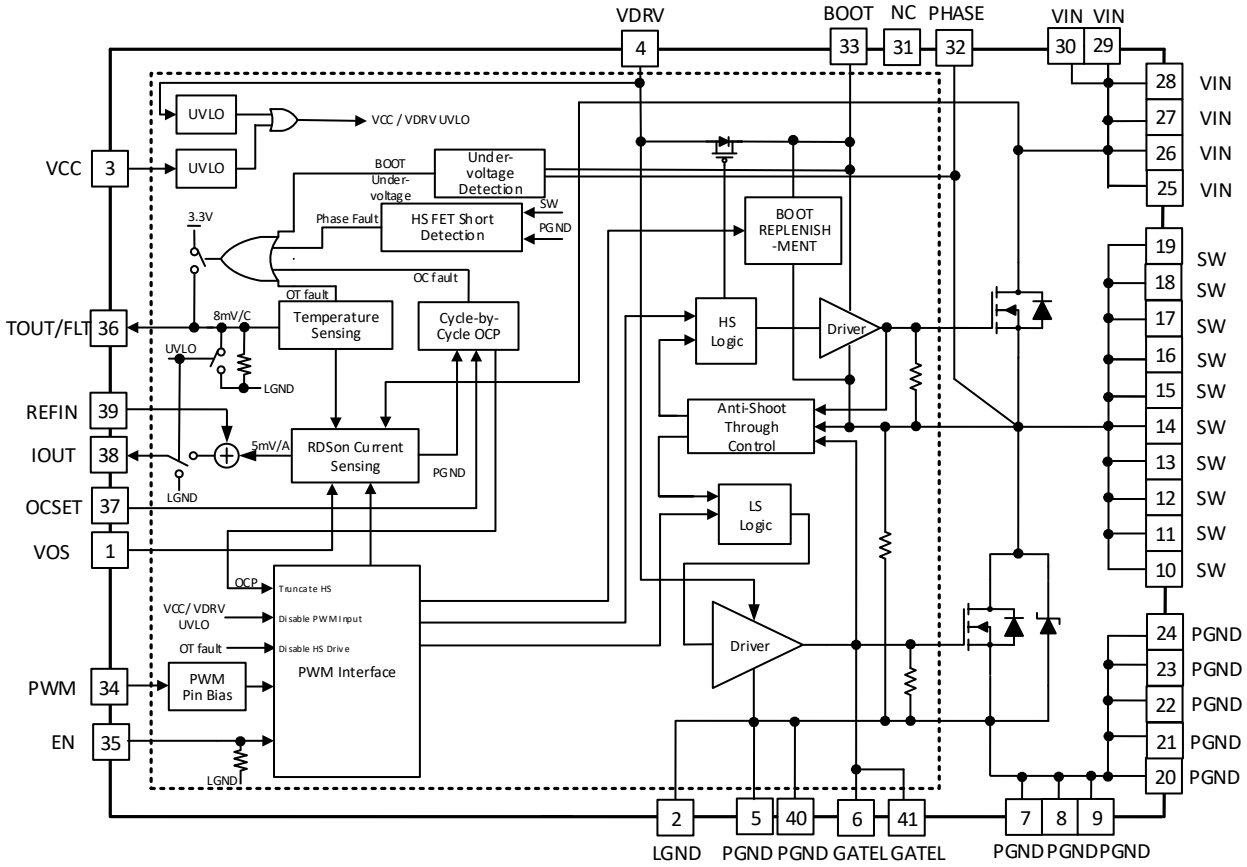

Figure 3 Block Diagram

Block Diagram

Table 2 I/O Signals

Pin No.	Name	Pin Type	Buffer Type	Function
1	VOS	I	Analog	Connect to output of the converter. It serves as the VOUT voltage sense input for inductor current emulation during body braking. Kelvin connection in layout is not required.
6, 41	GATEL	I/O	Analog	Low-side MOSFET driver pin that can be connected to a test point in order to observe the waveform.
10-19	SW	O	Analog	High Current switching node connection of the synchronous buck converter.
32	PHASE	I	Analog	Internal connection to the high-side MOSFET source. For Bootstrap capacitor connection only.
33	BOOT	I	Analog	Bootstrap capacitor connection. The bootstrap capacitor provides the charge to turn on the high-side MOSFET. Connect a minimum 0.22-µF, X7R ceramic capacitor from BOOT to PHASE pin. For applications with input voltage higher than 13.2 V, use a 2-Ω bootstrap resistor in series with bootstrap capacitor to reduce SW node voltage spike and improve switching noise immunity.
34	PWM	I/O	Logic	3.3-V logic level PWM input. PWM input: “High” turns high-side MOSFET on; floating or driving PWM to the “Tri-state” turns both MOSFETs off; “Low” turns low-side MOSFET on.
35	EN	I	Logic	Pulling EN high enables the driver; pulling EN low disables the driver and enters ultra-low quiescent current mode. Floating this pin is not recommended, however a low current pull-down is embedded to keep the driver off if the pin is floating. The EN pin is VCC tolerant.
36	TOUT/FLT	O	Analog	The voltage at this pin is defined by the equation 8 mV * (Celsius Temperature) + 0.6 V. This pin will be pulled up to 3.3 V under severe over-temperature, over-current, bootstrap capacitor under-voltage, or phase fault condition.
37	OCSET	I/O	Analog	Program the over-current threshold by placing a resistor from OCSET pin to LGND. Floating OCSET or directly tying to VCC gives a fixed 120-A peak over-current threshold.
38	IOUT	O	Analog	Sensed current output signal referenced to the REFIN pin. V(IOUT – REFIN) voltage represents current information at 5 mV/A.
39	REFIN	I/O	Analog	The reference supply voltage for the IOUT information. This pin should be tied to a fixed voltage between 1.1 V and 2.0 V. The bias rails from typical PWM controllers are normally utilized with no additional decoupling needed at the power stage.

Block Diagram

Table 3 Power Supply

Pin No.	Name	Pin Type	Buffer Type	Function
4	VDRV	POWER	–	The gate driver supply. Connect a X7R, 1-µF ceramic capacitor between VDRV and PGND. VDRV should be connected to the +5 V power supply.
3	VCC	POWER	–	Bias voltage for control logic. Connect a X7R, 1-µF ceramic capacitor between VCC and LGND, and a 1-Ω resistor between VCC and VDRV.
25-30	VIN	POWER	–	4.25-V to 16-V high current input voltage connection. Place a 0402, X7R, 0.1-µF capacitor and a 0402 or 0603, X7R, 1-µF capacitor close to VIN pin and PGND pin. Also connect at least one X7R, 10-µF ceramic capacitor.

Table 4 Ground Pins

Pin No.	Name	Pin Type	Buffer Type	Function
2	LGND	GND	–	Signal ground. All signals are referenced to this pin.
5, 7-9, 20-24, 40	PGND	GND	–	Power ground. It is also the power ground of the low-side MOSFET.

Table 5 Not Connected

Pin No.	Name	Pin Type	Buffer Type	Function
31	NC	–	–	Leave this pin unconnected.

5 Electrical Specification

5.1 Absolute Maximum Ratings

Note: T_A = 25 °C

Stresses above those listed in Table 6 “Absolute Maximum Ratings” may cause permanent damage to the device. These are absolute stress ratings only and operation of the device is not implied or recommended at these or any other conditions in excess of those given in the operational sections of this specification. Exposure over values of the recommended ratings for extended periods may adversely affect the operation and reliability of the device.

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency of PWM input	f_{SW}	0.2	–	1.5	MHz	
Maximum peak load current	I_{OUT_PEAK}	–	–	90	A	
Maximum average load current	I_{OUT}	–	–	70	A	
Input Voltage	V_{IN}	-0.30	–	25	V	Pin VIN
Logic supply voltage	V_{CC}	-0.30	–	6	V	Pin VCC
High and low-side driver voltage	V_{DRV}	-0.30	–	6	V	Pin VDRV
Switch node voltage	V_{SW}	Below -5 V for 5 ns, -0.3 V DC	–	34 V for 1 ns, 25 V DC	V	Pin SW
PHASE voltage	V_{PHASE}	Below -5 V for 5 ns, -0.3 V DC	–	34 V for 1 ns, 25 V DC	V	Pin PHASE
VIN – PHASE voltage	V_{VIN} - V_{PHASE}	Below -5 V for 5 ns, -0.3 V DC		34 V for 1 ns, 25 V DC	V	VIN – PHASE
BOOT voltage	V_{BOOT}	Below -0.3 V for 5 ns, -0.3 V DC	–	29	V	Pin BOOT
	$V_{BOOT-PHASE}$	-0.3	–	7 V for 5 ns, 6 V DC	V	BOOT – PHASE
EN voltage	V_{EN}	-0.3	–	VCC + 0.3	V	Pin EN
PWM voltage	V_{PWM}	-0.3	–	VCC + 0.3	V	Pin PWM
TOUT	V_{TOUT}	-0.3	–	VCC + 0.3	V	Pin TOUT/FLT
IOUT	V_{IOUT}	-0.3	–	VCC + 0.3	V	Pin IOUT
VOS	V_{OS}	-0.3	–	VCC + 0.3	V	Pin VOS
OCSET	V_{OCSET}	-0.3	–	VCC + 0.3	V	Pin OCSET
REFIN	V_{REFIN}	-0.3	–	3.5	V	Pin REFIN
Junction temperature	T_{Jmax}	-40	–	150	°C	–
Storage temperature	T_{STG}	-65	–	150	°C	–

- All rated voltages are relative to voltages on the LGND and PGND pins unless otherwise specified.

5.2 Thermal Characteristics

Table 7 Thermal Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal Resistance-Junction to PCB	θ_{JC_PCB}	–	1.5	–	K/W	Referenced to Pin 24
Thermal Resistance-Junction to top of package	θ_{JC_Top}	–	16.7	–		–
Thermal Resistance to Ambient	θ_{JA} Note	–	20.5	–		–

Note: Thermal Resistance (θ_{JA}) is measured with the component mounted on a highly effective thermal conductivity test board in free air.

5.3 Recommended Operating Conditions

Table 8 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Voltage	V_{IN}	4.25	–	16	V	
MOSFET Driver Voltage	V_{DRV}	4.25	–	5.5		
Logic Supply Voltage	V_{CC}	4.25	–	5.5		
PWM Switching Frequency	f_{SW}	200	–	1500	kHz	
Reference Voltage	V_{REFIN}	1.1	–	2.0	V	Additional fixed current sense amplifier offset of –0.35 A at VREFIN = 1.8 V
Junction Temperature	$T_{JUNCTION}$	-40	–	+125	°C	

5.4 Electrical Characteristics

Note: $V_{DRV} = V_{CC} = 5$ V, $T_J = 65$ °C, $V_{REFIN} = 1.2$ V, $f_{SW} = 600$ kHz, $V_{OUT} = 1.8$ V

Table 9 Voltage Supply, Biasing Current

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
UVLO VCC/VDRV Rising	$V_{UVLO\_VCC\_RISE}$	-	3.85	4.0	V	
UVLO VCC/VDRV Falling	$V_{UVLO\_VCC\_FALL}$	3.3	3.45	-		
Hysteresis	V_{HYST}		0.4			
Driver Current	I_{VDRV}	–	20	–	mA	EN = 3.3 V, f_{SW} = 600 kHz, D=15%
		–	15	–	µA	EN = 3.3 V , PWM floating
		–	0.2	–	µA	EN = 0 V
Supply Current	I_{VCC}	-	3.2	–	mA	EN = 3.3 V
		-	45	–	µA	EN = 0 V
VIN Bias Current	I_{VIN}	-	35	–	µA	VIN = 15 V, EN = 3.3 V, V(PWM) = 1.7 V
		-	0.1	–	µA	EN = 0 V

Table 10 Current Sense and Temperature Sense

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
IOUT	Current Sense Gain	A_{CS}	4.8	5	5.2	mV/A	
	Offset at Trim	A_{CS_OST}	-0.8	-	0.8	A	0-A load

Table 11 Temperature Sense and Fault Communication

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TOUT	Temperature Sense Slope	A_{TOUT_GAIN}	7.8	8.0	8.2	mV/°C	0 °C ≤ T_J ≤ 125 °C, Note 1
	Temperature Sense Offset Voltage	V_{TOUT_OFFSET}	1.108	1.120	1.132	V	T_J = 65 °C, 0.6 V + 8 mV/°C * T_J

Table 12 Other Logic Functions, Inputs/Outputs And Thresholds

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
EN	Enable Power-on Delay	$t_{EN\_DELAY\_ON}$	-	5	–	µs	PWM = 0. Measured from EN rising edge to GATEL > 1 V.
	Enable Power-off Delay	$t_{EN\_DELAY\_OFF}$	-	50	–	ns	PWM = 0. Measured from EN falling edge to GATEL < 4 V.
	Internal Pull-down Resistance	R_{EN_PULLDN}	-	450	–	kΩ	EN floating
	Input High Voltage	V_{EN_HIGH}	2	-	-	V	
		V_{EN_LOW}	-	-	0.8		
PWM	PWM Input High Threshold	V_{IH}	2.4	-	-	V	PWM Low or Tri-state to High
	PWM Input Low Threshold	V_{IL}	-	-	0.8	V	PWM High or Tri-state to Low
	PWM Hysteresis	I_{PWM_HYS}	-	160	-	mV	Active to Tri-state or Tri-state to Active

Table 13 Protection

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
OTP	Over-Temperature Rising Threshold	T_{OTP_RISE}	-	140	-	°C	TOUT/FLT pulled high, Note 1
	Over-Temperature Falling Threshold	T_{OTP_FALL}	-	120	-	°C	TOUT/FLT released, Note 1
PHASE FAULT	High-side MOSFET Short Threshold	V_{PHSFLT_TH}	–	850	–	mV	V(SW) – V(PGND)
	TOUT/FLT Delay	N_{FLT_DELAY}	-	7	-	Cycle	PWM High-Low Cycles to TOUT/FLT high
OCP	Programmable Peak Over-Current Threshold Range	I_{OCP}	20	-	-	A	Program through R_{OCSET}
	Constant Peak Over-Current Threshold	I_{OCP_PEAK}	-	120	-	A	OCSET open or connected to VCC
	TOUT/FLT Delay	t_{FLT_DELY}	10	-	-	Cycle	PWM High-Low Cycles to TOUT/FLT high

Notes

1. Guaranteed by design but not tested in production.

6 Typical Operating Characteristics

Single Phase Circuit of Figure 18, V_{IN} = 12 V, V_{OUT} = 1.8V, f_{SW} = 600kHz, L = 150nH, VCC = VDRV = 5 V, $T_{AMBIENT}$ = 25°C, no heat sink, no air flow, 8-layer PCB board of 3.7"(L) x 2.6"(W), no PWM controller loss, no inductor loss, unless specified otherwise.

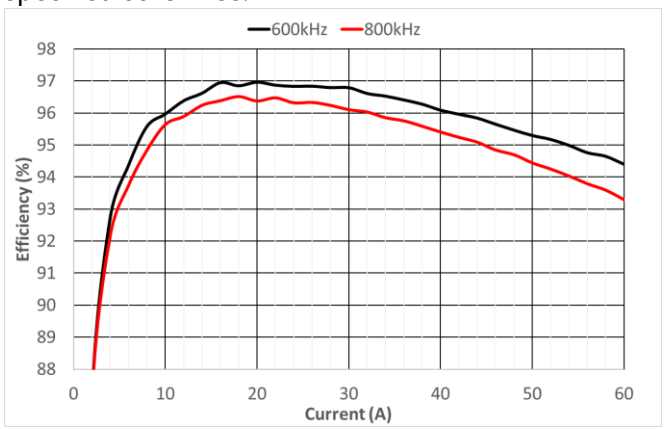

Figure 4 Power Stage Efficiency

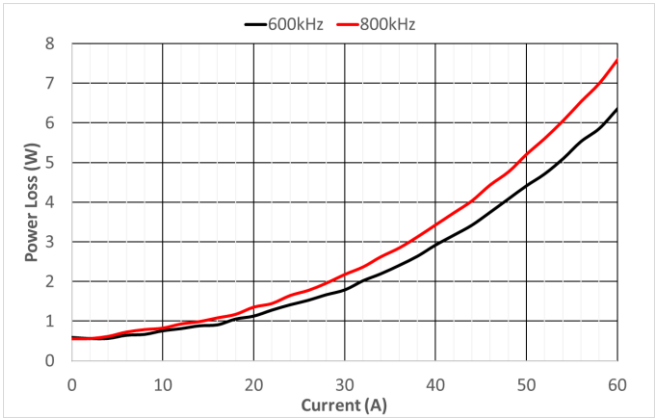

Figure 5 Power Stage Loss

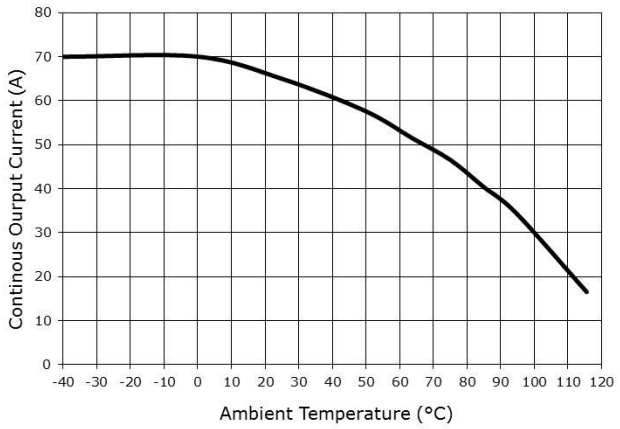

Figure 6 Thermal Derating, Tcase <= 125 °C

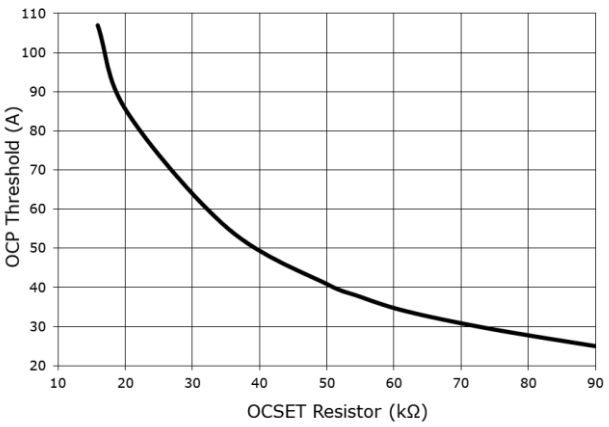

Figure 7 Programmable OCP Threshold

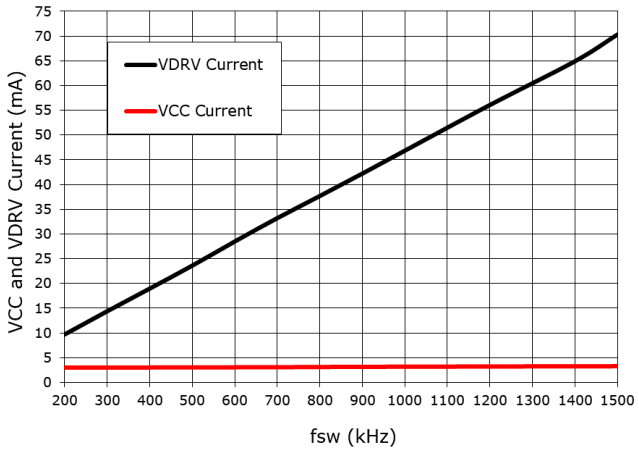

Figure 8 Vcc and Vdrv Current

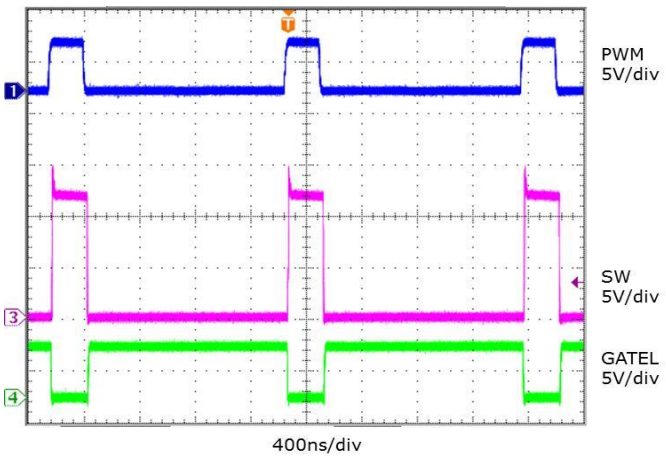

Figure 9 Switching Waveform at 0A

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