EiceDRIVER™

2EDN7424

Fast Dual Channel 4 A Low-Side Gate Driver

Fast, precise, strong and compatible

- Highly efficient SMPS enabled by 6 ns fast slew rates and 19 ns propagation delay precision for fast MOSFET and GaN switching
- 1 ns channel-to-channel propagation delay accuracy enables safe use of two channels in parallel
- Two independent 4 A channels enable numerous deployment options
- Industry standard packages and pinout enable ease system-design upgrades
- Qualified for industrial grade applications according to JEDEC (JESD47, J-STD20 and JESD22)

The new Reference in Ruggedness

- 4.2 V and 8 V UVLO (Under Voltage Lock Out) options ensure instant MOSFET protection under abnormal conditions
- -10 V control and enable input robustness delivers crucial safety margin when driving pulse-transformers or driving MOSFETs in through hole packaging
- 5 A reverse current robustness eliminates the need for output protection circuitry.

Typical Applications

- Server SMPS
- TeleCom SMPS
- DC-to-DC Converter
- Bricks
- Power Tools
- Industrial SMPS
- Motor Control
- Solar SMPS

Example Topologies

- Single and interleaved PFC
- LLC, ZVS with pulse transformer
- Synchronous Rectification

Description

The 2EDN7424 is an advanced dual-channel driver. It is suited to drive logic and normal level MOSFETs and supports OptiMOS™, CoolMOS™, Standard Level MOSFETs, Superjunction MOSFETs, as well as IGBTs and GaN Power devices.

The control and enable inputs are LV-TTL compatible (CMOS 3.3 V) with an input voltage range up to +22V.

4.2 V (Under Voltage Lock Out) options ensure instant MOSFET and GaN protection under abnormal conditions. Under such circumstances, this UVLO mechanism provides crucial independence from whether and when other supervisors circuitries detect abnormal conditions.

Each of the two outputs is able to sink and source 4 A currents utilizing a true rail-to-rail stage. This ensures very low on resistance of 0.84 Ω up to the positive and 0.66 Ω down to the negative rail respectively. Very tight channel to channel delay matching, typ. 2 ns, permits parallel use of two channels, leading to a source and sink capability of 8 A. Industry leading reverse current robustness eliminates the need for Schottky diodes at the outputs and reduces the bill-of-material.

The pinout of the 2EDN family is compatible with the industry standard. Two package variants, DSO 8-pin and TSSOP 8-pin, allow optimization of PCB board space usage and thermal characteristics.

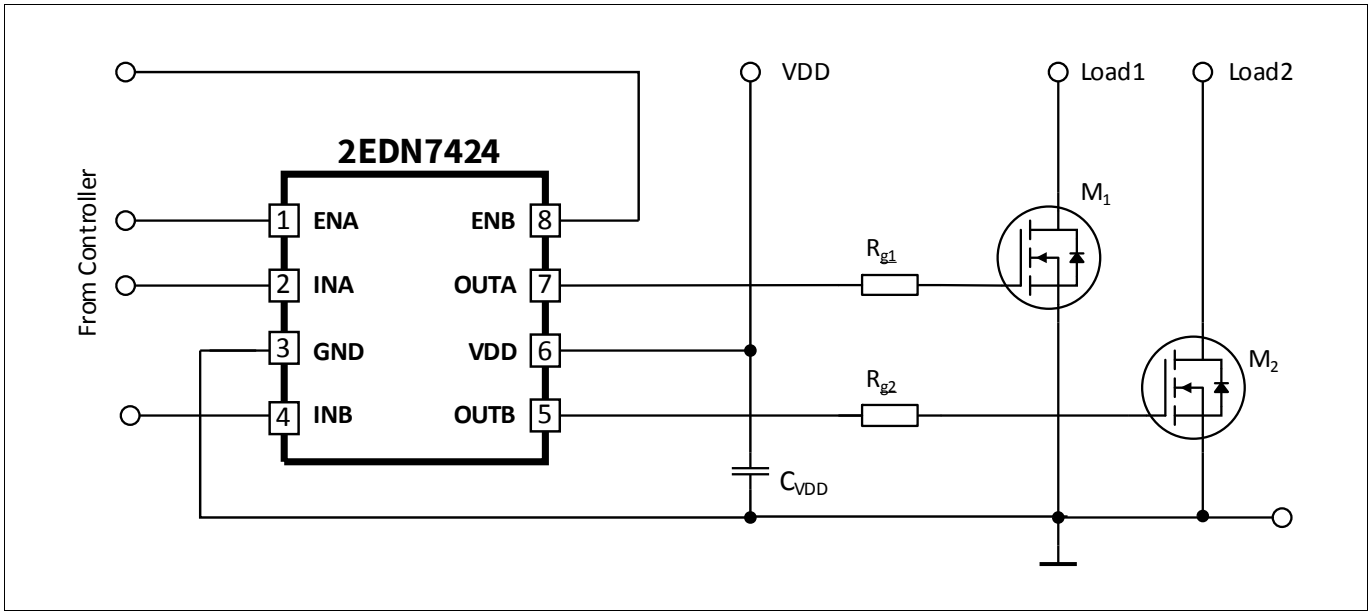
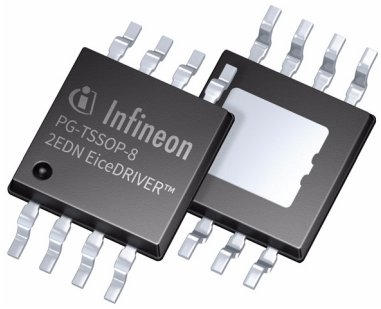


Table of Contents

1 Product Versions

The 2EDN7424 are available in 2 package versions.

Table 1 Product Versions

Package	Type. UVLO	Control Input	Part Number	IC Topside Marking Code
PG-DSO-8-60				
	4.2V	direct	2EDN7424F	2N7424AF EiceDRIV XXHYYWW
PG-TSSOP-8-1				
	4.2V	direct	2EDN7424R	2N7424 AR_XXX HYYWW

1.1 Undervoltage Lockout

The Undervoltage Lockout enables robust start-up and shutdown behavior.

Please refer to the functional description section for more details in **Chapter 4** (**Undervoltage Lockout (UVLO)**).

1.2 Logic Version

The logic relations between inputs, enable pins and outputs are given in **Table 2**. The state of the driving output is defined by the state of the respective input, if the enable inputs ENA and ENB are high (or left open). A logic “low” at an enable input or an undervoltage lockout event, due to low voltage at V_{DD}, causes the respective output to be low too, regardless of the input signal.

Functional description is shown in **Chapter 3** (**Block Diagram**) and **Chapter 4** (**Input Configuration**).

Table 2 Logic Table

Inputs					Output	
ENA	**ENB**	**INA**	**INB**	**UVLO[1)]**	**OUTA**	**OUTB**
x	x	x	x	active	L	L
L	L	x	x	inactive	L	L
H	L	L	x	inactive	L	L
H	L	H	x	inactive	H	L
L	H	x	L	inactive	L	L
L	H	x	H	inactive	L	H
H	H	L	L	inactive	L	L
H	H	H	L	inactive	H	L
H	H	L	H	inactive	L	H
H	H	H	H	inactive	H	H

1) Inactive means that VDD is above UVLO threshold voltage and release logic to control output stage.
Active means that UVLO disable active the output stages.

1.3 Package Versions

The logic and UVLO versions are available in2 different packages.

- a standard PG-DSO-8-60 (designated by “F”)
- a small PG-TSSOP-8-1 (designated by “R”)

Drawings can be viewed in **Chapter 8** (**Outline Dimensions**).

2 Pin Configuration and Description

The pin configuration for 2EDN7424F in the PG-DSO-8-60 package is shown in **Figure 1**. Drawings can be viewed in **Chapter 8** (**PG-DSO-8-60**).

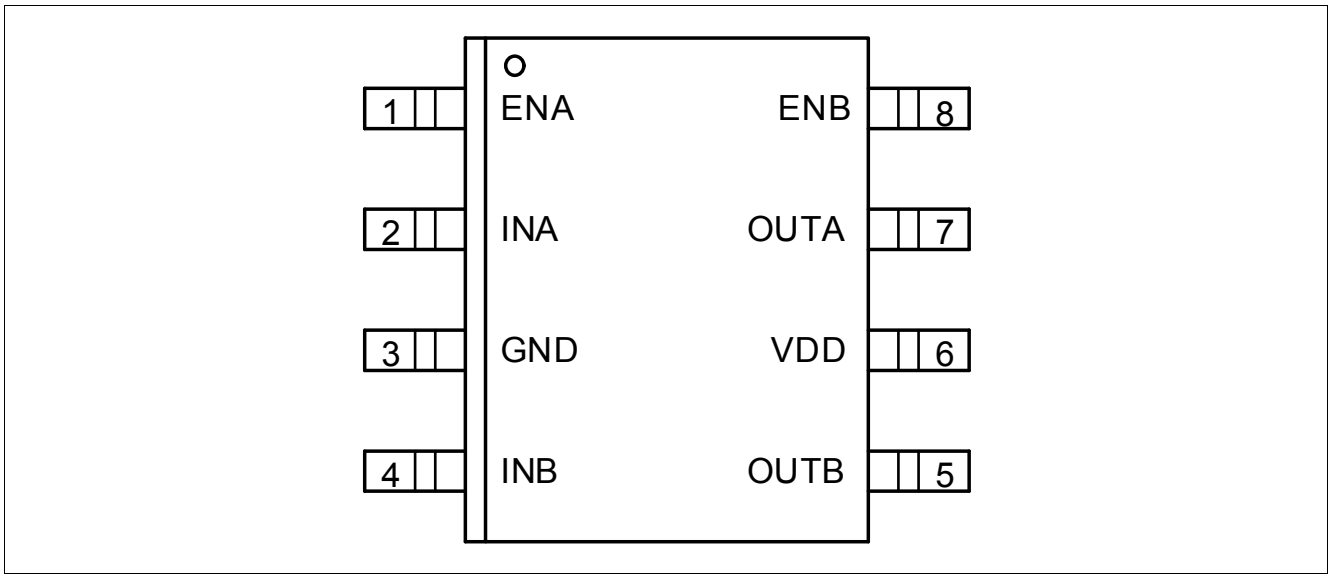


Figure 1 Pin Configuration PG-DSO-8-60, Top View

Table 3 Pin Configuration 2EDN7424F in the PG-DSO-8-60 Package

Pin	Symbol	Description
1	ENA	Enable input channel A Logic input; if ENA is high or left open, OUTA is controlled by INA; ENA low causes OUTA low
2	INA	Input signal channel A Logic input, controlling OUTA
3	GND	Ground
4	INB	Input signal channel B Logic input, controlling OUTB
5	OUTB	Driver output channel B Low-impedance output with source and sink capability
6	VDD	Positive supply voltage Operating range 4.5 V to 20 V
7	OUTA	Driver output channel A Low-impedance output with source and sink capability
8	ENB	Enable input channel B Logic Input; if ENB is high or left open, OUTB is controlled by INB; ENB low causes OUTB low

Pin Configuration and Description

The pin configuration for 2EDN7424R in the PG-TSSOP-8-1 package is shown in **Figure 2**. Drawings can be viewed in **Chapter 8** (**PG-TSSOP-8-1**).

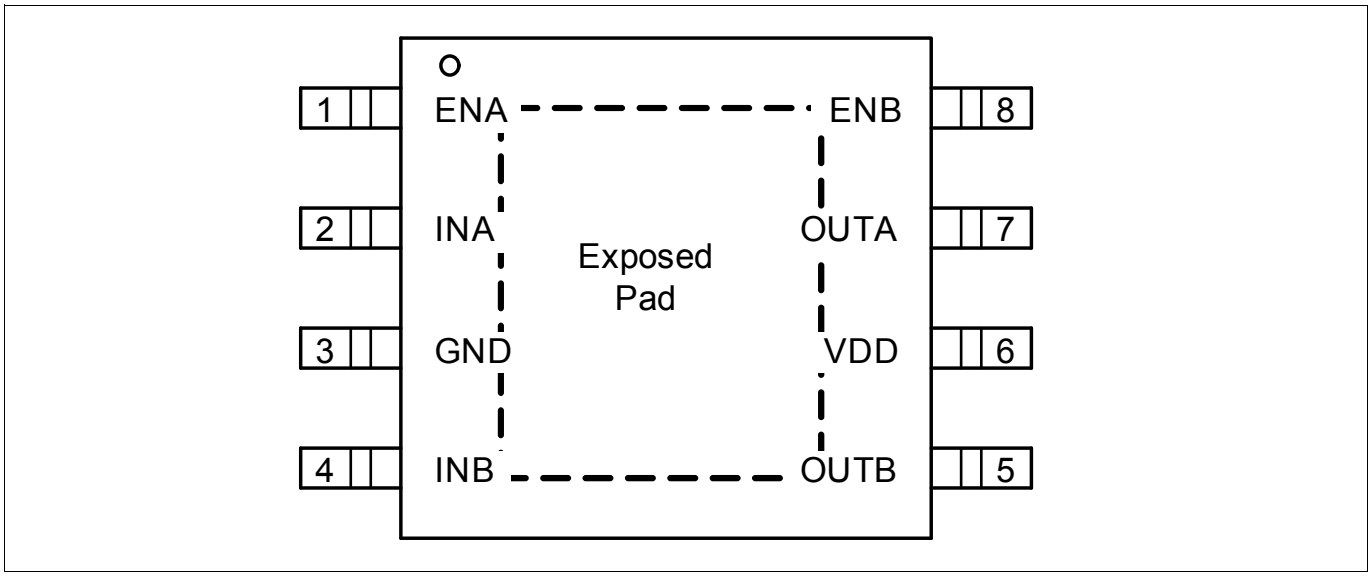


Figure 2 Pin Configuration PG-TSSOP-8-1, Top View

Table 4 Pin Configuration 2EDN7424R in the PG-TSSOP-8-1 Package

Pin	Symbol	Description
1	ENA	Enable input channel A Logic input; if ENA is high or left open, OUTA is controlled by INA; ENA low causes OUTA low
2	INA	Input signal channel A Logic input, controlling OUTA
3	GND	Ground[1)]
4	INB	Input signal channel B Logic input, controlling OUTB
5	OUTB	Driver output channel B Low-impedance output with source and sink capability
6	VDD	Positive supply voltage Operating range 4.5 V to 20 V
7	OUTA	Driver output channel A Low-impedance output with source and sink capability
8	ENB	Enable input channel B Logic Input; if ENB is high or left open, OUTB is controlled by INB; ENB low causes OUTB low

1) Exposed Pad sink of PG-TSSOP-8-1 packages has to be connected to GND pin.

3 Block Diagram

A simplified functional block diagram is given in **Figure 3**. Please refer to the functional description section for more details in **Chapter 4**.

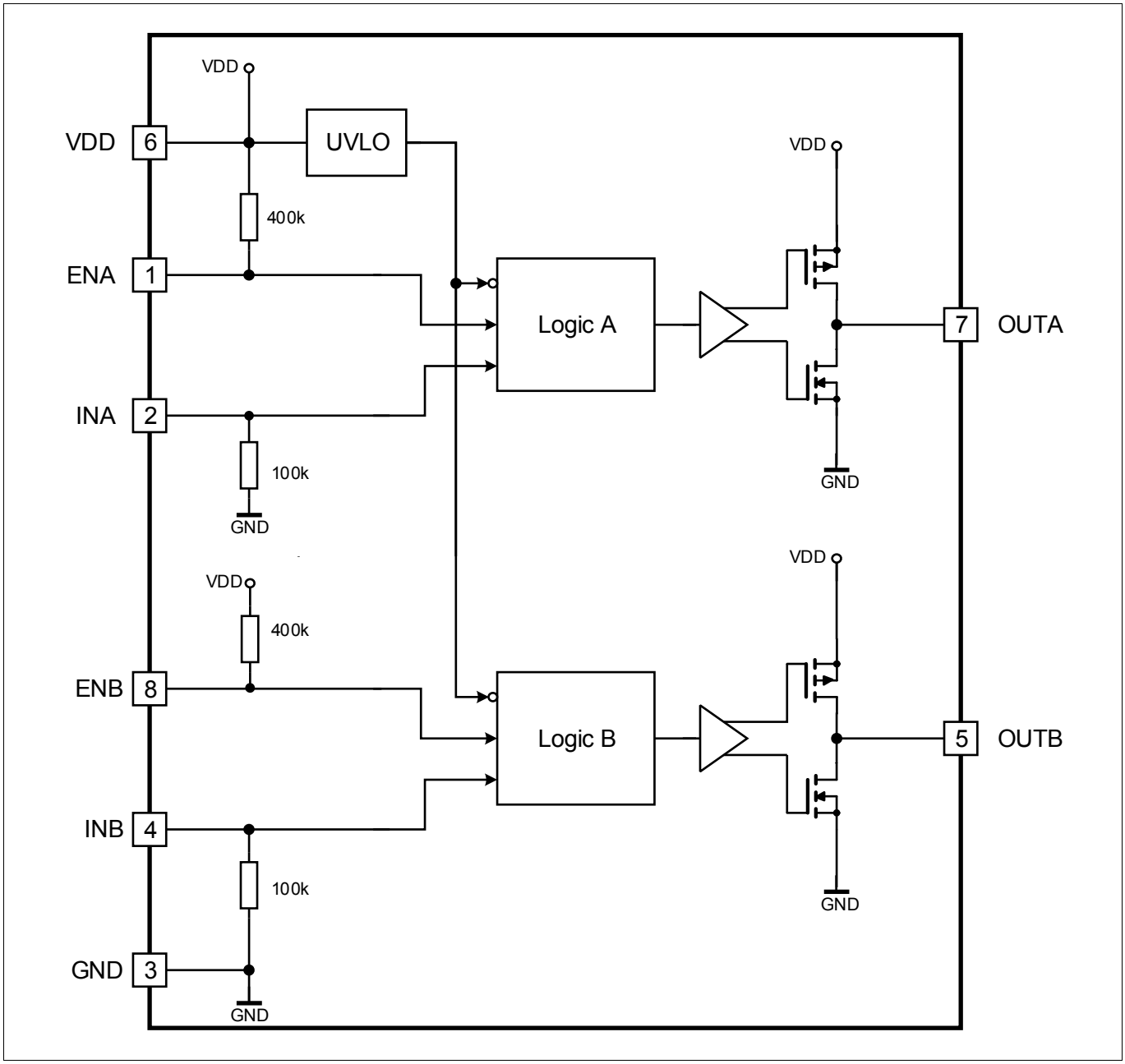


Figure 3 Block Diagram,pull-up/pull-down resistor configuration

4 Functional Description

4.1 Introduction

The 2EDN7424 is a fast dual-channel driver for low-side switches. Two true rail-to-rail output stages with very low output impedance and high current capability are chosen to ensure highest flexibility and cover a high variety of applications.

All inputs are compatible with LV-TTL signal levels. The threshold voltages with a typical hysteresis of 1.1 V are kept constant over the supply voltage range.

Since the 2EDN7424 aims particularly at fast-switching applications, signal delays and rise/fall times have been minimized. Special effort has been made towards minimizing delay differences between the 2 channels to very low values of typically 2 ns.

4.2 Supply Voltage

The maximum supply voltage is 20 V. This high voltage can be valuable in order to exploit the full current capability of 2EDN7424 when driving very large MOSFETs. The minimum operating supply voltage is set by the undervoltage lockout function to a typical default value of 4.2 V. This lockout function protects power MOSFETs from running into linear mode with subsequent high power dissipation.

4.3 Input Configuration

As described in **Chapter 1**, 2EDN7424 is available with respect to the logic configuration of the 4 input pins (input plus enable).

The enable inputs are internally pulled up to a logic high voltage, i.e. the driver is enabled with these pins left open. The direct PWM inputs are internally pulled down to a logic low voltage. This prevents a switch-on event during power up and a not driven input condition. Version with inverted PWM input have an internal pull up resistor to prevent unwanted switch-on.

All inputs are compatible with LV-TTL levels and provide a hysteresis of 1.1 V typ. This hysteresis is independent of the supply voltage.

All input pins have a negative extended voltage range. This prevents cross current over single wires during GND shifts between signal source (controller) and driver input.

4.4 Driver Outputs

The two rail-to-rail output stages realized with complementary MOS transistors are able to provide a typical 4 A of sourcing and sinking current. This driver output stage has a shoot through protection and current limiting behavior. After a switching event, current limitation is raised up to achieve the typical current peak for an excellent fast reaction time of the following power MOS transistor.

The output impedance is very low with a typical value below 0.84 Ω for the sourcing p-channel MOS and 0.66 Ω for the sinking n-channel MOS transistor. The use of a p-channel sourcing transistor is crucial for achieving true rail-to-rail behaviour and avoiding a source follower's voltage drop.

Gate Drive Outputs held active low in case of floating inputs ENx, INx or during startup or power down once UVLO is not exceeded. Under any situation, startup, UVLO or shutdown, outputs are held under defined conditions.

4.5 Undervoltage Lockout (UVLO)

The Undervoltage Lockout function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO threshold voltage. Thus it can be guaranteed, that the switch transistor is not switched on if the driving voltage is too low to completely switch it on, thereby avoiding excessive power dissipation.

The UVLO level is set to a typical value of 4.2 V (with hysteresis).

5 Characteristics

The absolute maximum ratings are listed in **Table 5**. Stresses beyond these values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.1 Absolute Maximum Ratings

Table 5 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Positive supply voltage	V_{VDD}	-0.3		22	V	
Voltage at pins INA, INB, ENA, ENB	V_{IN}	-10		22	V	
Voltage at pins OUTA, OUTB	V_{OUT}	-0.3		V_{VDD}+0.3	V	Note [1]
Reverse current peak at pins OUTA and OUTB	I_{SRCREV}			5	A_{pk}	< 500ns
	I_{SNKREV}			-5	A_{pk}	
Junction temperature	T_J	-40		150	°C	
Storage temperature	T_S	-55		150	°C	
ESD capability	V_{ESD}			1.5	kV	Charged Device Mode (CDM) [2]
ESD capability	V_{ESD}			2.5	kV	Human Body Model (HBM) [3]

1) Voltage spikes resulting from reverse current peaks are allowed.
2) According to JESD22-C101
3) According to JESD22-A114

5.2 Thermal Characteristics

Table 6 Thermal Characteristics for PG-DSO-8-60 (T_{amb}=25°C)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction-ambient [1]	RthJA25		125		K/W	
Thermal resistance junction-case (top) [2]	RthJC25		66		K/W	
Thermal resistance junction-board [3]	RthJB25		62		K/W	
Characterization parameter junction-top [4]	ΨthJC25		16		K/W	
Characterization parameter junction-board [5]	ΨthJB25		55		K/W	

1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
4) The characterization parameter junction-top, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining Rth, using a procedure described in JESD51-2a (sections 6 and 7).
5) The characterization parameter junction-board, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining Rth, using a procedure described in JESD51-2a (sections 6 and 7).

Table 7 Thermal Characteristics for PG-TSSOP-8-1 (T_{amb}=25°C)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction-ambient [1]	RthJA25		64		K/W	
Thermal resistance junction-case (top) [2]	RthJP25		56		K/W	
Thermal resistance junction-board [3]	RthJB25		55		K/W	
Characterization parameter junction-top [4]	ΨthJC25		9		K/W	
Characterization parameter junction-board [5]	ΨthJB25		13		K/W	

1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
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5) The characterization parameter junction-board, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining Rth, using a procedure described in JESD51-2a (sections 6 and 7).

5.3 Operating Range

Table 8 Operating Range

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{VDD}	4.5		20	V	Min. defined by UVLO
Logic input voltage	V_{IN}	-5		20	V	
Junction temperature	T_J	-40		150	°C	[1]

1) Continuous operation above 125 °C may reduce life time.

5.4 Electrical Characteristics

Unless otherwise noted, min./max. values of characteristics are the lower and upper limits respectively. They are valid within the full operating range. The supply voltage is V_{VDD}= 12 V. Typical values are given at T_J=25°C.

Table 9 Power Supply

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VDD quiescent current	I_{VDDQU1}	0.5	0.7	1.2	mA	OUT = high, V_{VDD}= 12 V
VDD quiescent current	I_{VDDQU2}	0.3	0.48	0.7	mA	OUT = low, V_{VDD}= 12 V

Table 10 Undervoltage Lockout

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold	$UVLO_{ON}$	3.9	4.2	4.5	V	
Undervoltage Lockout (UVLO) turn off threshold	$UVLO_{OFF}$	3.6	3.9	4.2	V	
UVLO threshold hysteresis	$UVLO_{HYS}$		0.3		V	

Table 11 Logic Inputs INA, INB, ENA, ENB

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage threshold for transition LH	V_{INH}	1.9	2.1	2.3	V	
Input voltage threshold for transition HL	V_{INL}	0.8	1.0	1.2	V	
Input pull up resistor[1)]	R_{INH}		400		kΩ	
Input pull down resistor[2)]	R_{INL}		100		kΩ	

1) Inputs with initial high logic level
2) Inputs with initial low logic level

Table 12 Static Output Caracteristics (see Figure 4)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High Level (Sourcing) Output Resistance	R_{ONSRC}	0.35	0.84	1.2	Ω	I_{SRC} = 50mA
High Level (Sourcing) Output Current	$I_{SRCPEAK}$		4.0	[1)]	A	
Low Level (Sinking) Output Resistance	R_{ONSNK}	0.28	0.66	1.0	Ω	I_{SNK} = 50mA
Low Level (Sinking) Output Current	$I_{SNKPEAK}$		-4.0	[2)]	A	

1) Active limited by design at approx. 6.5Apk, parameter is not subject to production test - verified by design / characterization, max. power dissipation must be observed
2) Active limited by design at approx. -6.5Apk, parameter is not subject to production test - verified by design / characterization, max. power dissipation must be observed

Table 13 Dynamic Characteristics (see Figure 4, Figure 5 and Figure 6)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input/Enable to output propagation delay	T_{PDlh}	15	19	25	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V; low to high transition at Input/Enable
Input/Enable to output propagation delay	T_{PDhl}	15	19	25	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V high to low transition at Input/Enable
Input/Enable to output propagation delay mismatch between the two channels on the same IC	delta t_{PD}			2	ns	
Rise Time	T_{RISE}	—	6.4	10 [1)]	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V
Fall Time	T_{FAll}	—	5.4	10 [1)]	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V
Minimum input pulse width that changes output state	T_{PW}	—	10	20 [1)]	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V

1) Parameter verified by design, not 100% tested in production.

6 Timing Diagrams

Figure 4 shows the definition of rise, fall and delay times for the inputs of the non-inverting / direct version (with Enable pin high or open).

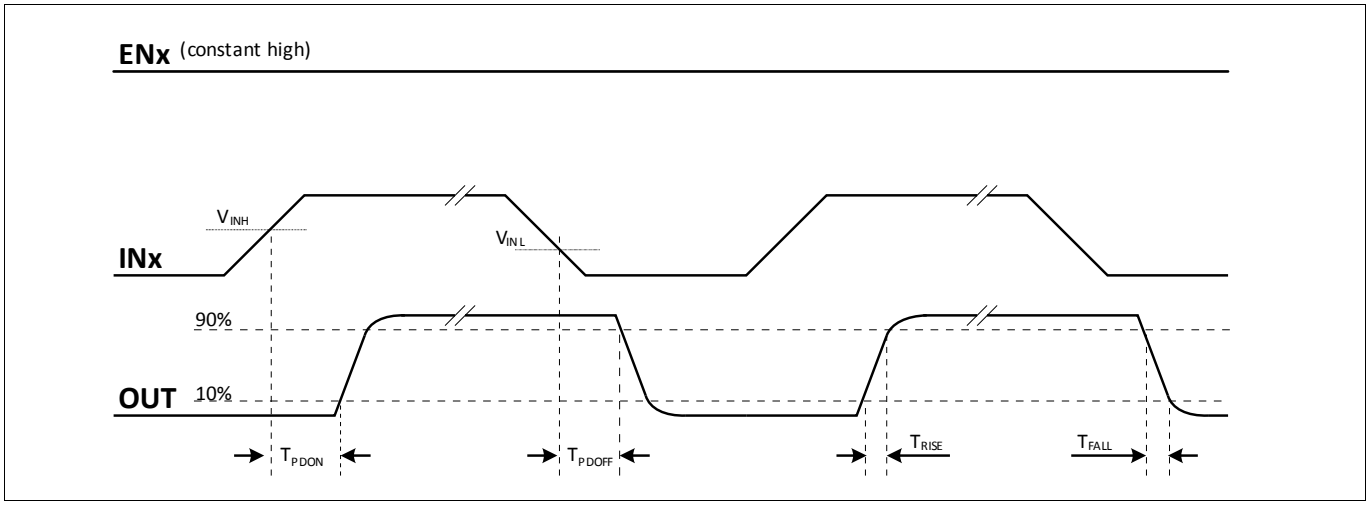

Figure 4 Propagation delay, rise and fall time, non-inverted

Figure 5 illustrates the undervoltage lockout function.

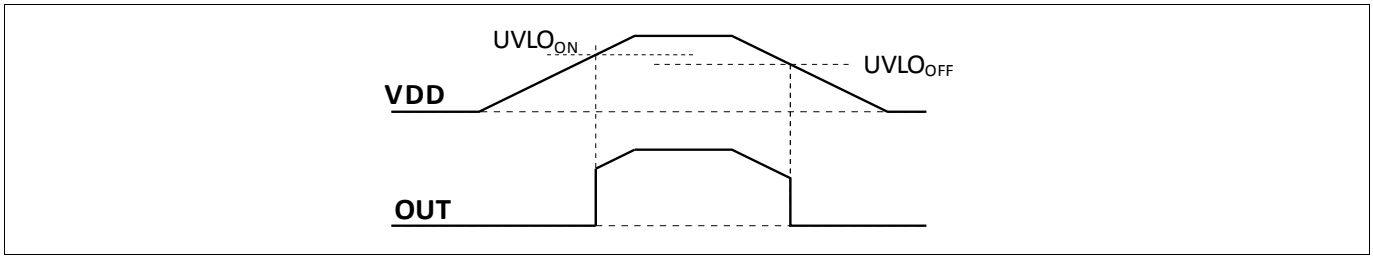

Figure 5 UVLO behaviour, input ENx and INx drives OUTx normally high

Figure 6 illustrates the minimum input pulse width that changes output state.

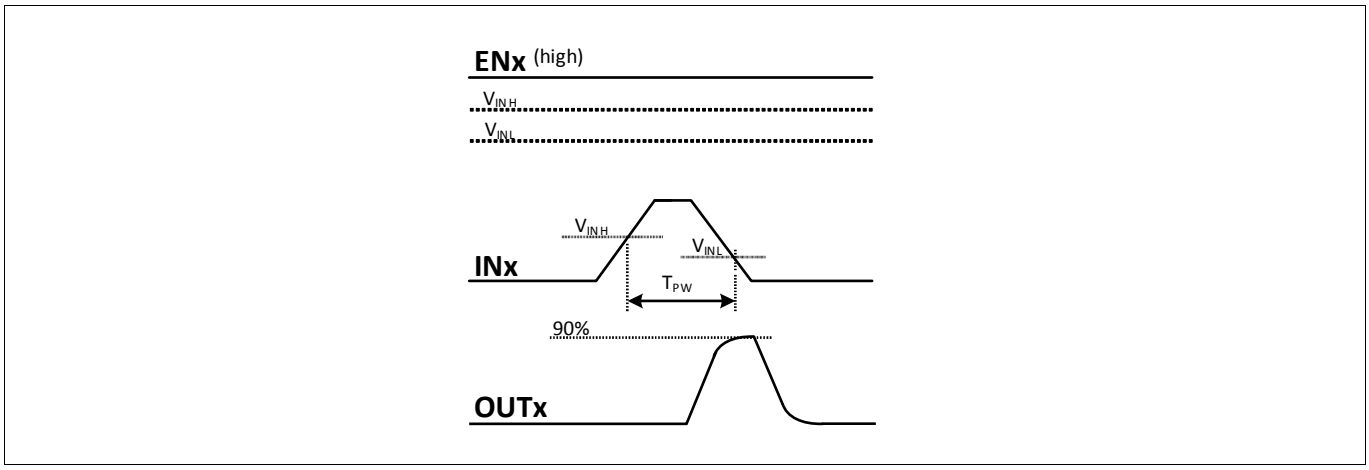

Figure 6 TPW, minimum input pulse width that changes output state

7 Typical Characteristics

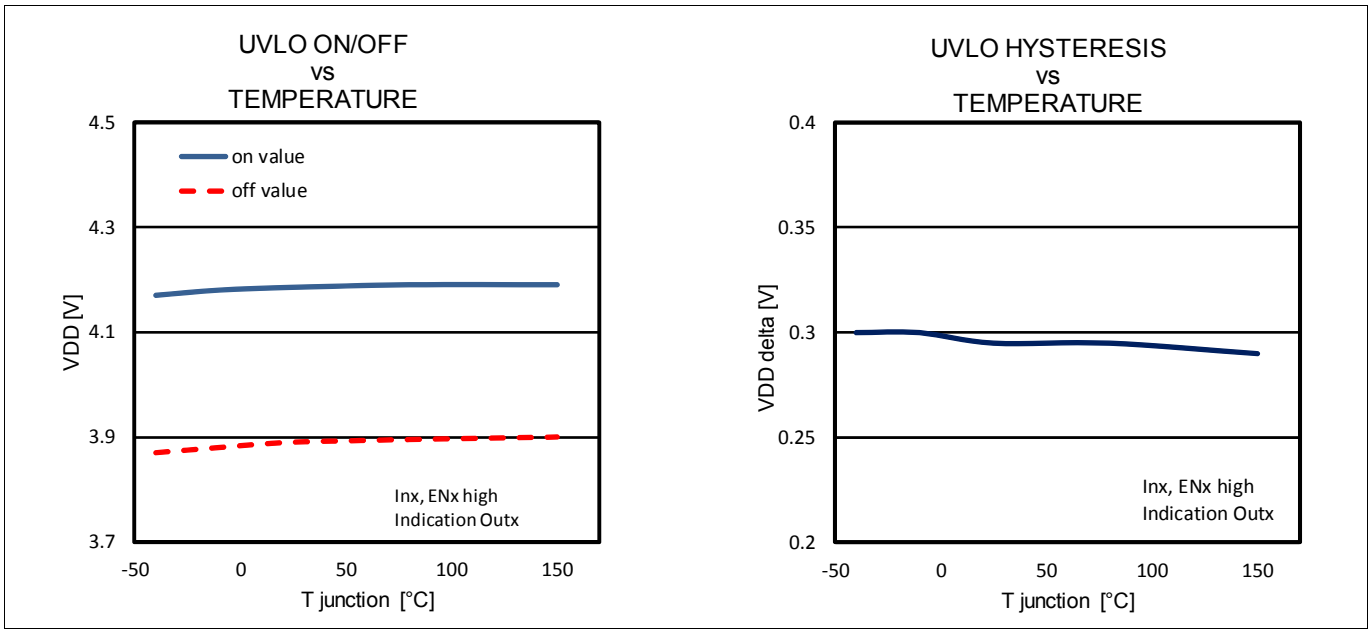

Figure 7 Undervoltage lockout (4.2V)

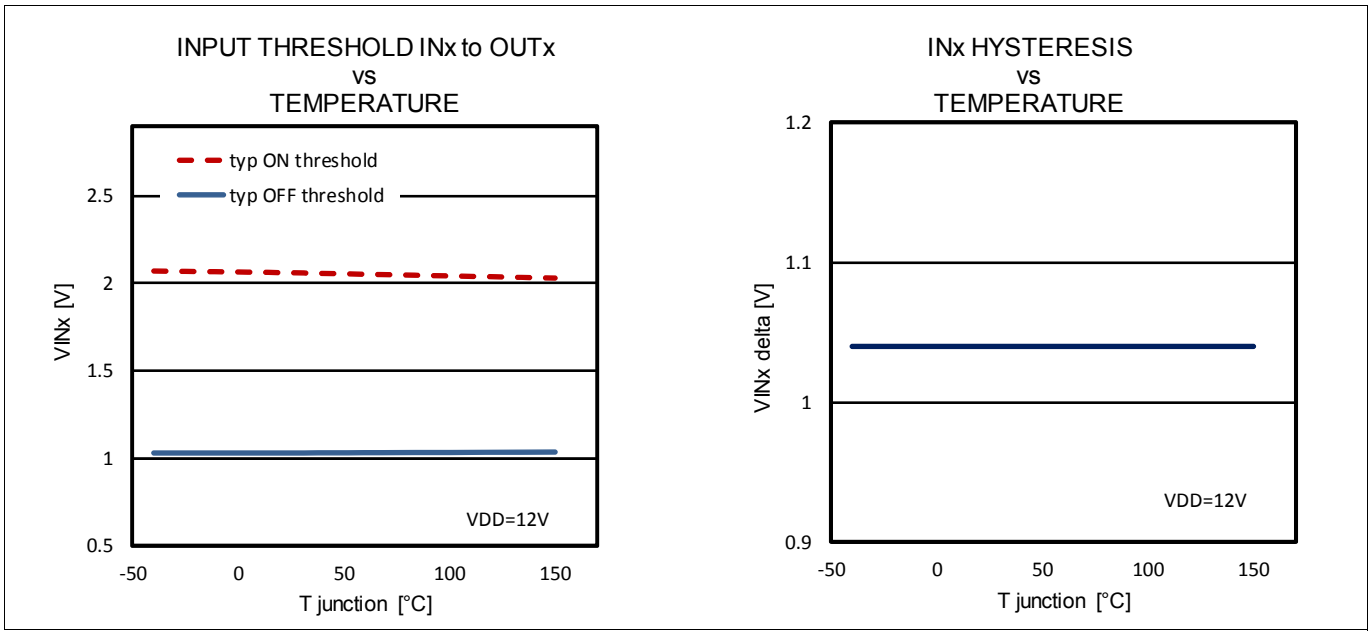

Figure 8 Input (INx) characteristic

Typical Characteristics

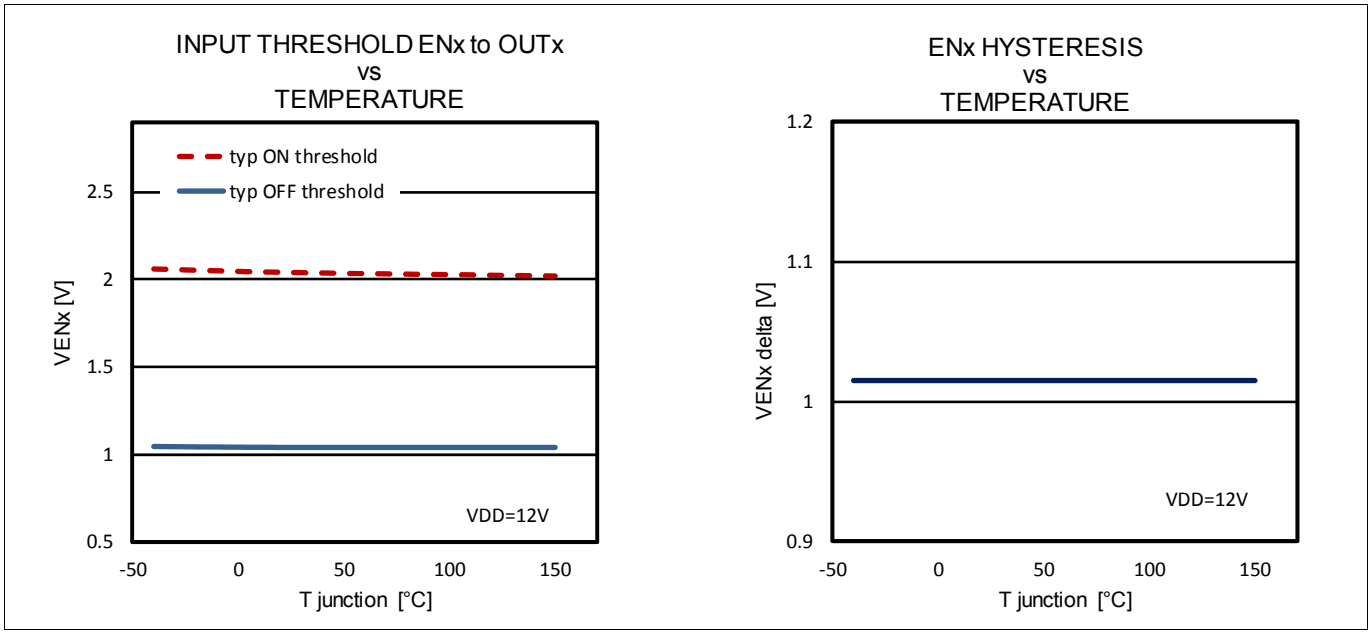

Figure 9 Input (ENx) characteristic

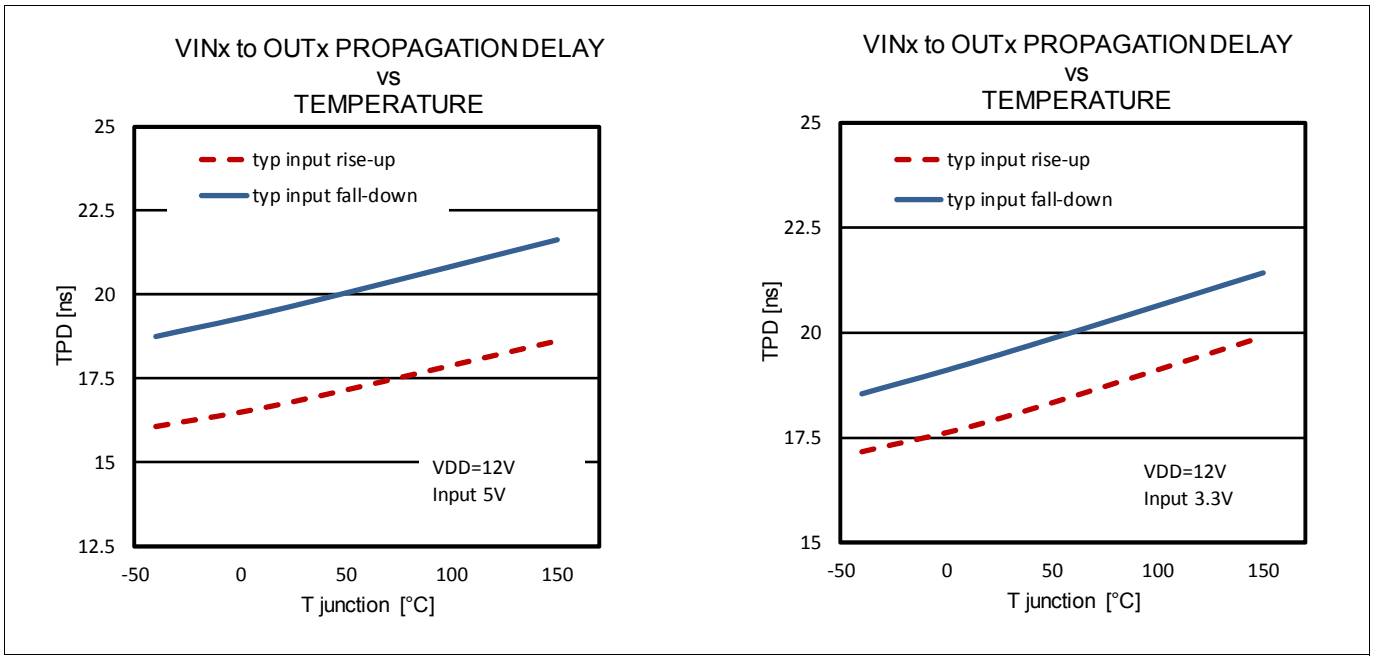

Figure 10 Propagation delay (INx) on different input logic levels (see Figure 4)

Typical Characteristics

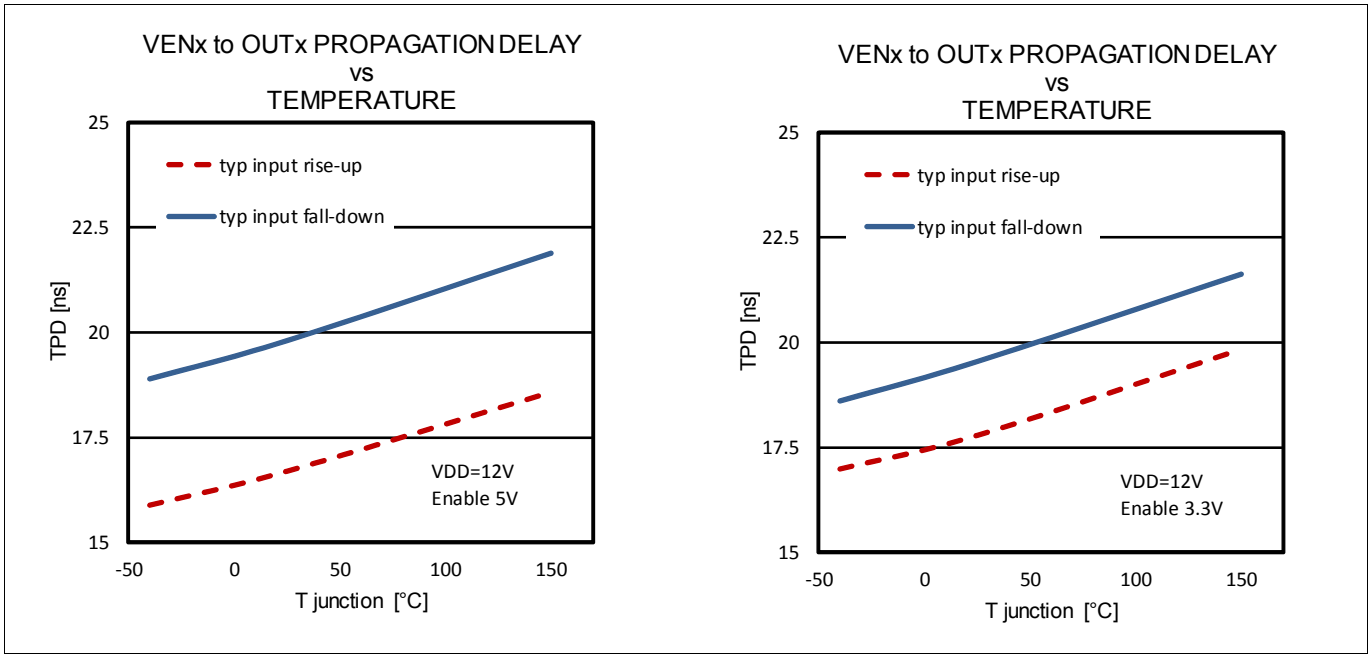

Figure 11 Propagation delay (ENx) on different input logic levels (see Figure 4)

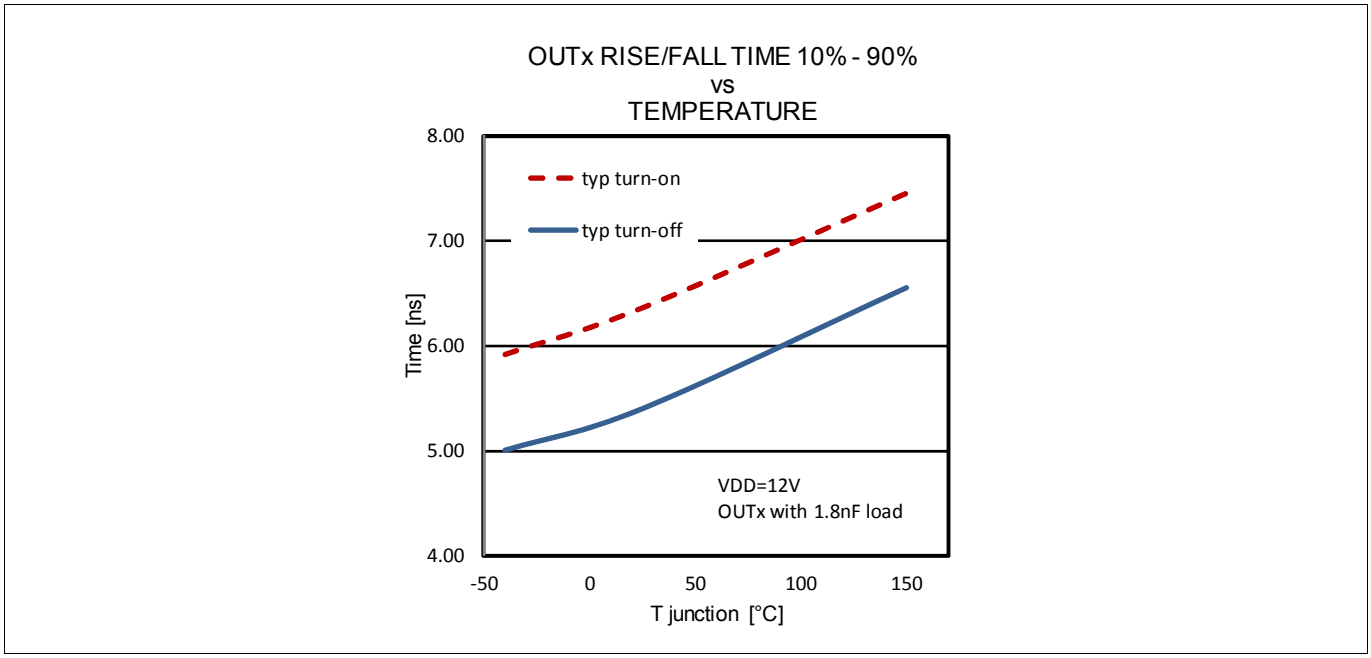

Figure 12 Rise / fall times with load on output (see Figure 4)

Typical Characteristics

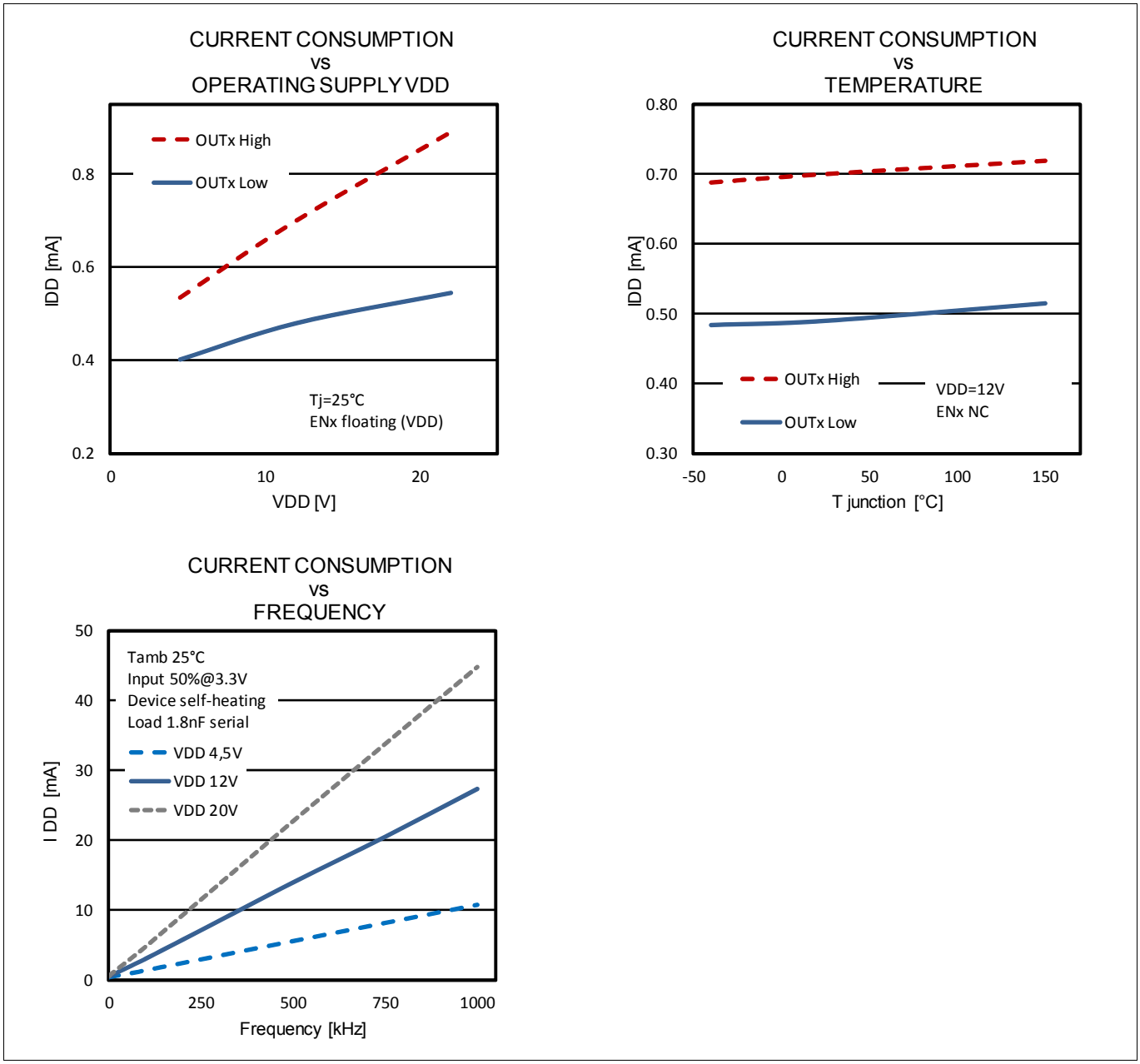

Figure 13 Power consumption related to temperature, supply voltage and frequency

8 Outline Dimensions

Notes

1. *For further information on package types, recommendation for board assembly, please go to: http://www.infineon.com/cms/en/product/technology/packages/.*

8.1 PG-DSO-8-60

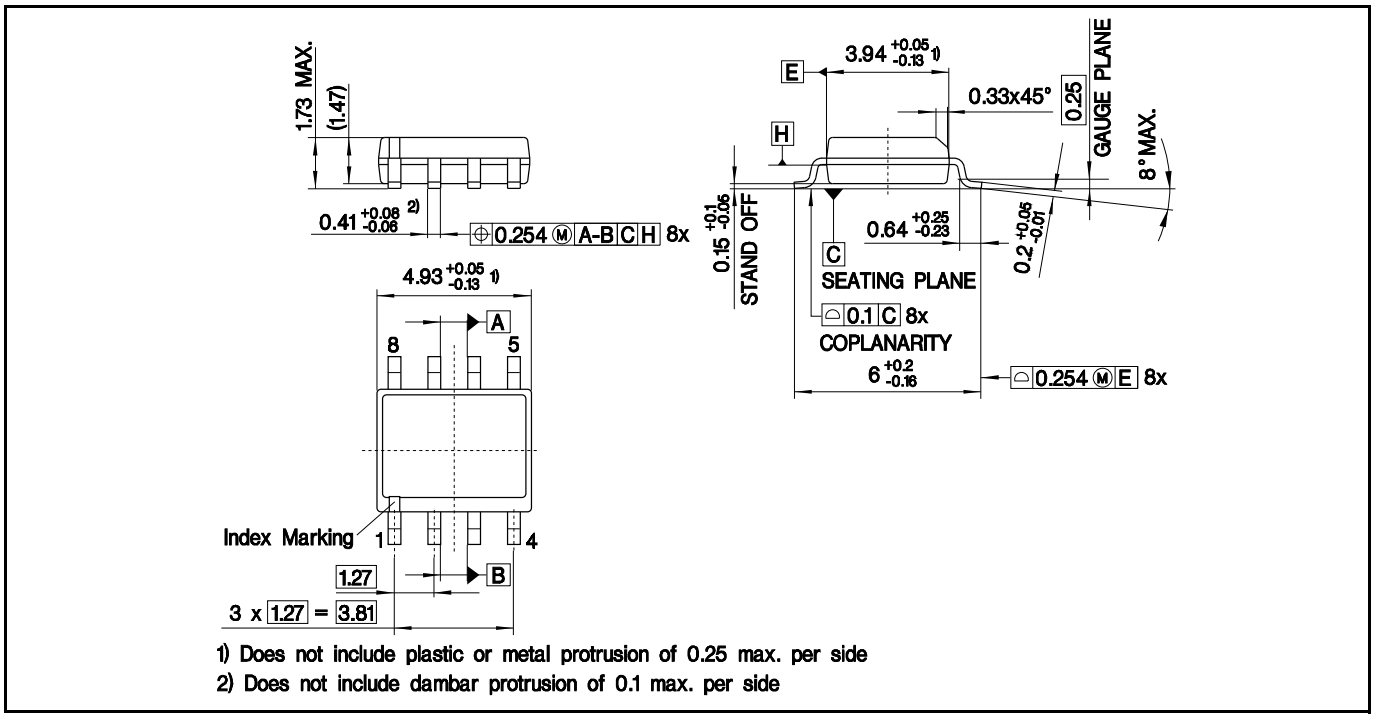

Figure 8-1 PG-DSO-8-60 outline

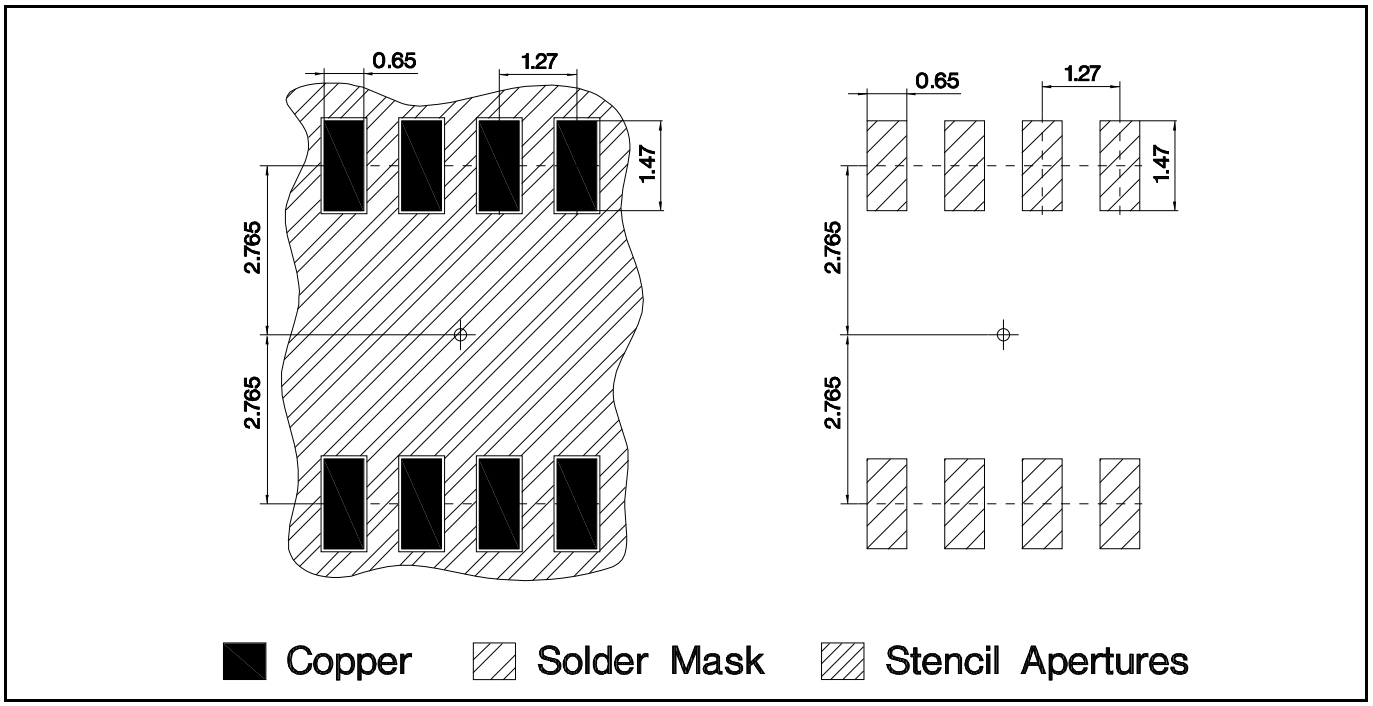

Figure 8-2 PG-DSO-8-60 footprint

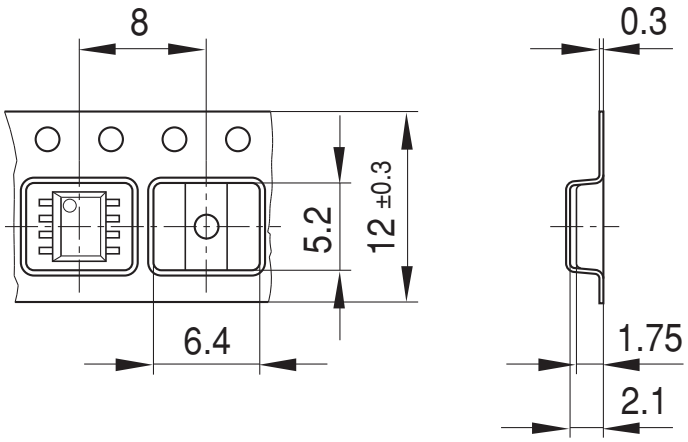

Figure 8-3 PG-DSO-8-60 packaging

8.2 PG-TSSOP-8-1

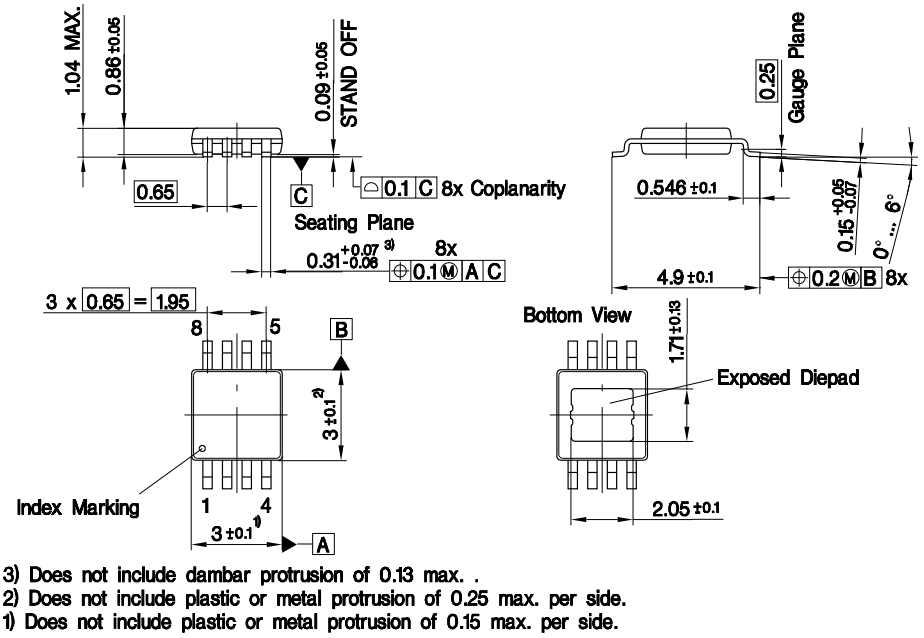

Figure 8-4 PG-TSSOP-8-1 outline

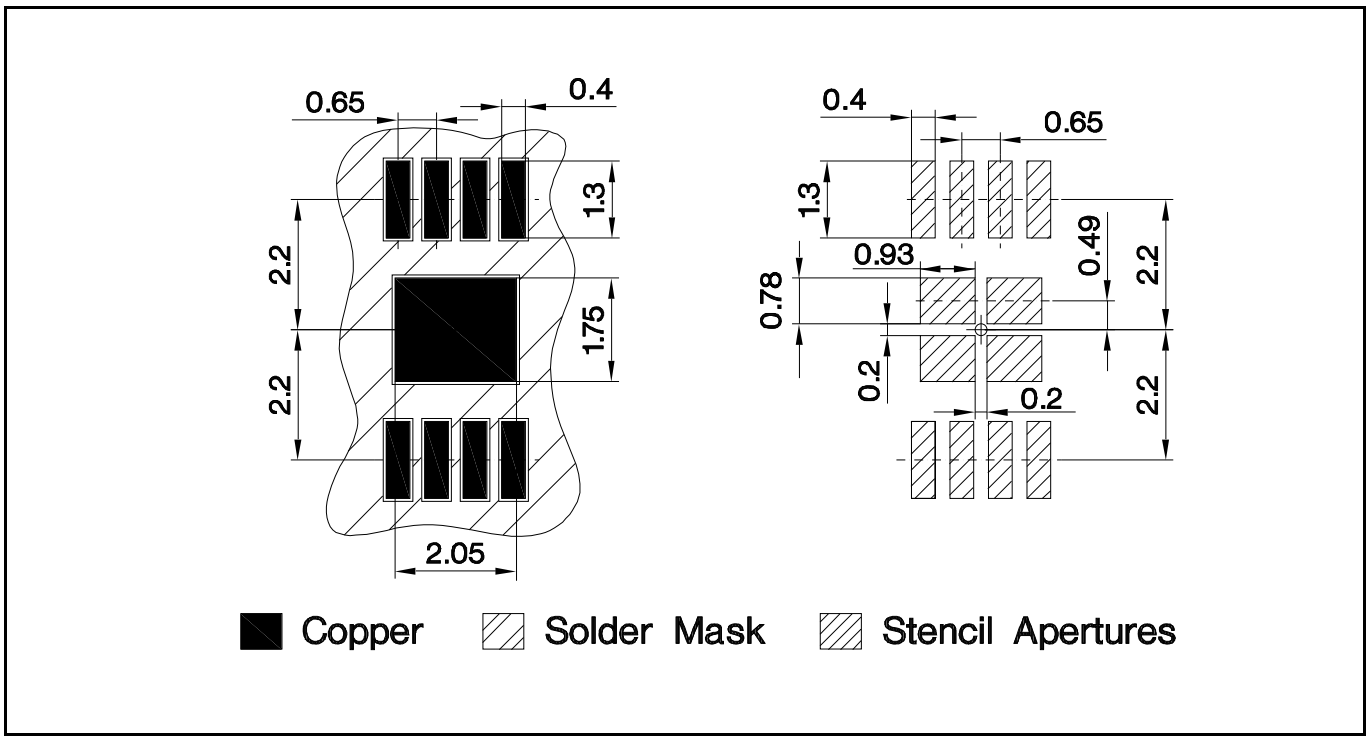

Figure 8-5 PG-TSSOP-8-1 footprint

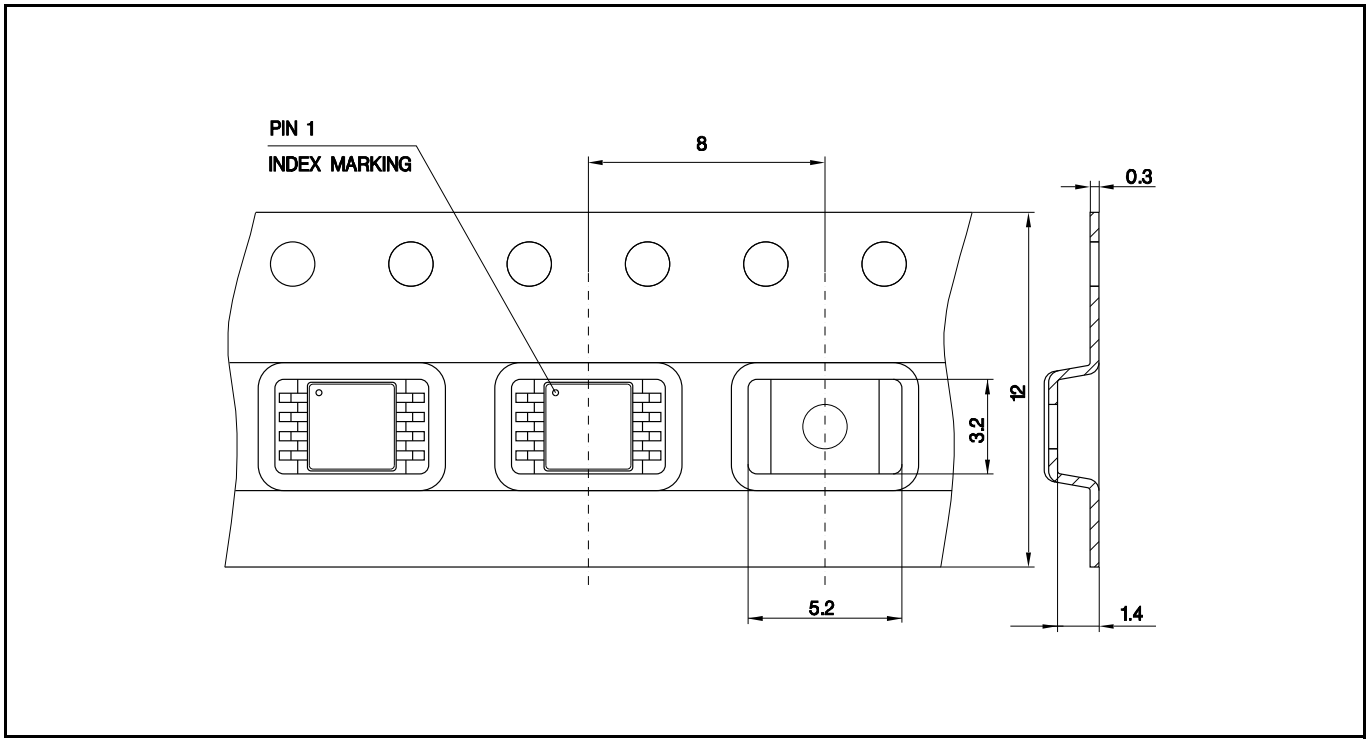

Figure 8-6 PG-TSSOP-8-1 packaging

9 Revision History

Revision 2.0, 2016-11-09			
Page/ Item	**Subjects (major changes since previous revision)**	**Responsible**	**Date**
	first version		
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