OptiMOS™-5 Power-Transistor

AEC Qualified RoHS

Features

- OptiMOS™ - power MOSFET for automotive applications
- N-channel - Enhancement mode - Logic Level
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Quality Features

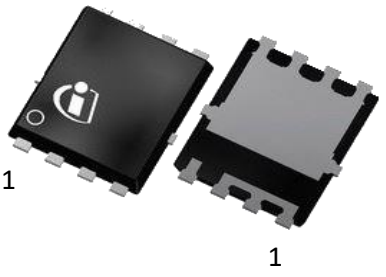
- Infineon Automotive Quality
- Extended qualification beyond AEC Q101
- Enhanced testing
- Advanced adhesion against delamination
- Complementary testing for board level reliability

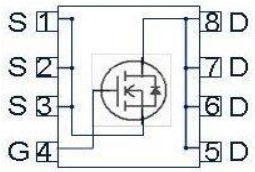
Advanced adhesion Robust Enhanced tested

Product Summary

V_{DS}	80	V
$R_{DS(on)}$	23	mΩ
I_D	28	A

PG-TDSON-8





Type	Package	Marking
IAUC28N08S5L230	PG-TDSON-8	5N08L230

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continous drain current	I_D	T_C=25°C, V_{GS}=10V	28	A
		T_C=100 °C, V_{GS}=10 V[1)]	20	
Pulsed drain current[1)]	$I_{D,pulse}$	T_C=25°C	112	
Avalanche energy, single pulse[1)]	E_{AS}	I_D=14 A	28	mJ
Avalanche current, single pulse	I_{AS}	-	14	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	T_C=25 °C	38	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics[1]						
Thermal resistance, junction - case	R_{thJC}	-	-	-	3.9	K/W
Thermal resistance, junction - ambient[2]	R_{thJA}	-	-	28.5	-	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	80	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=11 µA	1.2	1.6	2.0	
Zero gate voltage drain current	I_{DSS}	V_{DS}=80 V, V_{GS}=0 V, T_j=25 °C	-	-	1	µA
		V_{DS}=80 V, V_{GS}=0 V, T_j=85 °C[1]	-	-	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=14 A	-	21	28	mΩ
		V_{GS}=10 V, I_D=14 A	-	15	23	
Gate resistance[1]	R_G	-	-	0.9	-	Ω

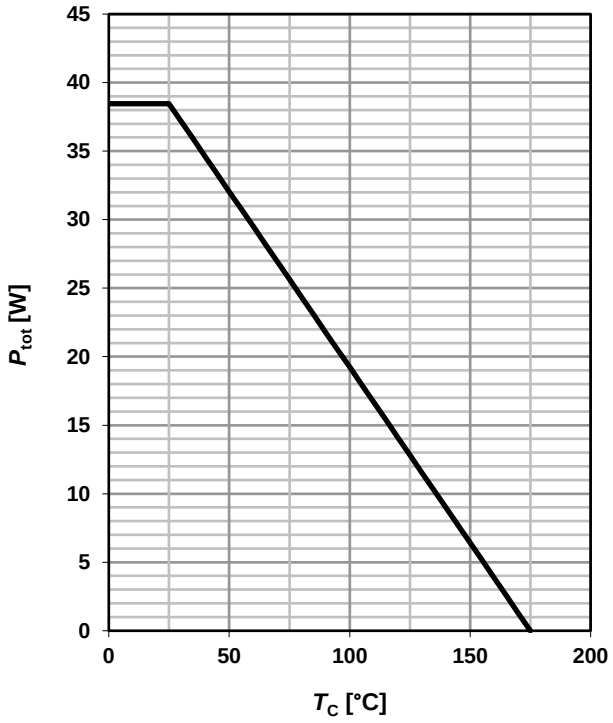
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[1]						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz	-	667	867	pF
Output capacitance	C_{oss}		-	118	153	
Reverse transfer capacitance	C_{rss}		-	9.3	14	
Turn-on delay time	$t_{d(on)}$	V_{DD}=40 V, V_{GS}=10 V, I_D=28 A, R_G=3.5 Ω	-	2	-	ns
Rise time	t_r		-	1	-	
Turn-off delay time	$t_{d(off)}$		-	6	-	
Fall time	t_f		-	4	-	
Gate Charge Characteristics[1]						
Gate to source charge	Q_{gs}	V_{DD}=40 V, I_D=14 A, V_{GS}=0 to 10 V	-	2.1	2.7	nC
Gate to drain charge	Q_{gd}		-	2.5	3.7	
Gate charge total	Q_g		-	11.6	15.1	
Gate plateau voltage	$V_{plateau}$		-	3.1	-	V
Reverse Diode						
Diode continous forward current[1]	I_S	T_C=25 °C	-	-	28	A
Diode pulse current[1]	$I_{S,pulse}$		-	-	70	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=14 A, T_j=25 °C	-	0.9	1.2	V
Reverse recovery time[1]	t_{rr}	V_R=40 V, I_F=28A, di_F/dt=100 A/µs	-	30	-	ns
Reverse recovery charge[1]	Q_{rr}		-	22	-	nC

[1] The parameter is not subject to production test - verified by design/chracterization.

[2] Device on four layer 2s2p PCB defined in accordance with JEDEC standards (JESD51-5-7).
PCB is vertical in still air.

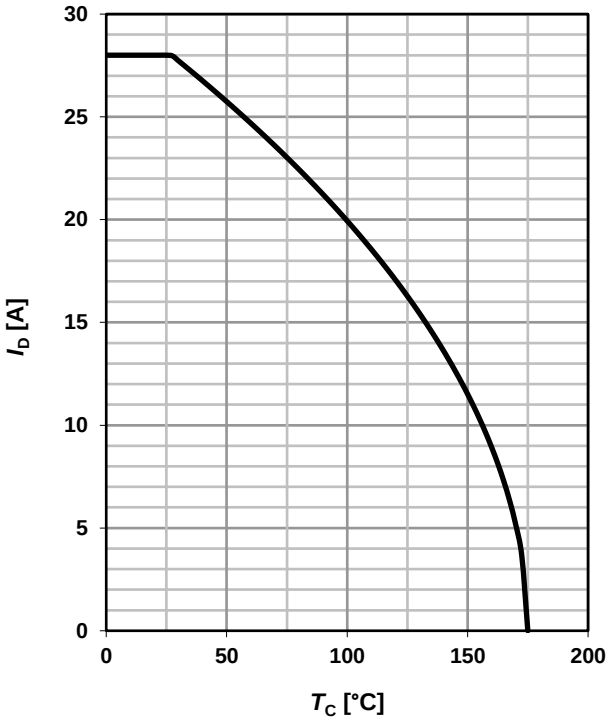
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V



2 Drain current

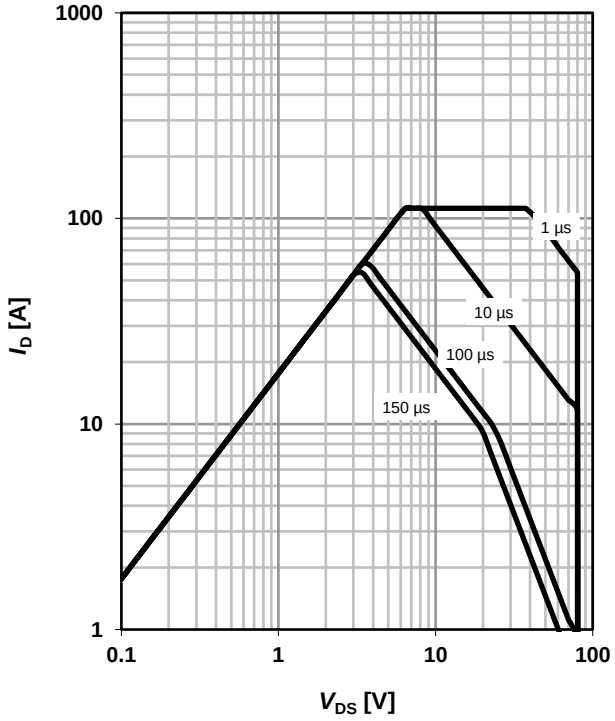
$I_D = f(T_C)$; $V_{GS} \geq 6$ V



3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$

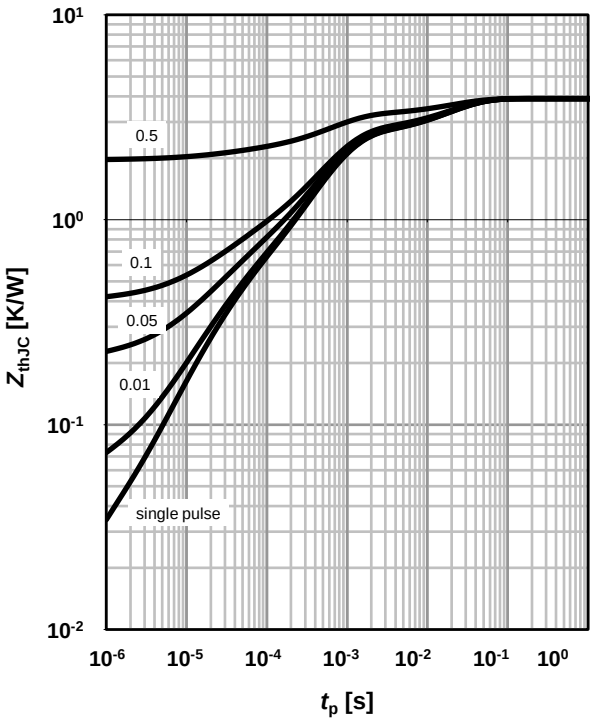
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

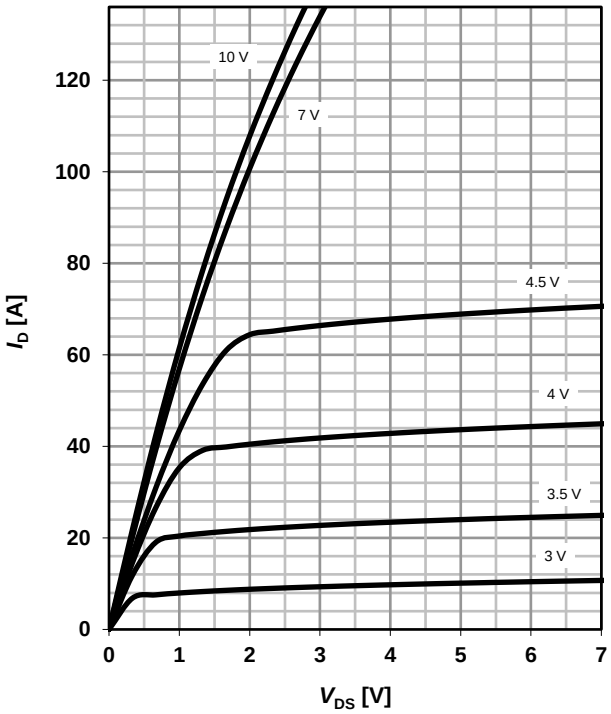
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C

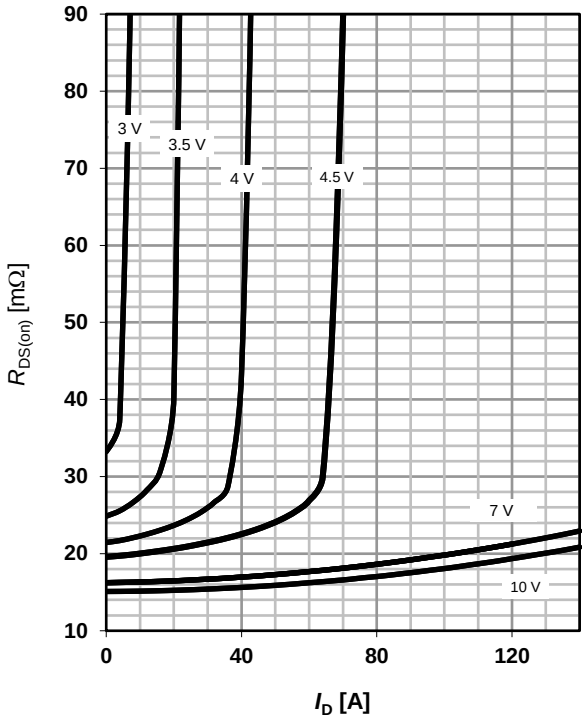
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = (I_D)$; $T_j = 25$ °C

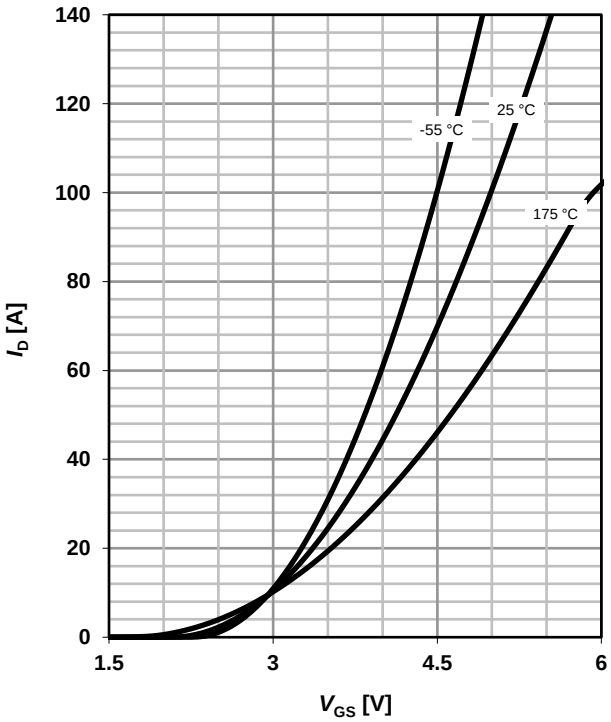
parameter: V_{GS}



7 Typ. transfer characteristics

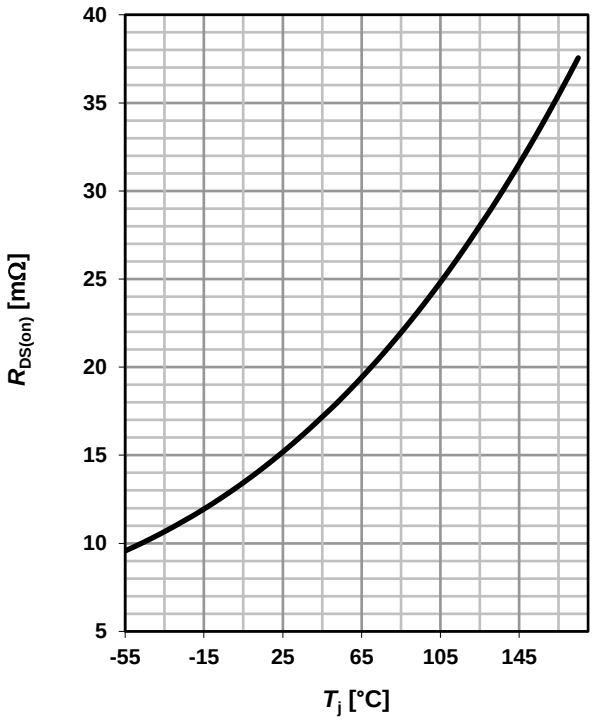
$I_D = f(V_{GS})$; $V_{DS} = 6$V

parameter: T_j



8 Typ. drain-source on-state resistance

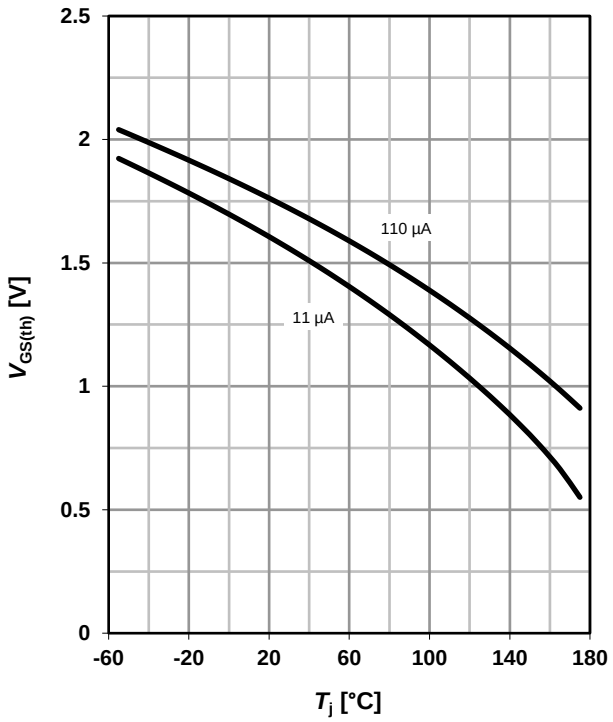
$R_{DS(on)} = f(T_j)$; $I_D = 14$ A; $V_{GS} = 10$ V



9 Typ. gate threshold voltage

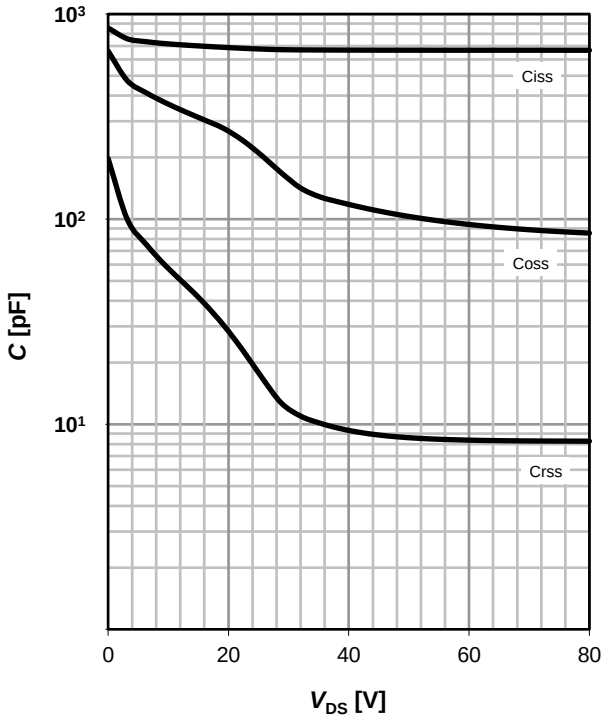
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

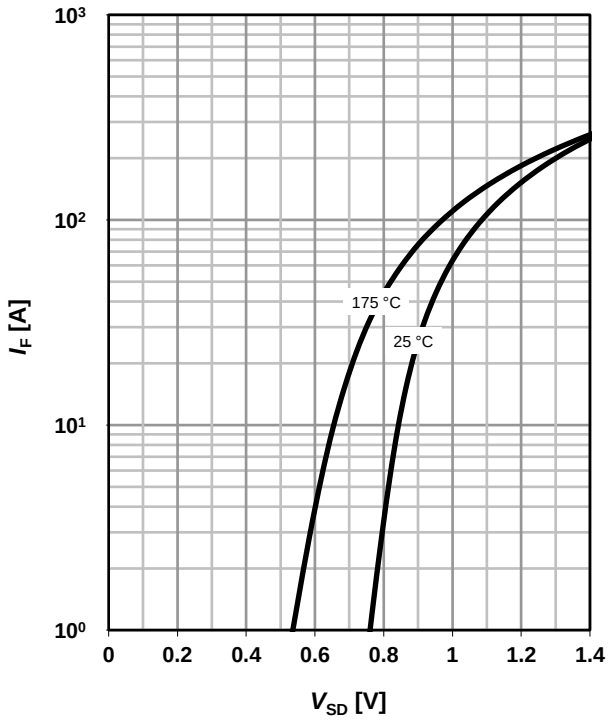
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



11 Typical forward diode characteristicis

IF = f(V_{SD})

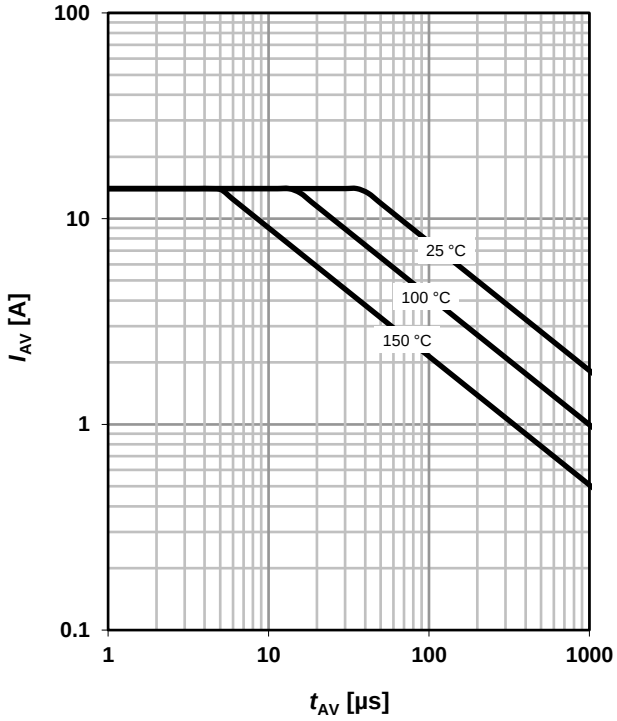
parameter: T_j



12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$

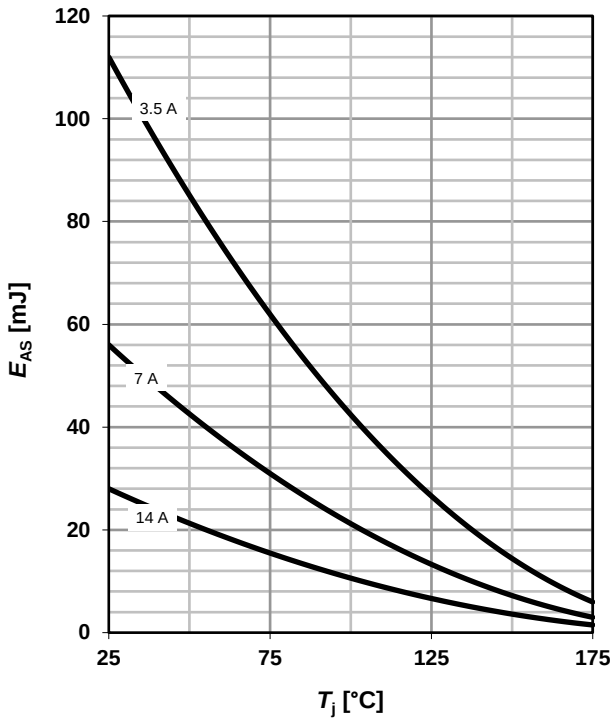
parameter: $T_{j(start)}$



13 Typical avalanche energy

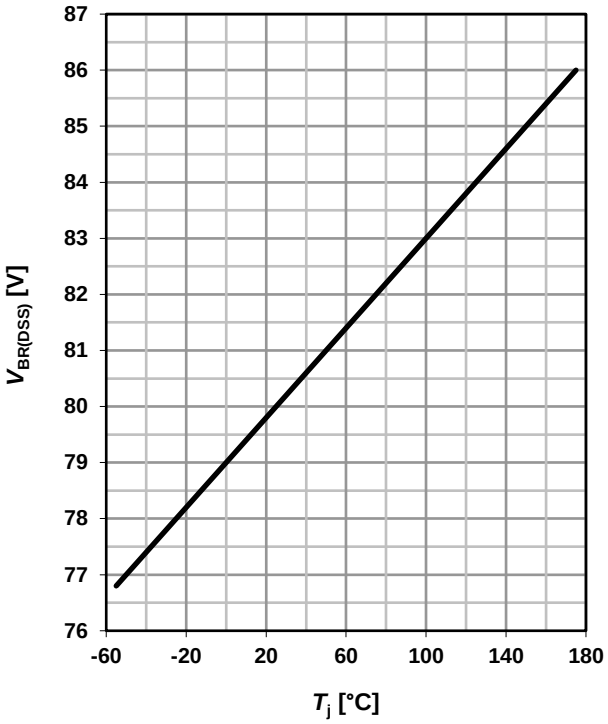
$E_{AS} = f(T_j)$

parameter: I_D



14 Drain-source breakdown voltage

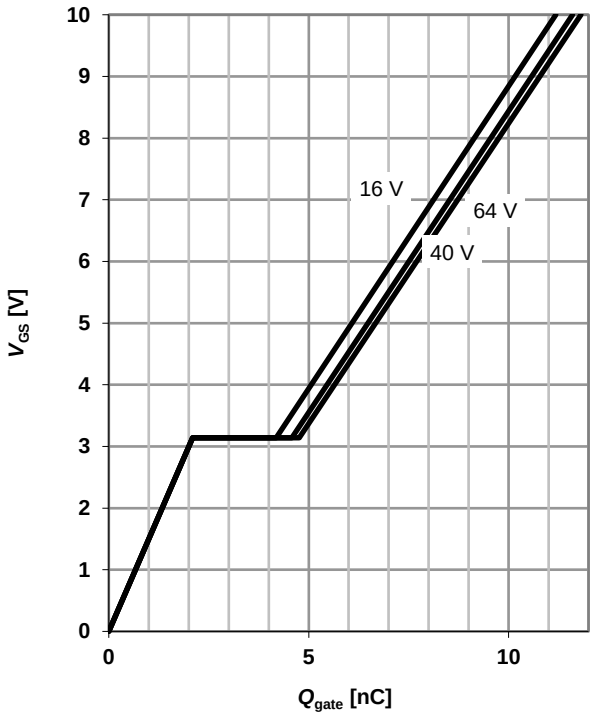
$V_{BR(DSS)} = f(T_j)$; $I_{D\_typ} = 1$ mA



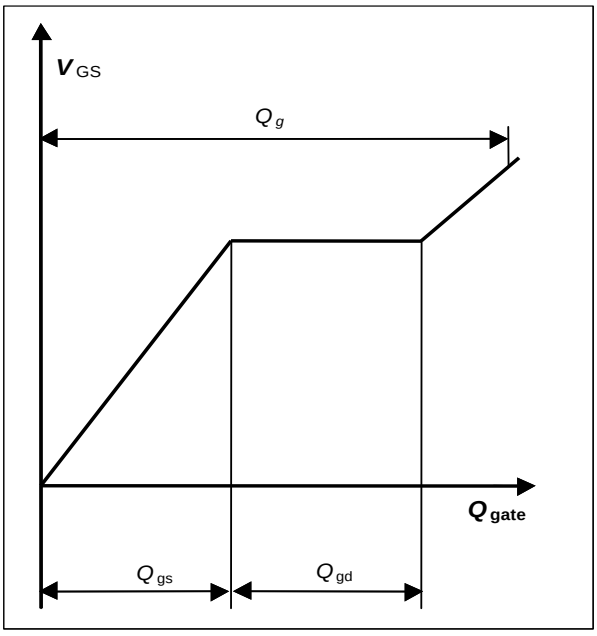
15 Typ. gate charge

$V_{GS} = f(Q_{gate})$; $I_D = 14$ A pulsed

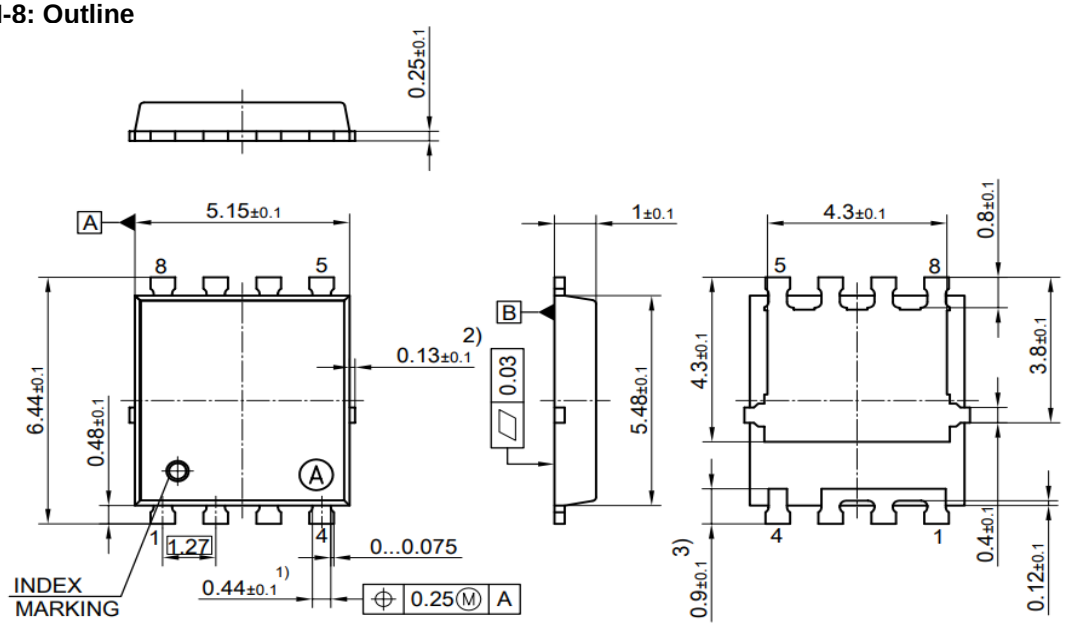
parameter: V_{DD}



16 Gate charge waveforms

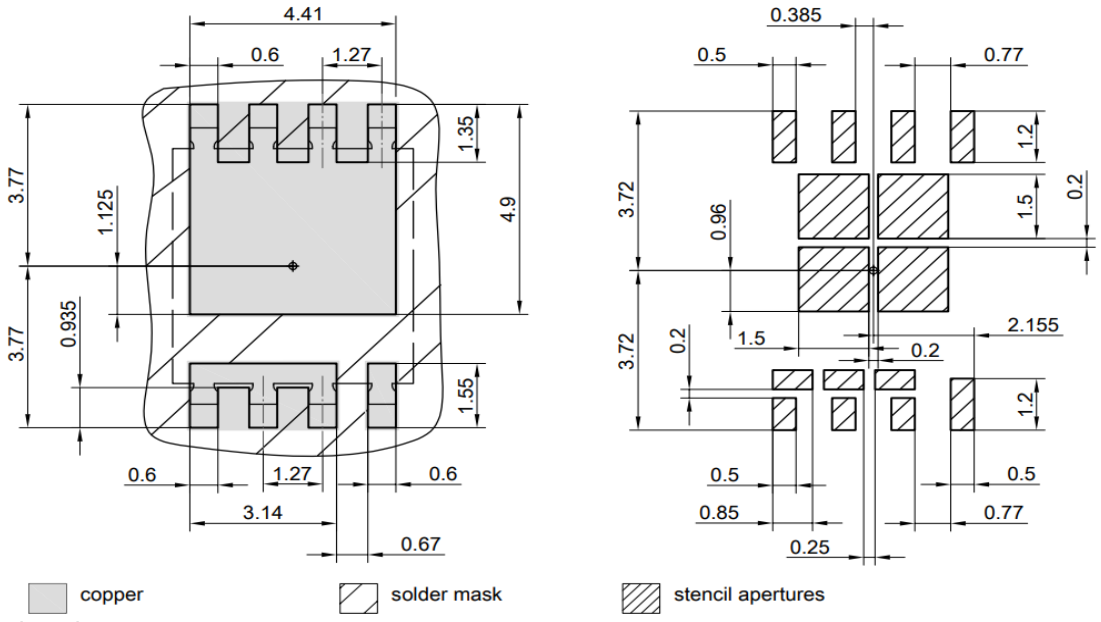


PG-TDSON-8: Outline



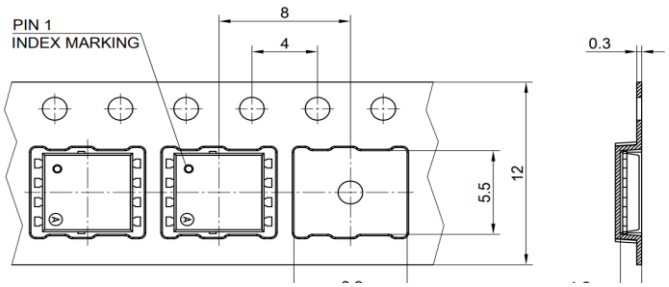
1) EXCLUDE MOLD FLASH
2) REMOVAL ON MOLD GATE, INTRUSION 0.1MM AND PROTRUSION 0.1MM
3) LEAD LENGTH UP TO ANTI FLASH LINE
4)ALL METAL SURFACE ARE PLATED, EXCEPT AREA OF CUT
ALL DIMENSIONS ARE IN UNITS MM
THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 [ ]

Footprint



Dimensions in mm

Packaging



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