



## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which permanent damage to the device may occur. These are stress ratings only, functional operation of the device at these or any other condition beyond those indicated in the "Recommended Operating Condition" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability. All voltage parameters are absolute voltages referenced to GND unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured mounted on board in free air condition.

Symbol	Definition	Min	Max	Units
V <sub>CC-GND</sub>	V <sub>CC</sub> to Gnd maximum voltage	-0.3	+37	V
V <sub>CC-V<sub>EE</sub></sub>	V <sub>CC</sub> to V <sub>EE</sub> maximum voltage	-0.3	+37	
V <sub>CC-V<sub>IN</sub></sub>	V <sub>CC</sub> to V <sub>IN</sub> maximum voltage	-0.3	+37	
V <sub>CC-V<sub>LPM</sub></sub>	V <sub>CC</sub> to V <sub>LPM</sub> maximum voltage	-0.3	+37	
V <sub>CB</sub>	CB to OUTH max voltage	-0.3	+5.5	mA
I <sub>LPM</sub>	LPM pin maximum current	-10	+10	
I <sub>IN</sub>	IN pin maximum current	-10	+10	V
V <sub>OUTH</sub>	OUTH pin maximum voltage, DC operation	V <sub>CC</sub> - 37	V <sub>CC</sub> + 0.3	
V <sub>OUTL</sub>	OUTL pin maximum voltage, DC operation	V <sub>EE</sub> - 0.2	V <sub>CC</sub> + 0.3	A
I <sub>OUTH</sub>	Maximum input transient current to OUTH pin (t < 1us, Ron = 2Ω)	---	2	
I <sub>OUTL</sub>	Maximum output transient current from OUTL pin (t < 1us, Roff = 2Ω)	---	1.5	W
PD	Package power dissipation @ T <sub>A</sub> ≤ 25 °C	—	1	
R <sub>thJA</sub>	Thermal resistance, junction to ambient	—	80	K/W
T <sub>J</sub>	Junction temperature	-40	150	°C
T <sub>S</sub>	Storage temperature	-55	150	
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300	

## Recommended Operating Conditions

The recommended conditions represent the AUIR08152 optimum performances for the typical application

Symbol	Definition	Min.	Max.	Units
V <sub>CC-GND</sub>	Gate driver positive supply voltage	15	25	V
GND-V <sub>EE</sub>	Recommended negative gate bias	0	-10	
V <sub>CC-V<sub>EE</sub></sub>	Total supply voltage	15	35	
V <sub>OUTH</sub>	OUTH Output voltage	V <sub>CC</sub> - 35	V <sub>CC</sub>	
V <sub>IN,LPM</sub>	IN and LPM pins voltage range	V <sub>CC</sub> -35	V <sub>CC</sub>	nF
C <sub>boot</sub>	Recommended bootstrap ceramic capacitor	10	47	
C <sub>load</sub>	Maximum recommended equivalent gate capacitor	—	240	μF
C <sub>dec</sub>	Recommended V <sub>CC</sub> & V <sub>EE</sub> decoupling capacitors*	22	33	
R <sub>on</sub>	OUTH series resistor to gate	1.5	20	Ω
R <sub>off</sub>	OUTL series resistor to gate	1.5	20	
R <sub>pull-up</sub>	Recommended pull-up resistor for IN and LPM pins	10	100	kΩ
PW <sub>off</sub>	Minimum recommended OFF time on the IN pin	1	—	μs
PW <sub>on</sub>	Minimum recommended ON time on the IN pin	1	—	

\* Due to the high current application a good quality low ESR capacitor has to be used. Numbers are indicative, a value about 40 times the load capacitance seen at the OutH and OutL pins is suggested.

**Static Electrical Characteristics**
 $V_{CC} - Gnd = 15V$ ,  $V_{EE} - Gnd = -5V$ ,  $C_{boot} = 15nF$ ,  $R_{on} = R_{off} = 3\Omega$ ,  $-40\text{ }^\circ\text{C} < T_A < 125\text{ }^\circ\text{C}$  unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$V_{CCUV+}$	$V_{CC}$ -GND under-voltage rising edge	—	11.7	12.8	V	LPM = X, IN = Vcc, Vee = Gnd;
$V_{CCUV-}$	$V_{CC}$ -GND under-voltage falling edge	9.6	10.5	—		
$V_{CCUVH}$	$V_{CC}$ -GND under-voltage hysteresis	0.5	1.2	—		
$VCB_{UV} (*)$	VCB under-voltage lockout	2.8	4	5.7		
$I_{QGG}$	Current out of the Gnd pin	—	20	60	$\mu\text{A}$	IN = X, LPM = X
$I_{QOUTL1}$	Current flowing into the OUTL pin	—	0	1.5		IN = Vcc, LPM = X, OUTH = NC, $V_{OUTL-Gnd} = 15V$
$I_{QEESW}$	$V_{EE}$ pin current, IN cycling	—	3	8	mA	IN = 10kHz - 50% duty cycle LPM = Vcc, $C_{LOAD} = 0nF$
$I_{QEE0}$	$V_{EE}$ pin current – output OFF – normal mode	—	1.5	4		IN = Gnd, LPM = Vcc
$I_{QEE1}$	$V_{EE}$ pin current – output ON – normal mode	—	0.8	1.6		IN = Vcc, LPM = Vcc
$I_{QEELQ0}$	$V_{EE}$ pin current – output OFF – low power mode	—	0.6	2.0		IN = Gnd, LPM = Gnd
$I_{QEELQ1}$	$V_{EE}$ pin current – output ON – low power mode	—	0.8	1.6		IN = Vcc, LPM = Gnd
$I_{QEEUV}$	$V_{EE}$ pin current at low Vcc supply	—	0.6	1.6		IN = X, LPM = X, $V_{CC} < V_{CCUV-}$
$I_{QB}$	CB pin sink current	—	0.5	1		IN = Vcc, LPM = Vcc, $V_{CB-VOUTH} = 5.5V$
$I_{QOUTH0}$	OUTH pin sourced current – normal mode	—	1	3.5		IN = Gnd, LPM = Vcc OUTH = $V_{EE}$ , OUTL = NC
$I_{QOUTH0LQ}$	OUTH pin sourced current – low power mode	—	0.2	0.5		IN = Gnd, LPM = Gnd OUTH = $V_{EE}$ , OUTL = NC
$I_{BOUTH}$	CB pin sourced current – normal mode	30	90	—		IN = Gnd, LPM = Vcc, OUTL = NC, CB = OUTH = Vee
$I_{BOUTH\_pl}$	CB pin pulsed sourced current – normal mode	90	200	—		Min pulse length 2us guaranteed by design
$I_{BOUTH\_LQ}$	CB pin sourced current – low power mode	0.5	5	23		IN = Gnd, LPM = Gnd, OUTL = NC, CB = OUTH = Vee
$I_{OUTH+} / I_{OUTL-}$	OUTH /OUTL pins output current capability	10	—	—		A LPM = X $V_{OUTL-}$ : $t < 100\mu\text{s}$ , $V_{OUTH+}$ : CB charged
$V_{CC-VinH}$	IN pin – output ON voltage	1.5	2.5	—		V
$V_{CC-VinL}$	IN pin – output OFF voltage	—	4.5	5.5		
$V_{INhys}$	IN pin voltage hysteresis	1	2	—		
$V_{CC-VLPMH}$	LPM pin normal mode voltage	1.4	2	—		
$V_{CC-VLPML}$	LPM pin low power mode voltage	—	3.2	3.8		
$V_{LPMhys}$	LPM pin voltage hysteresis	0.3	1.1	—		
$I_{IN15}$	IN pin sourced current	40	90	180	$\mu\text{A}$	IN = Gnd
$I_{LPM15}$	LPM pin sourced current	10	25	50		LPM = Gnd
$R_{dson\ OUTH}$	OUTH transistor $R_{dson}$	—	100	200	m $\Omega$	IN = Vcc, $I_{out} 10A$ , $t < 100\mu\text{s}$ , Gnd = Vee, $V_{CB} = V_{OUTH} + 5.5V$
$R_{dson\ OUTL}$	OUTL transistor $R_{dson}$	—	200	400		-IN = Gnd, $I_{out} = 10A$ , $t < 100\mu\text{s}$ , Gnd = Vee
$I_{PMOS} (*)$	OUTH Pulling- up current source	15	30	120	mA	IN = Vcc, LPM = X, $V_{CC} - V_{OUTH} = 1.5V$

(\*)When  $V_{CB} - V_{OUTH} < V_{CB_{UV}}$ , OUTH pin remaining pulled-up to Vcc is guaranteed for at least 3usec with low impedance (=Ron) via Vdmos then continuously with larger impedance via Pmos (=Ipmos, see block diagram).

### Switching Electrical Characteristics

$V_{CC} - Gnd = 15V$ ,  $V_{EE} - Gnd = -9V$ ,  $C_{boot} = 15nF$ ,  $R_{on} = R_{off} = 3\Omega$ ,  $C_{LOAD} = 220nF$ ,  $-40\text{ }^\circ\text{C} < T_A < 125\text{ }^\circ\text{C}$  unless otherwise specified.

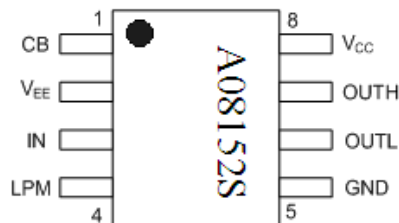
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions	
$t_{on}$	OUTH turn on propagation delay	—	150	350	ns	See parameters definitions LPM = X	
$t_{off}$	OUTL turn off propagation delay	—	230	350			
$t_{off\_VCBuv}$	OUTL turn off prop. delay when $V_{CB} < V_{CBuv}$ *	—	90	350			
$t_r$	OUTH rise time	—	50	150			
$t_f$	OUTL fall time	—	50	150			
$t_{rLQ}$	OUTH rise time (IN=1, $V_{CC}$ ramping up, LPM = Gnd)	—	50	250			$V_{EE} = LPM = Gnd$ , IN = $V_{CC}$
$t_{fLQ}$	OUTL fall time (IN=1, $V_{CC}$ ramping down, LPM = Gnd)	—	50	250			$V_{EE} = LPM = Gnd$ , IN = $V_{CC}$
Min Out-ON	ON time for 0.5 $\mu$ s IN pulse	200	600	900			Load = open
Min Out-OFF cb discharged	OFF time for 0.5 $\mu$ s IN pulse, CB discharged	200	500	900			Load = open, CB = 15 nF
Min Out-OFF cb charged	OFF time for 0.5 $\mu$ s IN pulse, CB charged	200	400	900	Load = open, CB = 15 nF		
$t_{onLPM}$	LPM activation time (from LPM edge to $I_{cb} < I_{BOUTH/2}$ )	—	0.6	3	$\mu$ s	by design	
$t_{offLPM}$	LPM deactivation time (from LPM edge to $I_{cb} > I_{BOUTH/2}$ )	—	0.6	3			

\* See also Fig. 5

### Truth Table

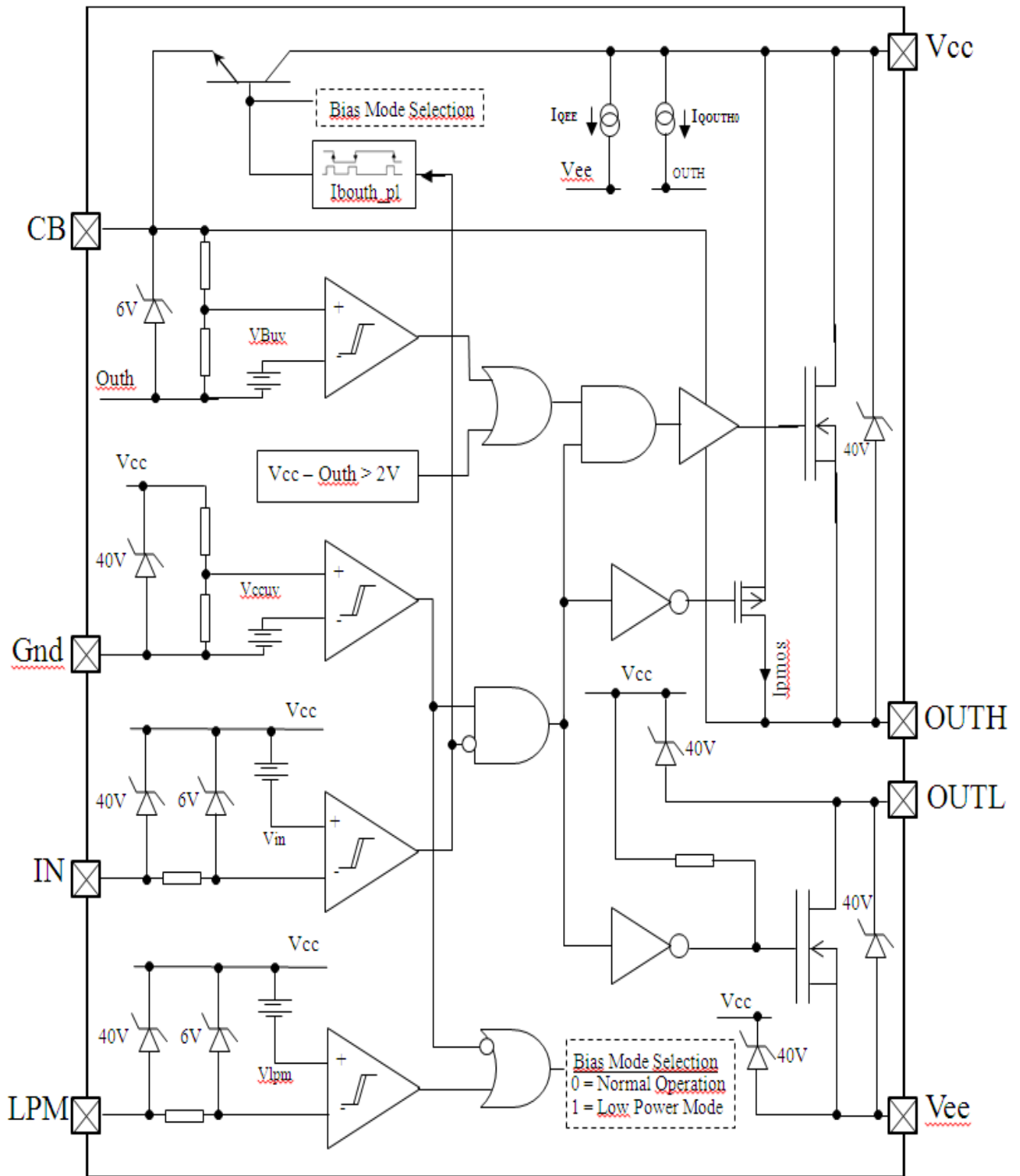
IN	LPM	VCC	OUTH	OUTL	Status
X	X	< $V_{CCuv}$	Open	Vee	IGBT or MOSFET = OFF – Low power mode
Gnd	Gnd	> $V_{CCuv}$	Open	Vee	IGBT or MOSFET = OFF – Low power mode
Gnd	Vcc	> $V_{CCuv}$	Open	Vee	IGBT or MOSFET = OFF – Normal mode
Vcc	Gnd	> $V_{CCuv}$	Vcc	Open	IGBT or MOSFET = ON – Low power mode
Vcc	Vcc	> $V_{CCuv}$	Vcc	Open	IGBT or MOSFET = ON – Normal mode

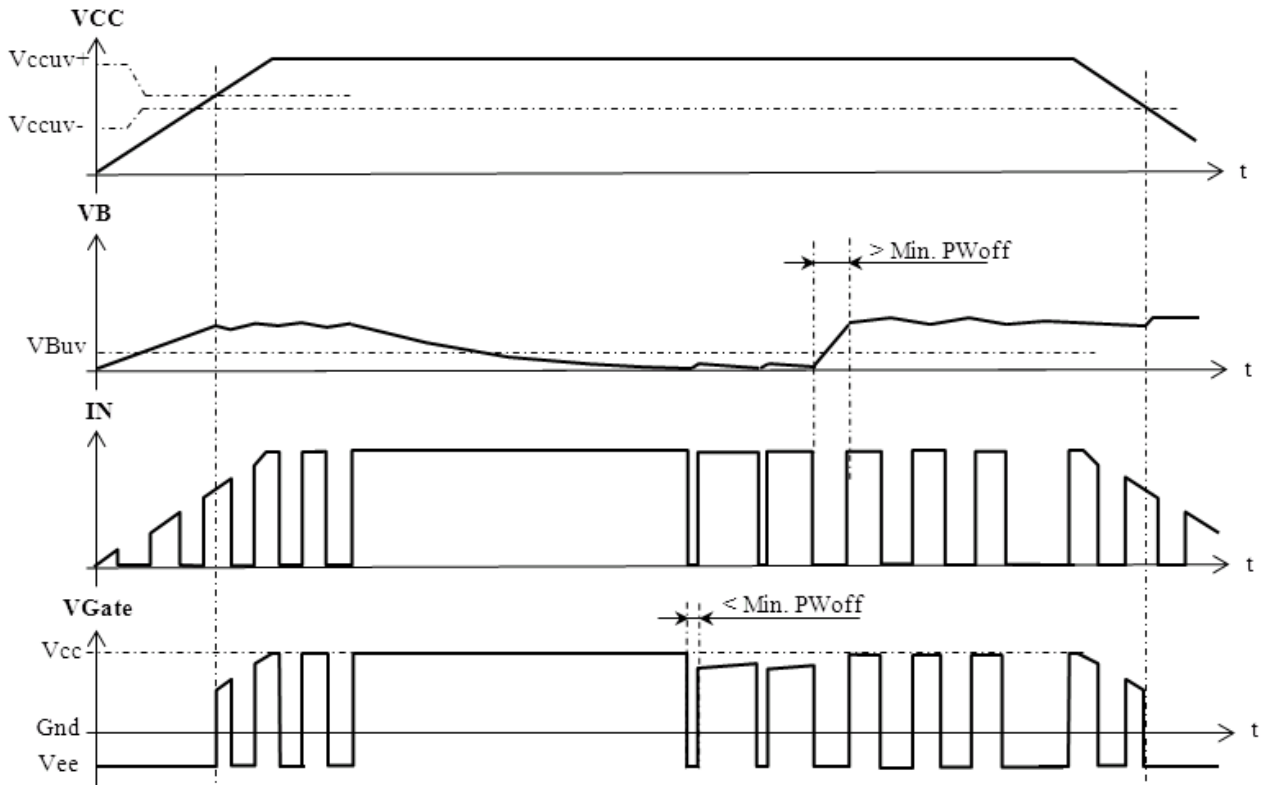
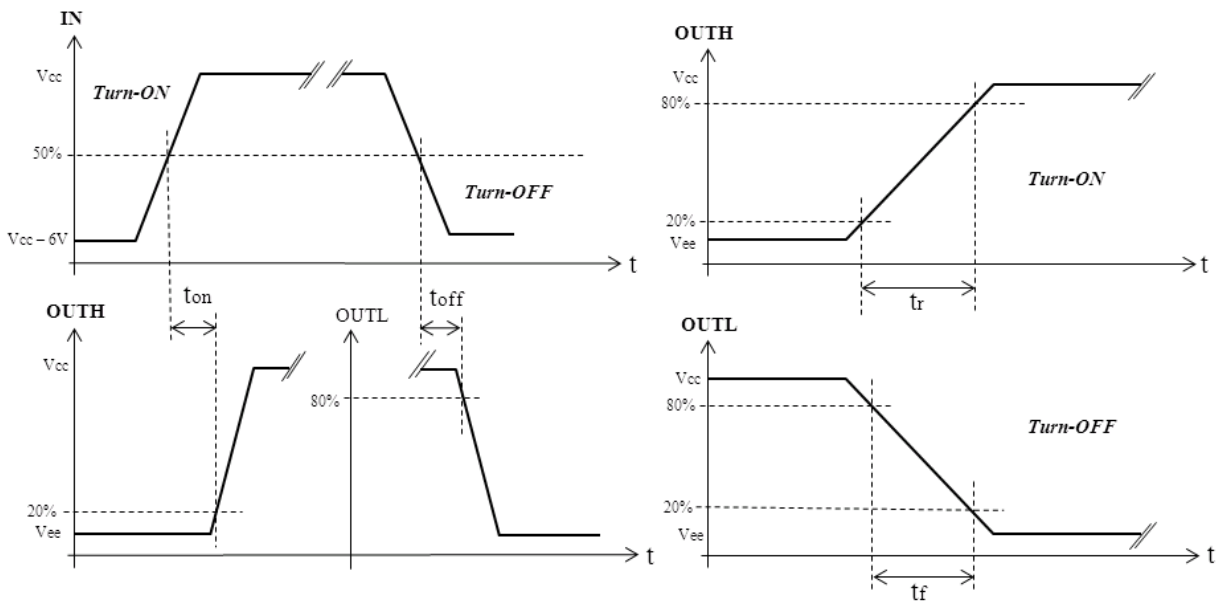
### Lead Assignments



### Lead Definitions

Symbol	Description	Pin
CB	External Bootstrap capacitor (cf. typical connection schematic)	1
Vee	Negative Supply Pin	2
IN	Gate Drive Input, (IN= Vcc forces OutH = high)	3
LPM	Low Power Mode Input, LPM= GND activates the Low Power Mode	4
GND	0V – IGBT Emitter or MOSFET Source Connection (cf. typical connection schematic)	5
OUTL	Gate Drive Output Pull down	6
OUTH	Gate Drive Output Pull up	7
Vcc	Positive Supply Pin	8

**Functional Block Diagram**


**Timing Diagram**

**Parameters Definitions**


Propagation delay definitions

Rise and fall time definitions

## Parameters

Figures are given for typical value @  $T_j=25^\circ\text{C}$  otherwise specified

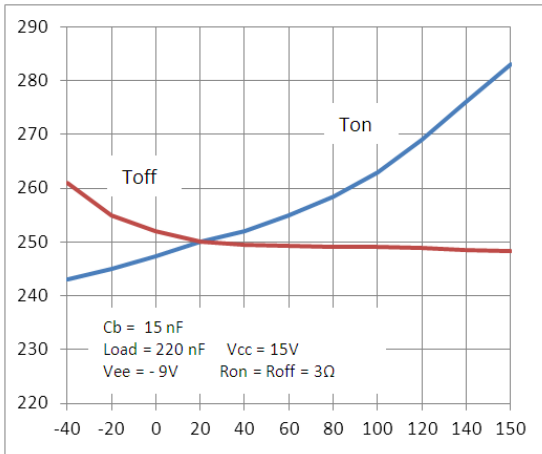


Figure 1: Ton and Toff (ns) Vs Temperature ( $^\circ\text{C}$ )

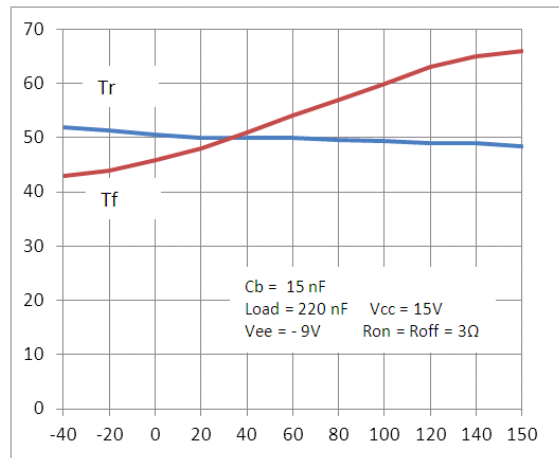


Figure 2: Tr and Tf (ns) Vs Temperature ( $^\circ\text{C}$ )

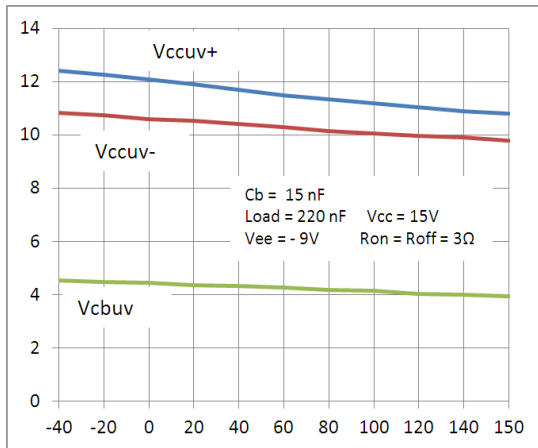


Figure 3: Vccuv+, Vccuv- and Vcbuv (V) Vs Temperature ( $^\circ\text{C}$ )

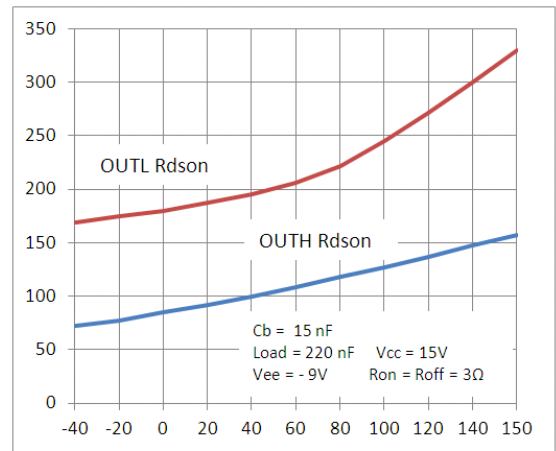


Figure 4: OUTH & OUTL Rdson's Vs Temperature ( $^\circ\text{C}$ )

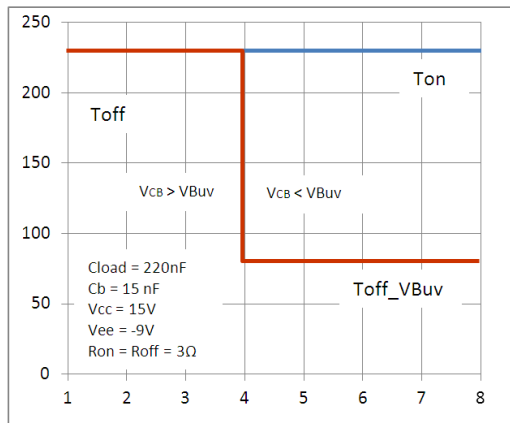


Figure 5: Ton, Toff (ns) Vs IN pulse duration ( $\mu\text{s}$ )

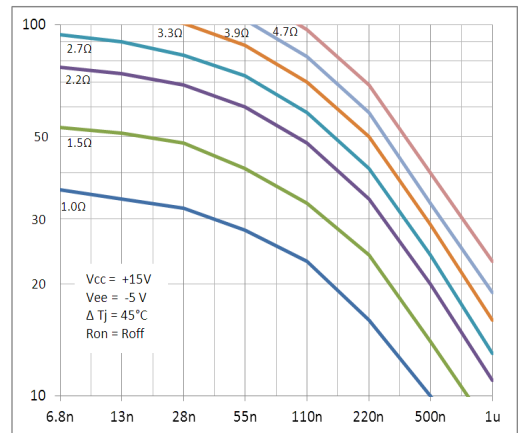


Figure 6: Max PWM Frequency (kHz) Vs Gate Capacitance (F) &  $R_g$  ( $\Omega$ )

## Examples of system schematics with HVIC

This section shows how the AUIR08152S can be driven by IR High Voltage IC (HVIC).

All the examples refer to an inverter leg; floating voltage sources to supply the high side AUIR08152S are named  $V_{cch}$  and  $V_{veh}$ , while voltage sources to supply the low side AUIR08152S are named  $V_{ccl}$  and  $V_{eel}$ .

In the examples, a 7V negative  $V_{veh}(l)$  is shown; this is usually enough to keep even big die size IGBT firmly clamped in their OFF state during  $dV/dt$  transients; in case the IGBTs do not require a negative gate voltage,  $V_{veh}(l)$  sources can simply be shorted to their relevant IC GND (h or l).

It is straightforward to say that, when multiple legs are considered, floating supplies must have galvanic isolation between each other (and w.r.to low side); low side supplies could be shared between the different legs but the choice if using multiple or shared low side supplies mostly depend upon the system layout.

Especially important in the emitter impedance  $Z_l$ , as shown in the figures. Non negligible value of the emitter inductance creates imbalance between the emitter returns and may suggest using separate supplies also for the low side gate drivers.

**Example1** : IGBT gate driving by AUIRS2181S and two AUIR08152S buffer ICs.

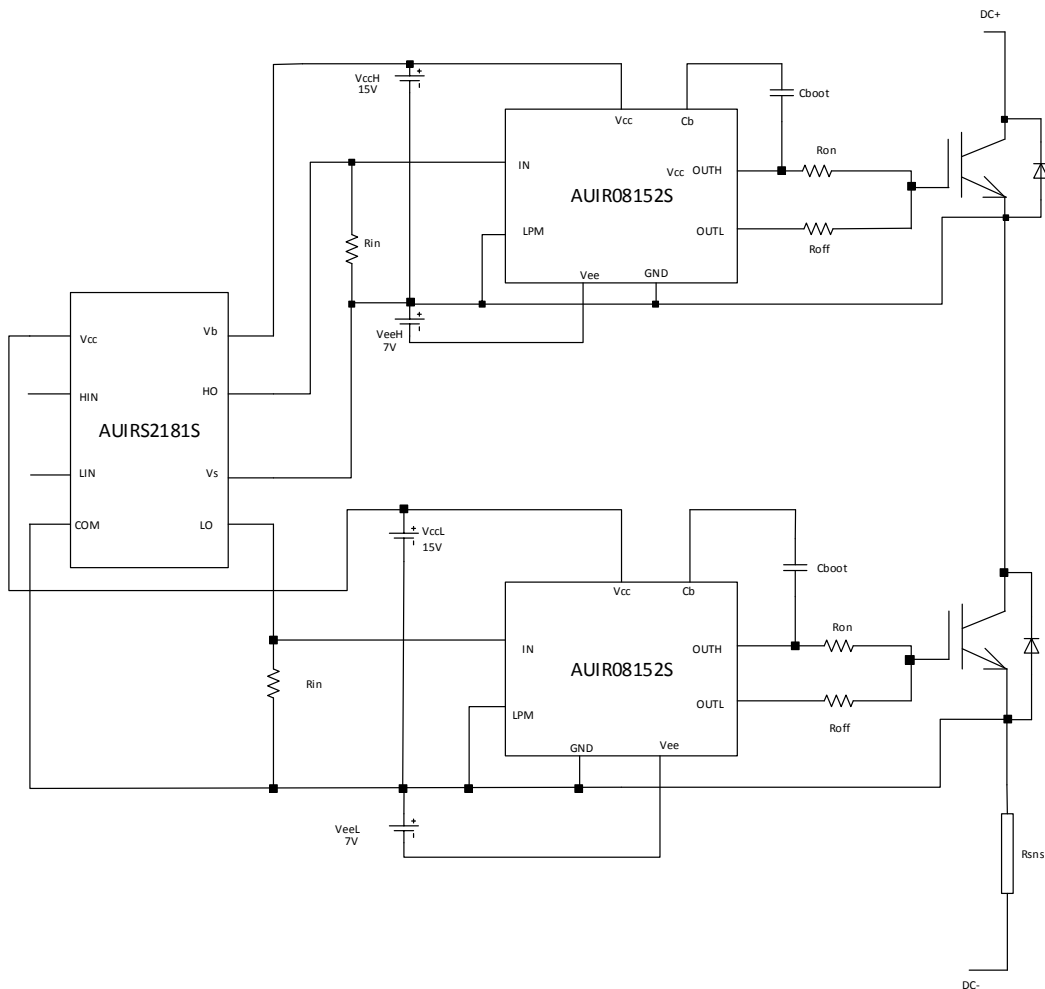


Figure A-1

The AUIRS2181S is an 8 pin SOIC and does not have separate COM (power GND) and  $V_{ss}$  (signal GND) pins. Therefore, COM is directly connected to the GND of the low side buffer IC but special care has to be taken when laying out power and control section.



**Example 2:** IGBT gate driving by AUIRS21814S (or AUIRS2191S) and two AUIR08152S buffer ICs.

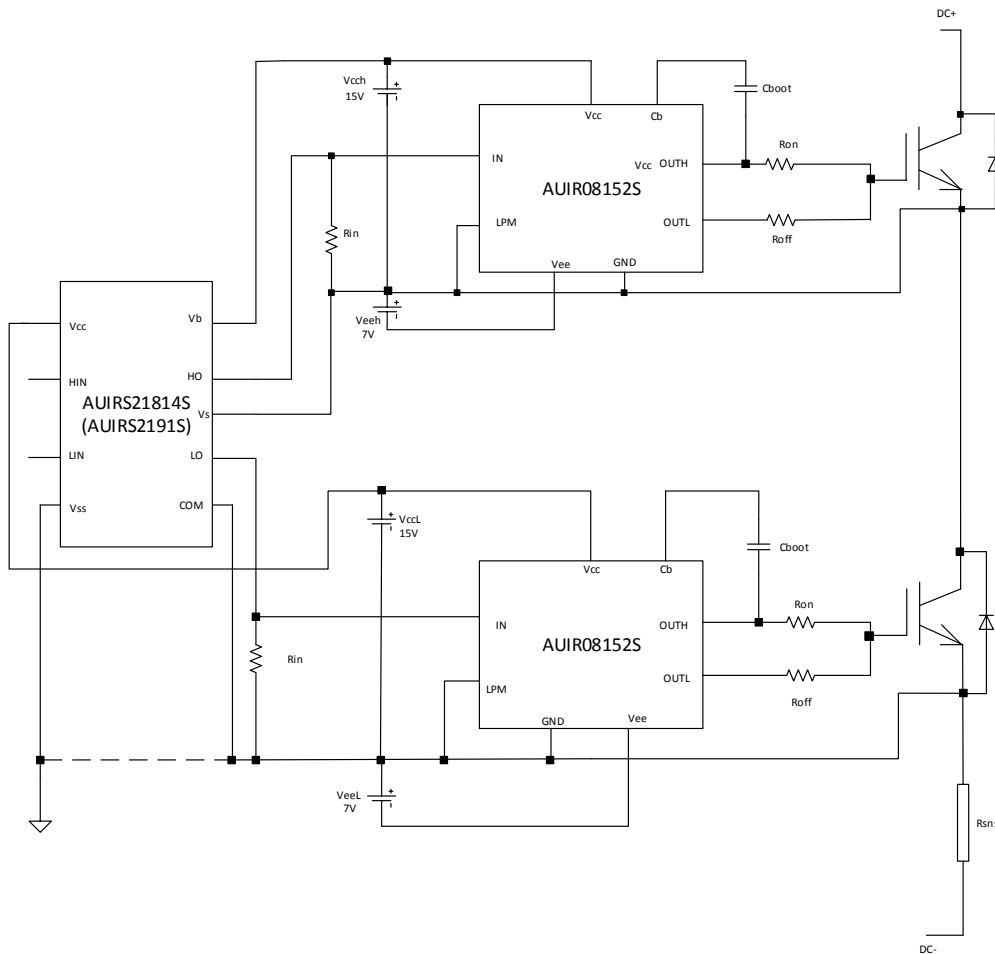


Figure A-2

The AUIRS21814S (and the AUIRS2191S) have separate Vss and COM pins. They can be simply connected together or, better, connected to separate logic and power GND.

In any case, the low side AUIR08152S GND pin has to be connected to the low side IGBT emitter, and layouting care has to be taken that, in case of separate Vss and COM grounding, the imbalance between these two points doesn't exceed the data sheet value (usually +/-5V).

**Example 3:** IGBT gate driving by two AUIRS2117S and two AUIR08152S buffer ICs.

Here, the situation is partially better in term of separation between logic and power GND, in that even the low side power GND can float -5V to +600V with respect to COM, which is connected to signal GND.

Actually, because the negative Vs transient capability of the AUIRS2117S, much more room is allowed for both positive and negative transients of the IGBT emitters w.r.to COM.

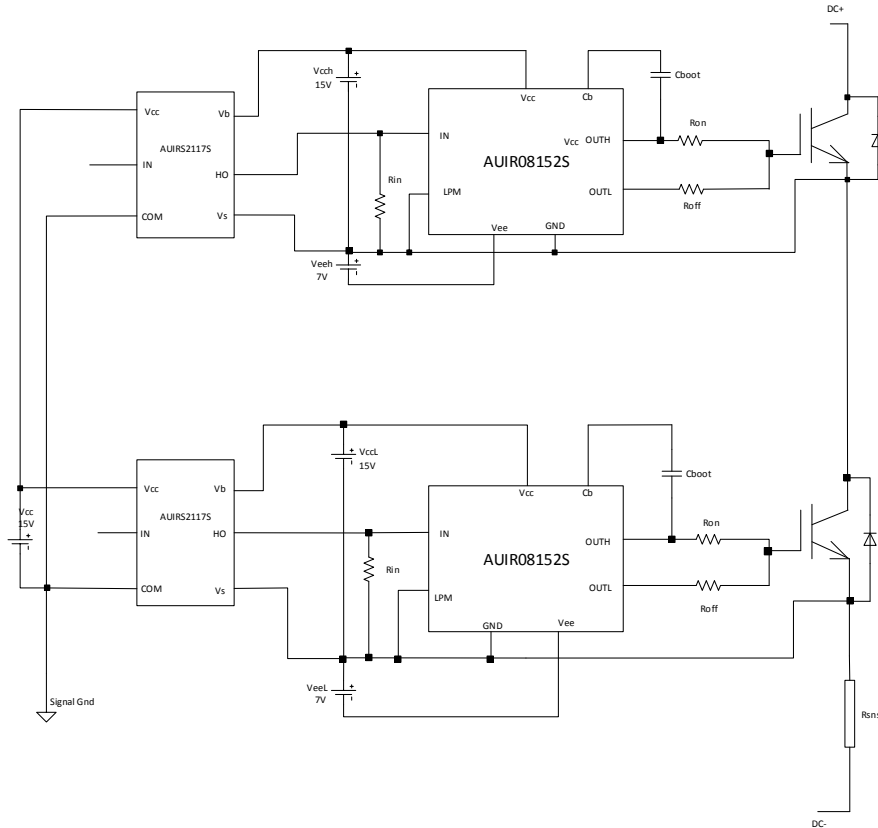


Figure A-3

## Examples of system schematics with Opto

The example in Figure A-4 is, again, a leg gate driver where the AUIR08152 are driven by optocouplers. The optocoupler only needs to drive a logic signal (the input of the buffer) so there is no need for high current capability. Its speed mostly depends upon system switching frequency and control aspects. The propagation delays and rise and fall times of the opto's stage must preferably be well below the buffer IC ones, to avoid introducing further delays which affect both the system control loop stability and the modulation depth. Figure A-4 shows the schematic of one of the leg sections ( high or low ) while Figure A-5 shows the layout.

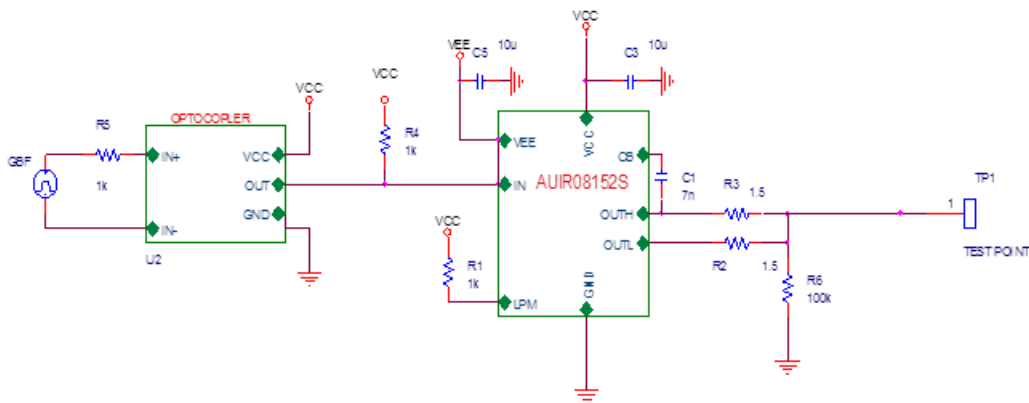


Figure A-4

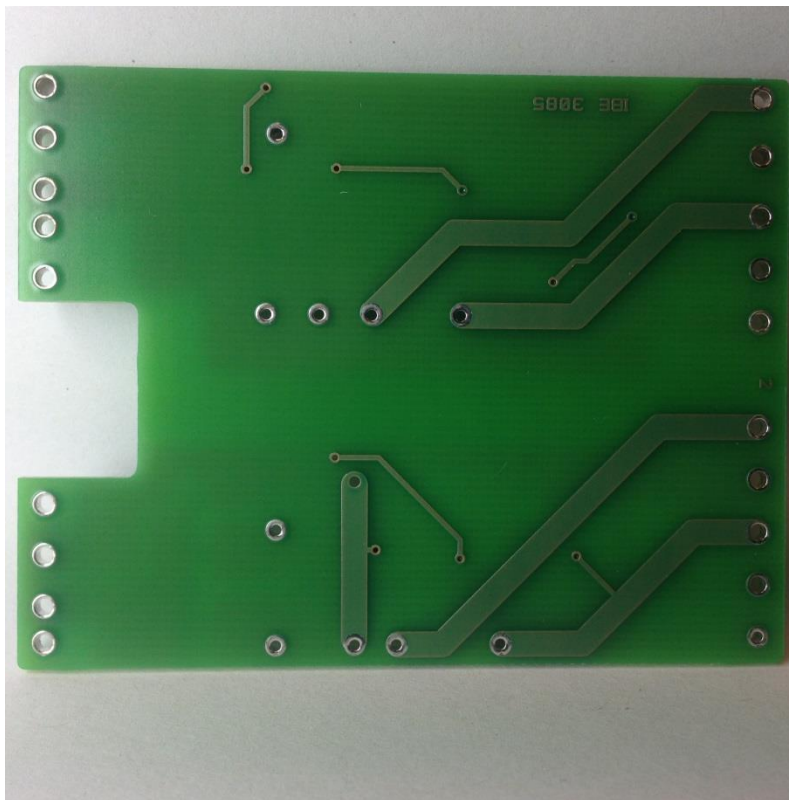


Figure A-5

## General Application Hints

### IN & LPM interface

IN and LPM have a current capability of 10mA max (source and sink); these limits only apply in case the stage driving these signals may go above  $V_{cc}$  or below  $V_{cc}-40V$ .

In the majority of cases, when the driving stage is only an open collector, referenced at GND or  $-V_{ee}$ , when looking at the functional block diagram, it appears the internal comparators have 6V zener clamp diodes, whose current is limited to much lower current by internal limiting resistors. These currents are  $I_{IN15}$  and  $I_{LPM15}$  and are reported in the static electrical characteristics for  $V_{cc}=15V$  and IN and LPM being pulled down at GND level.

In any case, when driving IN and LPM via open collector outputs, a pull-up resistor is needed, to guarantee clean rise times (fall time are uniquely determined by the speed the open collectors turns-on).

Rise time is determined by the pull-up resistor and the equivalent pin capacitance to  $V_{cc}$ . Typically few hundred Ohm to few kOhm are placed here.

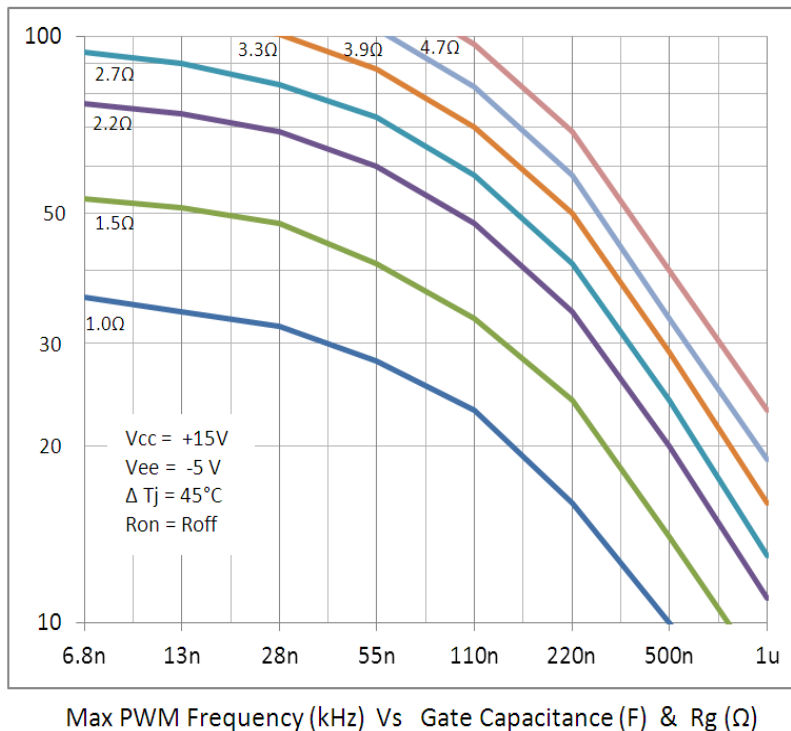
If a push pull, and not an open collector, stage is used to drive IN and LPM, no pull-up resistor is needed but pay attention the push pull stage is fed between  $V_{cc}$  and GND or  $V_{cc}$  and  $-V_{ee}$ .

A pull down resistor (few hundred kOhm) is suggested instead, especially if long traces or cables connect the predriver to the buffer IC.

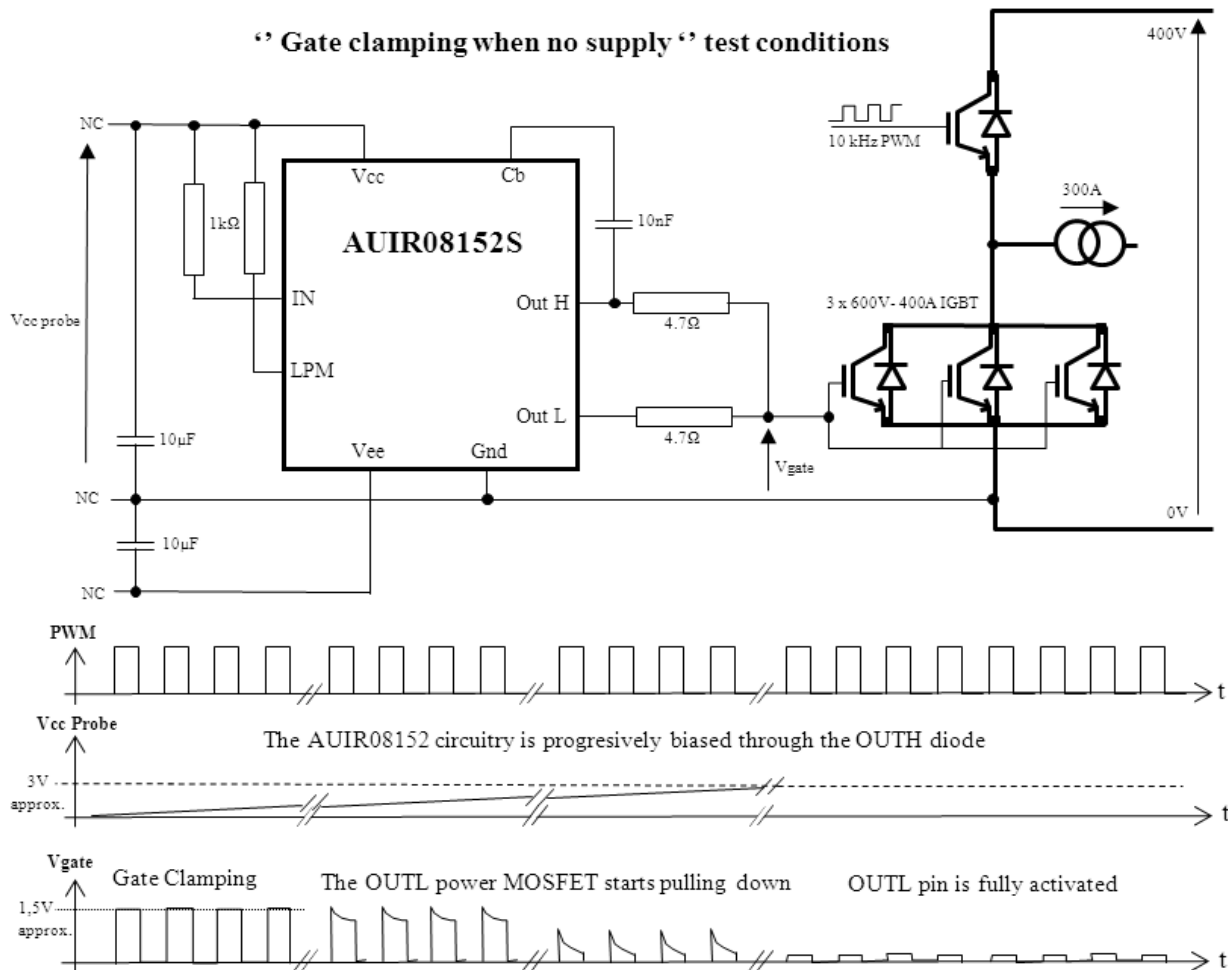
### IC power dissipation

This figure is mostly related to the switching frequency, the value of external gate resistances, and the equivalent load capacitance (the IGBT gate  $C_{iss}$ ).

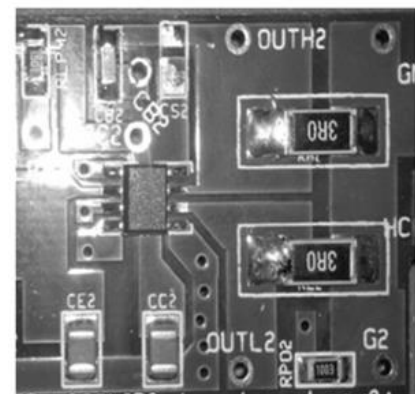
A complete characterization of the IC capabilities is given in figure 6, and shown here again for sake of clarity.



The AUIR08152S features a self-clamping gate protection in case of the auxiliary power supply disappears. A resistor is pulling up the gate of the OUTL internal power MOSFET to keep OutL pulled down until a minimum Vcc is applied, when Vcc disappears (< about 3V) then the Vgate is clamped via the OUTH ESD diode. In this situation forcing OutL high injects current into the pin that charges the Vcc decoupling capacitor and reactivates the internal OUTL output power MOSFET (for more info see the Functional Block Diagram).



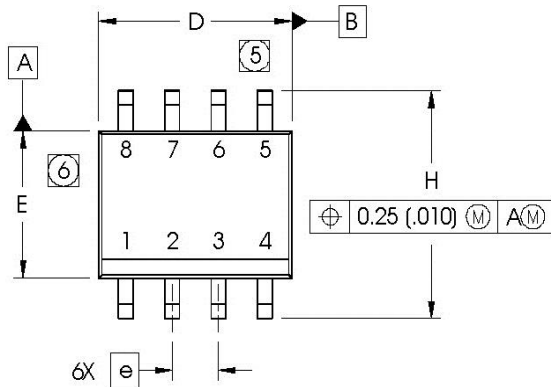
- a) If no negative bias is used, Vee shall be connected to Gnd
- b) OUTH and OUTL pins shall never be shorted together
- c) Decoupling capacitors shall be ceramic types and implemented as close as possible of the AUIR08152S supply pins
- d) The decoupling capacitors shall be at least 40 times bigger than the max. Cloud and of low ESR type, in order to avoid any Vccuv oscillations
- e) IN and LPM pins must never be left open



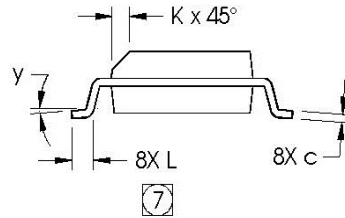
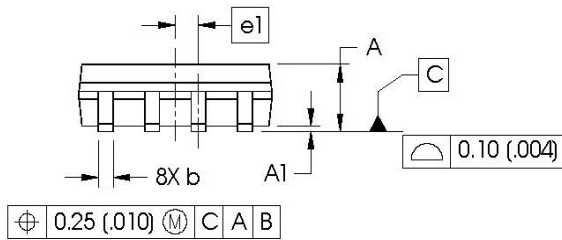
PCB Layout Example

**Case Outline – SO8**

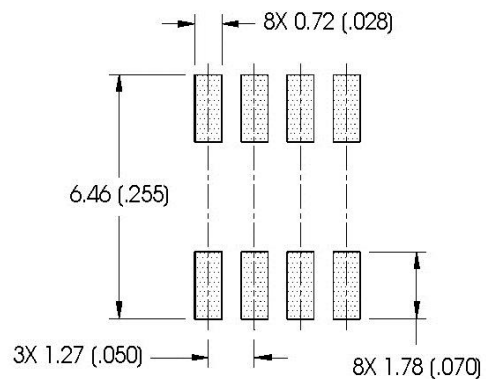
Dimensions are shown in millimeters (inches)



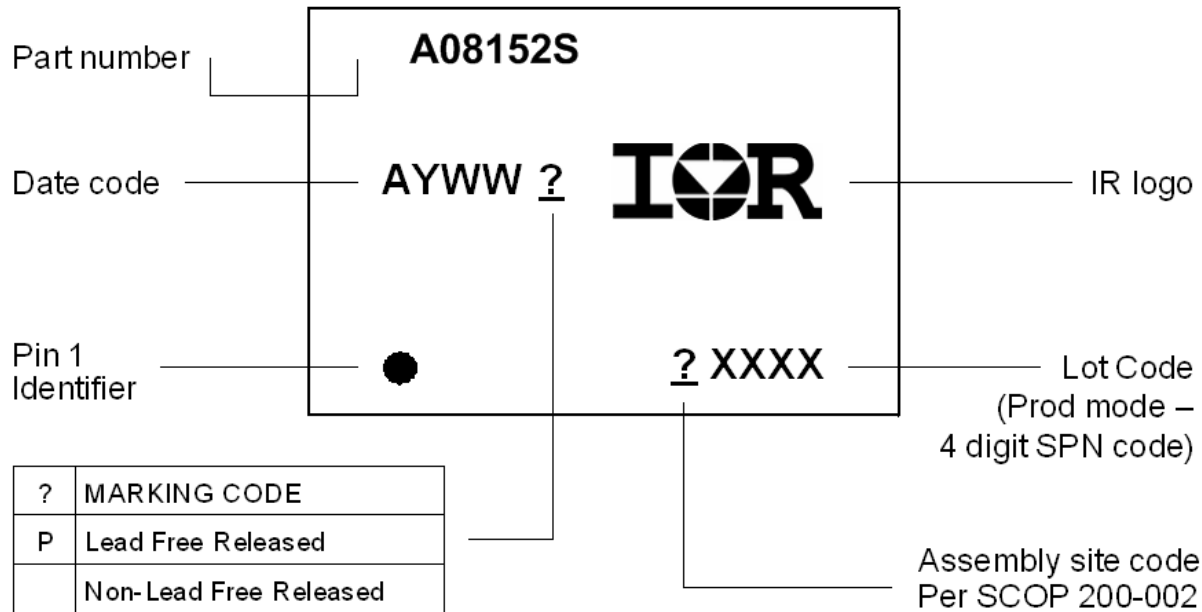
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
γ	0°	8°	0°	8°


**NOTES:**

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

**FOOTPRINT**




**Part Marking Information**

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>		Automotive (per AEC-Q100)	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		SOIC8N	MSL2 <sup>††</sup> 260°C (per IPC/JEDEC J-STD-020)
<b>ESD</b>	Machine Model	Class M2 (+/-200V) (per AEC-Q100-003)	
	Human Body Model	Class H2 (+/-2500V) (per AEC-Q100-002)	
	Charged Device Model	Class C4 (Pass +/-1000V) (per AEC-Q100-011)	
<b>IC Latch-Up Test</b>		Class II, Level A (per AEC-Q100-004)	
<b>RoHS Compliant</b>		Yes	

<sup>†</sup> Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>
<sup>††</sup> Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.



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