TDA 5221

ASK/FSK Single Conversion Receiver

Version 1.1

Wireless Control
Components

Infineon technologies

Never stop thinking.

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Page	Subjects (major changes since last revision)

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1 Product Description

1.1 Overview

The IC is a very low power consumption single chip FSK/ASK Superheterodyne Receiver (SHR) for the frequency band 300 to 340 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a PLL FSK demodulator, a data filter, an advanced data comparator (slicer) with selection between two threshold modes and a peak detector. Additionally there is a power down feature to save current and extend battery life, and two selectable alternatives of generating the data slicer threshold.

1.2 Features

- Low supply current (Is = 6.4 mA typ. in FSK mode, Is = 5.6 mA typ. in ASK mode)
- Supply voltage range 5V ±10%
- Power down mode with very low supply current (50nA typ.)
- FSK and ASK demodulation capability
- Fully integrated VCO and PLL Synthesiser
- ASK sensitivity better than -110 dBm over specified temperature range (- 40 to +105°C)
- Selectable frequency ranges 300-320 MHz and 320-340 MHz
- Switchable between two different frequency channels (see **Section 2.4.3**)
- Limiter with RSSI generation, operating at 10.7MHz
- 2nd order low pass data filter with external capacitors
- Data slicer with selection between two threshold modes (see **Section 2.4.8**)
- FSK sensitivity better than -102 dBm over specified temperature range (- 40 to +105°C)

1.3 Application

- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Low Bitrate Communication Systems

2 Functional Description

2.1 Pin Configuration

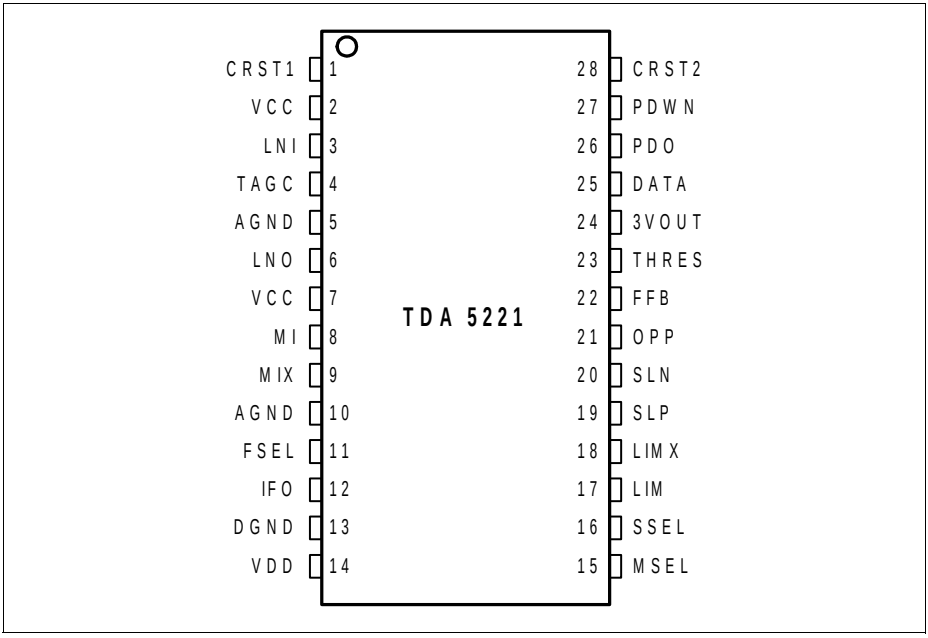
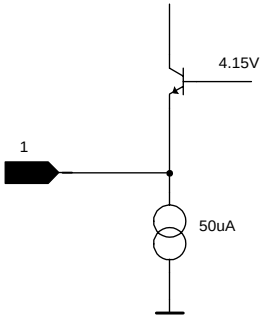
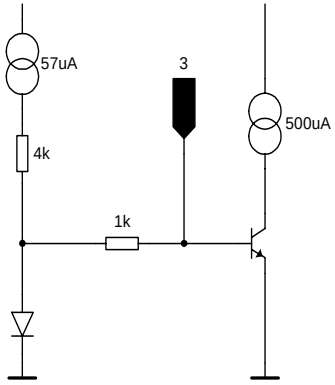
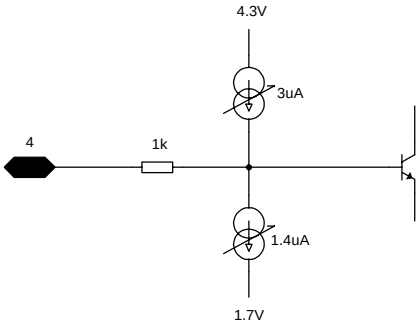
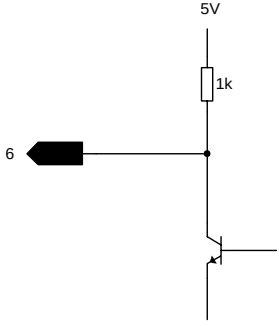


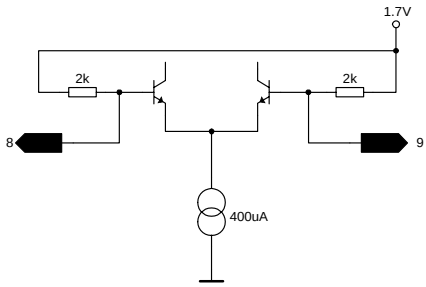
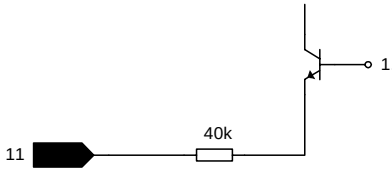
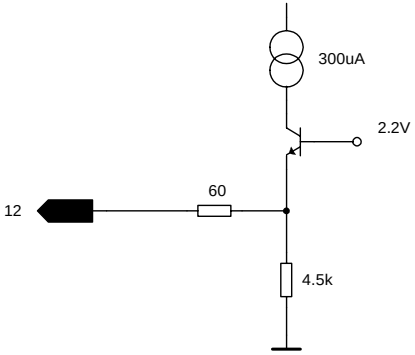
Figure 1 Pin Configuration

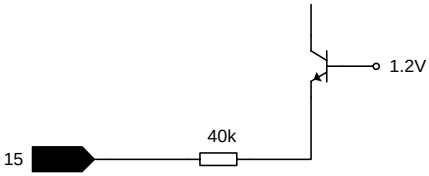
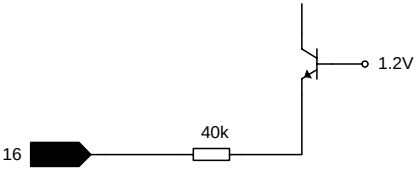
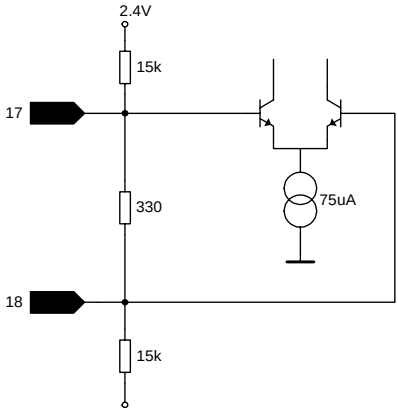
2.2 Pin Definition and Functions

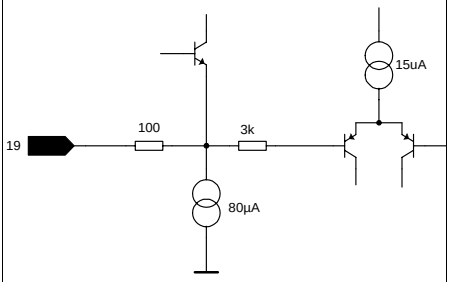
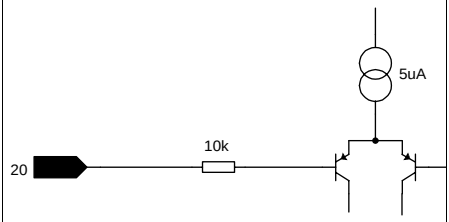
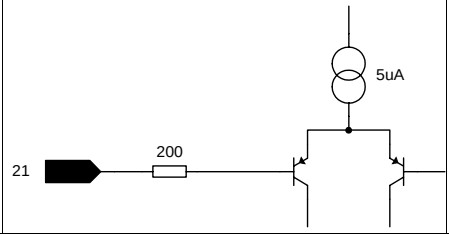
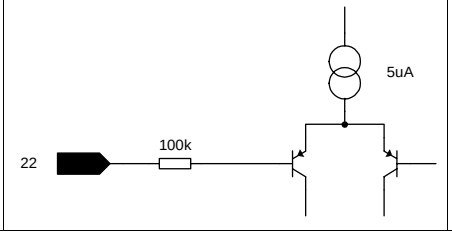
Table 1 Pin Defintion and Function

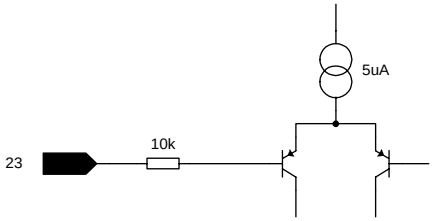
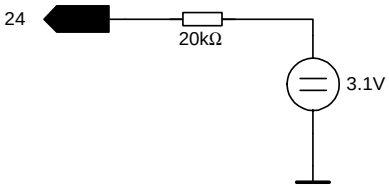
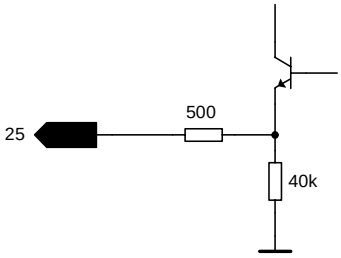
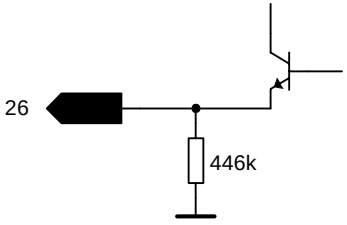
Pin No.	Symbol	Equivalent I/O Schematic	Function
1	CRST1		External Crystal Connector 1
2	VCC		5V Supply
3	LNI		LNA Input

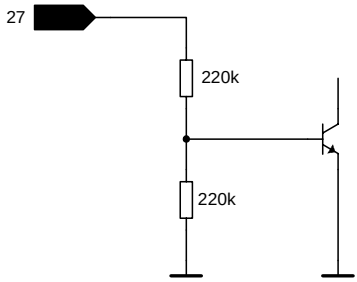
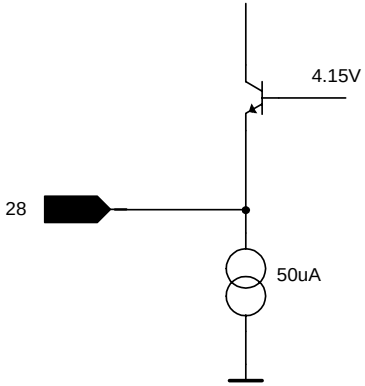
Pin No.	Symbol	Equivalent I/O Schematic	Function
4	TAGC		AGC Time Constant Control
5	AGND		Analogue Ground Return
6	LNO		LNA Output
7	VCC		5V Supply

Pin No.	Symbol	Equivalent I/O Schematic	Function
8	MI		Mixer Input
9	MIX		Complementary Mixer Input
10	AGND		Analogue Ground Return
11	FSEL		Frequency Selector
12	IFO		10.7 MHz IF Mixer Output
13	DGND		Digital Ground Return

Pin No.	Symbol	Equivalent I/O Schematic	Function
14	VDD		5V Supply (PLL Counter Circuity)
15	MSEL		ASK/FSK Modulation Format Sector
16	SSEL		Data Slicer Reference Level Sector
17 18	LIM LIMX		Limiter Input Complementary Limiter Input

Pin No.	Symbol	Equivalent I/O Schematic	Function
19	SLP		Data Slicer Positive Input
20	SLN		Data Slicer Negative Input
21	OPP		OpAmp Noninverting Input
22	FFB		Data Filter Feedback Pin

Pin No.	Symbol	Equivalent I/O Schematic	Function
23	THRES		AGC Threshold Input
24	3VOUT		3V Reference Output
25	DATA		Data Output
26	PDO		Peak Detector Output

Pin No.	Symbol	Equivalent I/O Schematic	Function
27	PDWN		Power Down Input
28	CRST2		External Crystal Connector 2

2.3 Functional Block Diagram

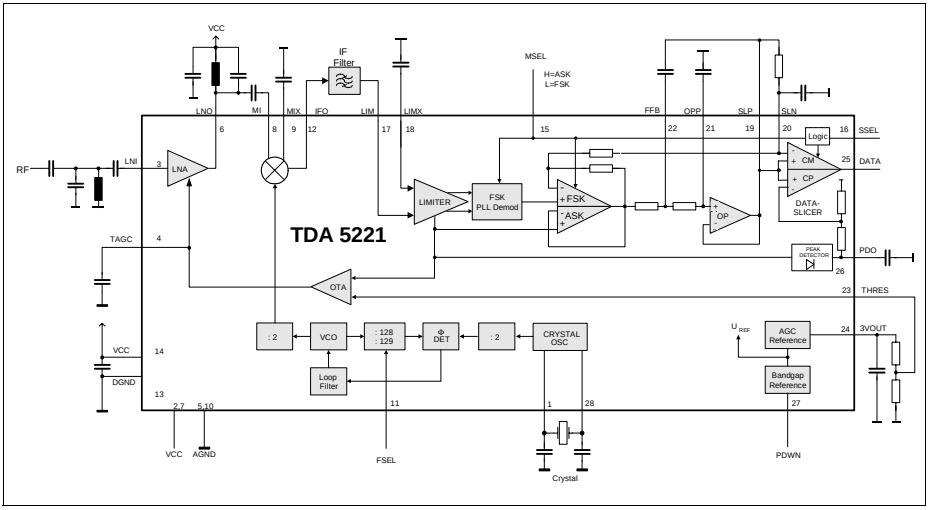


Figure 2 Block Diagram

2.4 Functional Block Description

2.4.1 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 to 20dB. The gain figure is determined by the external matching networks situated ahead of LNA and between the LNA output **LNO** (Pin 6) and the Mixer Inputs **MI** and **MIX** (Pins 8 and 9). The noise figure of the LNA is approximately 3dB, the current consumption is 500µA. The gain can be reduced by approximately 18dB. The switching point of this AGC action can be determined externally by applying a threshold voltage at the **THRES** pin (Pin 23). This voltage is compared internally with the received signal (RSSI) level generated by the limiter circuitry. In case that the RSSI level is higher than the threshold voltage the LNA gain is reduced and vice versa. The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin as described in Section 3.1. The time constant of the AGC action can be determined by connecting a capacitor to the **TAGC** pin (Pin 4) and should be chosen along with the appropriate threshold voltage according to the intended operating case and interference scenario to be expected during operation. The optimum choice of AGC time constant and the threshold voltage is described in Section 3.1.

2.4.2 Mixer

The Double Balanced Mixer downconverts the input frequency (RF) in the range of 310-350MHz to the intermediate frequency (IF) at 10.7MHz with a vol-tage gain of approximately 21dB by utilising either high- or low-side injection of the local oscillator signal. In case the mixer is interfaced only single-ended, the unused mixer input has to be tied to ground via a capacitor. The mixer is followed by a low pass filter with a corner frequency of 20MHz in order to suppress RF signals to appear at the IF output (**IFO** pin). The IF output is internally consisting of an emitter follower that has a source impedance of approximately 330Ω to facilitate interfacing the pin directly to a standard 10.7MHz ceramic filter without additional matching circuitry.

2.4.3 PLL Synthesizer

The Phase Locked Loop synthesizer consists of a VCO, an asynchronous divider chain, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCO is including spiral inductors and varactor diodes. The tuning range of the VCO was designed to guarantee over production spread and the specified temperature range a receive frequency range between 300 and 340 MHz depending on whether high- or low-side injection of the local oscillator is used. The oscillator signal is fed both to the synthesiser divider chain and to a divider that is dividing the signal by 2 before it is applied to the downconverting mixer. Local oscillator high side injection has to be used for receive frequencies between approximately 300 and 320 MHz, low side injection for receive frequencies between 320 and 340MHz - see also Section 3.4. To be able to switch between two different frequency channels a divider ratio of either 32 or 32.25 can be selected via the FSEL-Pin.

Table 2 Dependence of PLL overall division ratio on FSEL

FSEL	Ratio $r=(f_{L0}/f_{QU})$
Open	32
GND	32.25

2.4.4 Crystal Oscillator

The calculation of the value of the necessary crystal load capacitance is shown in Section 3.3, the crystal frequency calculation is explained in Section 3.4.

2.4.5 Limiter

The Limiter is an AC coupled multistage amplifier with a cumulative gain of approximately 80 dB that has a bandpass-characteristic centred around 10.7 MHz. It has a typical input impedance of 330 Ω to allow for easy interfacing to a 10.7 MHz ceramic IF filter. The limiter circuit also acts as a Receive Signal Strength Indicator

(RSSI) generator which produces a DC voltage that is directly proportional to the input signal level as can be seen in Figure 4. This signal is used to demodulate ASK-modulated receive signals in the subsequent baseband circuitry. The RSSI output is applied to the modulation format switch, to the Peak Detector input and to the AGC circuitry.

In order to demodulate ASK signals the MSEL pin has to be in its ‘High‘-state as described in the next chapter.

2.4.6 FSK Demodulator

To demodulate frequency shift keyed (FSK) signals a PLL circuit is used that is contained fully on chip. The Limiter output differential signal is fed to the linear phase detector as is the output of the 10.7 MHz center frequency VCO. The demodulator gain is typically 200µV/kHz. The passive loop filter output that is comprised fully on chip is fed to both the VCO and the modulation format switch described in more detail below. This signal is representing the demodulated signal with low frequencies applied to the demodulator demodulated to logic ones and high frequencies demodulated to logic zeroes. However this is only valid in case the local oscillator is low-side injected to the mixer which is applicable to receive frequencies above 320MHz. In case of receive frequencies below 320MHz (e.g.315MHz) high frequencies are demodulated as logical ones due to a sign inversion in the downconversion mixing process. See also Section 3.4.

The modulation format switch is actually a switchable amplifier with an AC gain of 11 that is controlled by the **MSEL** pin (Pin 15) as shown in the following table. This gain was chosen to facilitate detection in the subsequent circuits. The DC gain is 1 in order not to saturate the subsequent Data Filter wih the DC offset produced by the demodulator in case of large frequency offsets of the IF signal. The resulting frequency characteristic and details on the principle of operation of the switch are described in Section 3.6.

Table 3 MSEL Pin Operating States

MSEL	Modulation Format
Open	ASK
Shorted to ground	FSK

The demodulator circuit is switched off in case of reception of ASK signals.

2.4.7 Data Filter

The data filter comprises an OP-Amp with a bandwidth of 100kHz used as a voltage follower and two 100kΩ on-chip resistors. Along with two external capacitors a 2nd order

Sallen-Key low pass filter is formed. The selection of the capacitor values is described in Section 3.2.

2.4.8 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100 kHz. This allows for a maximum receive data rate of up to 100kBaud. The maximum achievable data rate also depends on the IF Filter bandwidth and the local oscillator tolerance values. Both inputs are accessible. The output delivers a digital data signal (CMOS-like levels) for subsequent circuits. A self-adjusting slicer-threshold on pin 20 its generated by a RC-term. In ASK-mode alternatively a scaled value of the voltage at the PDO-output (approx. 87%) can be used as the slicer-threshold as shown in Table 4. The data slicer threshold generation alternatives are described in more detail in Section 3.5.

Table 4 SSEL Pin Operating States

SSEL	MSEL	Selected Slicing Level (SL)
X	Low	external SL on Pin 20 (RC-term, e.g.)
High	High	external SL on Pin 20 (RC-term, e.g.)
Low	High	87% of PDO-output (approx.)

2.4.9 Peak Detector

The peak detector generates a DC voltage which is proportional to the peak value of the receive data signal. A capacitor is necessary. The input is connected to the output of the RSSI-output of the Limiter, the output is connected to the **PDO** pin (Pin 26). This output can be used as an indicator for the received signal strength to use in wake-up circuits and as a reference for the data slicer in ASK mode. Note that the RSSI level is also output in case of FSK mode.

2.4.10 Bandgap Reference Circuitry

A Bandgap Reference Circuit provides a temperature stable reference voltage for the device. A power down mode is available to switch off all subcircuits which is controlled by the PWDN pin (Pin 27) as shown in the following table. The supply current drawn in this case is typically 50nA.

Table 5 PDWN Pin Operating States

PDWN	Operating State
Open or tied to ground	Powerdown Mode
Tied to Vs	Receiver On

3 Applications

3.1 Application Circuit

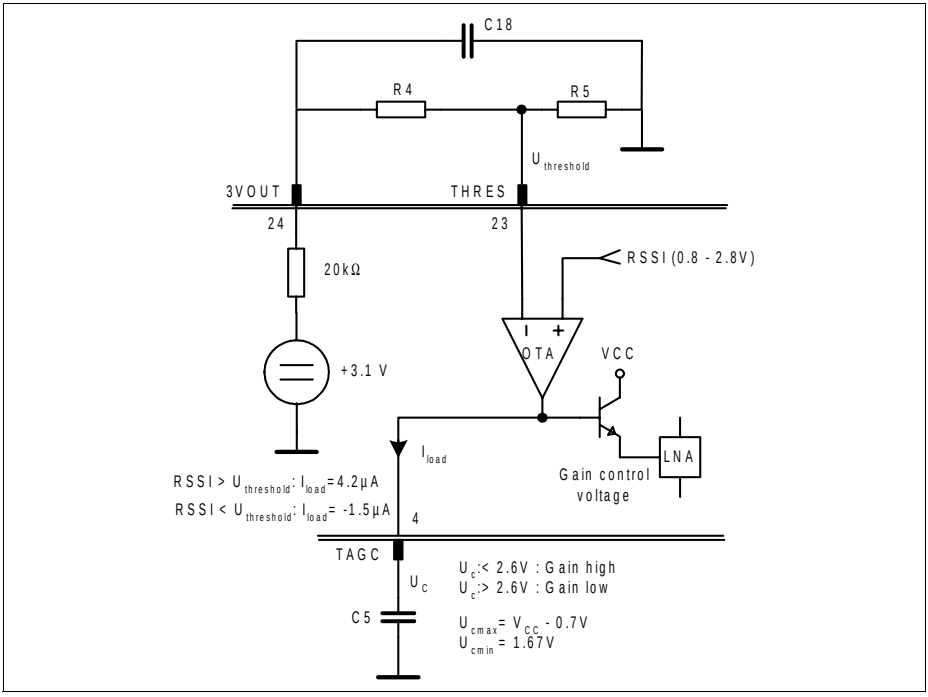


Figure 3 LNA Automatic Gain Control Circuity

The LNA automatic gain control circuitry consists of an operational transimpedance amplifier that is used to compare the received signal strength signal (RSSI) generated by the Limiter with an externally provided threshold voltage U_{thres}. As shown in the following figure the threshold voltage can have any value between approximately 0.8 and 2.8V to provide a switching point within the receive signal dynamic range.

This voltage U_{thres} is applied to the **THRES** pin (Pin 23) The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin
(Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin. If the RSSI level generated by the Limiter is higher than U_{thres}, the OTA generates a positive current I_{load}. This yields a voltage rise on the **TAGC** pin (Pin 4). Otherwise, the OTA generates a negative current. These currents do not have the same values in order to achieve a fast-attack and slow-release action of the

AGC and are used to charge an external capacitor which finally generates the LNA gain control voltage.

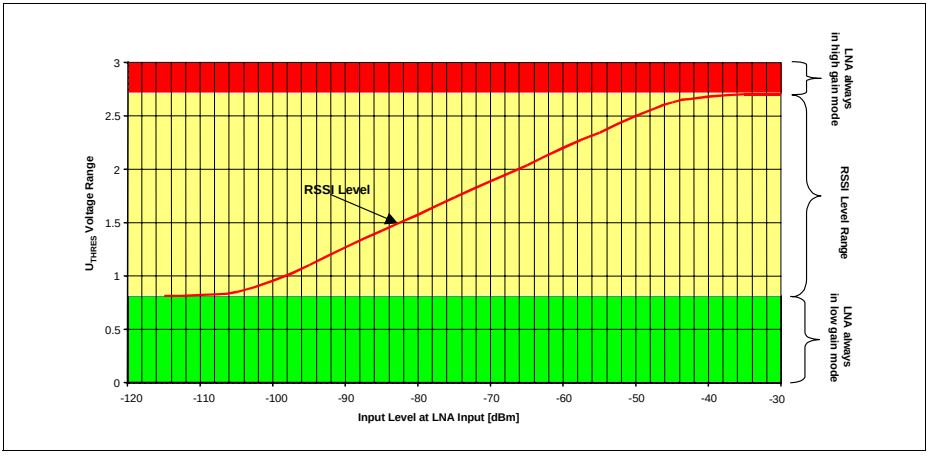


Figure 4 RSSI Level and Permissive AGC Threshold Levels

The switching point should be chosen according to the intended operating scenario. The determination of the optimum point is described in the accompanying Application Note, a threshold voltage level of 1.8V is apparently a viable choice. It should be noted that the output of the **3VOUT** pin is capable of driving up to 50µA, but that the **THRES** pin input current is only in the region of 40nA. As the current drawn out of the **3VOUT** pin is directly related to the receiver power consumption, the power divider resistors should have high impedance values. The sum of R1 and R2 has to be 600kΩ in order to yield 3V at the **3VOUT** pin. R1 can thus be chosen as 240kΩ, R2 as 360kΩ to yield an overall **3VOUT** output current of 5µA[1)] and a threshold voltage of 1.8V

Note: If the LNA gain shall be kept in either high or low gain mode this has to be accomplished by tying the **THRES** pin to a fixed voltage. In order to achieve high gain mode operation, a voltage higher than 2.8V shall be applied to the **THRES** pin, such as a short to the **3VOLT** pin. In order to achieve low gain mode operation **THRES** has to be connected to GND.

As stated above the capacitor connected to the **TAGC** pin is generating the gain control voltage of the LNA due to the charging and discharging currents of the OTA and thus is also responsible for the AGC time constant. As the charging and discharging currents are not equal two different time constants will result. The time constant corresponding to the charging process of the capacitor shall be chosen according to the data rate. According to measurements performed at Infineon the capacitor value should be greater than 47nF.

1) note the 20kΩ resistor in series with the 3.1V internal voltage source

3.2 Data Filter Design

Utilising the on-board voltage follower and the two 100kΩ on-chip resistors a 2nd order Sallen-Key low pass data filter can be constructed by adding 2 external capacitors between pins 19 (SLP) and 22 (FFB) and to pin 21 (OPP) as depicted in the following figure and described in the following formulas[1)].

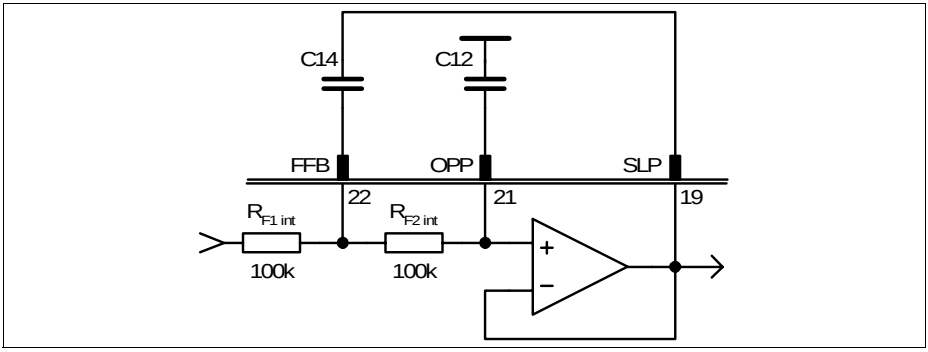


Figure 5 Data Filter Design

with $R_{F1int}=R_{F2int}=R$

$$C14=\frac{2Q\sqrt{b}}{R2\pi f_{3dB}} \quad C12=\frac{\sqrt{b}}{4QR\pi f_{3dB}}$$

with

$$Q=\frac{\sqrt{b}}{a}$$

Q is the qualify factor of the poles where, in case of a Bessel filter a=1.3617, b=0.618 and thus Q=0.577

and in case of a Butter worth filter a=1.414, b=1
and thus Q=0.71

Example: Butter worth filter with f_{3dB}=5kHz and R=100kΩ:
C14=450pF, C12=225pF

1) taken from Tietze/Schenk: Halbleiterschaltungstechnik, Springer Berlin, 1999

3.3 Crystal Load Capacitance Calculation

The value of the capacitor necessary to achieve that the crystal oscillator is operating at the intended frequency is determined by the reactive part of the negative resistance of the oscillator circuit as shown in Section 4.1.3 and by the crystal specifications given by the crystal manufacturer.

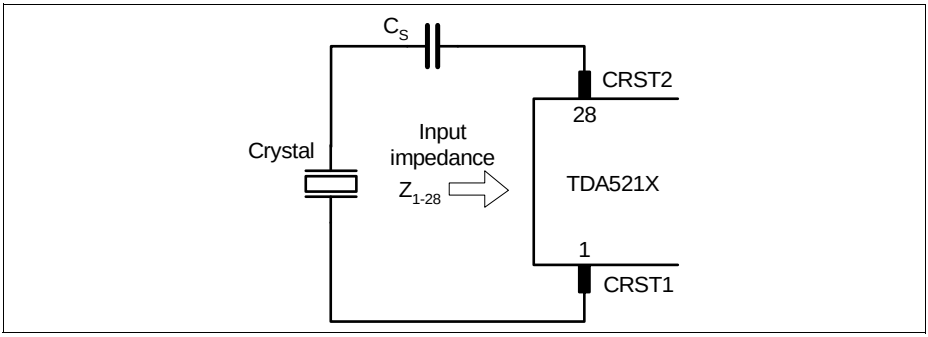


Figure 6 Determination of Series Capacitance Vale for the Quartz Oscillator

The required series capacitor for a crystal with specified load capacitance C_L can be calculated as

$$C_S = \frac{1}{\frac{1}{C_L} + 2\pi f X_L}$$

C_L is the nominal load capacitance specified by the crystal manufacturer.

Example:

10.18 MHz: C_L = 12 pF X_L=870 Ω C_S = 7.2 pF

This value may be obtained by putting two capacitors in series to the crystal, such as 18pF and 12pF in the 10.2MHz case.

But please note that the calculated C_S-value includes all parasitic.

3.4 Crystal Frequency Calculation

As described in Section 2.4.3 the operating range of the on-chip VCO is wide enough to guarantee a receive frequency range between 300 and 340MHz. The VCO signal is divided by 2 before applied to the mixer . This local oscillator signal can be used to downconvert the RF signals both with high- or low-side injection at the mixer. High-side

injection of the local oscillator has to be used for receive frequencies between 300 and 320 MHz. In this case the local oscillator frequency is calculated by adding the IF frequency (10.7 MHz) to the RF frequency. In this case the higher frequency of a FSK-modulated signal is demodulated as a logical one (high).

Low-side injection has to be used for receive frequencies between 320 and 340 MHz. The local oscillator frequency is calculated by subtracting the IF frequency (10.7 MHz) from the RF frequency then. Please note that in this case sign-inversion occurs and the higher frequency of a FSK-modulated signal is demodulated as a logical zero (low). The overall division ratios in the PLL are 32 or 32.25 depending on whether the FSEL-pin is left open or tied to ground.

Therefore the crystal frequency may be calculated by using the following formula:

$$f_{QU} = \frac{f_{RF} \pm 10.7}{r}$$

with f_{RF} receive frequency

f_{LO} local oscillator (PLL) frequency ($f_{RF} \pm 10.7$)

f_{QU} quartz crystal oscillator frequency

r ratio of local oscillator (PLL) frequency and crystal frequency as shown in the subsequent table

Table 6 Dependence of PLL Overall Division Ratio on FSEL

FSEL	Ratio $r=(f_{LO}/f_{QU})$
open	32
GND	32.25

This yields the following examples:

FSEL is „Low“:

$$f_{QU} = \frac{318.55\,MHz + 10.7\,MHz}{32.25} = 10.209375\ MHz$$

FSEL is „High“:

$$f_{QU} = \frac{316\ MHz + 10.7\,MHz}{32} = 10.209375\ MHz$$

3.5 Data Slicer Threshold Generation

The threshold of the data slicer can be generated using an external R-C integrator as shown in Figure 7.

The time constant T_A of this circuit including also the internal resistors R_{F3int} and R_{F4int} (see Figure 9) has to be significantly larger than the longest period of no signal change T_L within the data sequence.

In order to keep distortion low, the minimum value for R is 20kΩ.

T_A has to be calculated as

$$T_A = \frac{R1 \cdot (R_{F3int} + R_{F4int})}{R1 + R_{F3int} + R_{F4int}} \cdot C13 \quad = R1 II (R_{F3int} + R_{F4int}) \cdot C13 \quad \ldots for\ ASK$$

and

$$T_A = \frac{R1 \cdot R_{F4int}}{R1 + R_{F3int} + R_{F4int}} \cdot C13 \quad = \frac{R1 II (R_{F3int} + R_{F4int})}{v} \cdot C13 \quad \ldots for\ FSK$$

R1, $R_{F3\ int}$, $R_{F4\ int}$ and C13 see also Figure 7 and .Figure 9

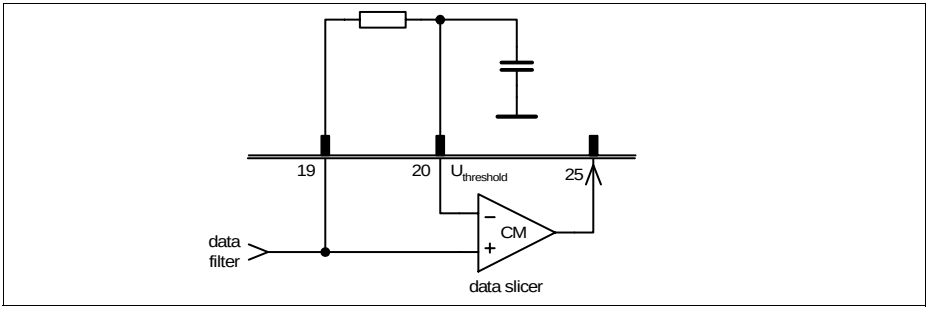


Figure 7 Data Slicer Threshold Generation with External R-C Integrator

In case of ASK operation another possibility for threshold generation is to use the peak detector in connection with an internal resistive divider and one capacitor as shown in the following Figure 8. For selecting the peak detector as reference for the slicing level a logic low as to be applied on the SSEL pin.

In case of MSEL is high (or open), which means that ASK-Mode is selected, a logic low on the SSEL pin yields a logic high on the AND-output and thus the peak-detector is selected (see Figure 9).

In case of FSK the MSEL-pin and furthermore the one input of the AND-gate is low, so the peak detector can not be selected.

The capacitor value is depending on the coding scheme and the protocol used.

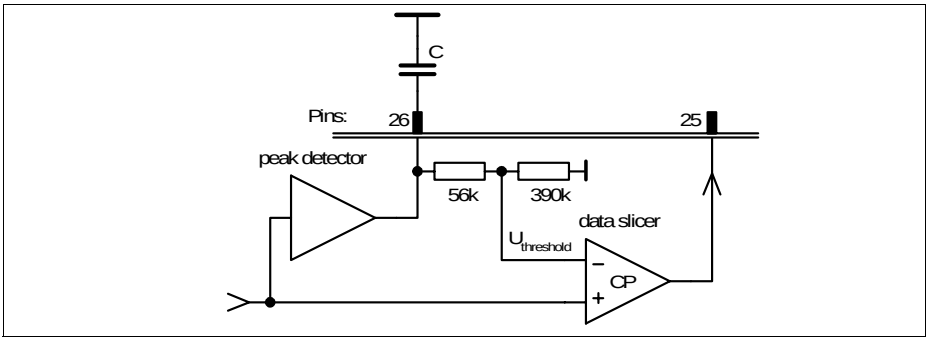


Figure 8 Data Slicer Threshold Generation Utilising the Peak Detector

3.6 ASK/FSK-Data Path Functional Description

The TDA5221 is containing an ASK/FSK switch which can be controlled via Pin 15 (MSEL). This switch is actually consisting of 2 operational amplifiers that are having a gain of 1 in case of the ASK amplifier and a gain of 11 in case of the FSK amplifier in order to achieve an appropriate demodulation gain characteristic. In order to compensate for the DC-offset generated especially in case of the FSK PLL demodulator there is a feedback connection between the threshold voltage of the bit slicer comparator (Pin 20) to the negative input of the FSK switch amplifier.

In ASK-mode alternatively to the voltage at Pin 20 (SLN) a value of approx. 87% of the peak-detector output-voltage at Pin 26 (PDO) can be used as the slicer-reference level.

The slicing reference level is generated by an internal voltage divider (R_{T1int}, R_{T2int}), which is applied on the peak detector output.

The selection between these modes is controlled by Pin 16 (SSEL), as described in Section 3.5.

This is shown in the following Figure 9.

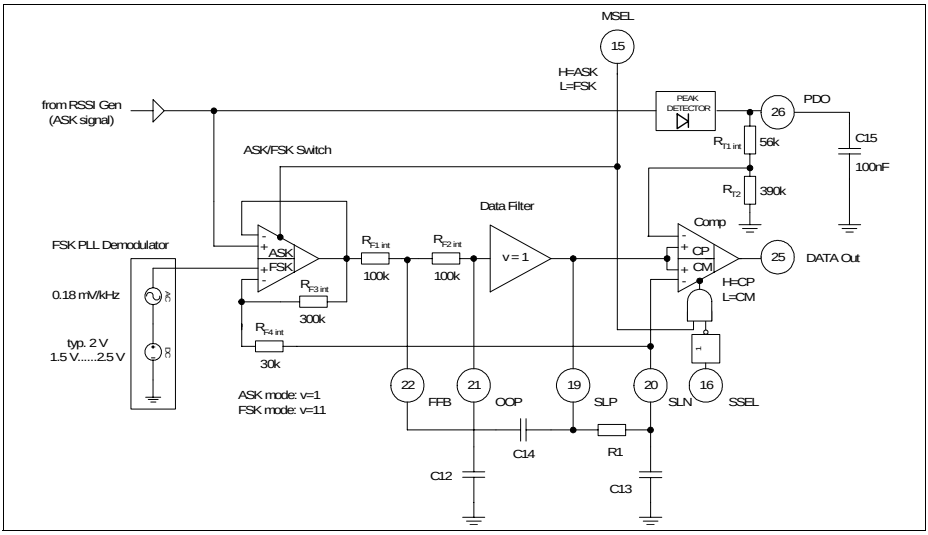


Figure 9 ASK/FSK mode datapath

3.7 FSK Mode

The FSK datapath has a bandpass characterisitc due to the feedback shown above (highpass) and the data filter (lowpass). The lower cutoff frequency f2 is determined by the external RC-combination. The upper cutoff frequency f3 is determined by the data filter bandwidth.

The demodulation gain of the FSK PLL demodulator is 200µV/kHz. This gain is increased by the gain v of the FSK switch, which is 11. Therefore the resulting dynamic gain of this circuit is 2.2mV/kHz within the bandpass. The gain for the DC content of FSK signal remains at 200µV/kHz. The cut-off frequencies of the bandpass have to be chosen such that the spectrum of the data signal is influenced in an acceptable amount.

In case that the user data is containing long sequences of logical zeroes the effect of the drift-off of the bit slicer threshold voltage can be lowered if the offset voltage inherent at the negative input of the slicer comparator (Pin20) is used. The comparator has no hysteresis built in.

This offset voltage is generated by the bias current of the negative input of the comparator (i.e. 20nA) running over the external resistor R. This voltage raises the voltage appearing at pin 20 (e.g. 1mV with R = 100kΩ). In order to obtain benefit of this

asymmetrical offset for the demodulation of long zeros the lower of the two FSK frequencies should be chosen in the transmitter as the zero-symbol frequency.

In the following figure the shape of the above mentioned bandpass is shown.

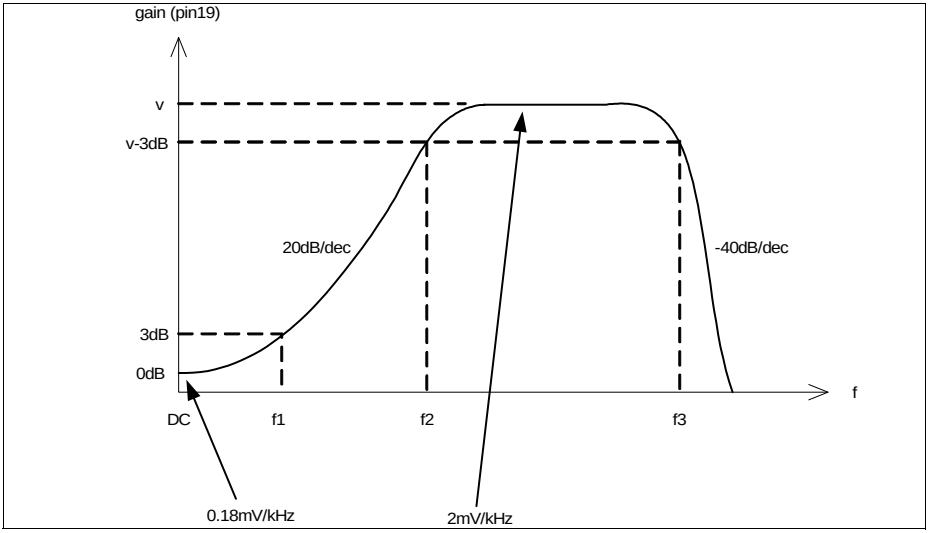


Figure 10 Frequency characteristic in case of FSK mode

The cutoff frequencies are calculated with the following formulas:

$$f_1 = \frac{1}{2\pi \frac{R1 \times 330k\Omega}{R1 + 330k\Omega} \times C13}$$

$$f_2 = v \times f_1 = 11 \times f_1$$

$$f_3 = f_{3dB}$$

f_3 is the 3dB cutoff frequency of the data filter - see Section 3.2.

Example:

R1 = 100kΩ, C13 = 47nF

This leads tof_1 = 44Hz and f_2 = 485Hz

3.8 ASK Mode

In case the receiver is operated in ASK mode the datapath frequency charactersitic is dominated by the data filter alone, thus it is lowpass shaped.The cutoff frequency is determined by the external capacitors C_{12} and C_{14} and the internal 100k resistors as described in Section 3.2

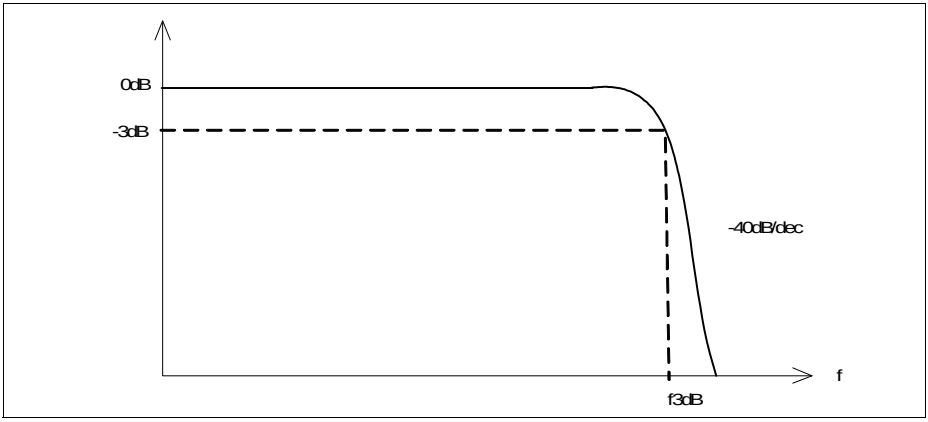


Figure 11 Frequency characteristic in case of ASK mode

3.9 Principle of the Precharge Circuit

In case the data slicer threshold shall be generated with an external RC network as described in Section 3.5 it is necessary to use large values for the capacitor C attached to the **SLN** pin (pin 20) in order to achieve long time constants. This results also from the fact that the choice of the value for R1 connected between the **SLP** and **SLN** pins (pins 19 and 20) is limited by the 330kΩ resistor appearing in parallel to R1 as can be seen in Figure 9. Apart from this a resistor value of 100kΩ leads to a voltage offset of 1mv at the comparator input. The resulting startup time constant τ_1 can be calculated with:

$$\tau_1 = \left(R1 \| 330k\Omega\right) \times C13$$

In case R1 is chosen to be 100kΩ and C13 is chosen as 47nF this leads to

$$\tau_1 = \left(100k\Omega \| 330k\Omega\right) \times 47nF = 77k\Omega \times 47nF = 3.6ms$$

When the device is turned on this time constant dominates the time necessary for the device to be able to demodulate data properly. In the powerdown mode the capacitor is only discharged by leakage currents.

In order to reduce the turn-on time in the presence of large values of C a precharge circuit was included in the TDA5221 as shown in the following figure.

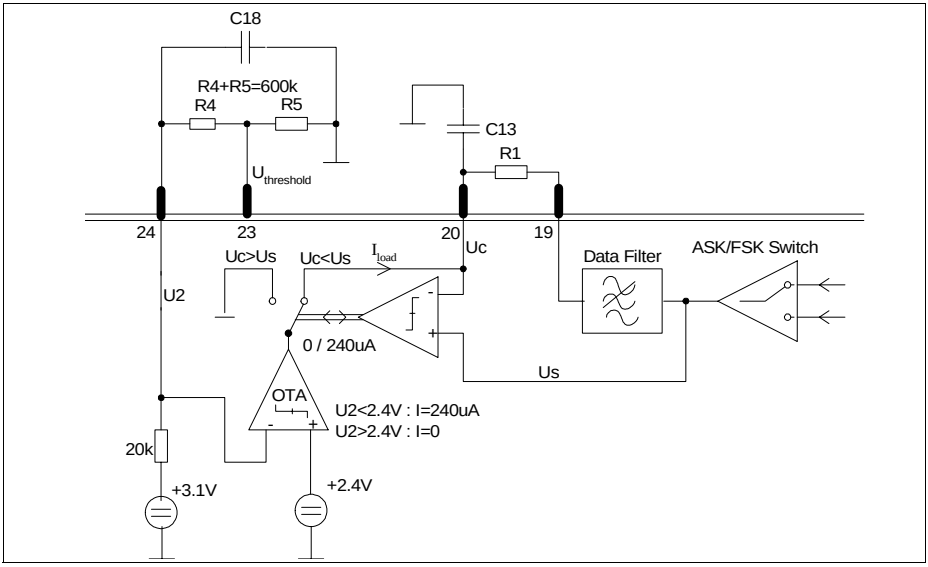


Figure 12 Principle of the precharge circuit

This circuit charges the capacitor C13 with an inrush current I_{load} of typically 220µA for a duration of T_2 until the voltage U_c appearing on the capacitor is equal to the voltage U_s at the input of the data filter. This voltage is limited to 2.5V. As soon as these voltages are equal or the duration T_2 is exceeded the precharge circuit is disabled.

τ_2 is the time constant of the charging process of C18 which can be calculated as

$$\tau_2 \approx 20k\Omega \times C2$$

as the sum of R4 and R5 is sufficiently large and thus can be neglected. T_2 can then be calculated according to the following formula:

$$T_2 = \tau_2 \ln\left(\frac{1}{1-\frac{2.4V}{3V}}\right) \approx \tau_2 \times 1.6$$

The voltage transient during the charging of C_2 is shown in the following figure:

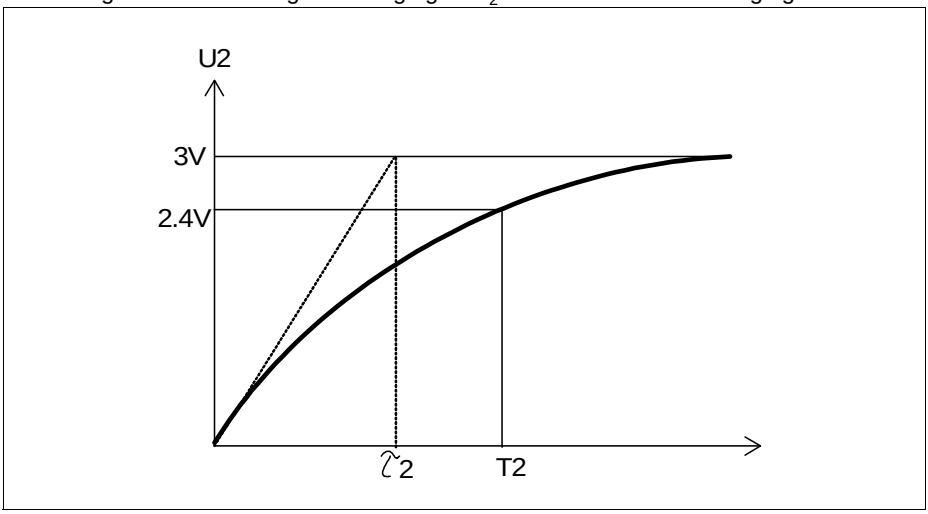


Figure 13 Voltage appearing on C18 during precharging process

The voltage appearing on the capacitor C13 connected to pin 20 is shown in the following figure. It can be seen that due to the fact that it is charged by a constant current source it exhibits is a linear increase in voltage which is limited to U_{Smax} = 2.5V which is also the approximate operating point of the data filter input. The time constant appearing in this case can be denoted as T_3, which can be calculated with:

$$T_3 = \frac{U_{S\max} \times C13}{220\mu A} = \frac{2.5V}{220\mu A} \times C13$$

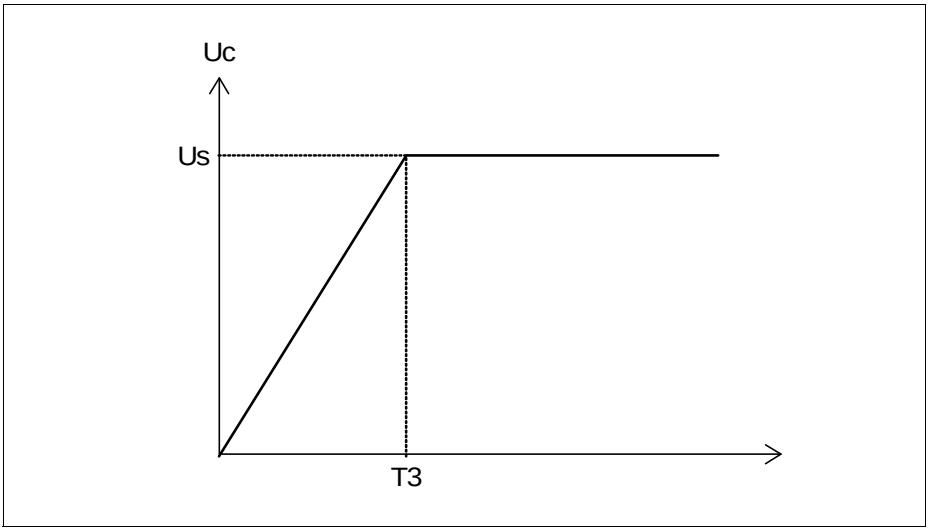


Figure 14 Voltage transient on capacitor C13 attached to pin 20

As an example the choice of C18 = 22nF and C13 = 47nF yields

τ_2 = 0.44ms

T_2 = 0.71ms

T_3 = 0.53ms

This means that in this case the inrush current could flow for a duration of 0.64ms but stops already after 0.49ms when the U_{Smax} limit has been reached. T_3 should always be chosen to be shorter than T_2.

It has to be noted finally that during the turn-on duration T_2 the overall device power consumption is increased by the 220µA needed to charge C13.

The precharge circuit may be disabled if C18 is not equipped. This yields a T_2 close to zero. Note that the sum of R_4 and R_5 has to be 600kΩ in order to produce 3V at the THRES pin as this voltage is internally used also as the reference for the FSK demodulator.

4 Reference

4.1 Electrical Data

4.1.1 Absolute Maximum Ratings

Attention: The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC may result. The AC/DC characteristic limits are not guaranteed.

Table 7 Absolute Maximum Ratings, T_{amb} = -40 °C … +105 °C

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
1	Supply Voltage	V_s	-0.3	5.5	V	
2	Junction Temperature	T_j	-40	+125	°C	
3	Storage Temperature	T_s	-40	+150	°C	
4	Thermal Resistance	R_{thJA}		114	K/W	
5	ESD integrity, all pins excl. Pins 1,3, 6, 28 ESD integrity Pins 1,3,6,28	V_{ESD}		+2 +1.5	kV kV	HBM according to MIL STD 883D, method 3015.7

4.1.2 Operating Range

Within the operational range the IC operates as explained in the circuit description. Currents flowing into the device are denoted as positive currents and vice versa. The device parameters marked with ■ are not part of the production test, but either verified by design or measured in the Infineon Evalboard as described in Section 4.2.

Supply voltage: VCC = 4.5V .. 5.5V

Table 8 Operating Range, T_{amb} = -40 °C … +105 °C

#	Parameter	Symbol	Limit Values		Unit	Test Conditions/ Notes	L
			min.	max.			
1	Supply Current	I_{SF} I_{SA}	4.1 3.5	8.1 7.3	mA mA		
2	Receiver Input Level ASK FSK, frequ. dev. ± 50kHz	RF_{in}	 -110 -102	 -13 -13	 dBm dBm		■
3	LNI Input Frequency	f_{RF}	300	340	MHz		

#	Parameter	Symbol	Limit Values		Unit	Test Conditions/ Notes	L
			min.	max.			
4	MI/X Input Frequency	f_{MI}	300	340	MHz		
5	3dB IF Frequency Range ASK FSK	$f_{IF\ -3dB}$	 5 10.4	 23 11	MHz		■
6	Powerdown Mode On	$PWDN_{ON}$	2	V_S	V		
7	Powerdown Mode Off	$PWDN_{OFF}$	0	0.8	V		
8	Gain Control Voltage, LNA high gain state	V_{THRES}	2.8	V_S	V		
9	Gain Control Voltage, LNA low gain state	V_{THRES}	0	0.7	V		

■ Not part of the production test - either verified by design or measured in an Infineon Evalboard described in Section 4.2.

4.1.3 AC/DC Characteristics at T_{AMB} = 25°C

AC/DC characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production. Currents flowing into the device are denoted as po-sitive currents and vice versa. The device performance parameters marked with ■ are not part of the production test, but either verified by design or measured in the Infineon Evalboard as described in Section 4.2.

Table 9 AC/DC Characteristics with T_A 25°C, V_{VCC}=4.5 ... 5.5 V

#	Parameter	Symbol	Limit Values			Unit	Test Conditions/ Notes	L
			min.	typ.	max.			
SUPPLY								
Supply Current								
1	Supply current, standby mode	$I_{S\ PDWN}$		50	100	nA	Pin 27 (PDWN) open or tied to 0 V	
2	Supply current, device operating in FSK mode	I_{SF}	5.1	6.2	7.1	mA	Pin 11 (FSEL) open, Pin 15 (MSEL) tied to GND	
3	Supply current, device operating in ASK mode	I_{SA}	4.5	5.5	6.3	mA	Pin 11 (FSEL) open, Pin 15 (MSEL) open	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions/ Notes	L
			min.	typ.	max.			
LNA								
Signal Input LNI (PIN 3), V_{THRES}>2.8V, high gain mode								
1	Average Power Level at BER = 2E-3 (Sensitivity)	RF_{in}		-113		dBm	Manchester encoded datarate 4kBit, 280kHz IF Bandwidth	■
2	Average Power Level at BER = 2E-3 (Sensitivity) FSK	RF_{in}		-105		dBm	Manchester enc. datarate 4kBit, 280kHz IF Bandw., ± 50kHz pk. dev.	■
3	Input impedance, f_{RF} = 315 MHz	$S_{11\ LNA}$	0.895 / -25.5 deg					■
4	Input level @ 1dB C.P. f_{RF}=315 MHz	$P1dB_{LNA}$		-14		dBm		■
5	Input 3rd order intercept point f_{RF} = 315 MHz	$IIP3_{LNA}$		-10		dBm	f_{in} = 315 & 317MHz	■
6	LO signal feedthrough at antenna port	LO_{LNI}		-119		dBm		■
Signal Output LNO (PIN 6), V_{THRES}>2.8V, high gain mode								
1	Gain f_{RF} = 315 MHz	$S_{21\ LNA}$	1.577 / 150.3 deg					■
2	Output impedance, f_{RF} = 315 MHz	$S_{22\ LNA}$	0.897 / -10.3 deg					■
3	Voltage Gain Antenna to MI f_{RF} = 315 MHz	G_{AntMI}		21		dB		■
4	Noise Figure	NF_{LNA}		2		dB	excluding matching network loss - see Appendix	■
Signal Input LNI, V_{THRES}=GND, lwo gain mode								
1	Input impedance, f_{RF} = 315 MHz	$S_{11\ LNA}$	0.918 / -25.2 deg					■
2	Input level @ 1dB C. P. f_{RF} = 315 MHz	$P1dB_{LNA}$		-7		dBm	matched input	■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions/ Notes	L
			min.	typ.	max.			
3	Input 3rd order intercept point f_{RF} = 315 MHz	$IIP3_{LNA}$		-13		dBm	f_{in} = 315 & 317MHz	■
Signal Output LNO, V_{THRES}=GND, lwo gain mode								
1	Gain f_{RF} = 315 MHz	$S_{21\ LNA}$	0.193 / 153.7 deg					■
2	Output impedance, f_{RF} = 315 MHz	$S_{22\ LNA}$	0.907 / -10.5 deg					■
3	Voltage Gain Antenna to MI f_{RF} = 315 MHz	G_{AntMI}		2		dB		■
Signal 3VOUT (PIN 24)								
1	Output voltage	V_{3VOUT}	2.9	3.1	3.3	V	3VOUT Pin open	
2	Current out	I_{3VOUT}	-3	-5	-10	µA	see Section 4.1	
Signal THRES (PIN 23)								
1	Input Voltage range	V_{THRES}	0		V_S-1	V	see Section 4.1	
2	LNA low gain mode	V_{THRES}	0			V		
3	LNA high gain mode	V_{THRES}	3		V_S-1	V	or shorted to Pin 24	
4	Current in	I_{THRES_in}		5		nA		■
Signal TAGC (PIN 4)								
1	Current out, LNA low gain state	I_{TAGC_out}	-3.6	-4.2	-5.5	µA	RSSI > V_{THRES}	
2	Current in, LNA high gain state	I_{TAGC_in}	1	1.6	2.2	µA	RSSI < V_{THRES}	
MIXER								
Signal Input MI/MIX (PINS 8/9)								
1	Input impedance, f_{RF} = 315 MHz	$S_{11\ MIX}$	0.954 / -10.9 deg					■
2	Input 3rd order intercept point	$IIP3_{MIX}$		-25		dBm		■
Signal Output IFO (PIN 12)								
1	Output impedance	Z_{IFO}		330		Ω		■
2	Conversion Voltage Gain f_{RF} = 315 MHz	G_{MIX}		21		dB		■
3	Noise Figure, SSB (≙DSB NF+3dB)	NF_{MIX}		13		dB		■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions/ Notes	L
			min.	typ.	max.			
4	RF to IF isolation	A_{RF-IF}		46		dB		■
LIMITER								
Signal Input LIM/X (PINS 17/18)								
1	Input Impedance	Z_{LIM}	264	330	396	Ω		■
2	RSSI dynamic range	DR_{RSSI}		70		dB		
3	RSSI linearity	LIN_{RSSI}		±1		dB		■
4	Operating frequency (3dB points)	f_{LIM}	5	10.7	23	MHz		■
DATA FILTER								
1	Useable bandwidth	$BW_{BB\ FILT}$			100	kHz		■
2	RSSI Level at Data Filter Output SLP, RF_{IN}=-103dBm	$RSSI_{low}$		1.1		V	LNA in high gain mode	
3	RSSI Level at Data Filter Output SLP, RF_{IN}=-30dBm	$RSSI_{high}$		2.65		V	LNA in high gain mode	
SLICER								
Signal Output DATA (PIN 25)								
1	Maximum Datarate	DR_{max}			100	kBps	NRZ, 20pF capacitive loading	■
2	LOW output voltage	V_{SLIC_L}	0		0.1	V		
3	HIGH output voltage	V_{SLIC_H}	V_S-1.3	V_S-1	V_S-0.7	V	output current=200µA	
Slicer, SLN (PIN 20)								
1	Precharge Current Out	I_{PCH_SLN}	-100	-220	-300	µA	see Section 3.9	
PEAK DETECTOR								
Signal Output PDO (PIN 26)								

#	Parameter	Symbol	Limit Values			Unit	Test Conditions/ Notes	L
			min.	typ.	max.			
1	Load current	I_{load}	-500			µA	static load current must not exceed -500µA	
2	Internal resistive load	R	357	446	535	kΩ		
CRYSTAL OSCILLATOR								
Signals CRSTL 1, CRSTL 2 (PINS 1/28)								
1	Operating frequency	f_{CRSTL}	5		11	MHz	fundamental mode, series resonance	
2	Input Impedance @ ~10MHz	Z_{1-28}		-700 + j 865		Ω		■
3	Serial Capacity @ ~10MHz	C_{S10}=C1		7.2		pF		■
ASK/FSK Signal Switch								
Signal MSEL (PIN 15)								
1	ASK Mode	V_{MSEL}	1.4		4	V	or open	
2	FSK Mode	V_{MSEL}	0		0.2	V	or tied to ground	
3	Input Bias Current MSEL	I_{MSEL}		-11	-19	µA	MSEL tied to GND	
FSK DEMODULATOR								
1	Demodulation Gain	G_{FMDEM}		200		µV/k Hz		
2	Useable IF Bandwidth	BW_{IFPLL}	10.2	10.7	11.2	MHz		
POWER DOWN MODE								
Signal PDWN (PIN 27)								
1	Powerdown Mode On	$PWDN_{ON}$	2.8		V_S	V		
2	Powerdown Mode Off	$PWDN_{Off}$	0		0.8	V		
3	Input bias current PDWN	I_{PDWN}		19		µA	Power On Mode	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions/ Notes	L
			min.	typ.	max.			
4	Start-up Time until valid IF signal is detected	T_{SU}		1		ms	depends on the used crystal	■
PLL DIVIDER								
Signal FSEL (PIN 11)								
1	Overal divison ratio 32	V_{FSEL}	1.4		4	V	or open	
2	Overal division ratio 32.25	V_{FSEL}	0		0.2	V	or tied to GND	
3	Input bias current FSEL	I_{FSEL}		-11	-19	µA	FSEL tied to GND	
DATA-SLICER REFERENCE-LEVEL								
Signal SSEL (PIN 16), ASK-Mode								
1	Slicer-Reference is voltage at Pin 20 (SLN)	V_{SSEL}	1.4		4	V	or open	
2	Slicer-Reference is approx. 87% of the voltage at Pin 26 (PDO)	V_{SSEL}	0		0.2	V		
3	Input bias current SSEL	I_{SSEL}		-11	-19	µA	SSEL tied to GND	

■ Not part of the production test - either verified by design or measured in the Infineon Evalboard as described in Section 4.2.

4.1.4 AC/DC Characteristics at T_{AMB}= -40 to 105°C

Currents flowing into the device are denoted as positive currents and vice versa.

Table 10 AC/DC Characteristics with T_{AMB} = -40°C ...+105°C, V_{VCC}=4.5 ... 5.5 V

#	Parameter	Symbol	Limit Values			Unit	Test Conditions/ Notes	L
			min.	typ.	max.			
SUPPLY								
Supply Current								
1	Supply current, standby mode	$I_{S\ PDWN}$		50	400	nA	Pin 27 (PDWN) open or tied to 0 V	
2	Supply current, device operating in FSK mode	I_{SF}	4.1	6.2	8.1	mA	Pin 11 (FSEL) open, Pin 15 (MSEL) tied to GND	
3	Supply current, device operating in ASK mode	I_{SA}	3.5	5.5	7.3	mA	Pin 11 (FSEL) open, Pin 15 (MSEL) open	
Signal Input 3VOUT (PIN 24)								
1	Output voltage	V_{3VOUT}	2.9	3.1	3.3	V	3VOUT Pin open	
2	Current out	I_{3VOUT}	-3	-5	-10	µA	see Section 4.1	
Signal THRES (PIN 23)								
1	Input Voltage range	V_{THRES}	0		V_S-1	V	see Section 4.1	
2	LNA low gain mode	V_{THRES}	0			V		
3	LNA high gain mode	V_{THRES}	3		V_S-1	V	or shorted to Pin 24	
4	Current in	I_{THRES_in}		5		nA		■
Signal TAGC (PIN 4)								
1	Current out, LNA low gain state	I_{TAGC_out}	-1	-4.2	-8	µA	RSSI > V_{THRES}	
2	Current in, LNA high gain state	V_{TAGC_in}	0.5	1.5	5	µA	RSSI < V_{THRES}	
MIXER								
1	Conversion Voltage Gain f_{RF} = 315 MHz	G_{MIX}		+19		dB		
LIMITER								

#	Parameter	Symbol	Limit Values			Unit	Test Conditions/ Notes	L
			min.	typ.	max.			
Signal Input LIM/X (PINS 17/18)								
1	RSSI dynamic range	DR_{RSSI}		70		dB		
2	RSSI Level at Data Filter Output SLP, RF_{IN}= -103dBm	$RSSI_{low}$		1.1		V	LNA in high gain mode	
3	RSSI Level at Data Filter Output SLP, RF_{IN}= -30dBm	$RSSI_{high}$		2.65		V	LNA in high gain mode	
DATA FILTER								
Slicer, Signal Output DATA (PIN 25)								
1	Maximum Datarate	DR_{max}			100	kBps	NRZ, 20pF capacitive loading	■
2	LOW output voltage	V_{SLIC_L}	0		0.1	V		
3	HIGH output voltage	V_{SLIC_H}	V_S-1.5	V_S-1	V_S-0.5	V	output current=200µA	
Slicer, Negative Input (PIN 20)								
1	Precharge Current Out	I_{PCH_SLN}	-100	-220	-300	µA	see Section 3.9	
PEAK DETECTOR								
Signal Output PDO (PIN 26)								
1	Load current	I_{load}	-400			µA	static load current must not exceed -500µA	
2	Internal resistive load	R	356	446	575	kΩ		
CRYSTAL OSCILLATOR								
Signals CRSTL 1, CRSTL 2 (PINS 1/28)								
1	Operating frequency	f_{CRSTL}	5		11	MHz	fundamental mode, series resonance	
ASK/FSK Signal Switch								
Signal MSEL (PIN 15)								
1	ASK Mode	V_{MSEL}	1.4		4	V	or open	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions/ Notes	L
			min.	typ.	max.			
2	FSK Mode	V_{MSEL}	0		0.2	V		
3	Input bias current MSEL	I_{MSEL}		-11	-20	µA	MSEL tied to GND	
FSK DEMODULATOR								
1	Demodulation Gain	G_{FMDEM}		200		µV/kHz		
2	Useable IF Bandwidth	BW_{IFPLL}	10.4	10.7	11	MHz		
POWER DOWN MODE								
Signal PDWN (PIN 27)								
1	Powerdown Mode On	$PWDN_{ON}$	2.8		V_S	V		
2	Powerdown Mode Off	$PWDN_{Off}$	0		0.8	V		
3	Start-up Time until valid signal is detected at IF	T_{SU}		1		ms	depends on the used crystal	■
PLL DIVIDER								
Signal FSEL (PIN 11)								
1	Overal divison ratio 32	V_{FSEL}	1.4		4	V	or open	
2	Overal division ratio 32.25	V_{FSEL}	0		0.2	V	or tied to GND	
3	Input bias current FSEL	I_{FSEL}		-11	-20	µA	FSEL tied to GND	
DATA-SLICER REFERENCE-LEVEL								
Signal SSEL (PIN 16), ASK-Mode								
1	Slicer-Reference is voltage at Pin 20 (SLN)	V_{SSEL}	1.4		4	V	or open	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions/ Notes	L
			min.	typ.	max.			
2	Slicer-Reference is approx. 87% of the voltage at Pin 26 (PDO)	V_{SSEL}	0		0.2	V		
3	Input bias current SSEL	I_{SSEL}		-11	-20	µA	SSEL tied to GND	

■ Not part of the production test - either verified by design or measured in the Infineon Evalboard as described in Section 4.2.

4.2 Test Circuit

The device performance parameters marked with ■ in **Section 4.1** were either verified by design or measured on an Infineon evaluation board. This evaluation board can be obtained together with evaluation boards of the accompanying transmitter device TDK5110 in an evaluation kit that may be ordered on the INFINEON Webpage www.infineon.com/Products More information on the kit is available on request.

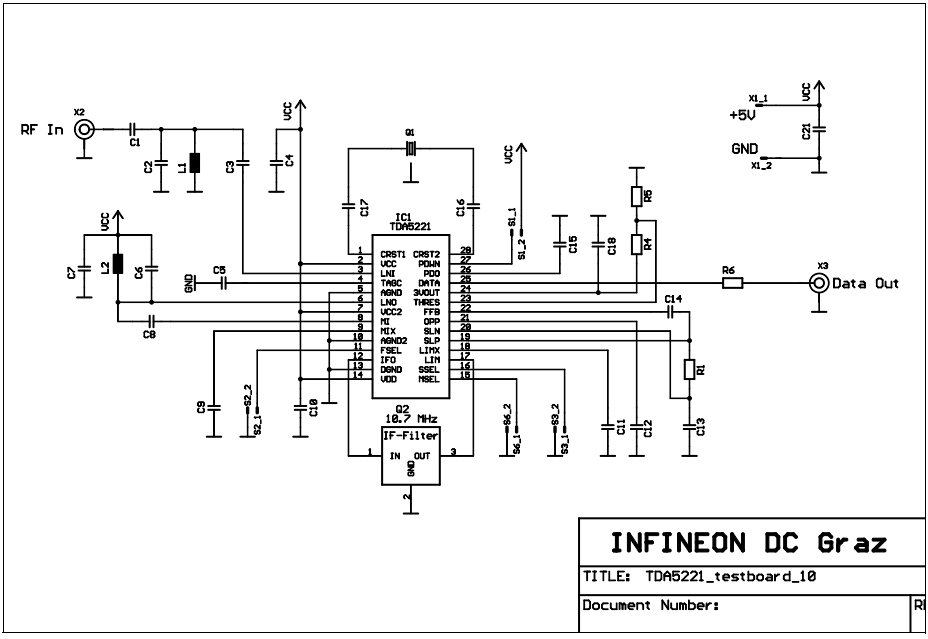


Figure 15 Schematic of the Evaluation Board

4.3 Test Board Layouts

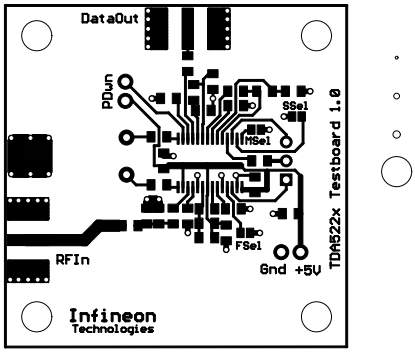


Figure 16 Top Side of the Evaluation Board

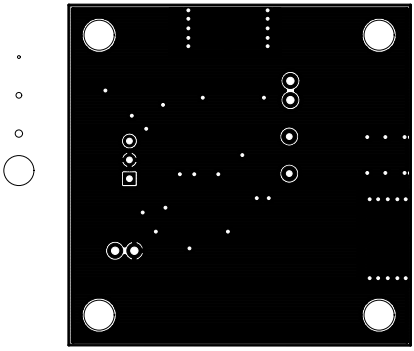


Figure 17 Bottom Side of the Evaluation Board

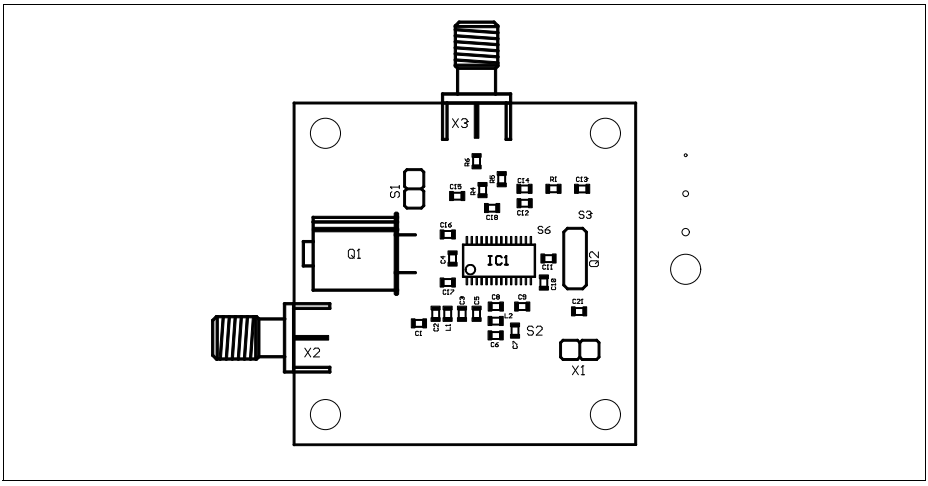


Figure 18 Component Placement on the Evaluation Board

4.4 Bill of Materials

The following components are necessary for evaluation of the TDA5221.

Table 11 Bill of Materials (cont'd)

Ref.	Value	Specification 315MHz
C1	3.3pF	0805, COG, +/-0.1pF
C2	10pF	0805, COG, +/-0.1pF
C3	6.8pF	0805, COG, +/-0.1pF
C4	100pF	0805, COG, +/-5%
C5	47nF	1206, X7R, +/-10%
C6	15nH	Toko, PTL2012-F15N0G
C7	100pF	0805, COG, +/-5%
C8	33pF	0805, COG, +/-5%
C9	100pF	0805, COG, +/-5%
C10	10nF	0805, X7R, +/-10%
C11	10nF	0805, X7R, +/-10%
C12	220pF	0805, COG, +/-5%

Ref.	Value	Specification 315MHz
C13	47nF	0805, X7R, +/-10%
C14	470pF	0805, COG, +/-5%
C15	47nF	0805, COG, +/-5%
C16	12pF	0805, COG, +/-1%
C17	22pF	0805, COG, +/-1%
C18	22nF	0805, X7R, +/-5%
C21	100nF	1206, X7R, +/-10%
IC1	TDA5221	Infineon
L1	15nH	Toko, PTL2012-F15N0G
L2	12pF	0805, COG, +/-1%
Q1	10,209375 MHz	1053-925
Q2	SFE_10.7MA5-A	Murata
R1	100kΩ	0805, +/-5%
R4	240kΩ	0805, +/-5%
R5	360kΩ	0805, +/-5%
R6	10kΩ	0805, +/-5%
S1	STL_2POL	2-pole pin connector
S2	SOL_JUMP	SOL_JUMP
S3	SOL_JUMP	SOL_JUMP
S6	SOL_JUMP	SOL_JUMP
X1	STL_2POL	2-pole pin connector
X2	A107-900A (1.6mm gold plated)	INPUT OUTPUT ENTERPRISE CORP
X3	A107-900A (1.6mm gold plated)	INPUT OUTPUT ENTERPRISE CORP

Please note that a capacitor has to be soldered in place L2 and an inductor in place C6.

5 Package Outlines

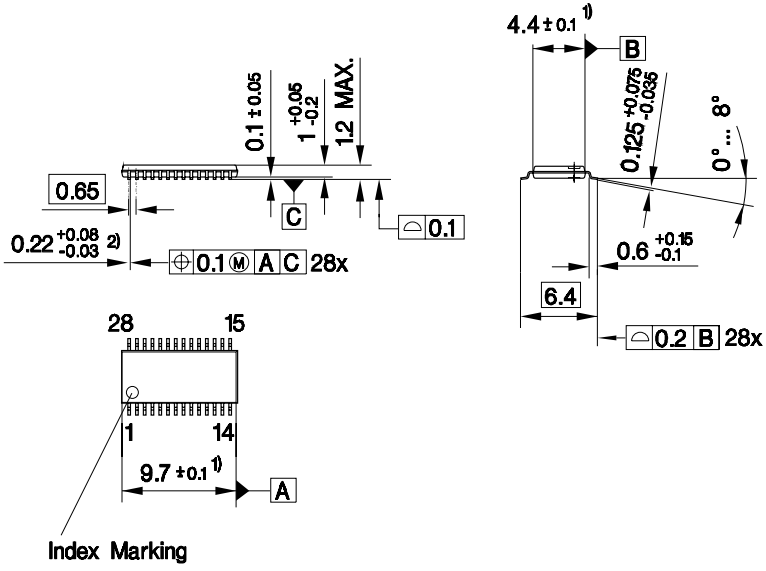


Figure 19 <Dev_Package1>

Table 12 Order Information

Type	Ordering Code	Package
TDA 5221	Q67100-H2051	<Dev_Package1>

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

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