

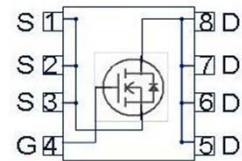
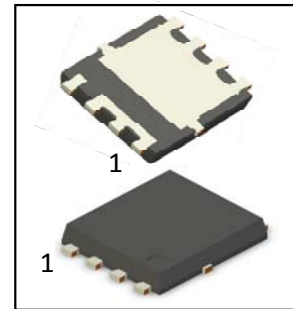
**OptiMOS™ - 6 Power-Transistor**

**Product Summary**

$V_{DS}$	40	V
$R_{DS(on),max}$	0.9	mΩ
$I_D$	120	A

**Features**

- OptiMOS™ - power MOSFET for automotive applications
- N-channel - Enhancement mode - Normal Level
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

**PG-TDSON-8**


Type	Package	Marking
IAUC120N04S6N009	PG-TDSON-8	6N04N009

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current <sup>1)</sup>	$I_D$	$T_C=25\text{ °C}$ , $V_{GS}=10\text{V}$	120	A
		$T_C=100\text{ °C}$ , $V_{GS}=10\text{V}^{2)}$	120	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	480	
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	$I_D=60\text{A}$ , $R_{G,min}=25\text{ }\Omega$	400	mJ
Avalanche current, single pulse	$I_{AS}$	$R_{G,min}=25\text{ }\Omega$	60	A
Gate source voltage	$V_{GS}$	-	$\pm 20$	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	150	W
Operating and storage temperature	$T_j$ , $T_{stg}$	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
<b>Thermal characteristics<sup>2)</sup></b>						
Thermal resistance, junction - case	$R_{thJC}$	-	-	-	1.0	K/W
Thermal resistance, junction - ambient	$R_{thJA}$	6 cm <sup>2</sup> cooling area <sup>3)</sup>	-	-	50	

**Electrical characteristics, at  $T_j=25^\circ\text{C}$ , unless otherwise specified**

**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=90\mu A$	2.2	2.8	3.4	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=40V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	-	1	$\mu A$
		$V_{DS}=40V, V_{GS}=0V, T_j=125^\circ\text{C}^{2)}$	-	-	100	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=7V, I_D=60A$	-	0.95	1.1	m $\Omega$
		$V_{GS}=10V, I_D=60A$	-	0.75	0.9	
Gate resistance <sup>2)</sup>	$R_G$		-	0.9	-	$\Omega$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics<sup>2)</sup>**

Input capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	5530	7360	pF
Output capacitance	$C_{oss}$		-	1550	2070	
Reverse transfer capacitance	$C_{rss}$		-	108	125	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20V, V_{GS}=10V,$ $I_D=120A, R_G=3.5\Omega$	-	10	-	ns
Rise time	$t_r$		-	6	-	
Turn-off delay time	$t_{d(off)}$		-	22	-	
Fall time	$t_f$		-	11	-	

**Gate Charge Characteristics<sup>2)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=32V, I_D=120A,$ $V_{GS}=0$ to 10V	-	25	33	nC
Gate to drain charge	$Q_{gd}$		-	15	28	
Gate charge total	$Q_g$		-	76	115	
Gate plateau voltage	$V_{plateau}$		-	4.5	-	V

**Reverse Diode**

Diode continuous forward current <sup>2)</sup>	$I_S$	$T_C=25^\circ C$	-	-	120	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$		-	-	480	
Diode forward voltage	$V_{SD}$	$V_{GS}=0V, I_F=60A,$ $T_J=25^\circ C$	-	0.8	1.1	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R=20V, I_F=120A,$ $di_F/dt=100A/\mu s$	-	60	-	ns
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$		-	73	-	nC

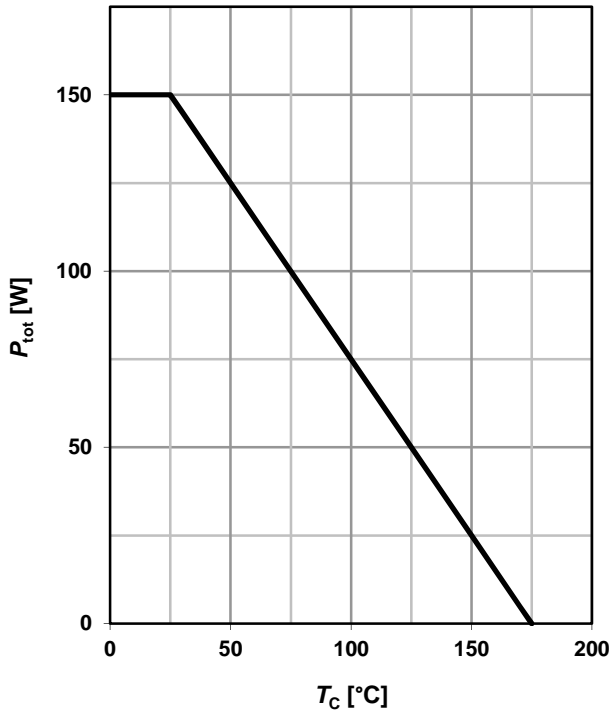
<sup>1)</sup> Current is limited by package; with an  $R_{thJC} = 1$  K/W the chip is able to carry 300 A at 25 °C.

<sup>2)</sup> The parameter is not subject to production test- verified by design/characterization.

<sup>3)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

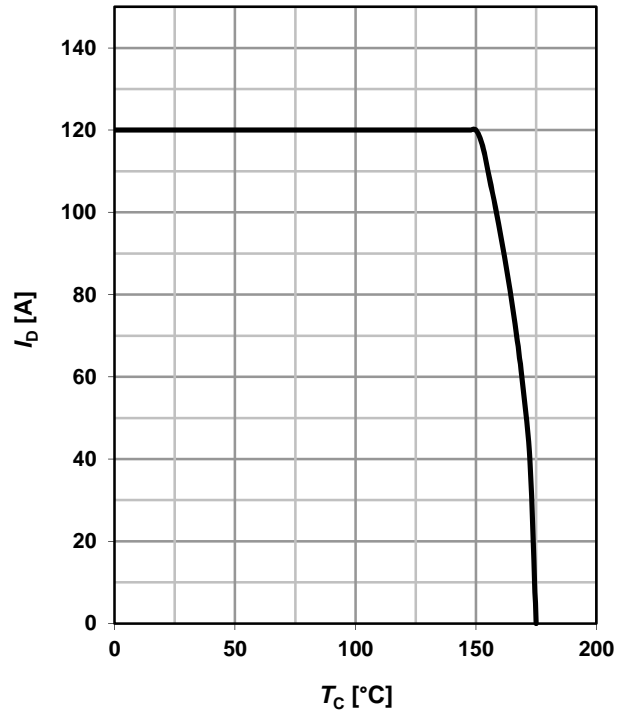
### 1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



### 2 Drain current

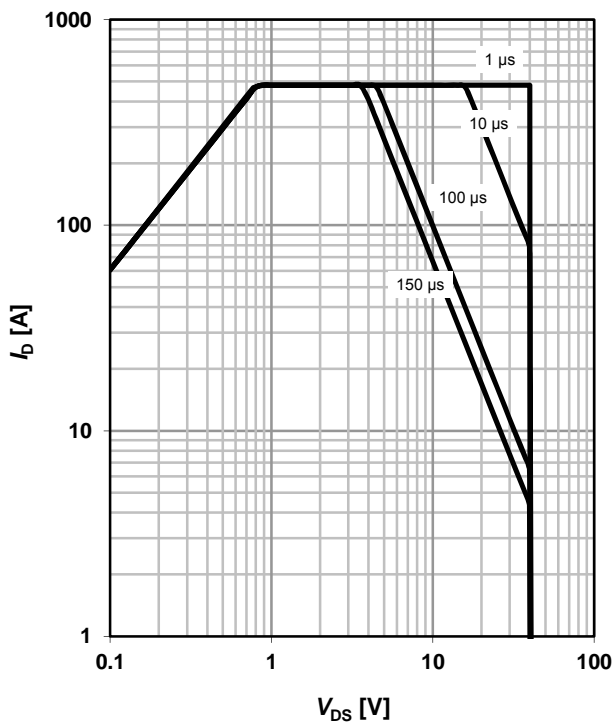
$$I_D = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



### 3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

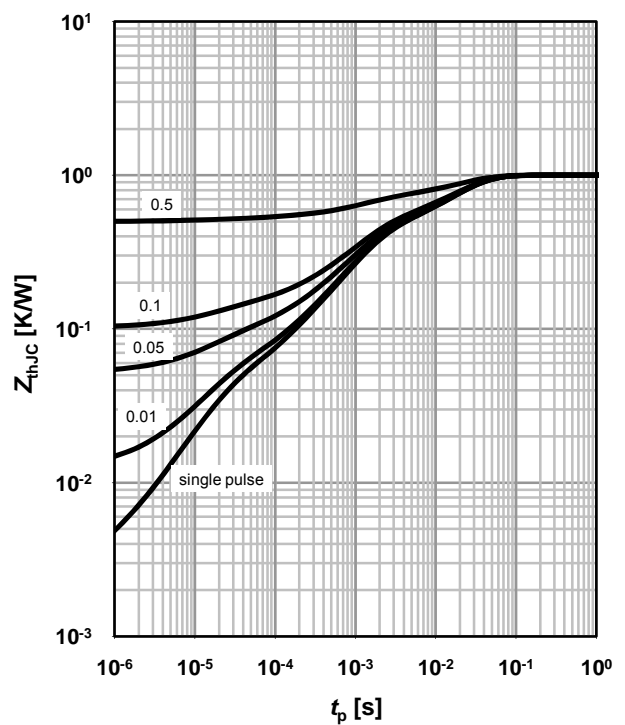
parameter:  $t_p$



### 4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

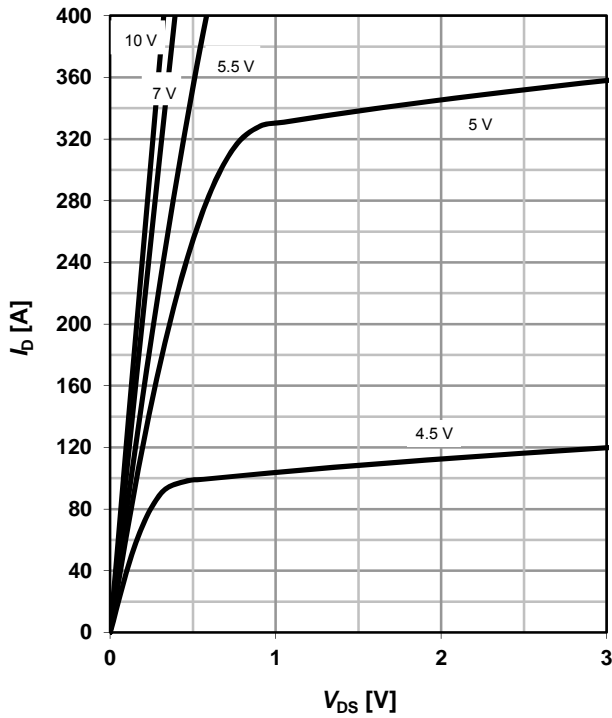
parameter:  $D = t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

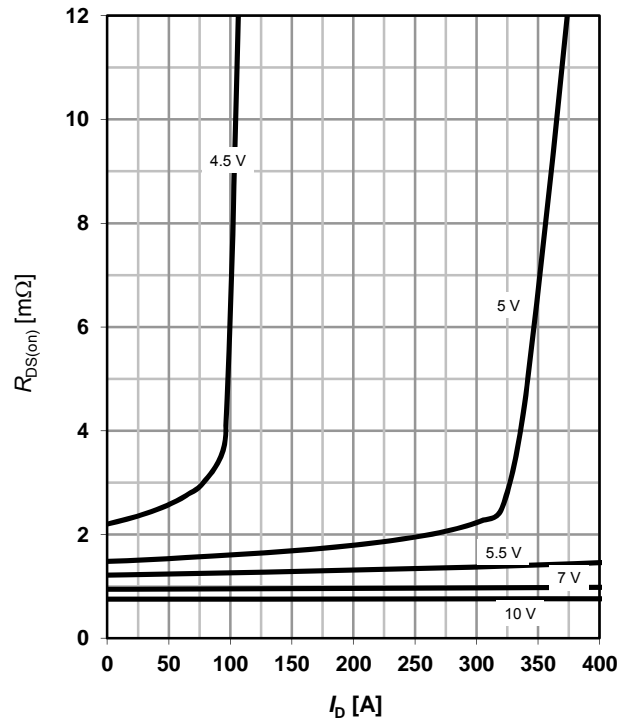
parameter:  $V_{GS}$



**6 Typ. drain-source on-state resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

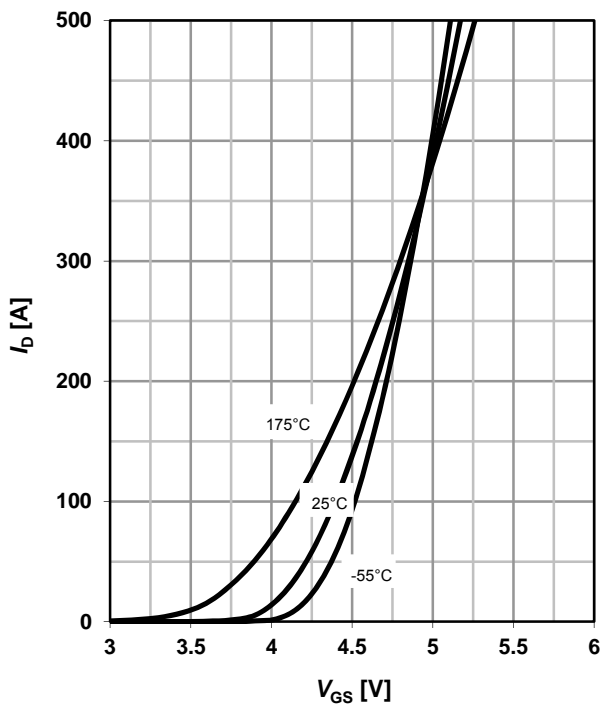
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

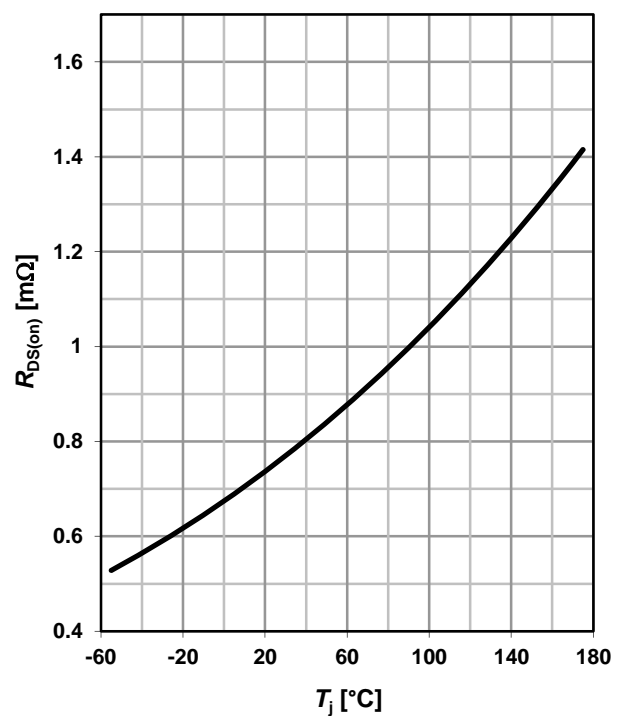
$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

parameter:  $T_j$



**8 Typ. drain-source on-state resistance**

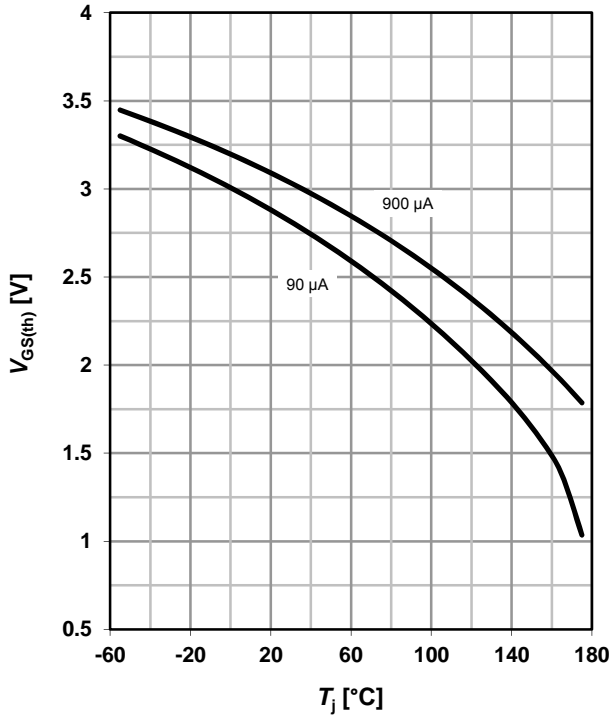
$R_{DS(on)} = f(T_j); I_D = 60\text{ A}; V_{GS} = 10\text{ V}$



**9 Typ. gate threshold voltage**

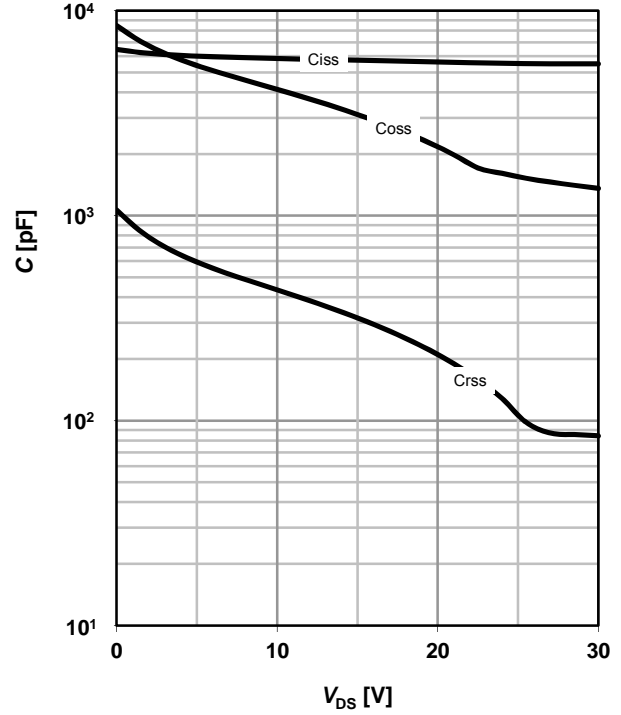
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter:  $I_D$



**10 Typ. capacitances**

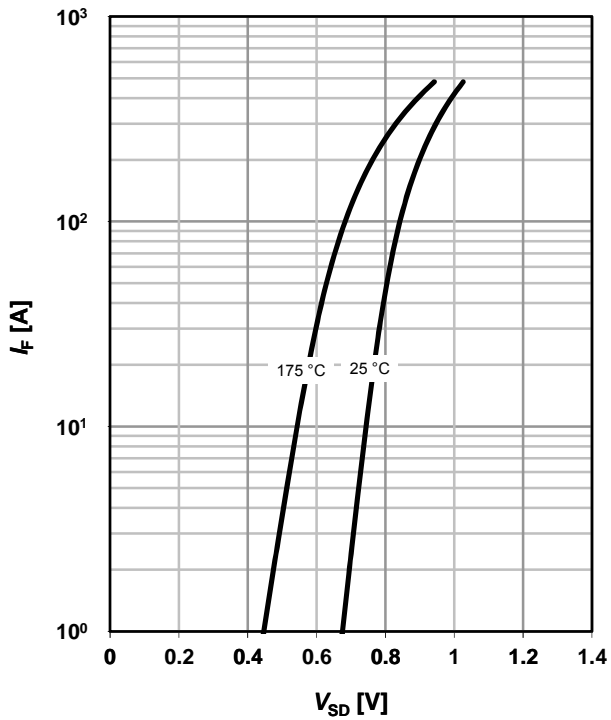
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



**11 Typical forward diode characteristics**

$I_F = f(V_{SD})$

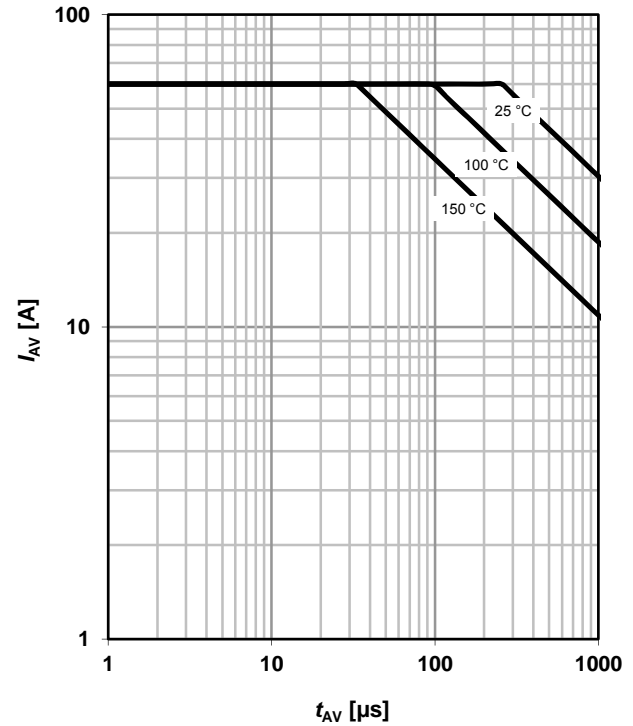
parameter:  $T_j$



**12 Avalanche characteristics**

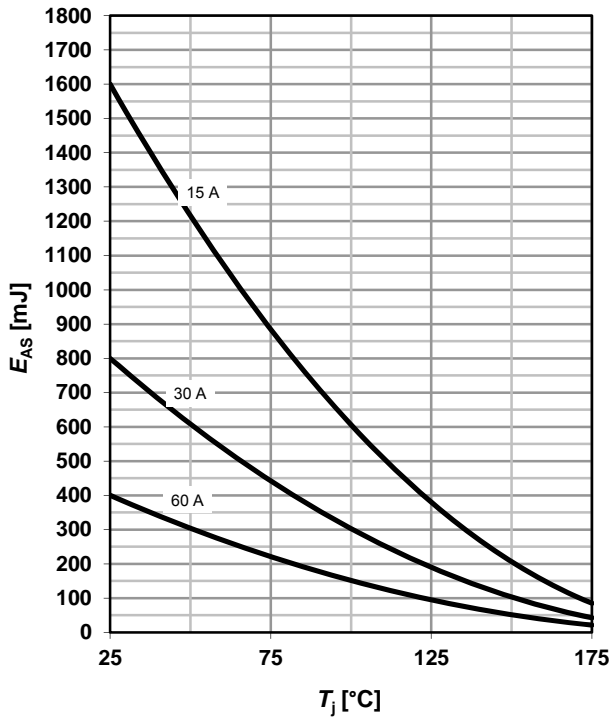
$I_{AS} = f(t_{AV})$

parameter:  $T_{j(start)}$

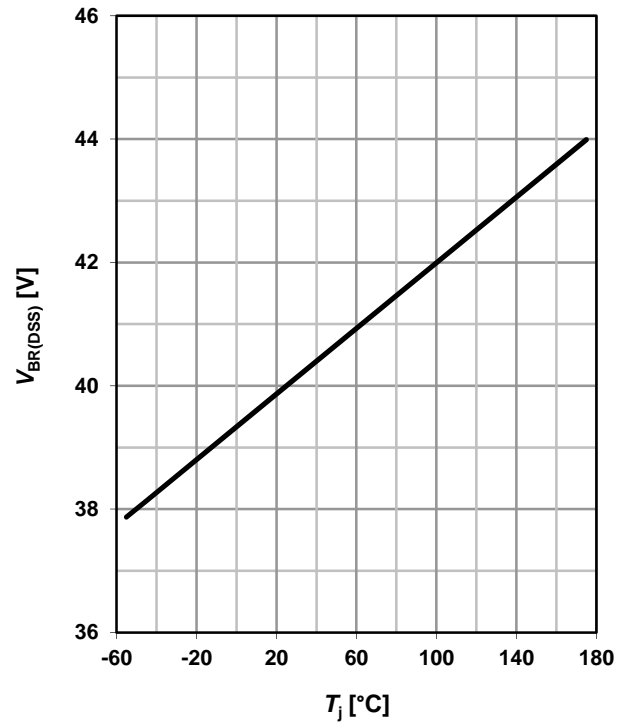


**13 Avalanche energy**

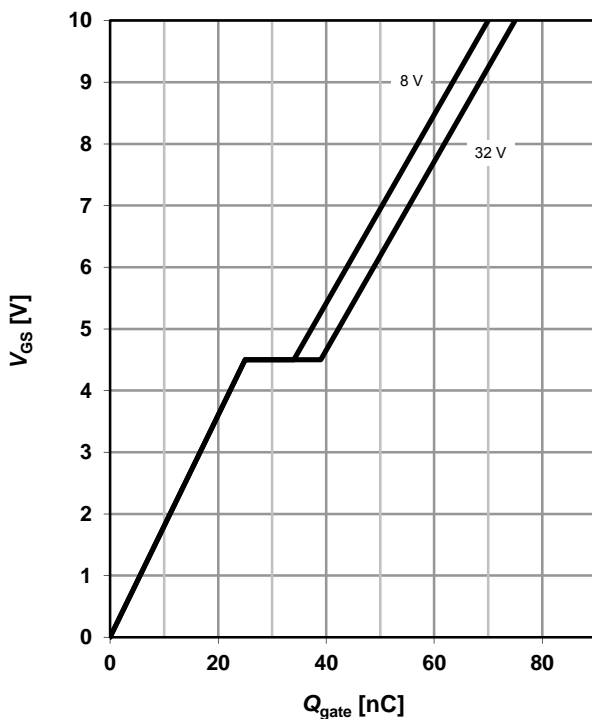
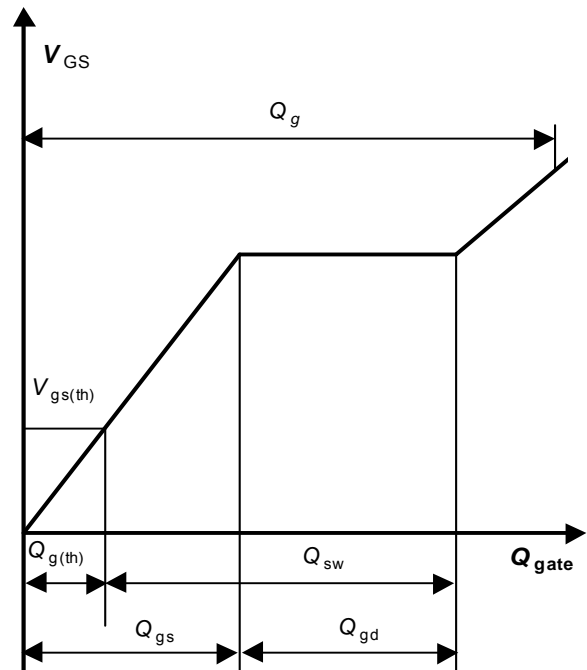
$$E_{AS} = f(T_j)$$


**14 Drain-source breakdown voltage**

$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$


**15 Typ. gate charge**

$$V_{GS} = f(Q_{gate}); I_D = 40 \text{ A pulsed}$$

 parameter:  $V_{DD}$ 

**16 Gate charge waveforms**


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## Revision History

Version	Date	Changes
Revision 1.0	2018-09-27	Final Data Sheet

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