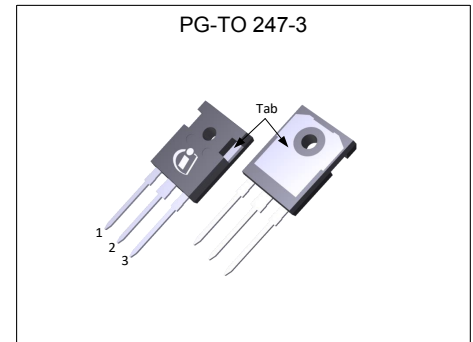


## MOSFET

### 650V CoolMOS™ CFD7 SJ Power Device

The latest 650 V CoolMOS™ CFD7 extends the voltage class offering of the CFD7 family and is a successor to the 650 V CoolMOS™ CFD2. Resulting from improved switching performance and excellent thermal behavior, 650 V CoolMOS™ CFD7 offers highest efficiency in resonant switching topologies, such as LLC and phase-shift-full-bridge (ZVS). As part of Infineon's fast body diode portfolio, this new product series blends all advantages of a fast switching technology together with superior hard commutation robustness. The CoolMOS™ CFD7 technology meets highest efficiency and reliability standards and furthermore supports high power density solutions.



### Features

- Ultra-fast body diode
- 650V break down voltage
- Best-in-class  $R_{DS(on)}$
- Reduced switching losses
- Low  $R_{DS(on)}$  dependency over temperature

### Benefits

- Excellent hard commutation ruggedness
- Extra safety margin for designs with increased bus voltage
- Enabling increased power density solutions
- Outstanding light load efficiency in industrial SMPS applications
- Improved full load efficiency in industrial SMPS applications
- Price competitiveness over previous CoolMOS™ families

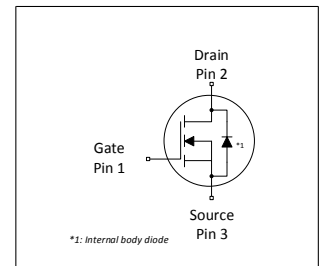
### Potential applications

Suitable for Soft Switching topologies  
Optimized for phase-shift full-bridge (ZVS), LLC Applications – Server, Telecom, EV Charging, Solar

### Product validation

Fully qualified according to JEDEC for Industrial Applications

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.*



RoHS

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	29	mΩ
$Q_{g,typ}$	145	nC
$I_{D,pulse}$	304	A
$E_{oss} @ 400V$	19.8	μJ
Body diode $di_F/dt$	1300	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPW65R029CFD7	PG-TO247-3	65R029F7	see Appendix A

## Table of Contents

Description .....	1
Maximum ratings .....	3
Thermal characteristics .....	4
Electrical characteristics .....	5
Electrical characteristics diagrams .....	7
Test Circuits .....	11
Package Outlines .....	12
Appendix A .....	13
Revision History .....	14
Trademarks .....	14
Disclaimer .....	14

## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	69 44	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	304	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	358	mJ	$I_D=7.3\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche energy, repetitive	$E_{AR}$	-	-	1.79	mJ	$I_D=7.3\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche current, single pulse	$I_{AS}$	-	-	7.3	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f>1\text{ Hz}$ )
Power dissipation	$P_{tot}$	-	-	305	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	$T_j$	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	60	Ncm	M3 and M3.5 screws
Continuous diode forward current <sup>1)</sup>	$I_S$	-	-	69	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	304	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	70	V/ns	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq 35.8\text{A}$ , $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di <sub>F</sub> /dt	-	-	1300	A/ $\mu\text{s}$	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq 35.8\text{A}$ , $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	$V_{ISO}$	-	-	n.a.	V	$V_{rms}$ , $T_C=25^\circ\text{C}$ , $t=1\text{min}$

<sup>1)</sup> Limited by  $T_{j,max}$ .

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_\theta$

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	0.41	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	62	°C/W	leaded
Thermal resistance, junction - ambient for SMD version	$R_{thJA}$	-	-	-	°C/W	n.a.
Soldering temperature, wavesoldering only allowed at leads	$T_{sold}$	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

### 3 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3.5	4	4.5	V	$V_{DS}=V_{GS}, I_D=1.79mA$
Zero gate voltage drain current <sup>1)</sup>	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS}=650V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=650V, V_{GS}=0V, T_j=125^\circ C$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.024	0.029	$\Omega$	$V_{GS}=10V, I_D=35.8A, T_j=25^\circ C$ $V_{GS}=10V, I_D=35.8A, T_j=150^\circ C$
Gate resistance	$R_G$	-	3.8	-	$\Omega$	$f=1MHz, \text{open drain}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	7149	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Output capacitance	$C_{oss}$	-	106	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Effective output capacitance, energy related <sup>2)</sup>	$C_{o(er)}$	-	247	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related <sup>3)</sup>	$C_{o(tr)}$	-	2584	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	54	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=35.8A, R_G=1.8\Omega; \text{see table 9}$
Rise time	$t_r$	-	13	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=35.8A, R_G=1.8\Omega; \text{see table 9}$
Turn-off delay time	$t_{d(off)}$	-	159	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=35.8A, R_G=1.8\Omega; \text{see table 9}$
Fall time	$t_f$	-	3	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=35.8A, R_G=1.8\Omega; \text{see table 9}$

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{GS}$	-	41	-	nC	$V_{DD}=400V, I_D=35.8A, V_{GS}=0 \text{ to } 10V$
Gate to drain charge	$Q_{gd}$	-	44	-	nC	$V_{DD}=400V, I_D=35.8A, V_{GS}=0 \text{ to } 10V$
Gate charge total	$Q_g$	-	145	-	nC	$V_{DD}=400V, I_D=35.8A, V_{GS}=0 \text{ to } 10V$
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	$V_{DD}=400V, I_D=35.8A, V_{GS}=0 \text{ to } 10V$

<sup>1)</sup> Maximum specification is defined by calculated six sigma upper confidence bound

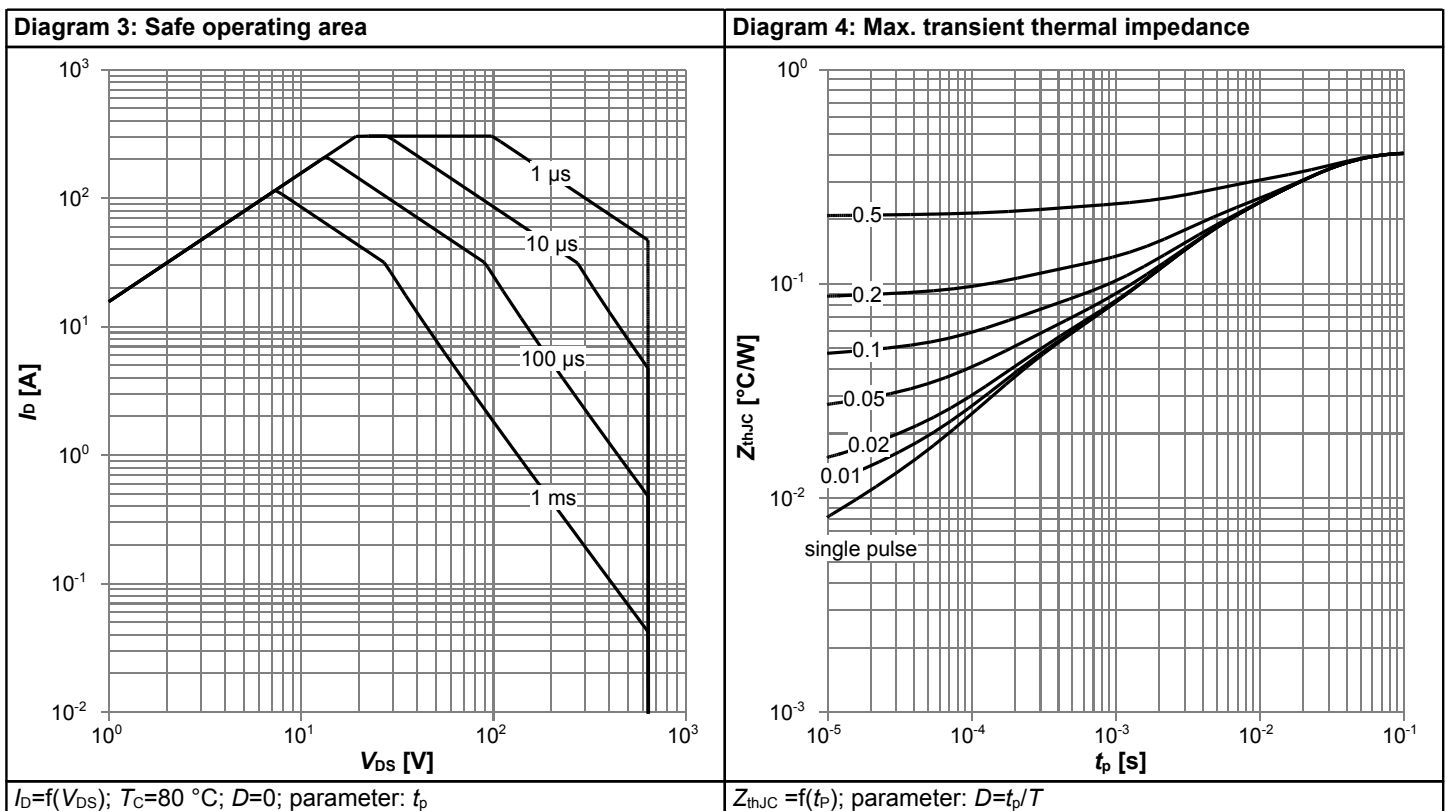
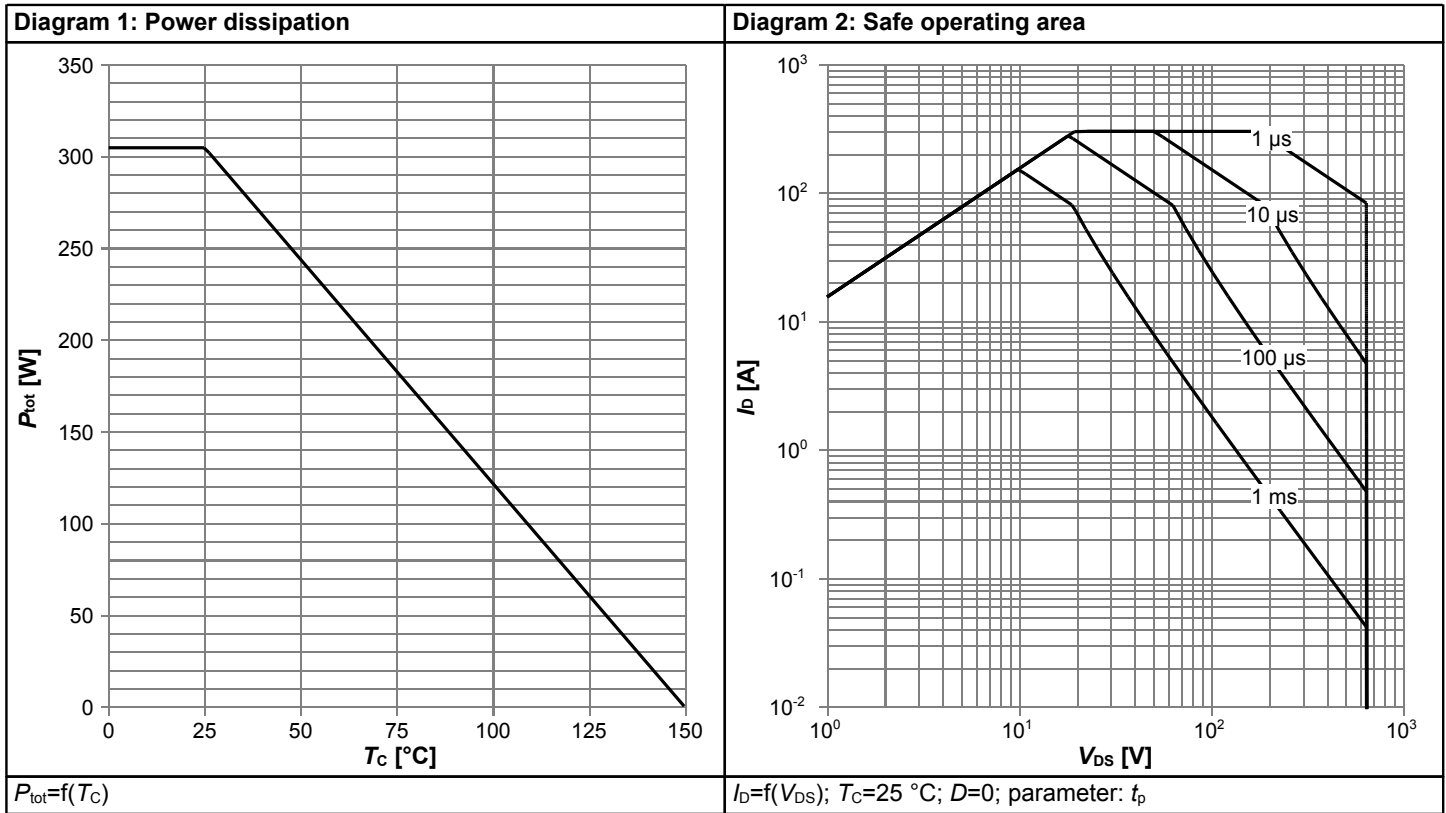
<sup>2)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>3)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

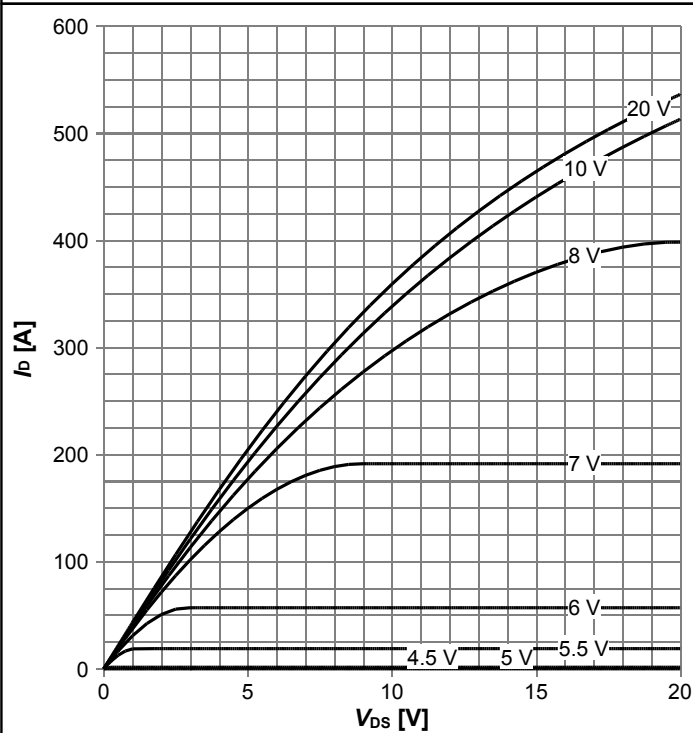
**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	1.0	-	V	$V_{GS}=0V, I_F=35.8A, T_j=25^{\circ}C$
Reverse recovery time	$t_{rr}$	-	208	312	ns	$V_R=400V, I_F=35.8A, di_F/dt=100A/\mu s$ ; see table 8
Reverse recovery charge	$Q_{rr}$	-	1.6	3.2	$\mu C$	$V_R=400V, I_F=35.8A, di_F/dt=100A/\mu s$ ; see table 8
Peak reverse recovery current	$I_{rrm}$	-	13.1	-	A	$V_R=400V, I_F=35.8A, di_F/dt=100A/\mu s$ ; see table 8

### 4 Electrical characteristics diagrams

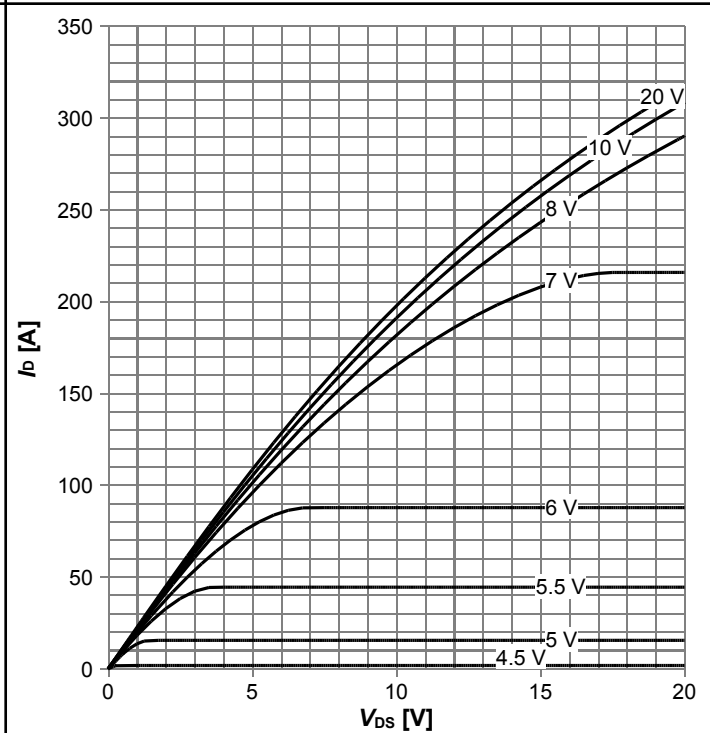


**Diagram 5: Typ. output characteristics**



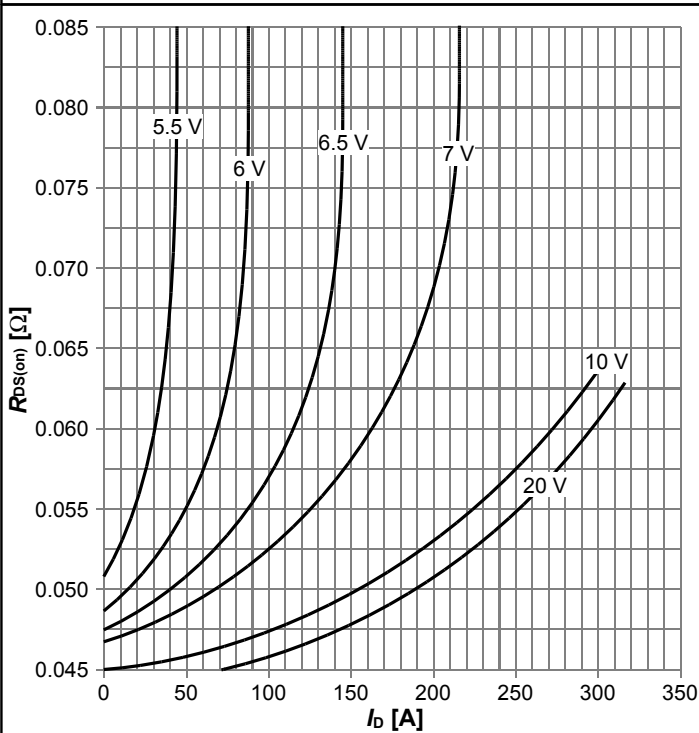
$I_D=f(V_{DS})$ ;  $T_j=25\text{ °C}$ ; parameter:  $V_{GS}$

**Diagram 6: Typ. output characteristics**



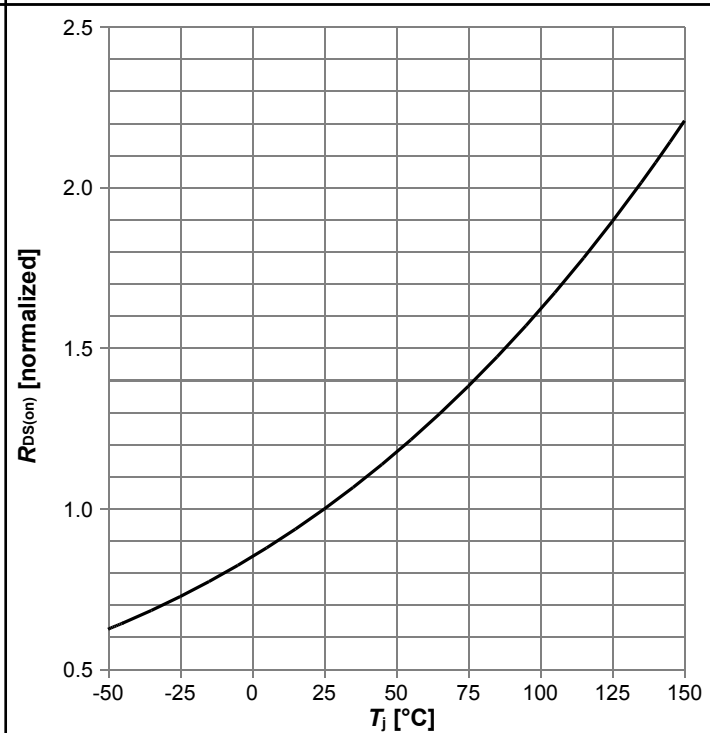
$I_D=f(V_{DS})$ ;  $T_j=125\text{ °C}$ ; parameter:  $V_{GS}$

**Diagram 7: Typ. drain-source on-state resistance**



$R_{DS(on)}=f(I_D)$ ;  $T_j=125\text{ °C}$ ; parameter:  $V_{GS}$

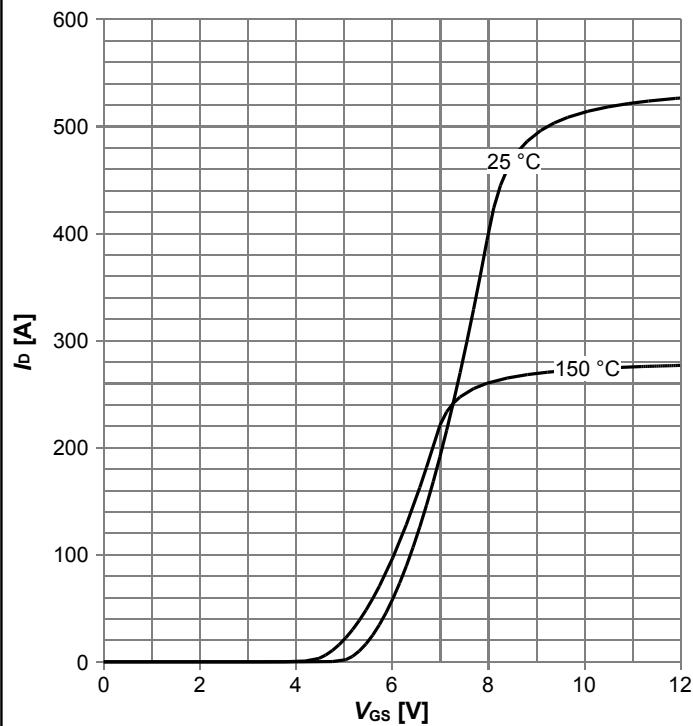
**Diagram 8: Drain-source on-state resistance**



$R_{DS(on)}=f(T_j)$ ;  $I_D=35.8\text{ A}$ ;  $V_{GS}=10\text{ V}$

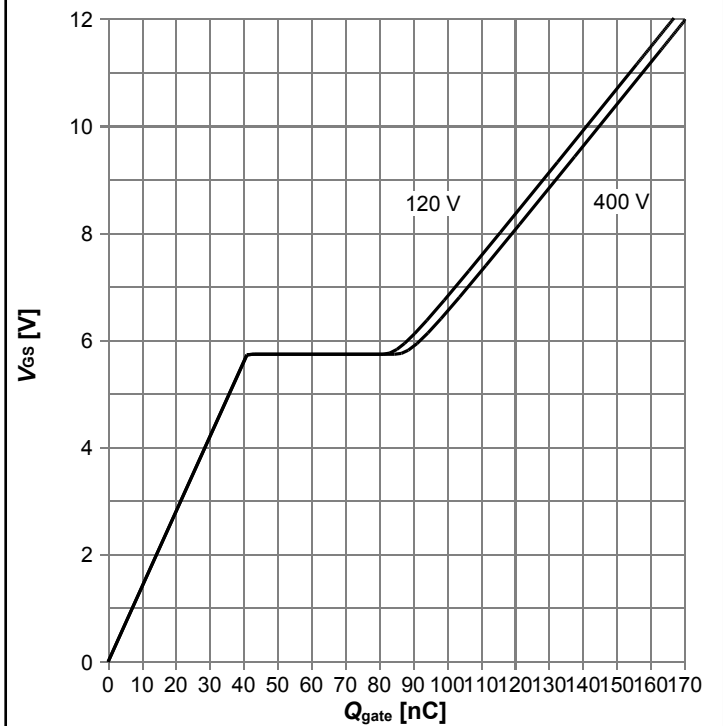


**Diagram 9: Typ. transfer characteristics**



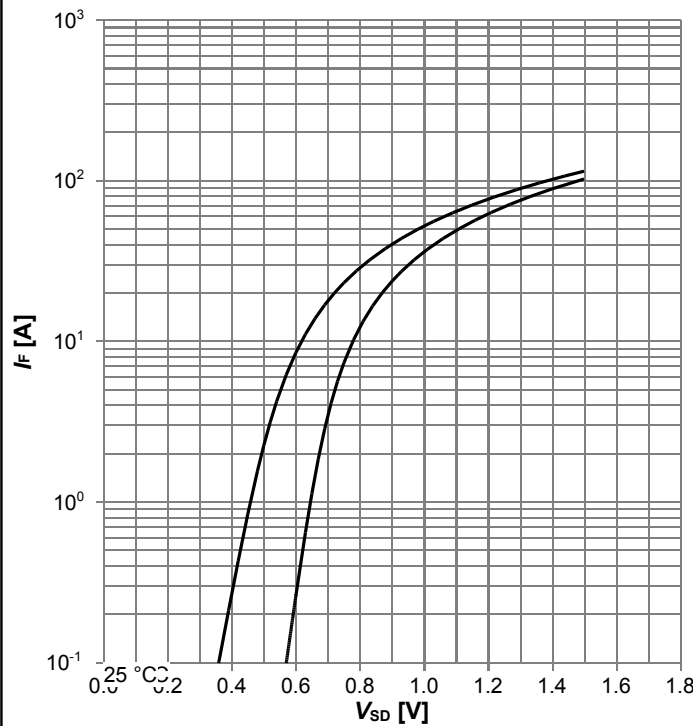
$I_D=f(V_{GS}); V_{DS}=20V; \text{parameter: } T_j$

**Diagram 10: Typ. gate charge**



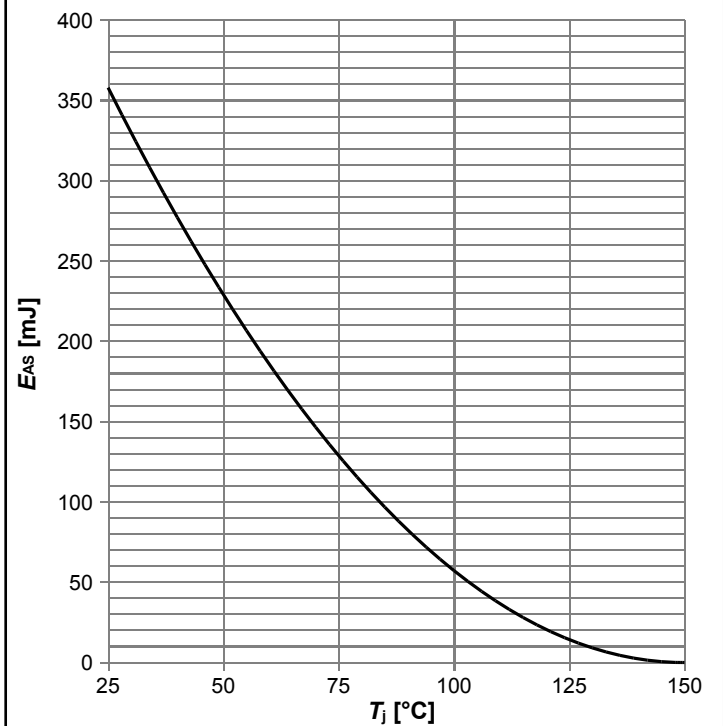
$V_{GS}=f(Q_{gate}); I_D=35.8 \text{ A pulsed}; \text{parameter: } V_{DD}$

**Diagram 11: Forward characteristics of reverse diode**



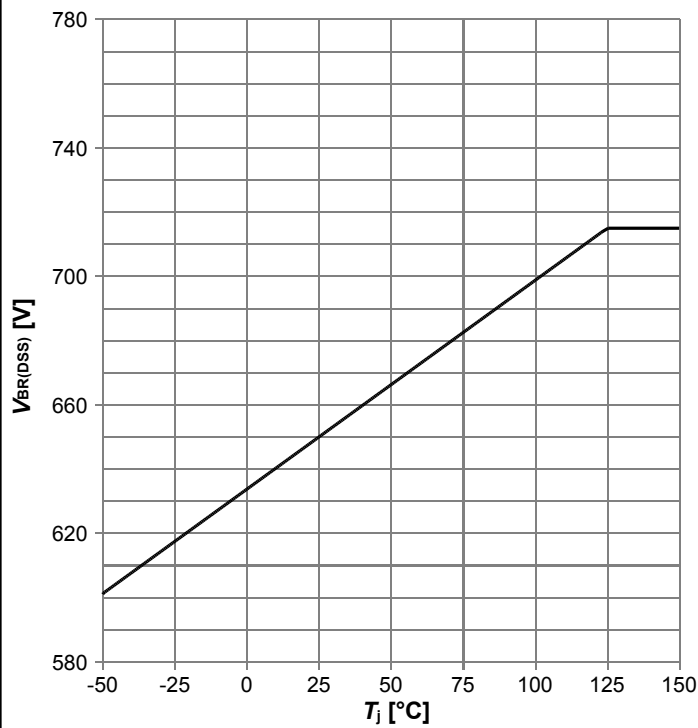
$I_F=f(V_{SD}); \text{parameter: } T_j$

**Diagram 12: Avalanche energy**



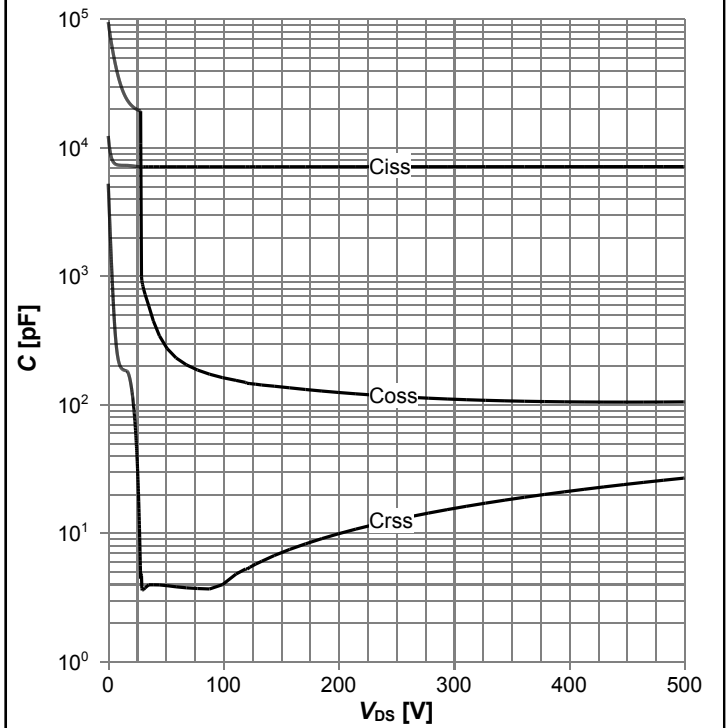
$E_{AS}=f(T_j); I_D=7.3 \text{ A}; V_{DD}=50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



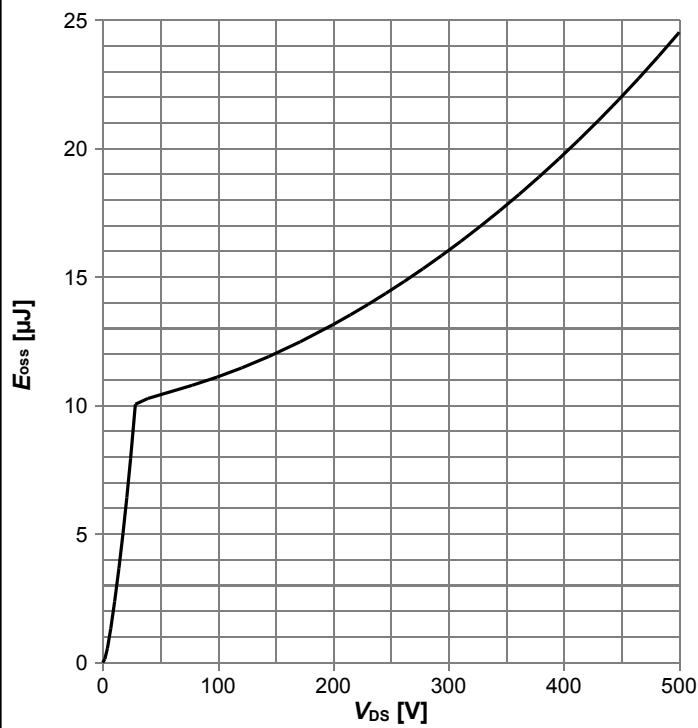
$V_{BR(DSS)}=f(T_j); I_D=1\text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=250\text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

## 5 Test Circuits

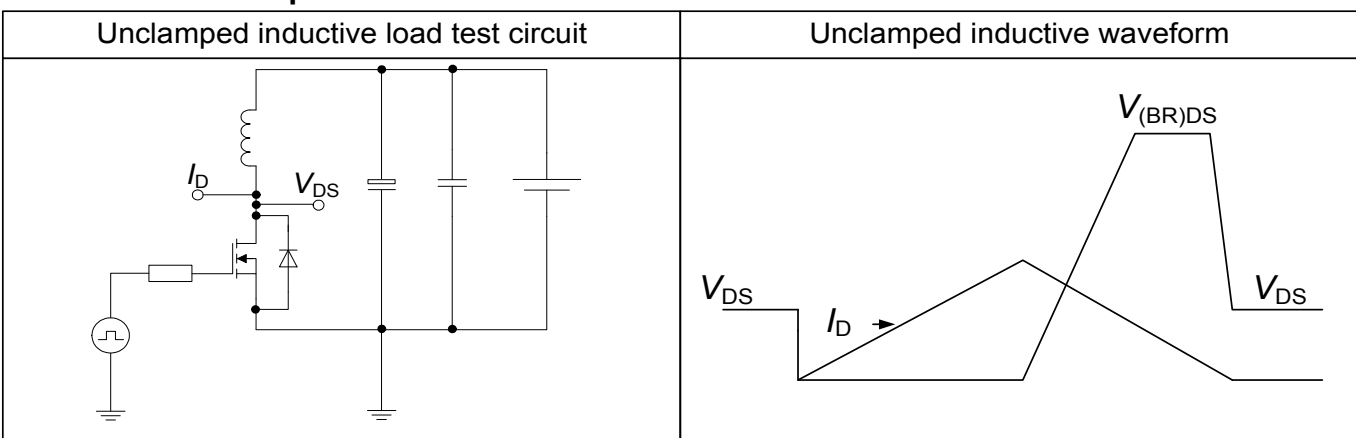
**Table 8 Diode characteristics**



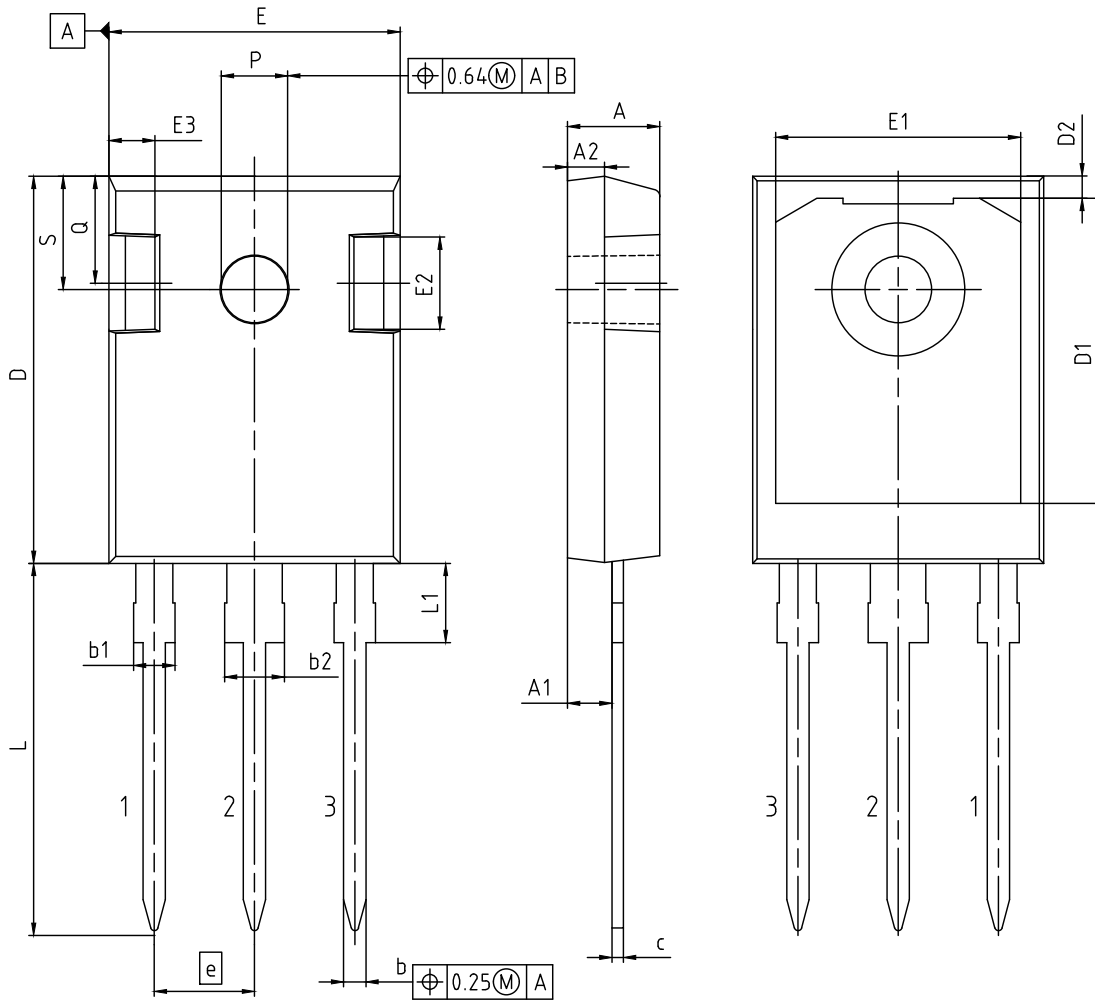
**Table 9 Switching times**



**Table 10 Unclamped inductive load**



## 6 Package Outlines



DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.70	5.30
A1	2.20	2.60
A2	1.50	2.50
b	1.00	1.40
b1	1.60	2.41
b2	2.57	3.43
c	0.38	0.89
D	20.70	21.50
D1	13.08	17.65
D2	0.51	1.35
E	15.50	16.30
E1	12.38	14.15
E2	3.40	5.10
E3	1.00	2.60
e	5.44	
L	19.80	20.40
L1	3.85	4.50
P	3.50	3.70
Q	5.35	6.25
S	6.04	6.30

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Figure 1 Outline PG-TO247-3, dimensions in mm

## 7 Appendix A

### Table 11 Related Links

- **IFX CoolMOS CFD7 650V Webpage:** [www.infineon.com](http://www.infineon.com)
- **IFX CoolMOS CFD7 650V application note:** [www.infineon.com](http://www.infineon.com)
- **IFX CoolMOS CFD7 650V simulation model:** [www.infineon.com](http://www.infineon.com)
- **IFX Design tools:** [www.infineon.com](http://www.infineon.com)

## Revision History

IPW65R029CFD7

**Revision: 2020-07-31, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2020-06-19	Release of final version
2.1	2020-07-31	Increased continuous diode forward current rating

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