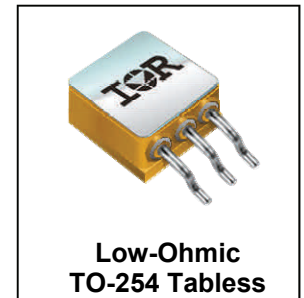


**RADIATION HARDENED  
POWER MOSFET  
SURFACE-MOUNT (Low Ohmic TO-254AA Tabless)**

**100V, N-CHANNEL  
R<sub>5</sub> TECHNOLOGY**

**Product Summary**

Part Number	Radiation Level	RDS(on)	I <sub>D</sub>
IRHMK57160	100 kRads(Si)	0.014Ω	45A*
IRHMK53160	300 kRads(Si)	0.014Ω	45A*
IRHMK55160	500 kRads(Si)	0.014Ω	45A*
IRHMK58160	1000 kRads(Si)	0.015Ω	45A*



**Description**

IRHMK57160 is part of the International Rectifier HiRel family of products. IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for both Total Dose and Single Event Effect (SEE) with useful performance up to LET of 80 (MeV/(mg/cm<sup>2</sup>)). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC-DC converters and motor controllers. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

**Features**

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Surface Mount
- Light Weight
- ESD Rating: Class 3B per MIL-STD-750, Method 1020

**Absolute Maximum Ratings**

**Pre-Irradiation**

	Parameter		Units
I <sub>D</sub> @ V <sub>GS</sub> = 12V, T <sub>C</sub> = 25°C	Continuous Drain Current	45*	A
I <sub>D</sub> @ V <sub>GS</sub> = 12V, T <sub>C</sub> = 100°C	Continuous Drain Current	45*	
I <sub>DM</sub>	Pulsed Drain Current ①	180	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	208	W
	Linear Derating Factor	1.67	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	493	mJ
I <sub>AR</sub>	Avalanche Current ①	45	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	20.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	6.7	V/ns
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	8.0 (Typical)	

\* Current is limited by package

For Footnotes, refer to the page 2.

**Electrical Characteristics @ T<sub>J</sub> = 25°C (Unless Otherwise Specified)**

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance	—	—	0.014	Ω	V <sub>GS</sub> = 12V, I <sub>D</sub> = 45A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1.0mA
G <sub>fs</sub>	Forward Transconductance	42	—	—	S	V <sub>DS</sub> = 15V, I <sub>D</sub> = 45A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	10	μA	V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V
		—	—	25		V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V <sub>GS</sub> = -20V
Q <sub>G</sub>	Total Gate Charge	—	—	160	nC	I <sub>D</sub> = 45A
Q <sub>GS</sub>	Gate-to-Source Charge	—	—	55		V <sub>DS</sub> = 50V
Q <sub>GD</sub>	Gate-to-Drain ('Miller') Charge	—	—	65		V <sub>GS</sub> = 12V
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	35	ns	V <sub>DD</sub> = 50V
t <sub>r</sub>	Rise Time	—	—	125		I <sub>D</sub> = 45A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	75		R <sub>G</sub> = 2.35Ω
t <sub>f</sub>	Fall Time	—	—	50		V <sub>GS</sub> = 12V
L <sub>s</sub> + L <sub>D</sub>	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm /0.25in from package) to Source lead (6mm/0.25in from package) with Source wire internally bonded from Source pin to Drain pad
C <sub>iss</sub>	Input Capacitance	—	6270	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	1620	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	35	—		f = 1.0MHz
R <sub>G</sub>	Internal Gate Resistance	—	1.0	—		f = 1.0MHz, open drain

**Source-Drain Diode Ratings and Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	45*	A	
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	180		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 45A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	—	270	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 45A, V <sub>DD</sub> ≤ 50V
Q <sub>rr</sub>	Reverse Recovery Charge	—	—	2.7	μC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

\* Current is limited by package

**Thermal Resistance**

	Parameter	Min.	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	—	0.60	°C/W
R <sub>θCS</sub>	Case -to-Sink	—	0.21	—	
R <sub>θJA</sub>	Junction-to-Ambient (Typical socket mount)	—	—	48	

**Footnotes:**

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V<sub>DD</sub> = 50V, starting T<sub>J</sub> = 25°C, L = 0.49mH, Peak I<sub>L</sub> = 45A, V<sub>GS</sub> = 12V
- ③ I<sub>SD</sub> ≤ 45A, di/dt ≤ 630A/μs, V<sub>DD</sub> ≤ 100V, T<sub>J</sub> ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
- ⑤ **Total Dose Irradiation with V<sub>GS</sub> Bias.** 12 volt V<sub>GS</sub> applied and V<sub>DS</sub> = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ **Total Dose Irradiation with V<sub>DS</sub> Bias.** 80 volt V<sub>DS</sub> applied and V<sub>GS</sub> = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

**Radiation Characteristics**

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥**

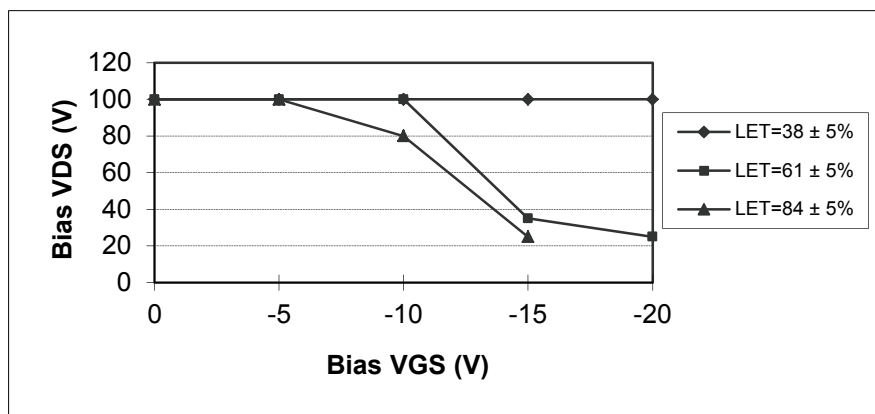
	Parameter	Up to 500 kRads (Si) <sup>1</sup>		1000 kRads (Si) <sup>2</sup>		Units	Test Conditions
		Min.	Max.	Min.	Max.		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	100	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	4.0	1.5	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1.0mA
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	100	—	100	nA	V <sub>GS</sub> = 20V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	-100	—	-100	nA	V <sub>GS</sub> = -20V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	10	—	25	μA	V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V
R <sub>DS(on)</sub>	Static Drain-to-Source On-State ④ Resistance (TO-3)	—	0.013	—	0.014	Ω	V <sub>GS</sub> = 12V, I <sub>D</sub> = 45A
R <sub>DS(on)</sub>	Static Drain-to-Source On-State ④ Resistance (TO-254AA Tabless)	—	0.014	—	0.015	Ω	V <sub>GS</sub> = 12V, I <sub>D</sub> = 45A
V <sub>SD</sub>	Diode Forward Voltage ④	—	1.2	—	1.2	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 45A

1. Part numbers IRHMK57160, IRHMK53160 and IRHMK55160
2. Part number IRHMK58160

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

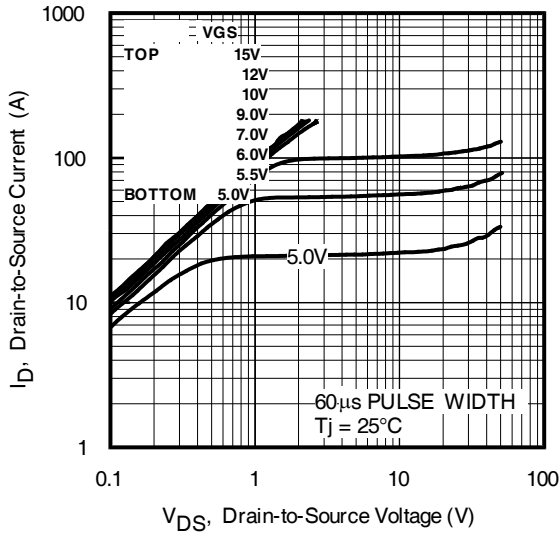
**Table 2. Typical Single Event Effect Safe Operating Area**

LET (MeV/(mg/cm <sup>2</sup> ))	Energy (MeV)	Range (μm)	VDS (V)				
			@ VGS = 0V	@ VGS=-5V	@ VGS=-10V	@ VGS =-15V	@ VGS=-20V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	100	100	100	100	100
61 ± 5%	330 ± 7.5%	31 ± 10%	100	100	100	35	25
84 ± 5%	350 ± 7.5%	28 ± 7.5%	100	100	80	25	—

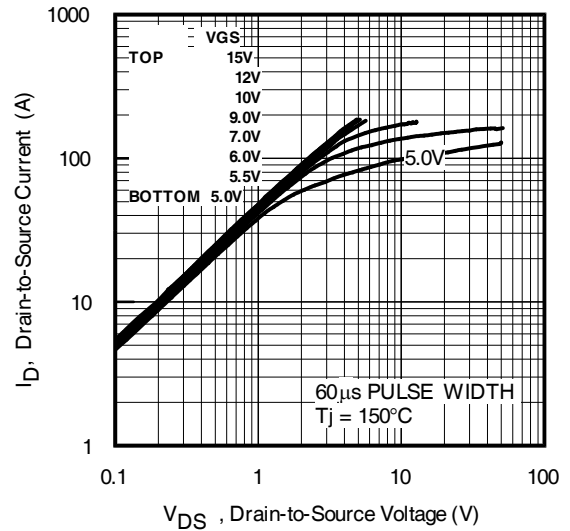


**Fig a. Typical Single Event Effect, Safe Operating Area**

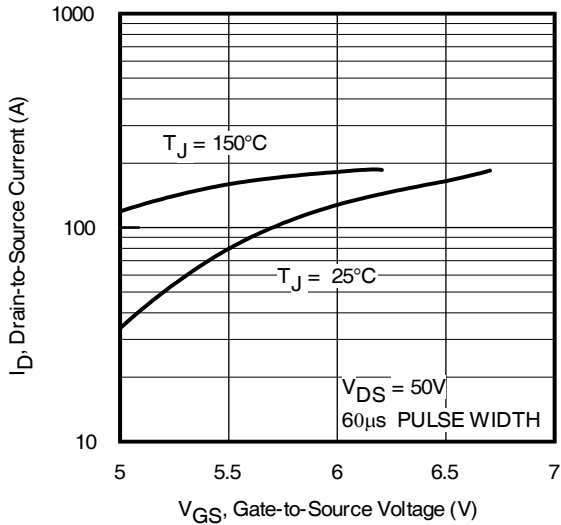
For Footnotes, refer to the page 2.



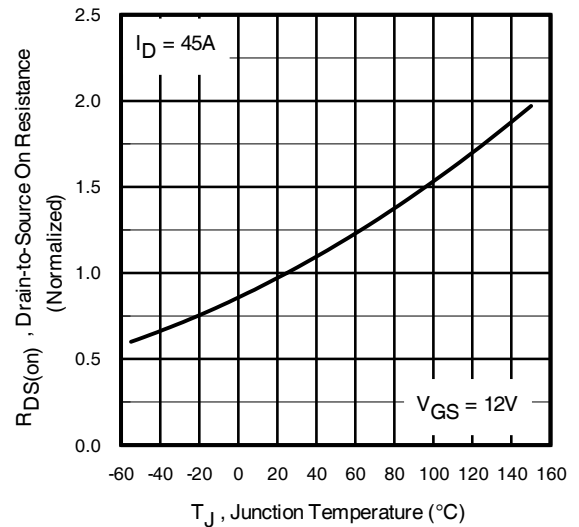
**Fig 1. Typical Output Characteristics**



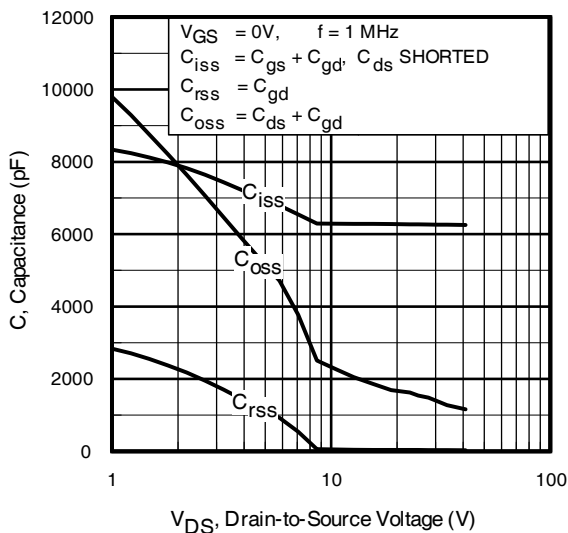
**Fig 2. Typical Output Characteristics**



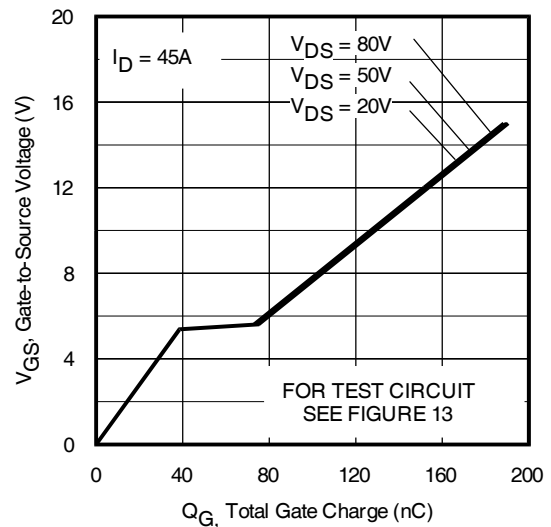
**Fig 3. Typical Transfer Characteristics**



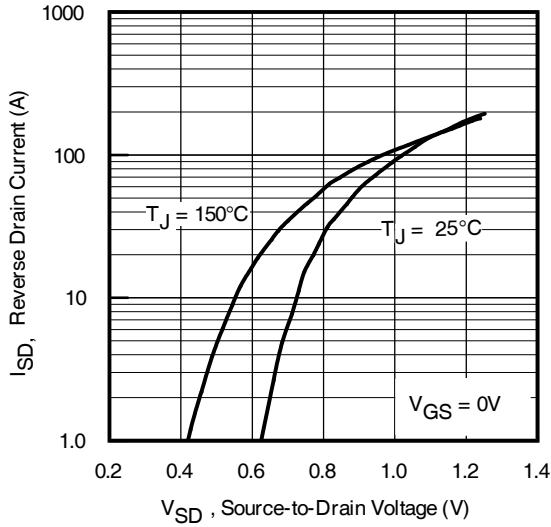
**Fig 4. Normalized On-Resistance Vs. Temperature**



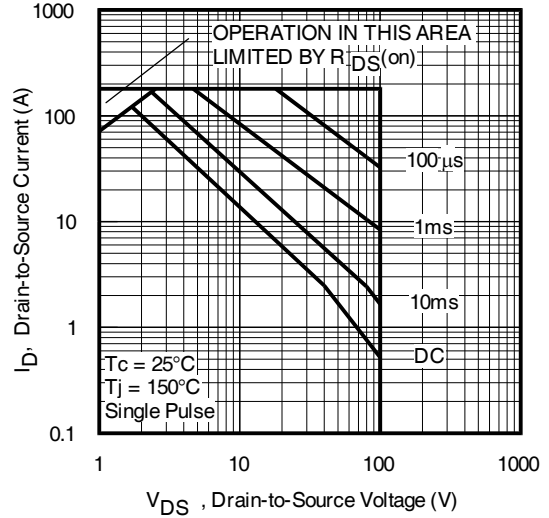
**Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage**



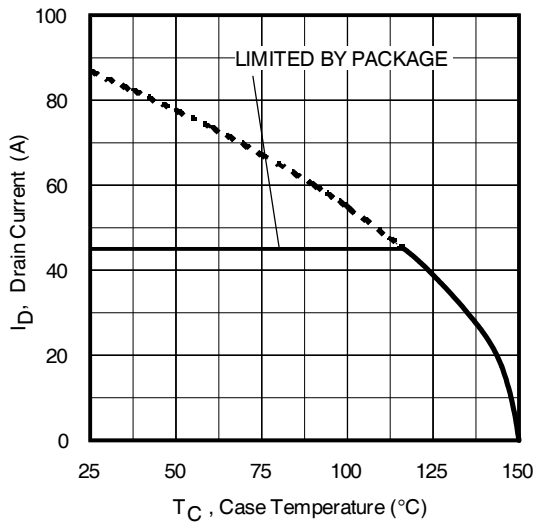
**Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage**



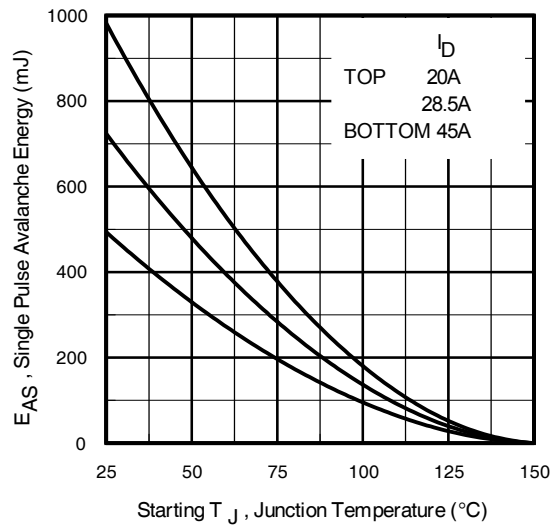
**Fig 7.** Typical Source-Drain Diode Forward Voltage



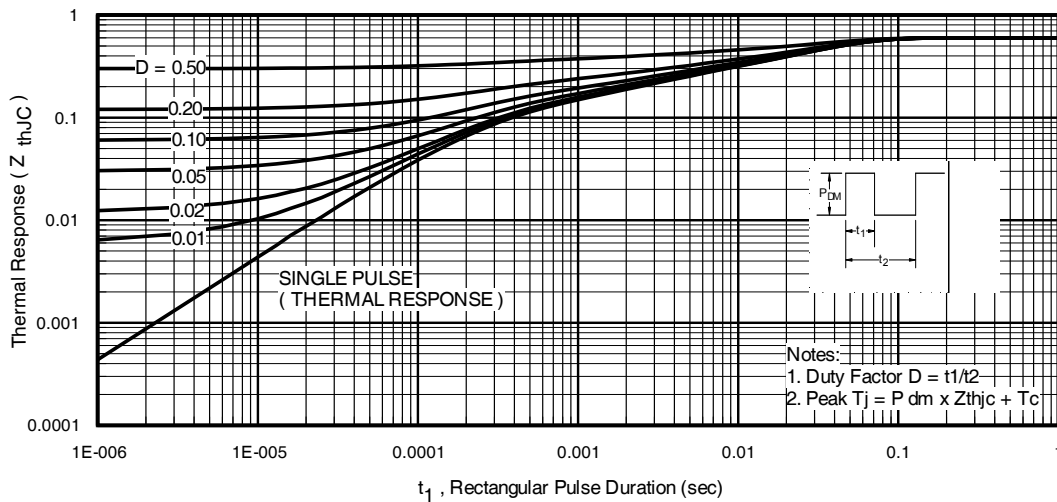
**Fig 8.** Maximum Safe Operating Area



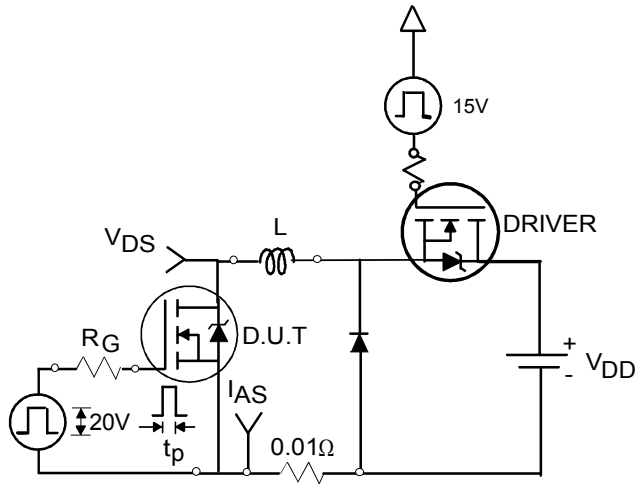
**Fig 9.** Maximum Drain Current Vs. Case Temperature



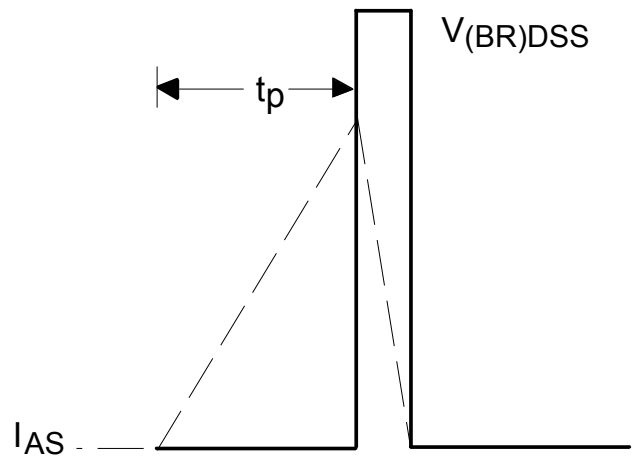
**Fig 10.** Maximum Avalanche Energy Vs. Drain Current



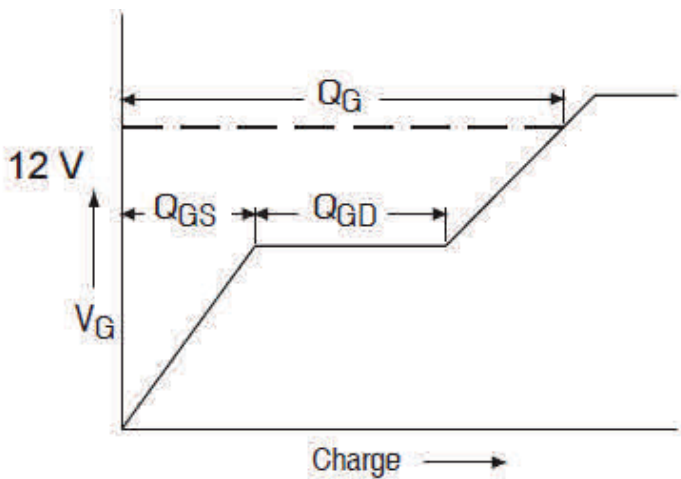
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



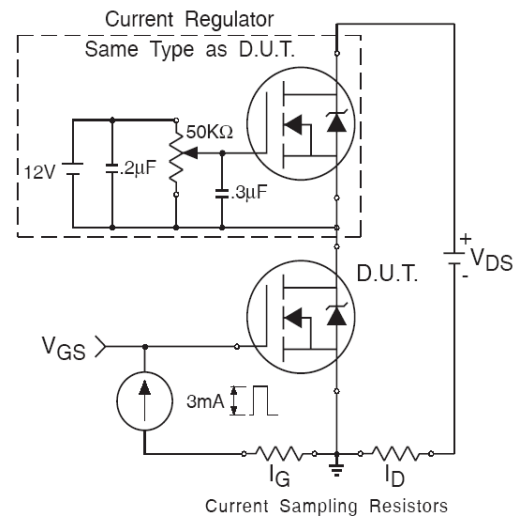
**Fig 12a.** Unclamped Inductive Test Circuit



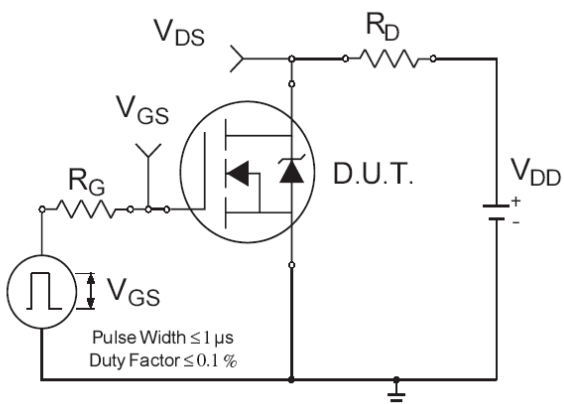
**Fig 12b.** Unclamped Inductive Waveforms



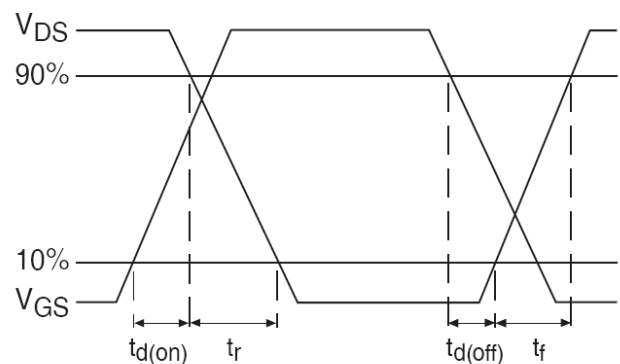
**Fig 13a.** Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

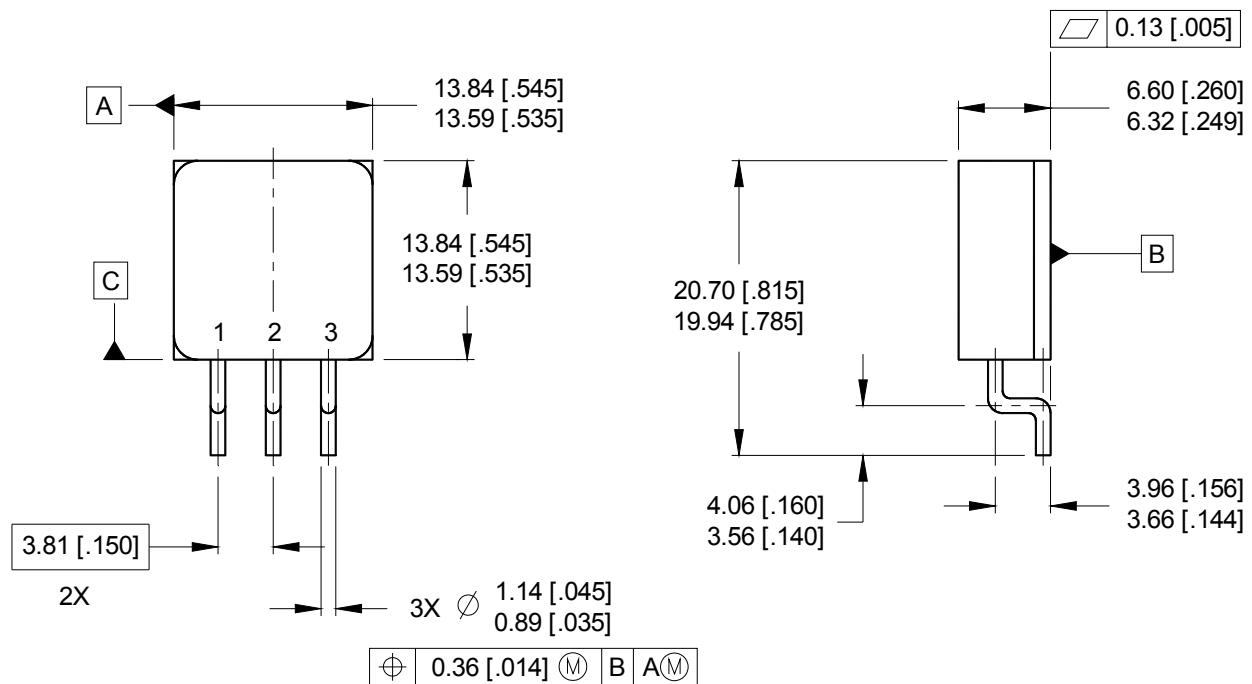


**Fig 14a.** Switching Time Test Circuit



**Fig 14b.** Switching Time Waveforms

**Case Outline and Dimensions — Low-Ohmic TO-254AA Tabless**



**NOTES:**

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-254AA.

**PIN ASSIGNMENTS**

- 1 = DRAIN
- 2 = SOURCE
- 3 = GATE

**BERYLLIA WARNING PER MIL-PRF-19500**

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

### **IMPORTANT NOTICE**

The information given in this document shall be in no event regarded as guarantee of conditions or characteristic. The data contained herein is a characterization of the component based on internal standards and is intended to demonstrate and provide guidance for typical part performance. It will require further evaluation, qualification and analysis to determine suitability in the application environment to confirm compliance to your system requirements.

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