

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS E6

650V CoolMOS™ E6 Power Transistor
IPx65R190E6

Data Sheet

Rev. 2.1, 2018-02-28
Final

Industrial & Multimarket

650V CoolMOS™ E6 Power Transistor

IPA65R190E6, IPB65R190E6
 IPI65R190E6, IPP65R190E6
 IPW65R190E6

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ E6 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The offered devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter, and cooler.

Features

- Extremely low losses due to very low FOM $R_{\text{son}} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- JEDEC¹⁾ qualified, Pb-free plating, Halogen free

Applications

PFC stages, hard switching PWM stages and resonant switching PWM stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

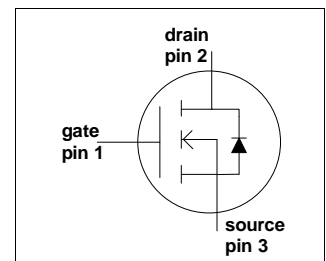
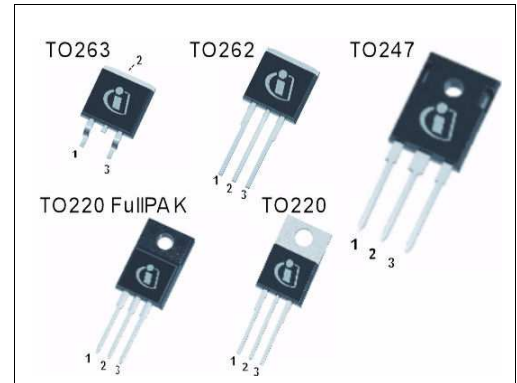


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{\text{DS}} @ T_{\text{j,max}}$	700	V
$R_{\text{DS(on),max}}$	0.19	Ω
$Q_{\text{g,typ}}$	73	nC
$I_{\text{D,pulse}}$	66	A
$E_{\text{oss}} @ 400\text{V}$	5.9	μJ
Body diode di/dt	500	$\text{A}/\mu\text{s}$

Type / Ordering Code	Package	Marking	Related Links
IPW65R190E6	PG-TO247	65E6190	IFX CoolMOS Webpage IFX Design tools
IPB65R190E6	PG-TO263		
IPI65R190E6	PG-TO262		
IPP65R190E6	PG-TO220		
IPA65R190E6	PG-TO220 FullPAK		

1) J-STD20 and JESD22

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2 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	20.2	A	$T_C = 25\text{ °C}$
				12.8		$T_C = 100\text{ °C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	66	A	$T_C = 25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	485	mJ	$I_D = 3.5\text{ A}, V_{DD} = 50\text{ V}$
Avalanche energy, repetitive	E_{AR}	-	-	0.73		$I_D = 3.5\text{ A}, V_{DD} = 50\text{ V}$
Avalanche current, repetitive	I_{AR}	-	-	3.5	A	
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS} = 0 \dots 480\text{ V}$
Gate source voltage	V_{GS}	-20	-	20	V	static
		-30		30		AC ($f > 1\text{ Hz}$)
Power dissipation for TO-220, TO-247, TO-262, TO-263	P_{tot}	-	-	151	W	$T_C = 25\text{ °C}$
Power dissipation for TO-220 FullPAK	P_{tot}	-	-	34		
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	
Mounting torque TO-220, TO-247		-	-	60	Ncm	M3 and M3.5 screws
Mounting torque TO-220 FullPAK				50		M2.5 screws
Continuous diode forward current	I_S	-	-	17.5	A	$T_C = 25\text{ °C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	66	A	$T_C = 25\text{ °C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS} = 0 \dots 400\text{ V}, I_{SD} \leq I_D,$ $T_j = 25\text{ °C}$
Maximum diode commutation speed ³⁾	di/dt			500	A/ μs	

1) Limited by $T_{j,max}$. Maximum duty cycle $D = 0.75$

2) Pulse width t_p limited by $T_{j,max}$

3) Identical low side and high side switch with identical R_G

3 Thermal characteristics

Table 3 Thermal characteristics non FullPAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.83	°C/W	leaded
Thermal resistance, junction - ambient	R_{thJA}	-	-	62		
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6 mm (0.063 in.) from case for 10 s

Table 4 Thermal characteristics FullPAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.7	°C/W	leaded
Thermal resistance, junction - ambient	R_{thJA}	-	-	80		
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6 mm (0.063 in.) from case for 10 s

Table 5 Thermal characteristics SMD

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.83	°C/W	SMD version, device on PCB, minimal footprint
Thermal resistance, junction - ambient	R_{thJA}	-	-	62		
		-	35	-		
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

1) Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70µm) for drain connection. PCB is vertical without air stream cooling.

4 Electrical characteristics

Electrical characteristics, at $T_J=25\text{ °C}$, unless otherwise specified.

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1.0\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5		$V_{DS}=V_{GS}$, $I_D=0.73\text{ mA}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=650\text{ V}$, $V_{GS}=0\text{ V}$, $T_J=25\text{ °C}$
		-	10	-		$V_{DS}=650\text{ V}$, $V_{GS}=0\text{ V}$, $T_J=150\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.17	0.19	Ω	$V_{GS}=10\text{ V}$, $I_D=7.3\text{ A}$, $T_J=25\text{ °C}$
		-	0.44	-		$V_{GS}=10\text{ V}$, $I_D=7.3\text{ A}$, $T_J=150\text{ °C}$
Gate resistance	R_G	-	6	-	Ω	$f=1\text{ MHz}$, open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1620	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	98	-		
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	65	-		
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	308	-		$I_D=\text{constant}$, $V_{GS}=0\text{ V}$, $V_{DS}=0\dots480\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	12	-	ns	$V_{DD}=400\text{ V}$, $V_{GS}=13\text{ V}$, $I_D=11\text{ A}$, $R_G=3.4\text{ }\Omega$
Rise time	t_r	-	11	-		
Turn-off delay time	$t_{d(off)}$	-	112	-		
Fall time	t_f	-	10	-		

1) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

2) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	8.9	-	nC	$V_{DD}=480\text{ V}$, $I_D=11\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	38	-		
Gate charge total	Q_g	-	73	-		
Gate plateau voltage	$V_{plateau}$	-	5.5	-	V	

Table 9 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0\text{ V}$, $I_F=11\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	410	-	ns	$V_R=400\text{ V}$, $I_F=11\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	6.1	-	μC	
Peak reverse recovery current	I_{rrm}	-	28	-	A	

5 Electrical characteristics diagrams

Table 10

Power dissipation Non FullPAK	Power dissipation FullPAK
$P_{tot} = f(T_c)$	$P_{tot} = f(T_c)$

Table 11

Max. transient thermal impedance Non FullPAK	Max. transient thermal impedance FullPAK
$Z_{(thJC)} = f(t_p)$; parameter: $D = t_p/T$	$Z_{(thJC)} = f(t_p)$; parameter: $D = t_p/T$

Electrical characteristics diagrams

Table 12

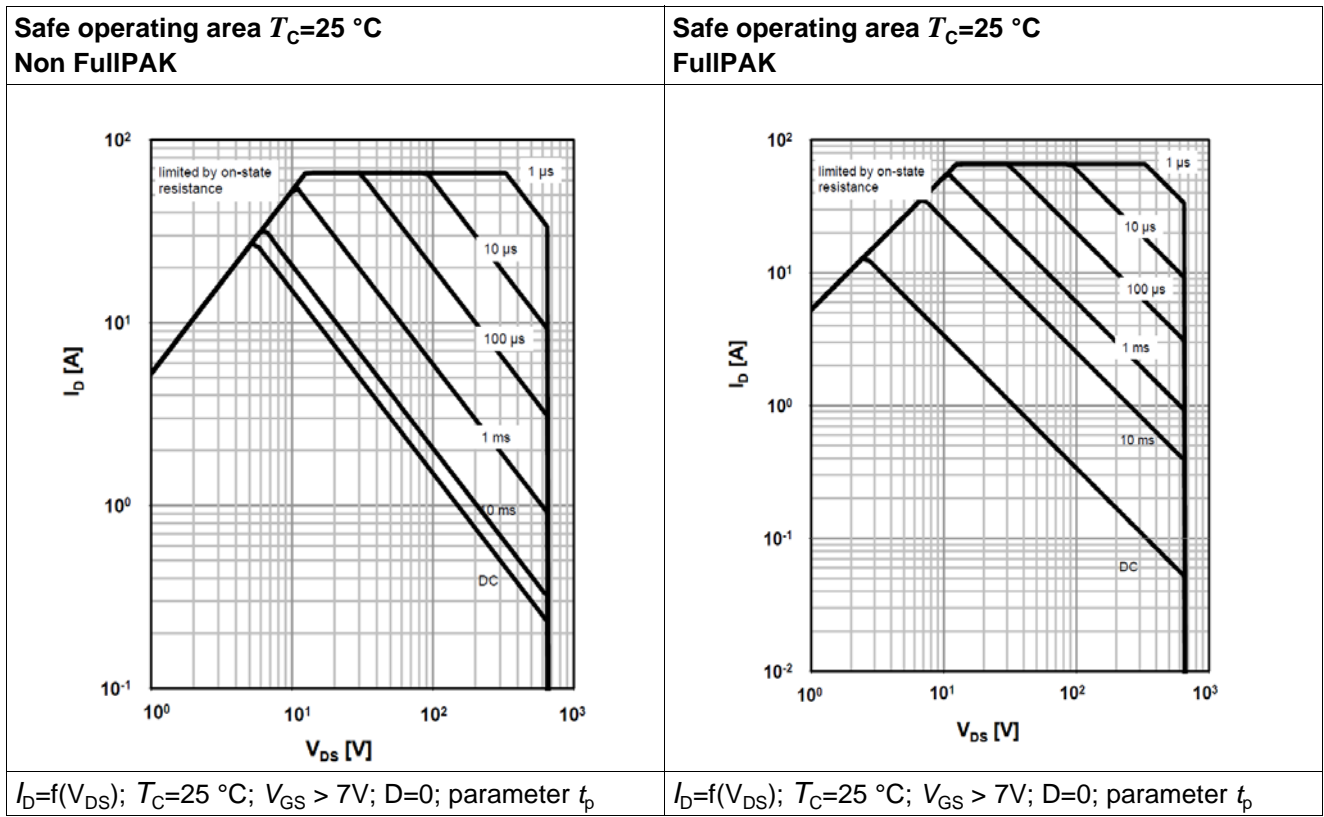


Table 13

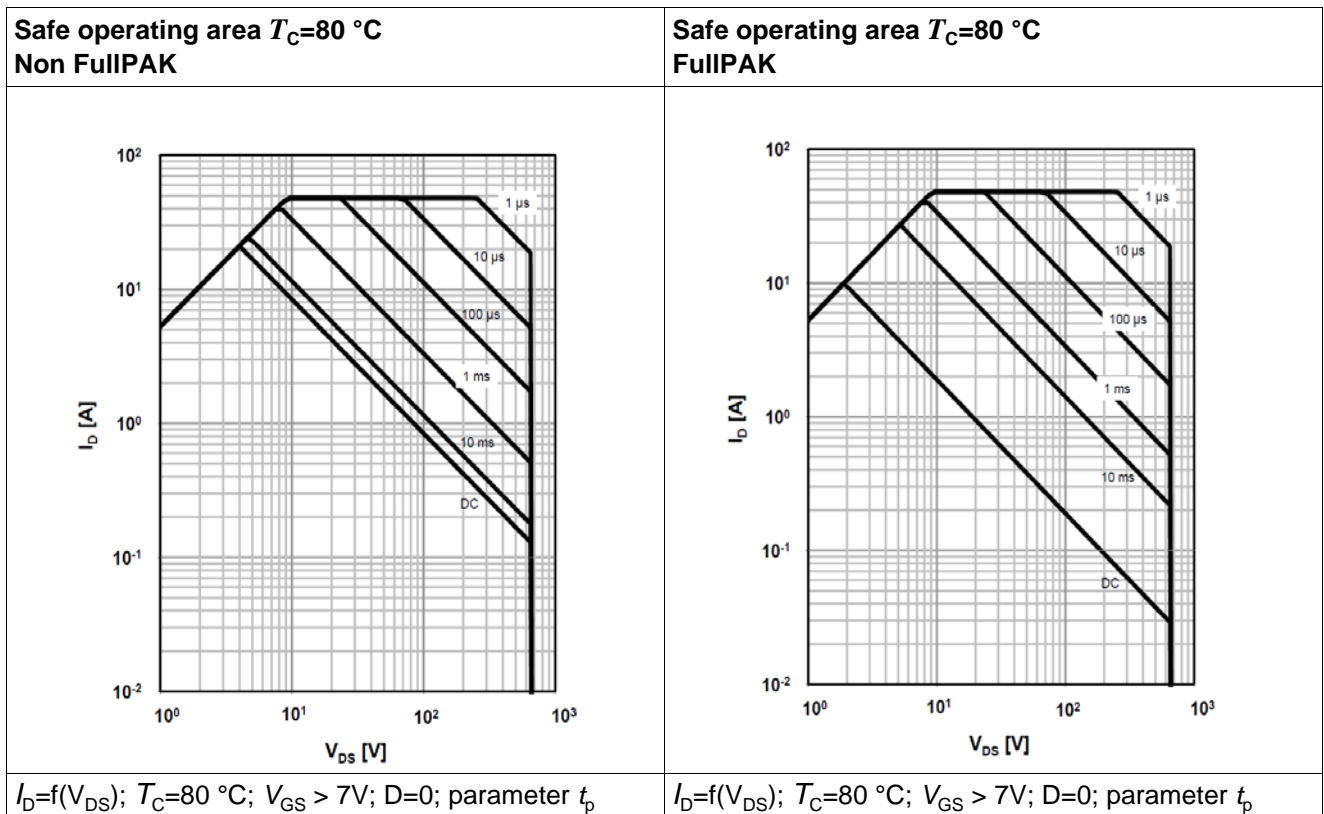


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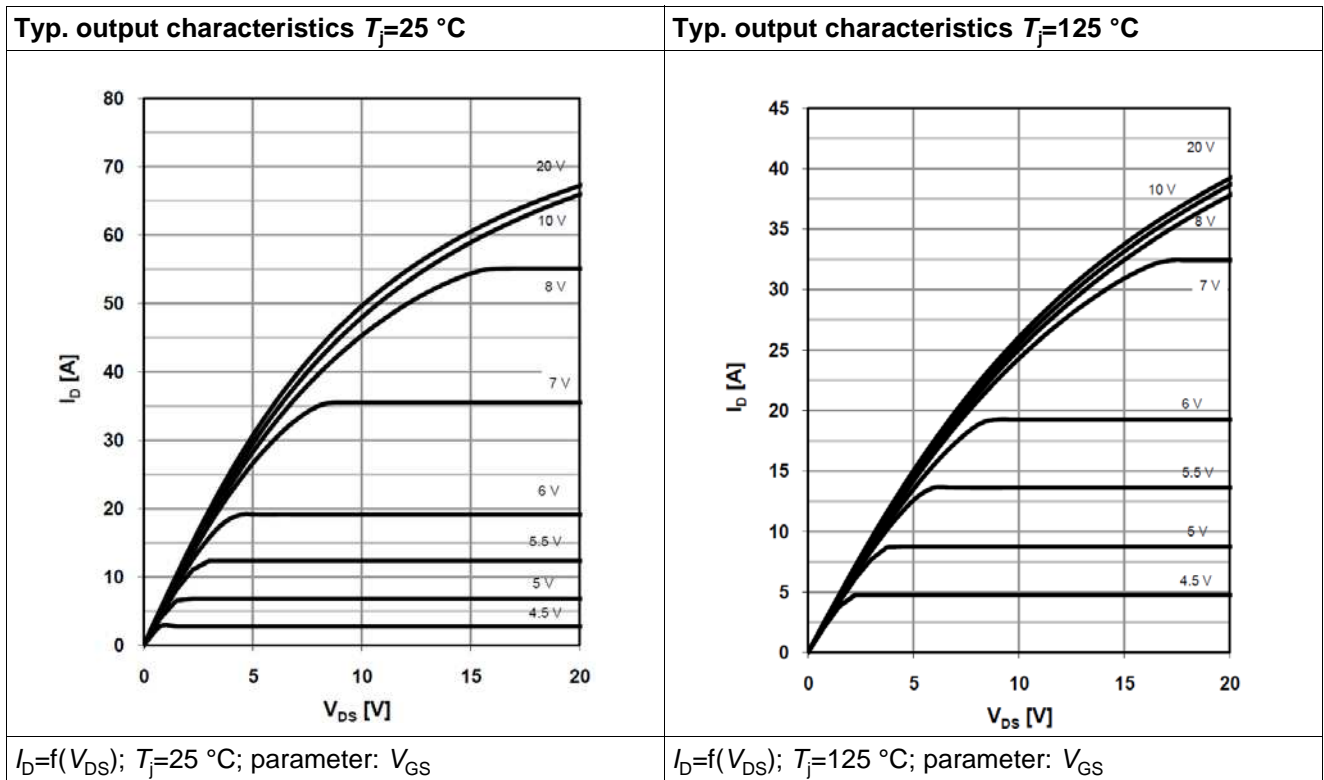


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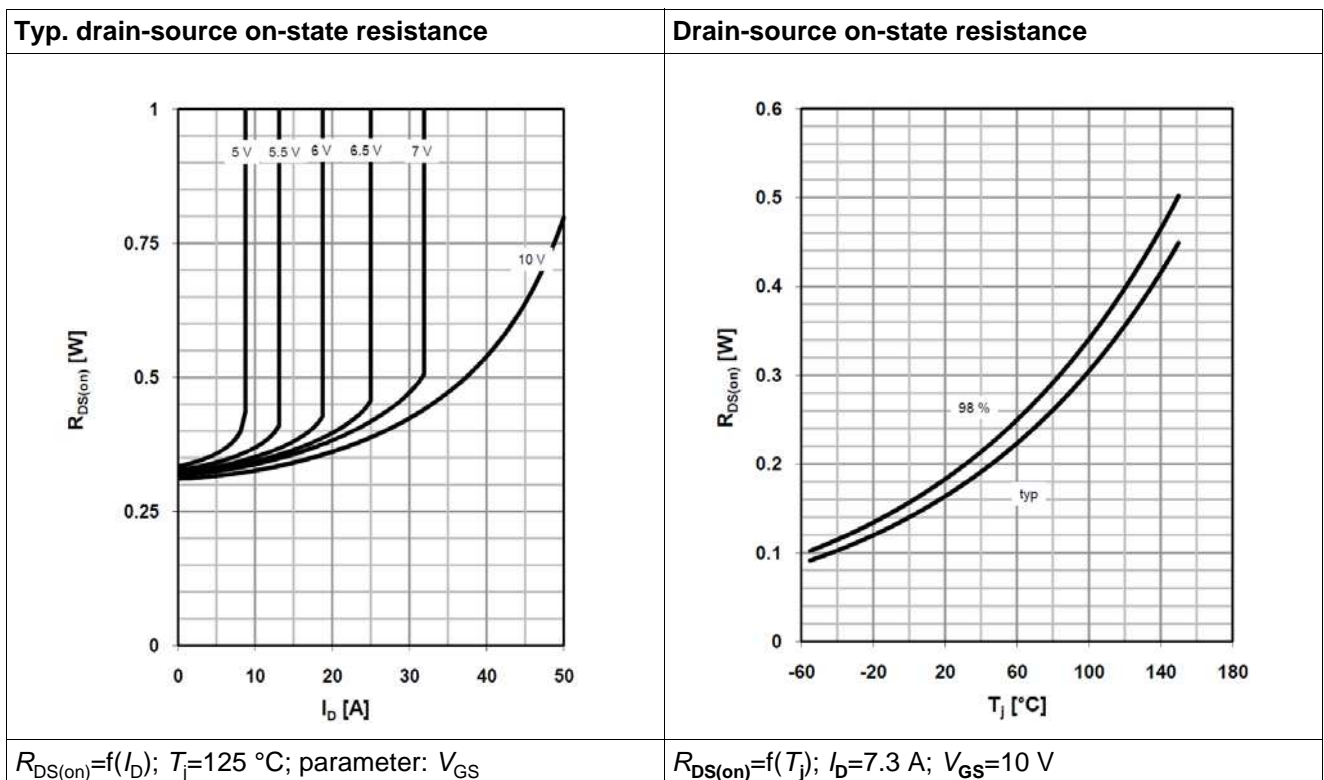


Table 16

Typ. transfer characteristics	Typ. gate charge
$I_D=f(V_{GS}); V_{DS}=20V$	$V_{GS}=f(Q_{gate}), I_D=11\text{ A pulsed}$

Table 17

Avalanche energy	Drain-source breakdown voltage
$E_{AS}=f(T_j); I_D=3.5\text{ A}; V_{DD}=50\text{ V}$	$V_{BR(DSS)}=f(T_j); I_D=1.0\text{ mA}$

Table 18

Typ. capacitances	Typ. C_{oss} stored energy
<p>A semi-logarithmic plot showing capacitance C [pF] on the y-axis (log scale from 10⁰ to 10⁵) versus drain-source voltage V_{DS} [V] on the x-axis (linear scale from 0 to 600). Three curves are shown: C_{iss} (input capacitance) is constant at approximately 2 × 10³ pF; C_{oss} (output capacitance) starts at ~10⁴ pF at 0 V and decreases to ~10¹ pF at 600 V; C_{rss} (reverse transfer capacitance) starts at ~10⁴ pF at 0 V, drops to a minimum of ~10¹ pF at ~100 V, and then slightly increases to ~10² pF at 600 V.</p>	<p>A linear plot showing stored energy E_{oss} [μJ] on the y-axis (linear scale from 0 to 4) versus drain-source voltage V_{DS} [V] on the x-axis (linear scale from 0 to 600). The curve shows that E_{oss} increases with V_{DS}, reaching approximately 4 μJ at 250 V.</p>
<p>$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$</p>	<p>$E_{Oss}=f(V_{DS})$</p>

Table 19

Forward characteristics of reverse diode
<p>A semi-logarithmic plot showing forward current I_F [A] on the y-axis (log scale from 10⁻¹ to 10²) versus reverse diode voltage V_{SD} [V] on the x-axis (linear scale from 0 to 2). Two curves are shown for different temperatures: 125 °C and 25 °C. Both curves show an exponential relationship between current and voltage, with the 125 °C curve shifted to the left of the 25 °C curve, indicating higher current for the same voltage at higher temperature.</p>
<p>$I_F=f(V_{SD}); \text{parameter: } T_j$</p>

6 Test circuits

Table 20 Switching times test circuit and waveform for inductive load

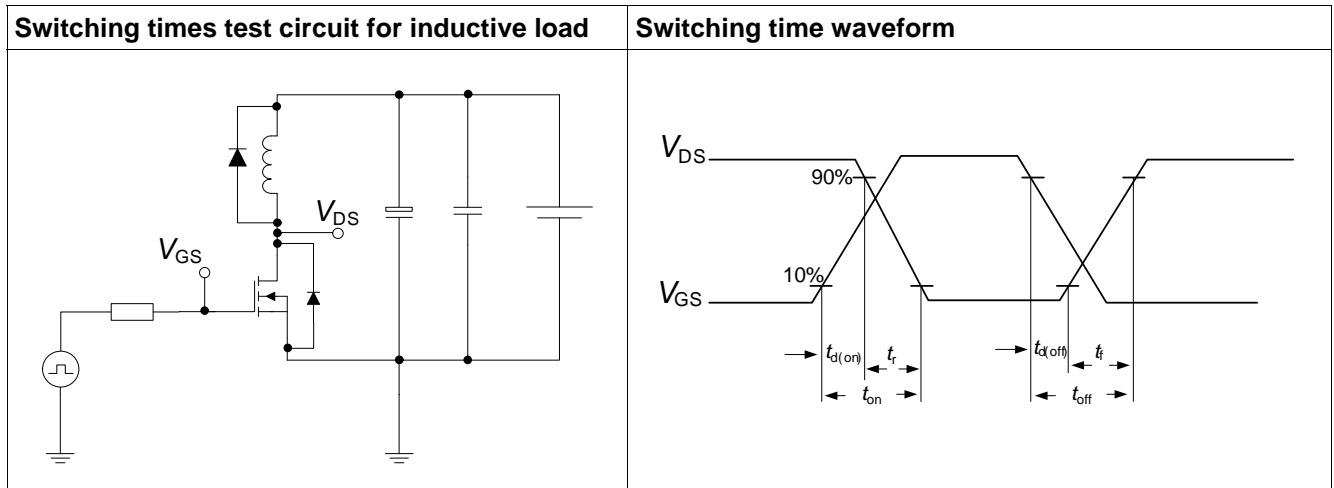


Table 21 Unclamped inductive load test circuit and waveform

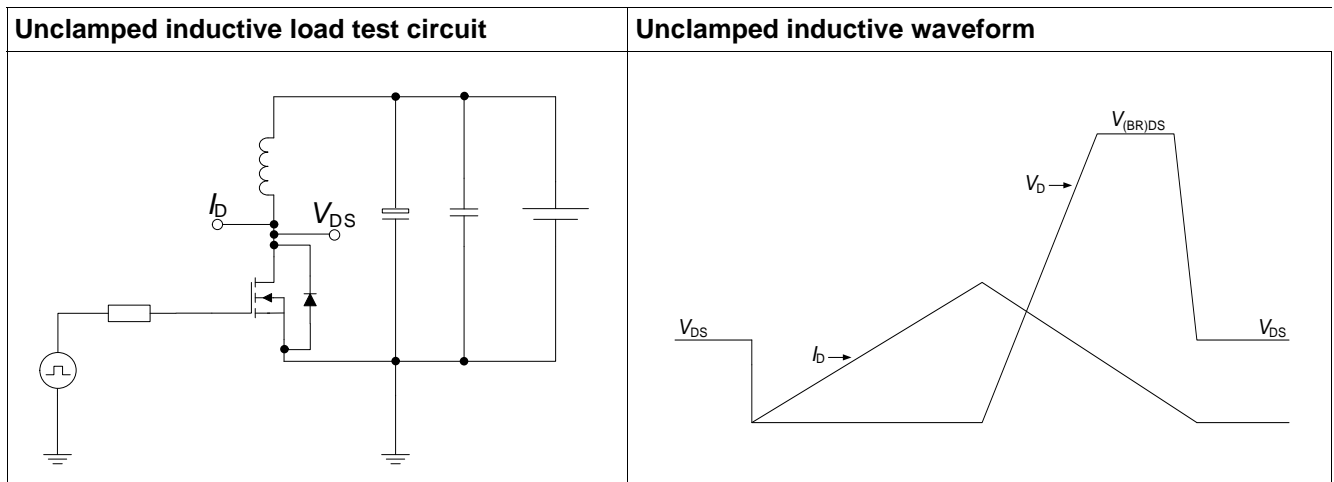
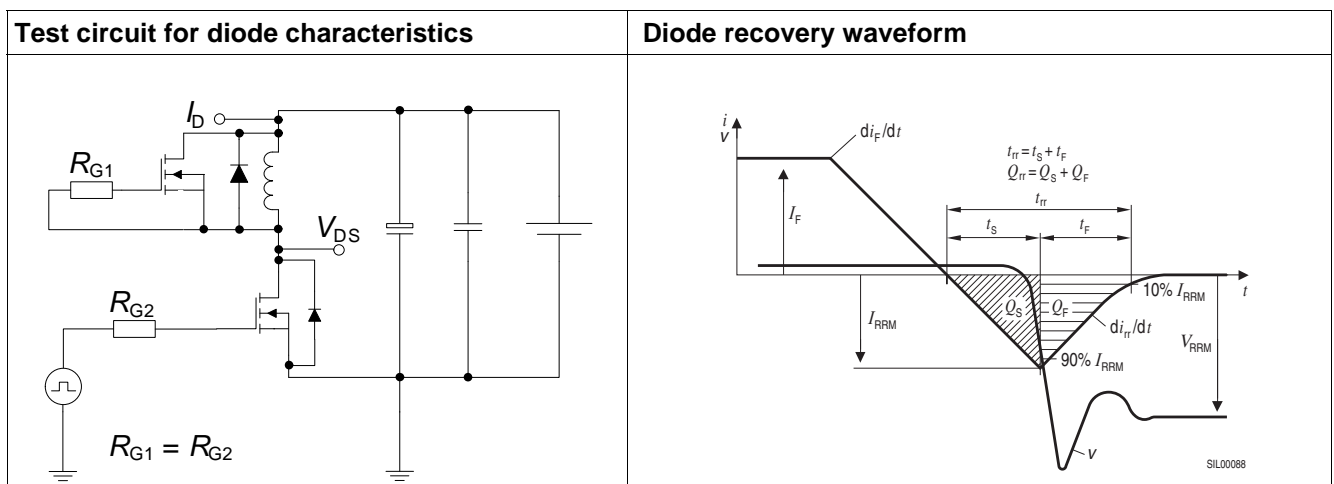


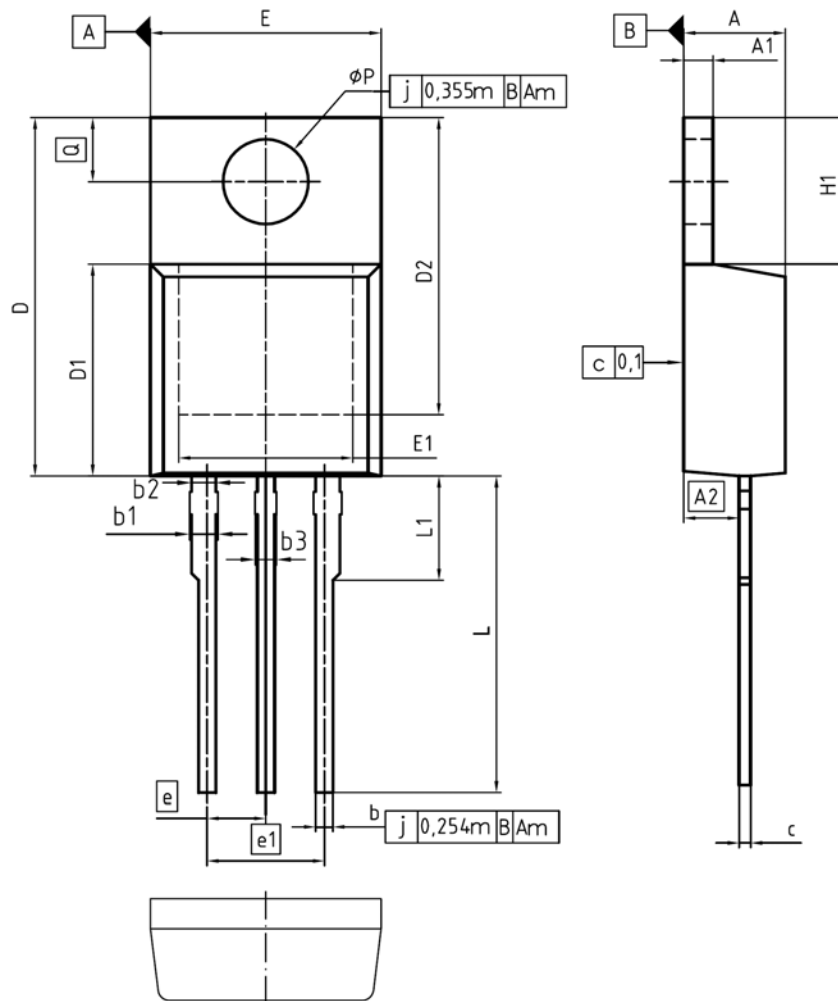
Table 22 Test circuit and waveform for diode characteristics



7 Package outlines



Figure 1 Outlines TO-247, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

DOCUMENT NO.
Z8B00003318

SCALE

EUROPEAN PROJECTION

ISSUE DATE
23-08-2007

REVISION
05

Figure 2 Outlines TO-220, dimensions in mm/inches

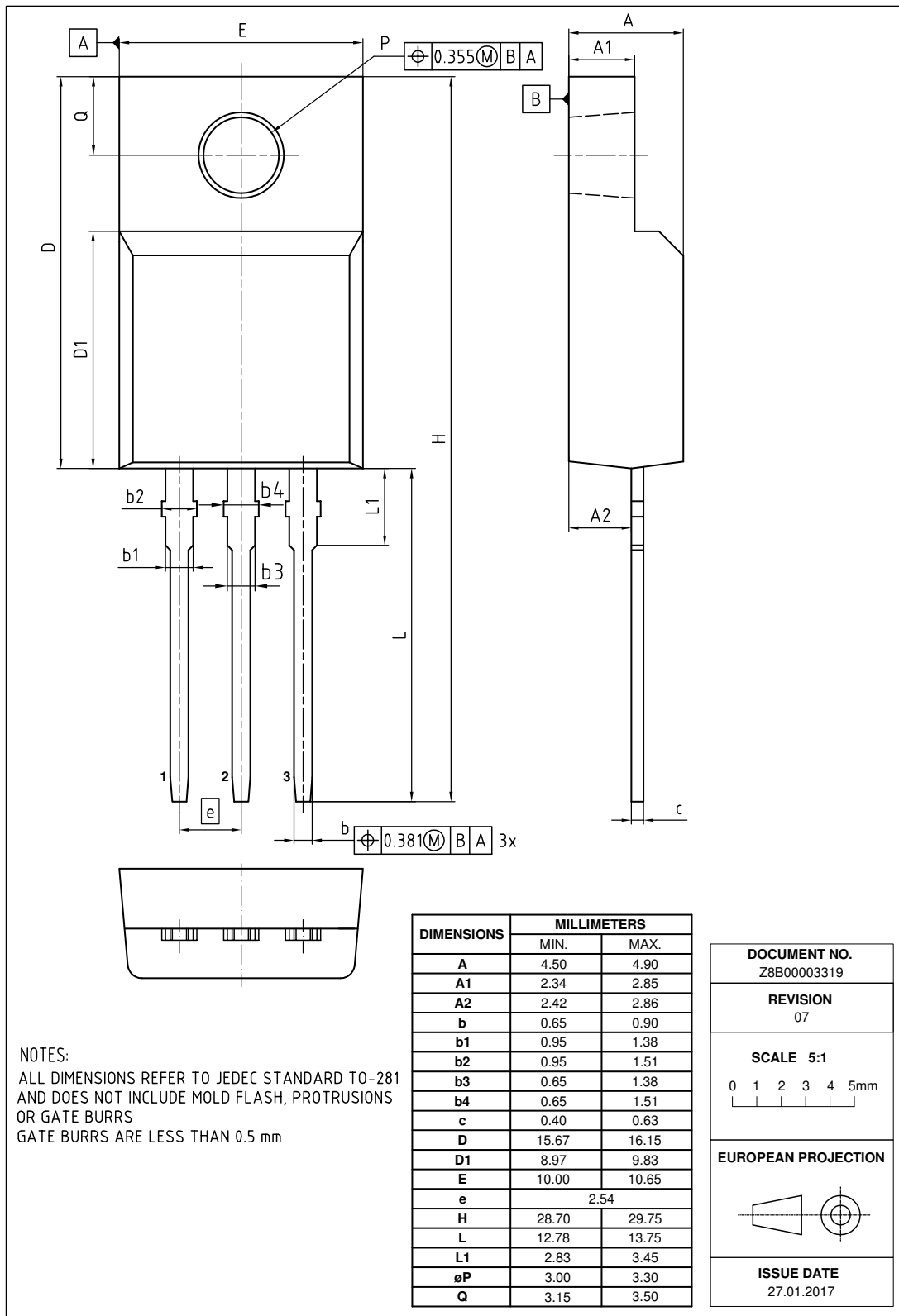
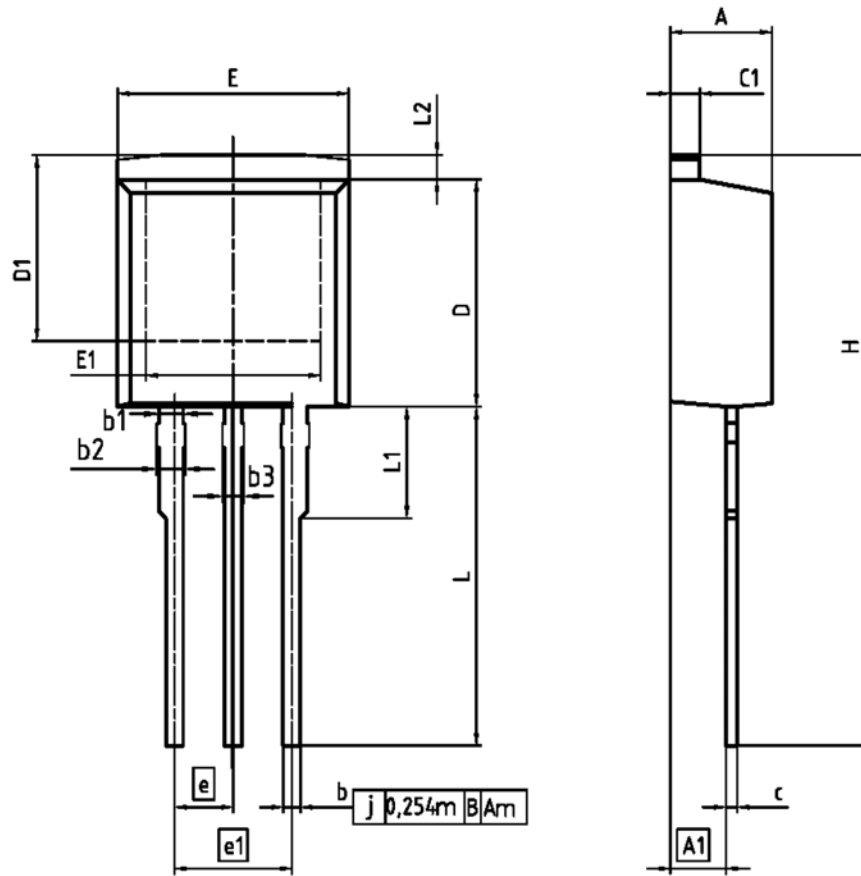


Figure 3 Outlines TO-220 FullPAK, dimensions in mm



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.300	4.572	0.169	0.180
A1	2.150	2.718	0.085	0.107
b	0.650	0.864	0.026	0.034
b1	0.950	1.093	0.037	0.043
b2	0.950	1.400	0.037	0.055
b3	0.850	1.118	0.026	0.044
c	0.330	0.600	0.013	0.024
c1	1.170	1.400	0.046	0.055
D	8.509	9.450	0.335	0.372
D1	6.900	-	0.272	-
E	9.700	10.383	0.382	0.408
E1	6.500	8.600	0.256	0.339
e	2.540		0.100	
e1	5.080		0.200	
N	3		3	
L	13.000	14.000	0.512	0.551
L1	-	4.800	-	0.189
L2	-	1.727	-	0.068

REFERENCE
JEDEC TO262

SCALE

EUROPEAN PROJECTION

ISSUE DATE
05-05-2006

FILE
TO262_1

Figure 4 Outlines TO-262, dimensions in mm/inches

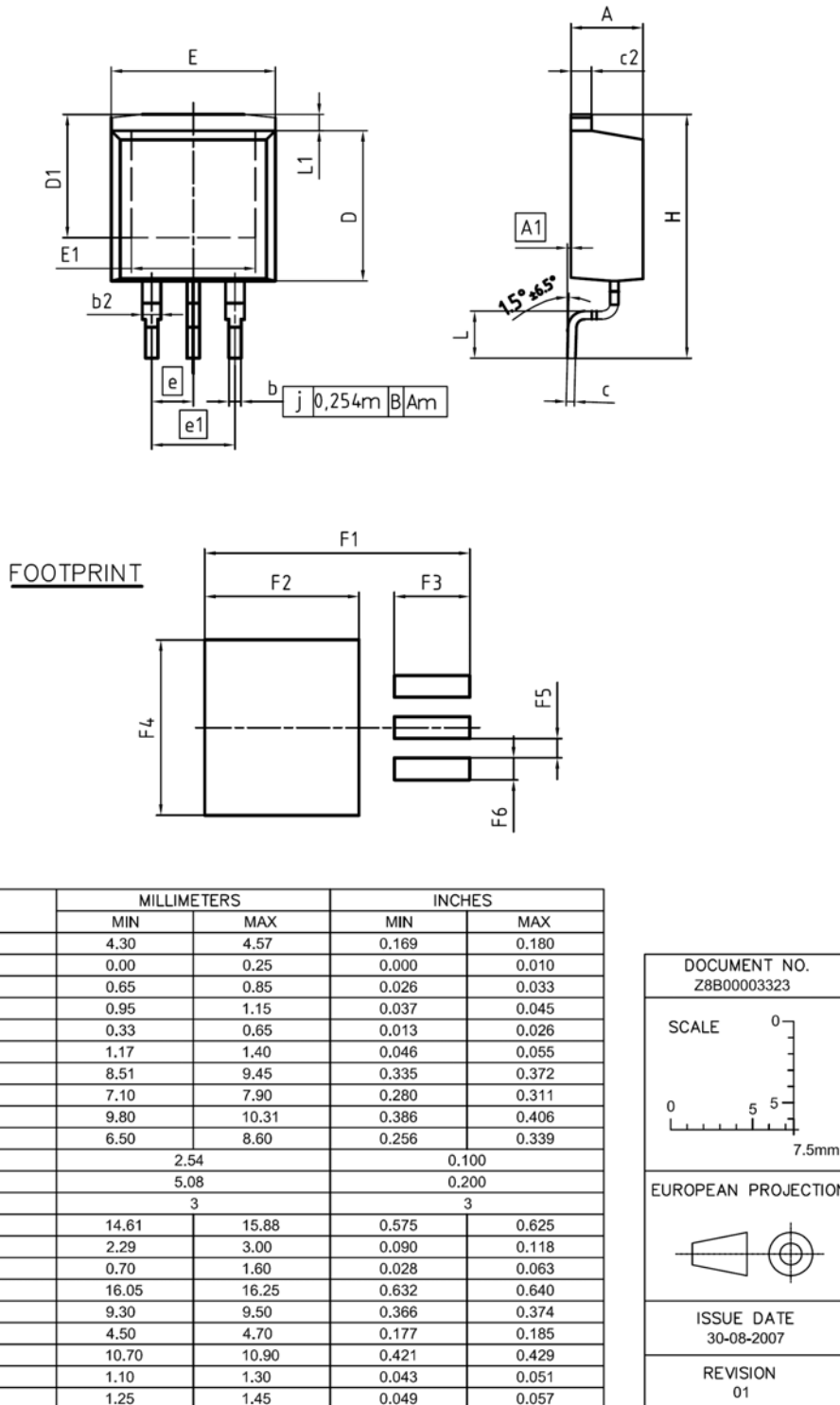


Figure 5 Outlines TO-263, dimensions in mm/inches

650V CoolMOS™ E6 Power Transistor

IPx65R190E6

Revision History

IPx65R190E6

Revision: 2018-03-05, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.1	2018-03-05	Outline PG-TO-220 FullPAK update

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