

# IRFP140NPbF

## HEXFET® Power MOSFET

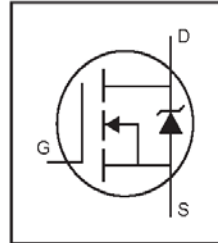
- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

- Lead-Free

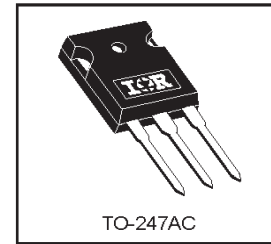
### Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.



$V_{DSS} = 100V$
$R_{DS(on)} = 0.052\Omega$
$I_D = 33A$



### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑤	33	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑤	23	
$I_{DM}$	Pulsed Drain Current ①⑤	110	
$P_D @ T_C = 25^\circ C$	Power Dissipation	140	W
	Linear Derating Factor	0.91	W/°C
$V_{GS}$	Gate-to-Source Voltage	±20	V
$E_{AS}$	Single Pulse Avalanche Energy ②⑤	300	mJ
$I_{AR}$	Avalanche Current①	16	A
$E_{AR}$	Repetitive Avalanche Energy①	14	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
$T_J$	Operating Junction and Storage Temperature Range	-55 to +175	°C
$T_{STG}$			
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

### Thermal Resistance

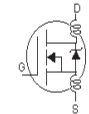
	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	40	

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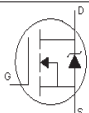
## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to $25^\circ\text{C}$ , $I_D = 1mA$ ⓐ
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.052	$\Omega$	$V_{GS} = 10V, I_D = 16A$ ⓐ
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	11	—	—	S	$V_{DS} = 50V, I_D = 16A$ ⓐ
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$Q_g$	Total Gate Charge	—	—	94	nC	$I_D = 16A$
$Q_{gs}$	Gate-to-Source Charge	—	—	15		$V_{DS} = 80V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	43		$V_{GS} = 10V$ , See Fig. 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	8.2	—	ns	$V_{DD} = 50V$
$t_r$	Rise Time	—	39	—		$I_D = 16A$
$t_{d(off)}$	Turn-Off Delay Time	—	44	—		$R_G = 5.1\Omega$
$t_f$	Fall Time	—	33	—		$R_D = 3.0\Omega$ , See Fig. 10 ④⑤
$L_D$	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	13	—		
$C_{iss}$	Input Capacitance	—	1400	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	330	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	170	—		$f = 1.0\text{MHz}$ , See Fig. 5⑤



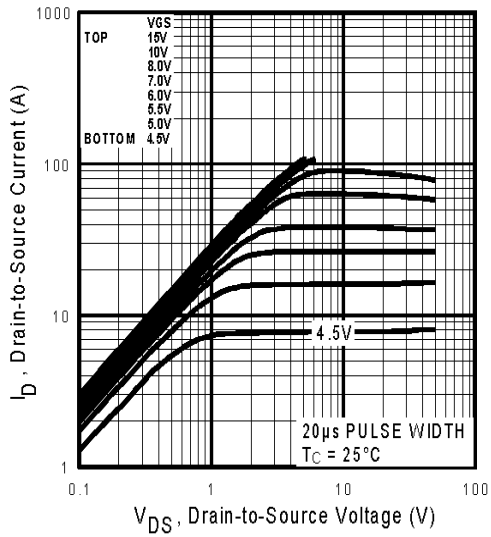
## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	33	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①⑤	—	—	110		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 16A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	170	250	ns	$T_J = 25^\circ\text{C}, I_F = 16A$
$Q_{rr}$	Reverse Recovery Charge	—	1.1	1.6	$\mu C$	$di/dt = 100A/\mu s$ ④⑤

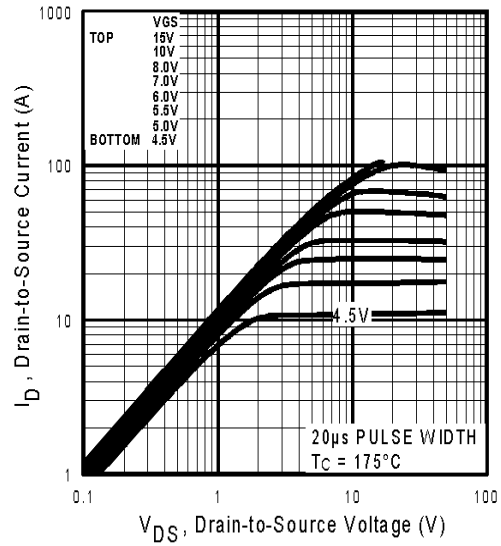


### Notes:

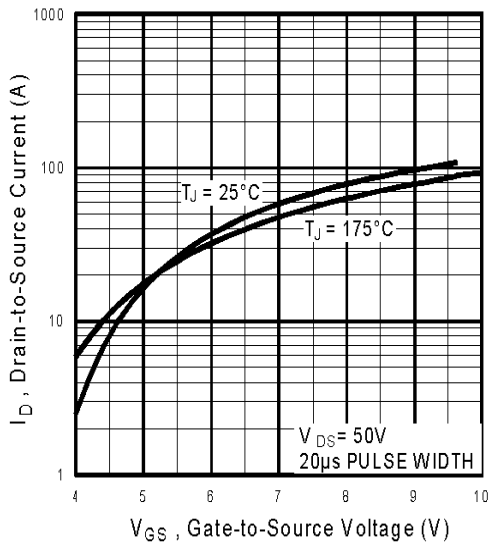
- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ②  $V_{DD} = 25V$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 2.0\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 16A$ . (See Figure 12)
- ③  $I_{SD} \leq 16A$ ,  $di/dt \leq 210A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤ Uses IRF540N data and test conditions.



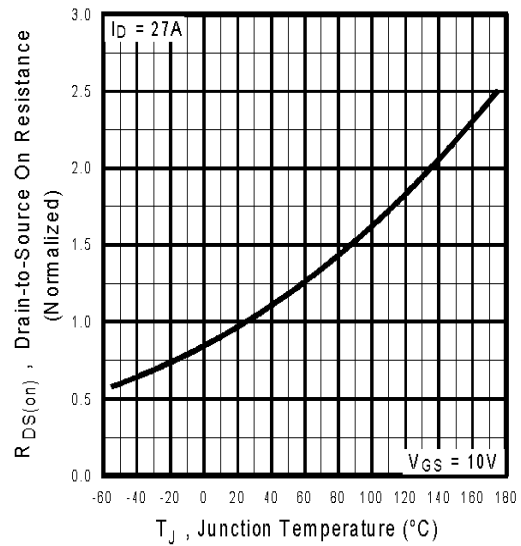
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics

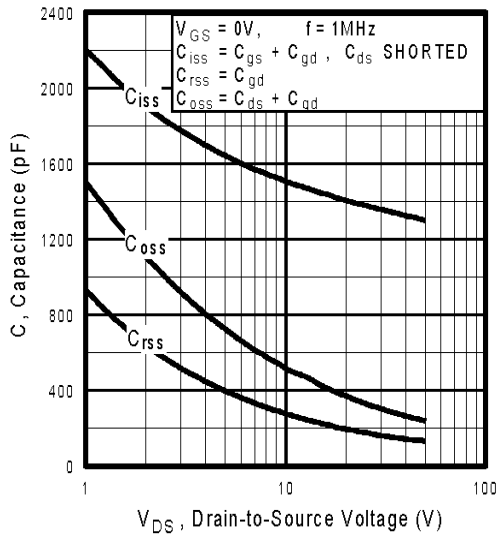


**Fig 3.** Typical Transfer Characteristics

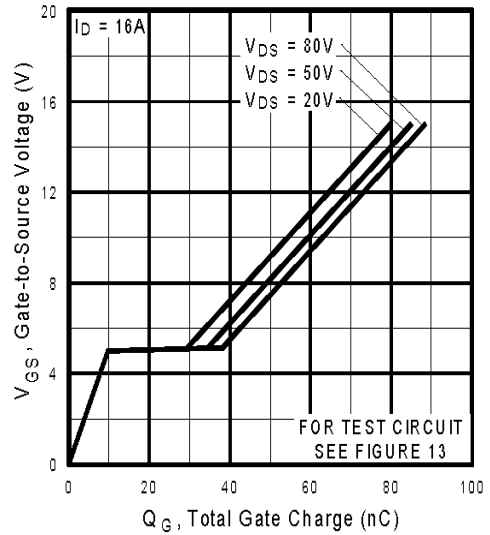


**Fig 4.** Normalized On-Resistance Vs. Temperature

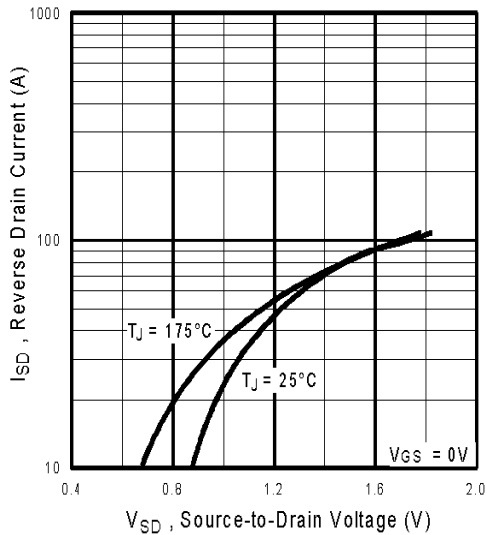
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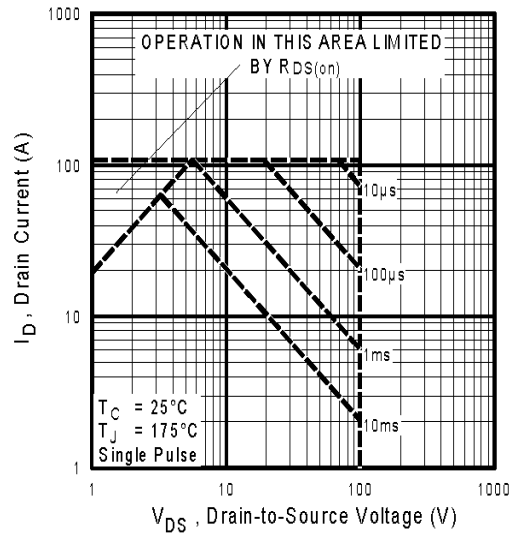
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



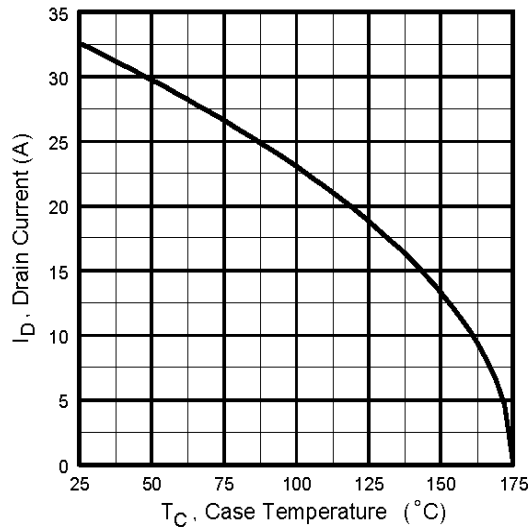
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



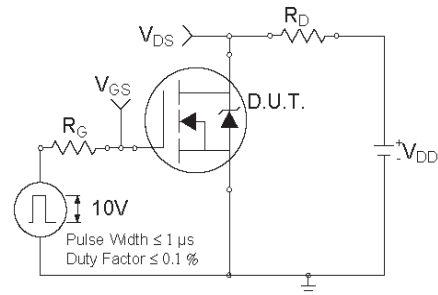
**Fig 7.** Typical Source-Drain Diode Forward Voltage



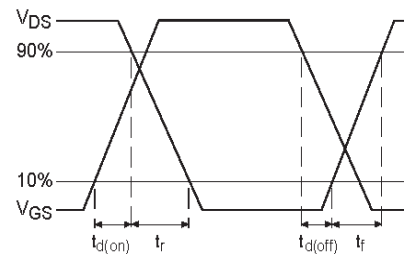
**Fig 8.** Maximum Safe Operating Area



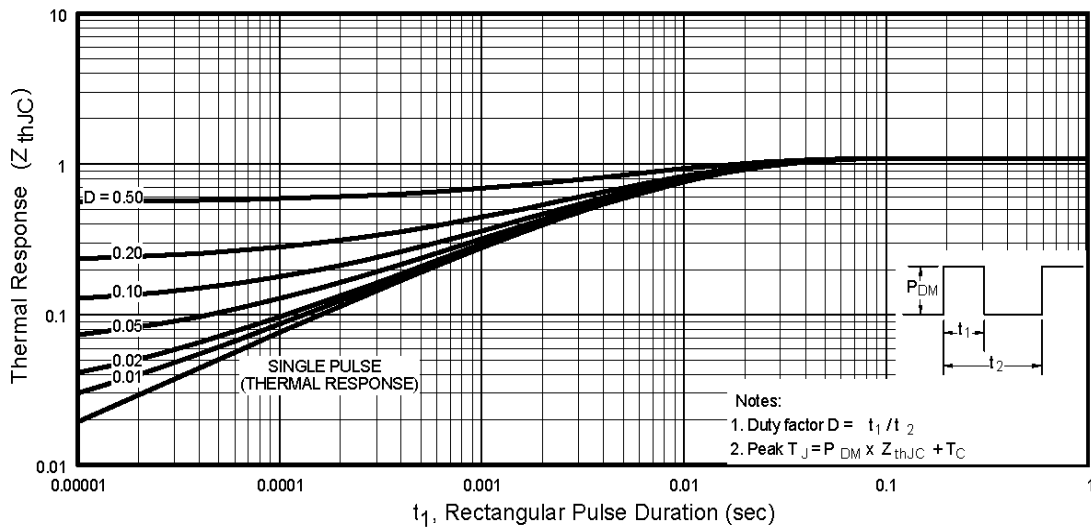
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



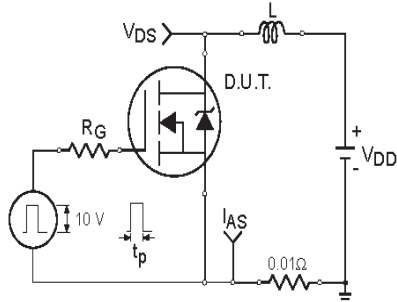
**Fig 10b.** Switching Time Waveforms



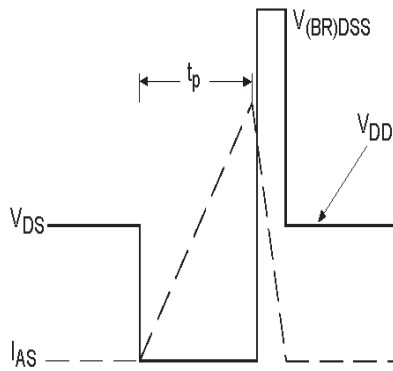
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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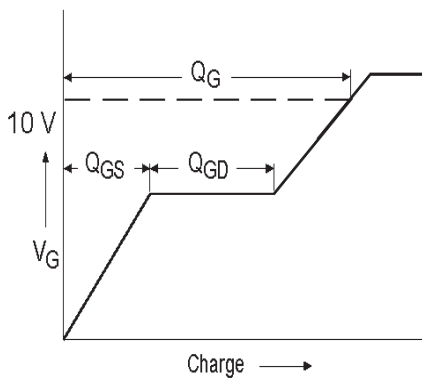
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**Fig 12a.** Unclamped Inductive Test Circuit

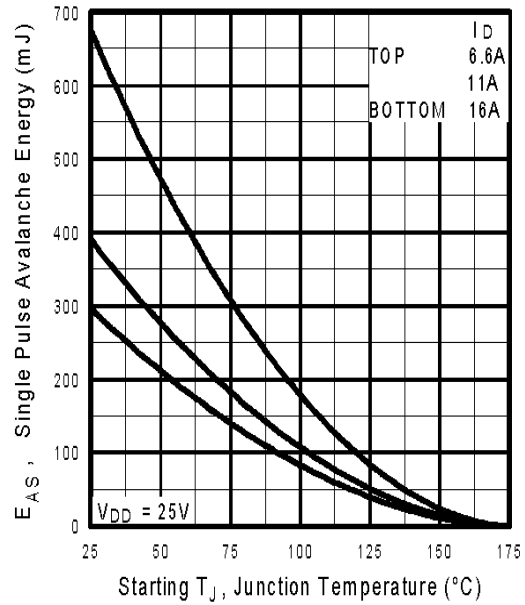


**Fig 12b.** Unclamped Inductive Waveforms

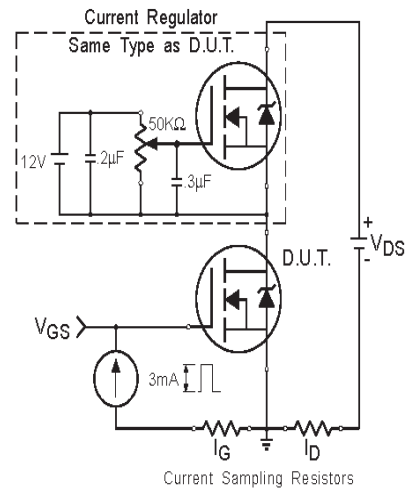


**Fig 13a.** Basic Gate Charge Waveform

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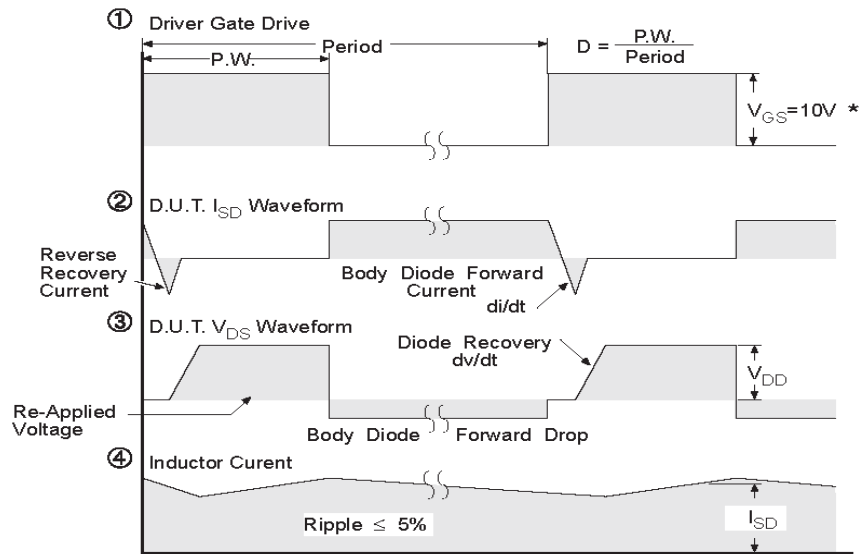
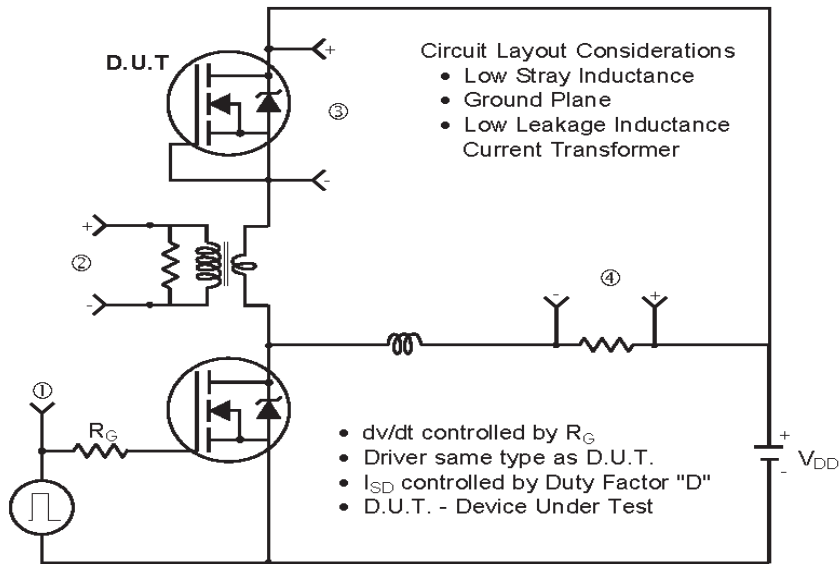
**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

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## Peak Diode Recovery dv/dt Test Circuit



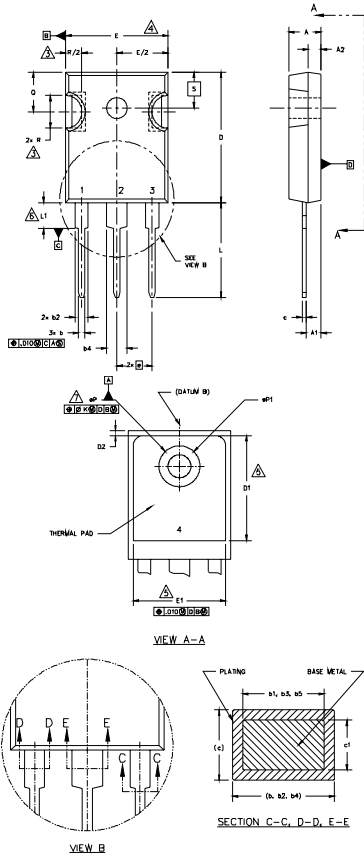
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFETS

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TO-247AC Package Outline Dimensions are shown in millimeters (inches)



NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
- CONTOUR OF SLOT OPTIONAL.
- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
- LEAD FINISH UNCONTROLLED IN L1.
- ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154" [3.91]
- OUTLINE CONFORMS TO JEDEC OUTLINE TO-247 WITH THE EXCEPTION OF DIMENSION e.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.065	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.37	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.034	0.38	0.86	
c1	.015	.030	0.38	0.76	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.030	0.51	0.76	
E	.602	.625	15.29	15.87	4
E1	.540	-	15.72	-	
e	.215 BSC		5.46 BSC		
Øk	.010		2.54		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
N	3		7.62 BSC		
ØP	.140	.144	3.56	3.66	
ØP1	-	.275	-	6.98	
Q	.209	.224	5.31	5.69	
R	.178	.216	4.52	5.49	
S	.217 BSC		5.51 BSC		

**LEAD ASSIGNMENTS**

**HEXFET**

- GATE
- DRAIN
- SOURCE
- DRAIN

**IGBTs, CoPACK**

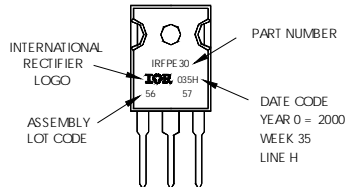
- GATE
- COLLECTOR
- EMITTER
- COLLECTOR

**DIODES**

- ANODE/OPEN
- CATHODE
- ANODE

## TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30  
WITH ASSEMBLY  
LOT CODE 5657  
ASSEMBLED ON WW35, 2000  
IN THE ASSEMBLY LINE "H"  
**Note:** "P" in assembly line  
position indicates "Lead-Free"



Data and specifications subject to change without notice.

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Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>

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