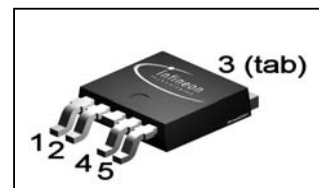


**OptiMOS® -P Power-Transistor**
**Features**

- P-Channel
- Enhancement mode
- Logic level
- 175°C operating temperature
- Avalanche rated
- $dv/dt$  rated
- High current rating
- Pb-free lead-plating, RoHS compliant


**PG-TO252-5**


Type	Package	Marking	Tape and reel information	Lead Free	Packing
SPD50P03L G	PG-TO252-5	50P03L	1000 pcs / reel	Yes	Non dry

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$T_C=25\text{ °C}^{1)}$	-50	A
		$T_C=100\text{ °C}^{1)}$	-50	
Pulsed drain current	$I_{D,pulse}$	$T_C=25\text{ °C}$	-200	
Avalanche energy, single pulse	$E_{AS}$	$I_D=-50\text{ A}$ , $R_{GS}=25\ \Omega$	256	mJ
Reverse diode $dv/dt$	$dv/dt$	$I_D=-50\text{ A}$ , $V_{DS}=24\text{ V}$ , $di/dt=-200\text{ A}/\mu\text{s}$ , $T_{j,max}=175\text{ °C}$	-6	kV/ $\mu\text{s}$
Gate source voltage	$V_{GS}$		$\pm 20$	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	150	W
Operating and storage temperature	$T_j$ , $T_{stg}$		-55...+175	°C
ESD class HBM			1C	
Soldering temperature			260	
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - case	$R_{thJC}$		-	-	1	K/W
Thermal resistance, junction - ambient	$R_{thJA}$	minimal footprint	-	-	75	
		6 cm <sup>2</sup> cooling area <sup>2)</sup>	-	-	50	

**Electrical characteristics, at  $T_j=25\text{ }^\circ\text{C}$ , unless otherwise specified**

**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=-250\text{ }\mu\text{A}$	-30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\text{ }\mu\text{A}$	-1	-1.5	-2	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=-30\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$	-	-0.1	-1	$\mu\text{A}$
		$V_{DS}=-30\text{ V}, V_{GS}=0\text{ V}, T_j=175\text{ }^\circ\text{C}$	-	-10	-100	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=-20\text{ V}, V_{DS}=0\text{ V}$	-	-10	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-4.5\text{ V}, I_D=-30\text{ A}$	-	8.5	12.5	m $\Omega$
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-10\text{ V}, I_D=-50\text{ A}$	-	5.7	7.0	
Transconductance	$g_{fs}$	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=-50\text{ A}$	47	94	-	S

<sup>1)</sup> Current is limited by bondwire; with an  $R_{thJC}=1\text{ K/W}$  the chip is able to carry 123 A.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V},$ $V_{DS}=-25\text{ V}, f=1\text{ MHz}$	-	4590	6880	pF
Output capacitance	$C_{oss}$		-	1220	1830	
Reverse transfer capacitance	$C_{rss}$		-	1000	1500	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-15\text{ V},$ $V_{GS}=-10\text{ V}, I_D=-1\text{ A},$ $R_G=6\ \Omega$	-	14.8	22	ns
Rise time	$t_r$		-	21.7	32	
Turn-off delay time	$t_{d(off)}$		-	139	208	
Fall time	$t_f$		-	104	156	

**Gate Charge Characteristics<sup>3)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=-24\text{ V}, I_D=-50\text{ A}$	-	-14	-19	nC
Gate to drain charge	$Q_{gd}$		-	-35	-53	
Gate charge total	$Q_g$	$V_{DD}=-24\text{ V}, I_D=-50\text{ A},$ $V_{GS}=0\text{ to }-10\text{ V}$	-	-95	-126	
Gate plateau voltage	$V_{plateau}$	$V_{DD}=-24\text{ V}, I_D=-50\text{ A}$	-	-3.0	-	V

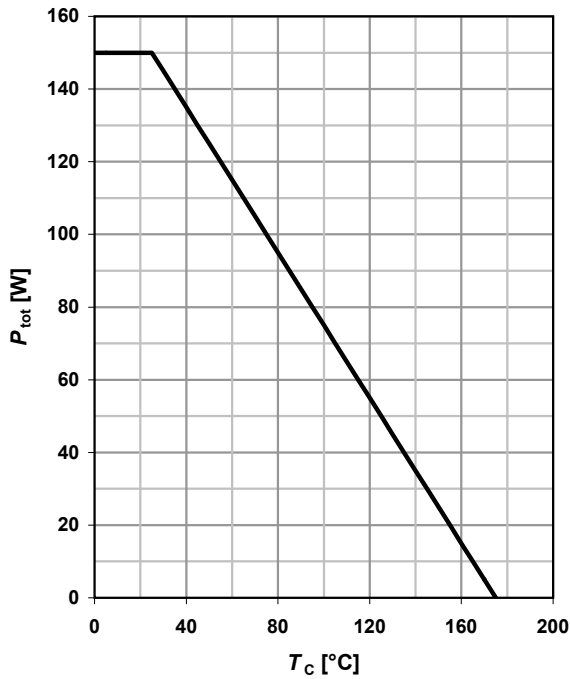
**Reverse Diode**

Diode continuous forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	-50	A
Diode pulse current	$I_{S,pulse}$		-	-	-200	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=50\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	-1	-1.65	V
Reverse recovery time	$t_{rr}$	$V_R=-15\text{ V}, I_F= I_S ,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	38	47	ns
Reverse recovery charge	$Q_{rr}$		-	46	57	

<sup>3)</sup> See figure 16 for gate charge parameter definition

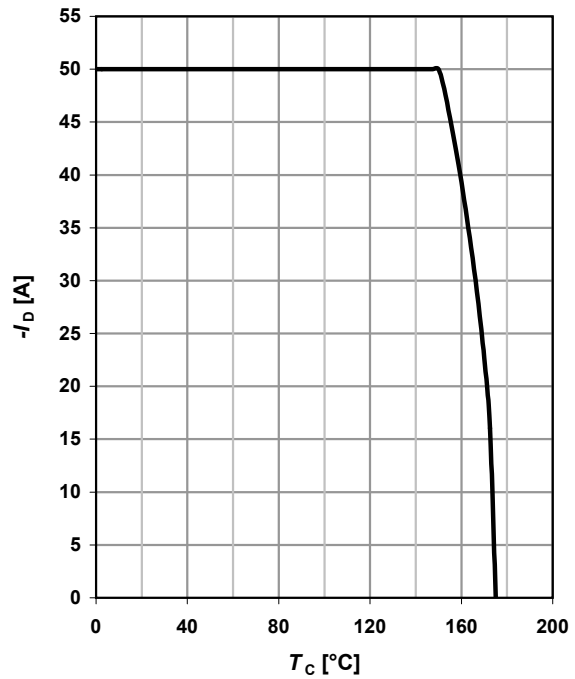
**1 Power dissipation**

$$P_{tot} = f(T_C)$$



**2 Drain current**

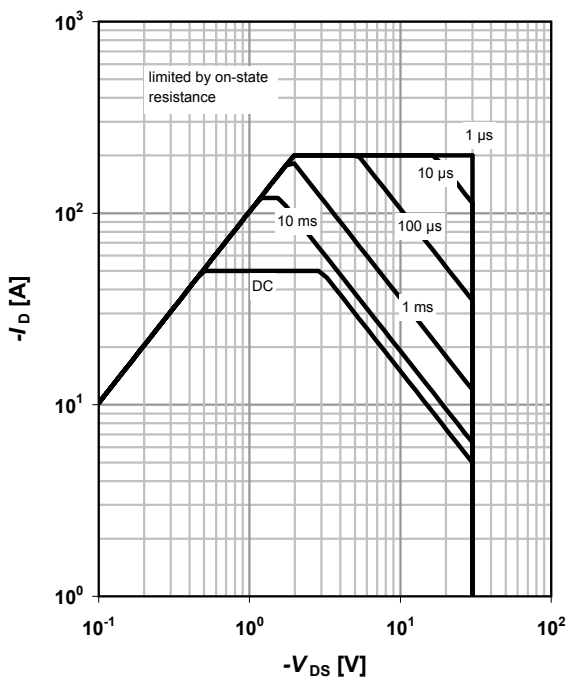
$$I_D = f(T_C); |V_{GS}| \geq 10 \text{ V}$$



**3 Safe operating area**

$$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$$

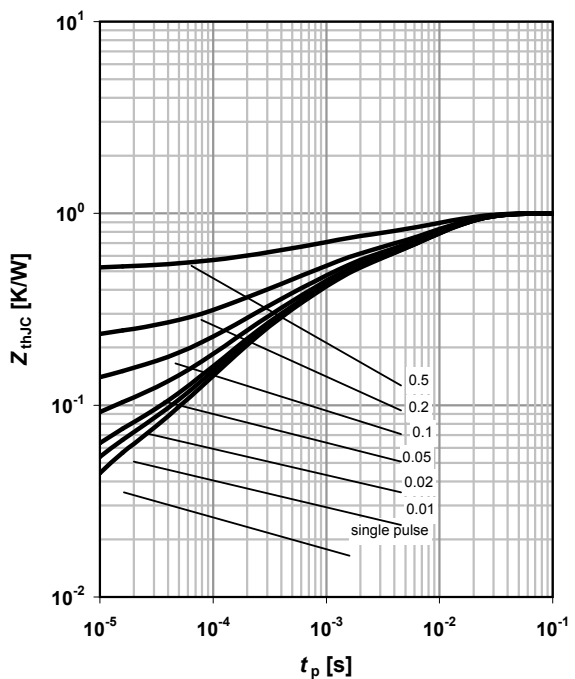
parameter:  $t_p$



**4 Max. transient thermal impedance**

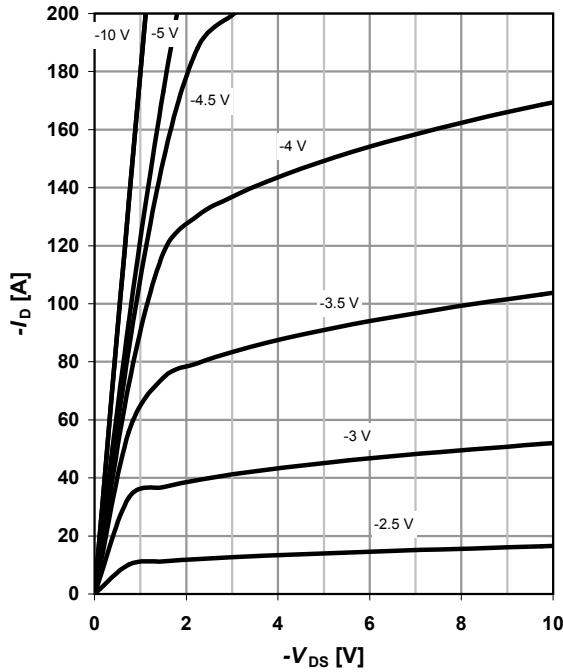
$$Z_{thJC} = f(t_p)$$

parameter:  $D = t_p / T$

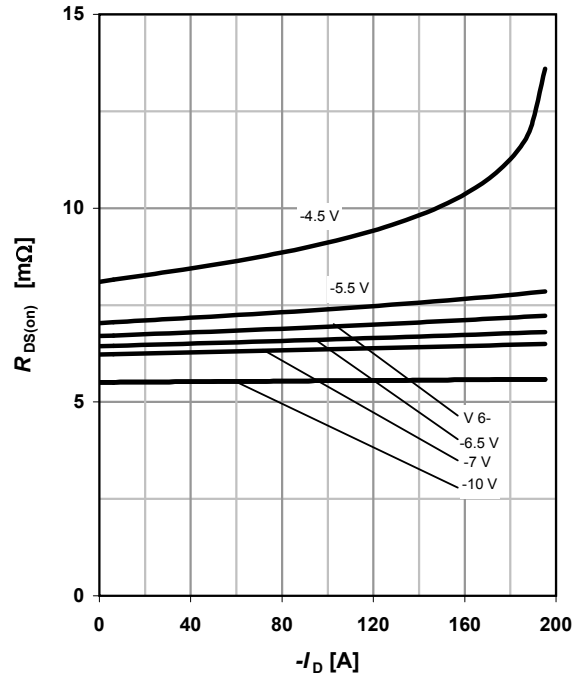


**5 Typ. output characteristics**

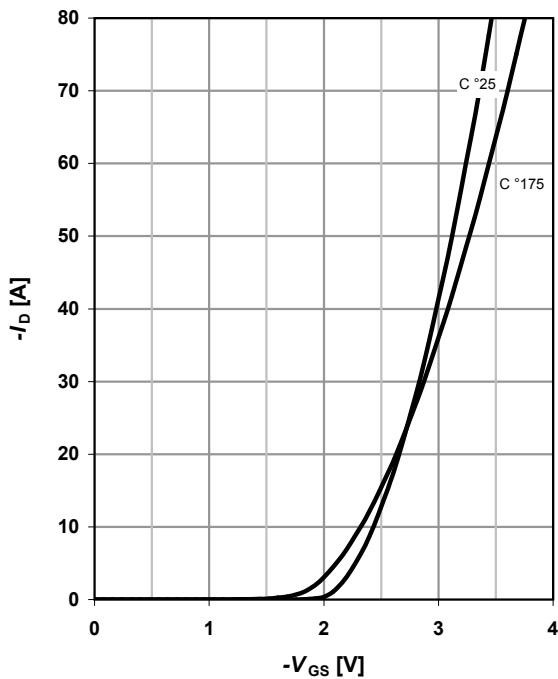
$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

 parameter:  $V_{GS}$ 

**6 Typ. drain-source on resistance**

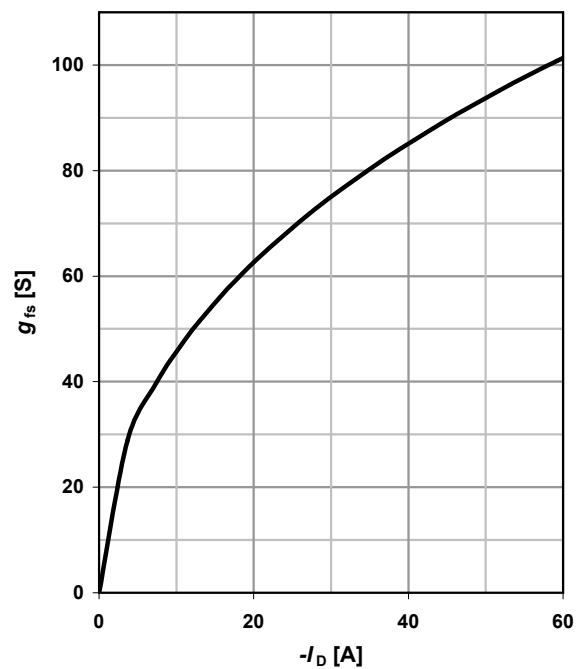
$$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$$

 parameter:  $V_{GS}$ 

**7 Typ. transfer characteristics**

$$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$$

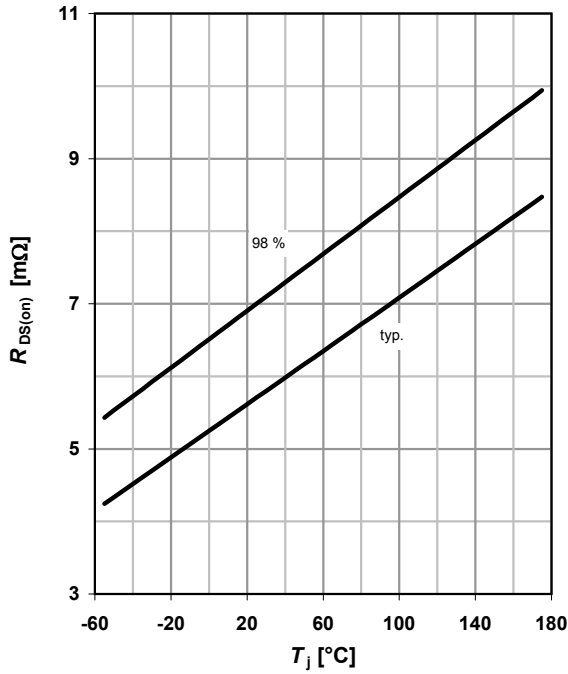
 parameter:  $T_j$ 

**8 Typ. forward transconductance**

$$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$$



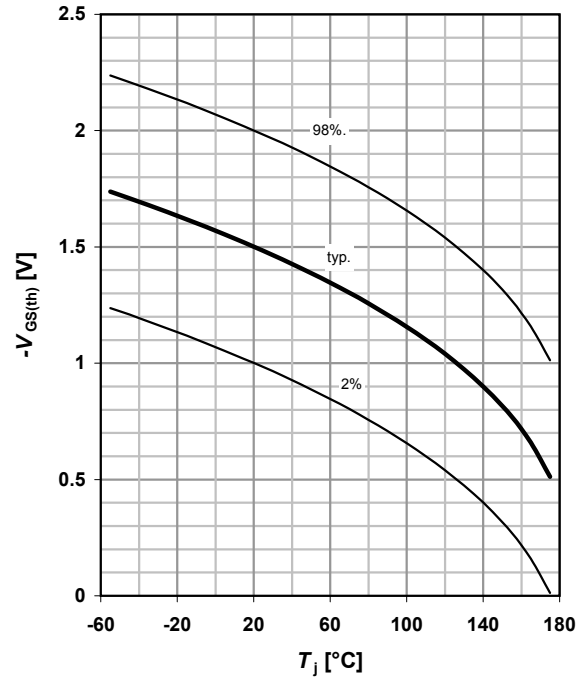
**9 Drain-source on-state resistance**

$R_{DS(on)} = f(T_j); I_D = -50 \text{ A}; V_{GS} = -10 \text{ V}$



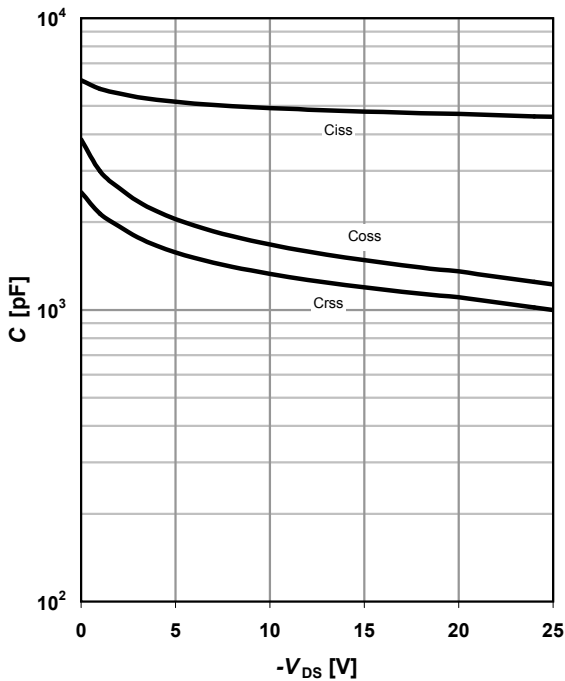
**10 Typ. gate threshold voltage**

$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = -250 \mu\text{A}$



**11 Typ. capacitances**

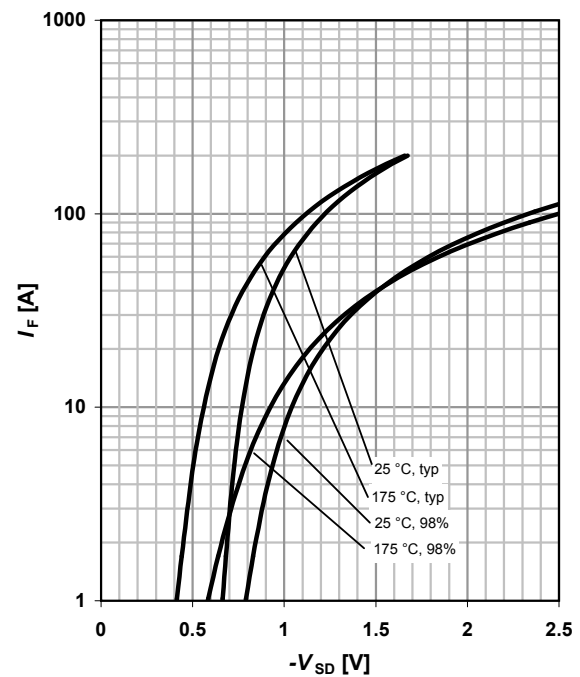
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



**12 Forward characteristics of reverse diode**

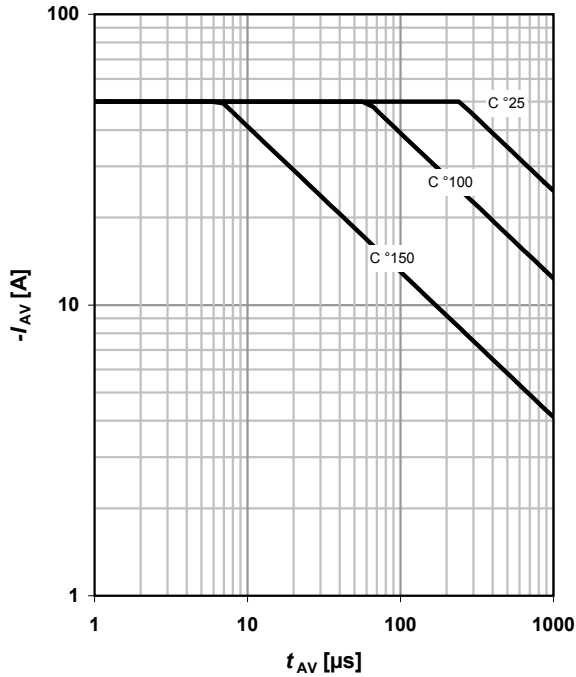
$I_F = f(V_{SD})$

parameter:  $T_j$

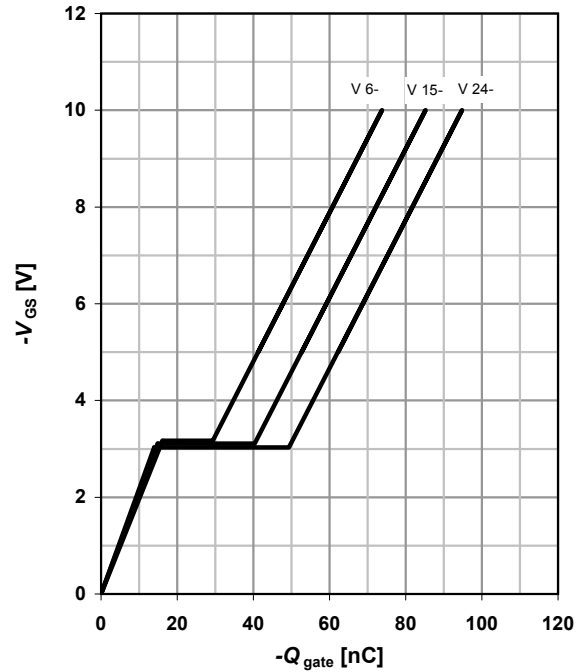


**13 Avalanche characteristics**

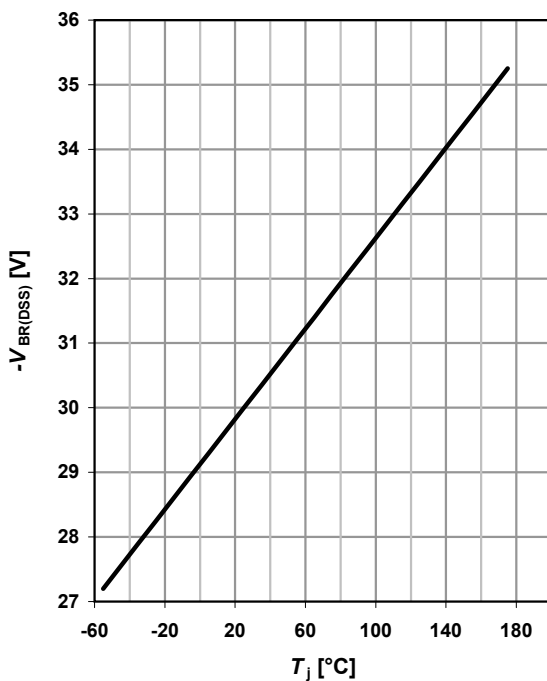
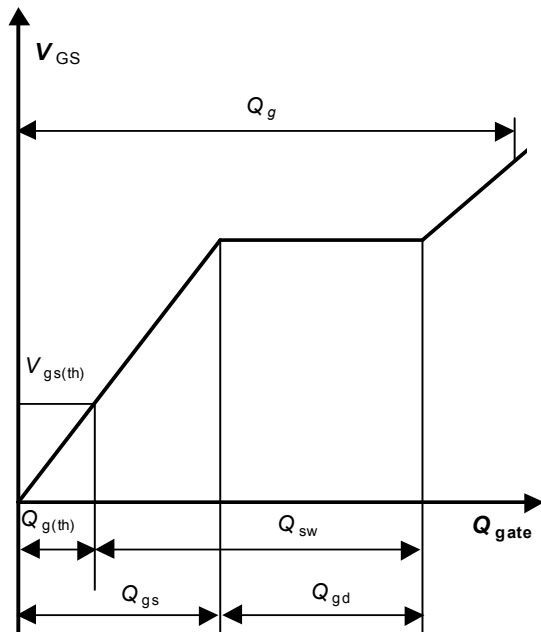
$$I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega$$

 parameter:  $T_{j(\text{start})}$ 

**14 Typ. gate charge**

$$V_{GS}=f(Q_{\text{gate}}); I_D=-50\ \text{A pulsed}$$

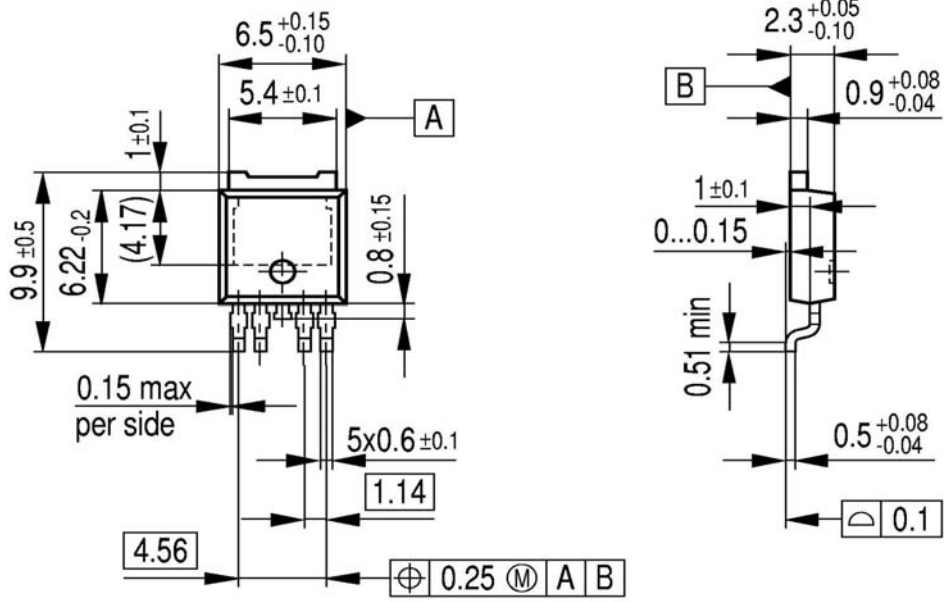
 parameter:  $V_{DD}$ 

**15 Drain-source breakdown voltage**

$$V_{BR(DSS)}=f(T_j); I_D=-250\ \mu\text{A}$$

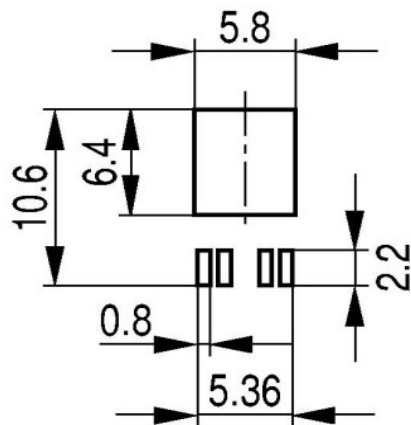

**16 Gate charge waveforms**


Package Outline

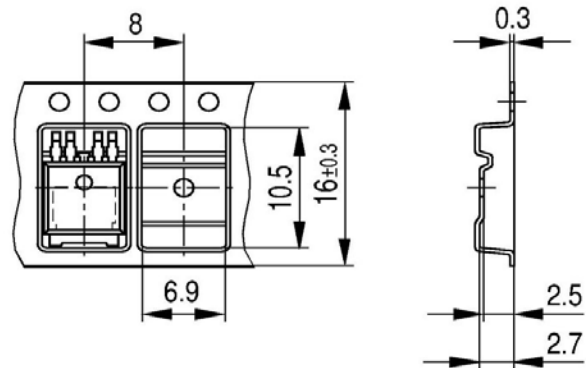
PG-T0252-5: Outline



Footprint



Packaging Tape



Dimensions in mm



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