International
IOR Rectifier

PD - 95463

# IRF3704ZPbF
# IRF3704ZSPbF
# IRF3704ZLPbF

HEXFET® Power MOSFET

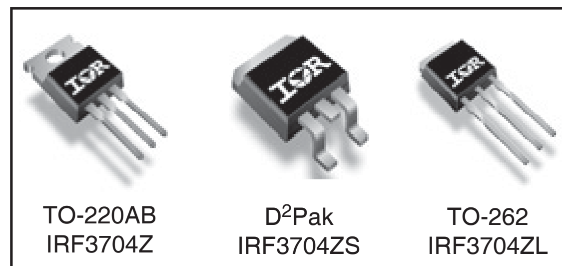
### Applications

- High Frequency Synchronous Buck Converters for Computer Processor Power
- Lead-Free

| $V_{DSS}$ | $R_{DS(on)}$ max | Qg |
|---|---|---|
| 20V | 7.9mΩ | 8.7nC |

### Benefits

- Low $R_{DS(on)}$ at 4.5V $V_{GS}$
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current



TO-220AB IRF3704Z | D²Pak IRF3704ZS | TO-262 IRF3704ZL

### Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $V_{DS}$ | Drain-to-Source Voltage | 20 | V |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | |
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V | 67 ⑥ | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V | 47 ⑥ | |
| $I_{DM}$ | Pulsed Drain Current ① | 260 | |
| $P_D$ @$T_C$ = 25°C | Maximum Power Dissipation | 57 | W |
| $P_D$ @$T_C$ = 100°C | Maximum Power Dissipation | 28 | |
| | Linear Derating Factor | 0.38 | W/°C |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 175 | °C |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case) | |
| | Mounting Torque, 6-32 or M3 screw ④ | 10 lbf•in (1.1N•m) | |

### Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case ⑦ | — | 2.65 | °C/W |
| $R_{\theta CS}$ | Case-to-Sink, Flat Greased Surface ④ | 0.50 | — | |
| $R_{\theta JA}$ | Junction-to-Ambient ④⑦ | — | 62 | |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB Mount) ⑤⑦ | — | 40 | |

Notes ① through ⑦ are on page 12



6/29/04

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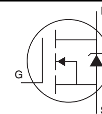
## Static @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | 20 | —— | —— | V | $V_{GS}$ = 0V, $I_D$ = 250μA |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | —— | 0.014 | —— | V/°C | Reference to 25°C, $I_D$ = 1mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | —— | 6.5 | 7.9 | mΩ | $V_{GS}$ = 10V, $I_D$ = 21A ③ |
| | | —— | 9.1 | 11.1 | | $V_{GS}$ = 4.5V, $I_D$ = 17A ③ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.65 | 2.1 | 2.55 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA |
| $\Delta V_{GS(th)}/\Delta T_J$ | Gate Threshold Voltage Coefficient | —— | -5.6 | —— | mV/°C | |
| $I_{DSS}$ | Drain-to-Source Leakage Current | —— | —— | 1.0 | μA | $V_{DS}$ = 16V, $V_{GS}$ = 0V |
| | | —— | —— | 150 | | $V_{DS}$ = 16V, $V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | —— | —— | 100 | nA | $V_{GS}$ = 20V |
| | Gate-to-Source Reverse Leakage | —— | —— | -100 | | $V_{GS}$ = -20V |
| gfs | Forward Transconductance | 48 | —— | —— | S | $V_{DS}$ = 10V, $I_D$ = 17A |
| $Q_g$ | Total Gate Charge | —— | 8.7 | 13 | nC | |
| $Q_{gs1}$ | Pre-Vth Gate-to-Source Charge | —— | 2.9 | —— | | $V_{DS}$ = 10V |
| $Q_{gs2}$ | Post-Vth Gate-to-Source Charge | —— | 1.1 | —— | | $V_{GS}$ = 4.5V |
| $Q_{gd}$ | Gate-to-Drain Charge | —— | 2.3 | —— | | $I_D$ = 17A |
| $Q_{godr}$ | Gate Charge Overdrive | —— | 2.4 | —— | | See Fig. 16 |
| $Q_{sw}$ | Switch Charge ($Q_{gs2}$ + $Q_{gd}$) | —— | 3.4 | —— | | |
| $Q_{oss}$ | Output Charge | —— | 5.6 | —— | nC | $V_{DS}$ = 10V, $V_{GS}$ = 0V |
| $t_{d(on)}$ | Turn-On Delay Time | —— | 8.9 | —— | ns | $V_{DD}$ = 10V, $V_{GS}$ = 4.5V ③ |
| $t_r$ | Rise Time | —— | 38 | —— | | $I_D$ = 17A |
| $t_{d(off)}$ | Turn-Off Delay Time | —— | 11 | —— | | Clamped Inductive Load |
| $t_f$ | Fall Time | —— | 4.2 | —— | | |
| $C_{iss}$ | Input Capacitance | —— | 1220 | —— | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | —— | 390 | —— | | $V_{DS}$ = 10V |
| $C_{rss}$ | Reverse Transfer Capacitance | —— | 190 | —— | | $f$ = 1.0MHz |

## Avalanche Characteristics

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $E_{AS}$ | Single Pulse Avalanche Energy② | —— | 36 | mJ |
| $I_{AR}$ | Avalanche Current ① | —— | 17 | A |
| $E_{AR}$ | Repetitive Avalanche Energy ① | —— | 5.7 | mJ |

## Diode Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | —— | —— | 67 ⑥ | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | —— | —— | 260 | | |
| $V_{SD}$ | Diode Forward Voltage | —— | —— | 1.0 | V | $T_J$ = 25°C, $I_S$ = 17A, $V_{GS}$ = 0V ③ |
| $t_{rr}$ | Reverse Recovery Time | —— | 11 | 17 | ns | $T_J$ = 25°C, $I_F$ = 17A, $V_{DD}$ = 10V |
| $Q_{rr}$ | Reverse Recovery Charge | —— | 2.3 | 3.5 | nC | di/dt = 100A/μs ③ |



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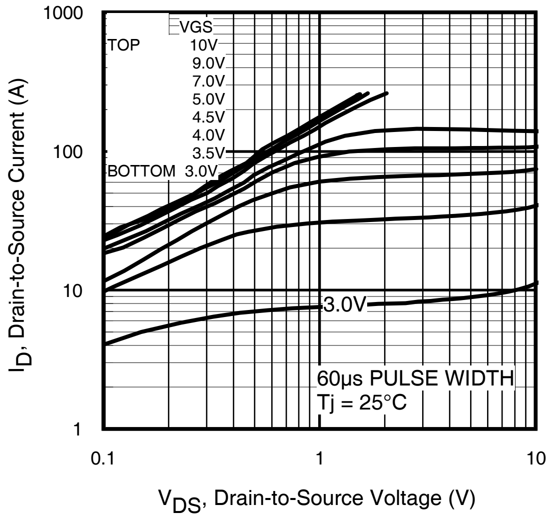


**Fig 1.** Typical Output Characteristics

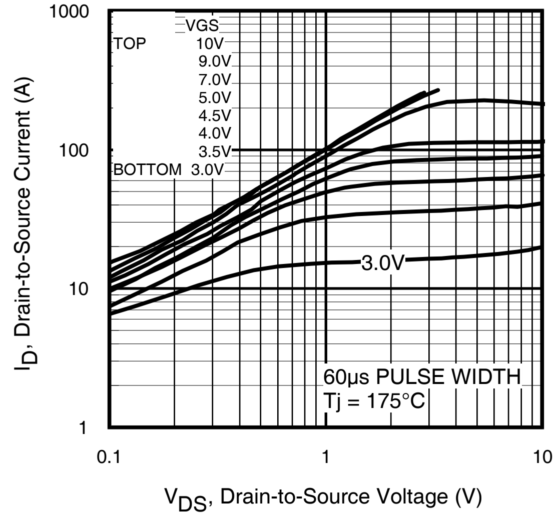


**Fig 2.** Typical Output Characteristics

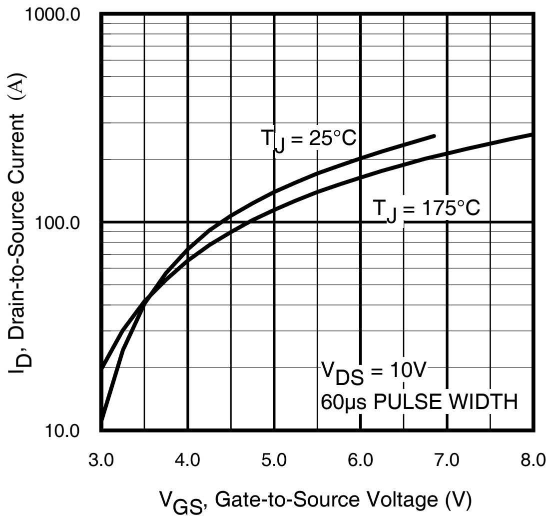


**Fig 3.** Typical Transfer Characteristics

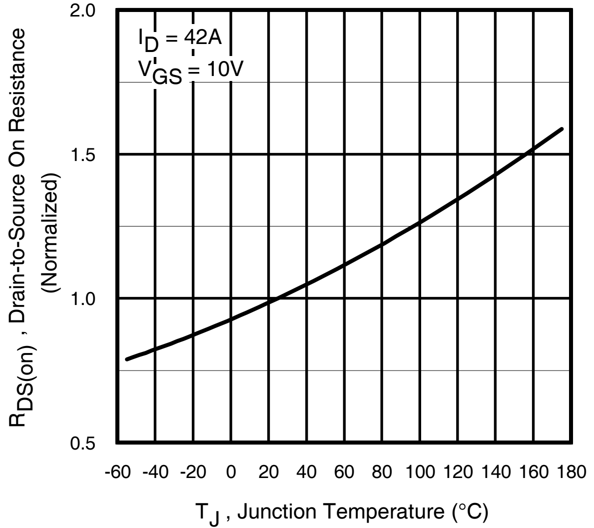


**Fig 4.** Normalized On-Resistance vs. Temperature



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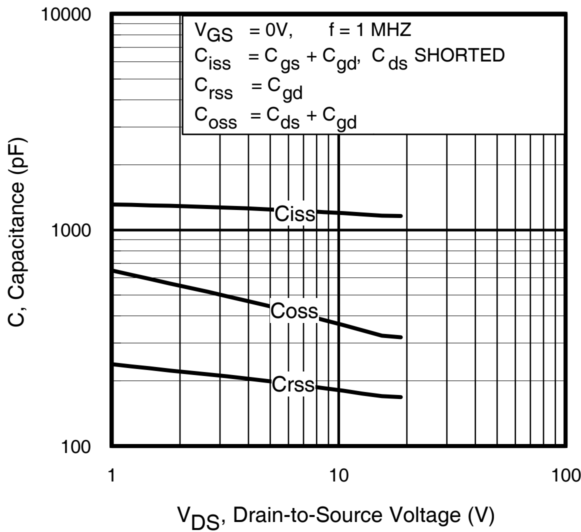


**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

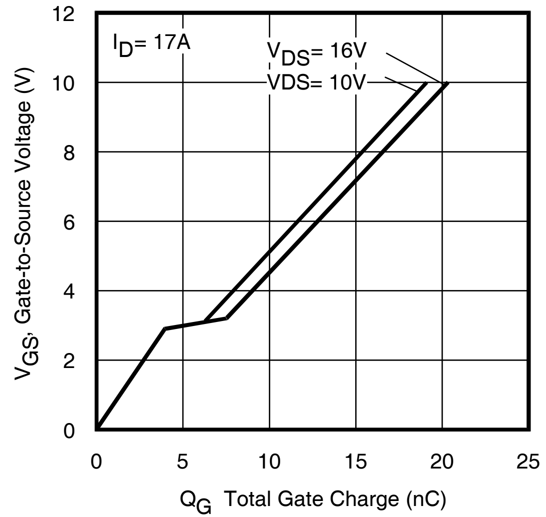


**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

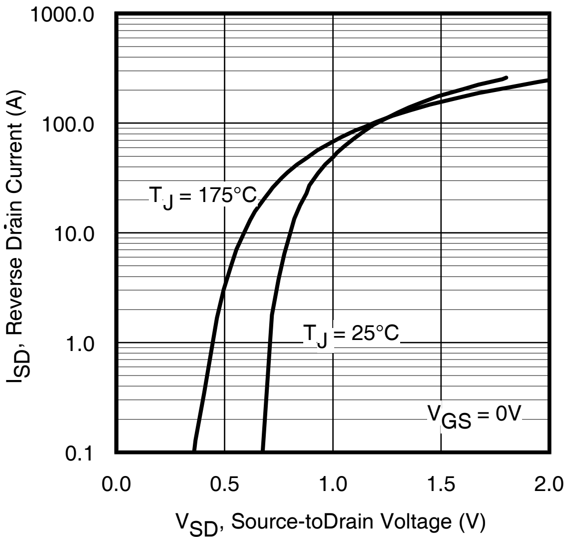


**Fig 7.** Typical Source-Drain Diode Forward Voltage

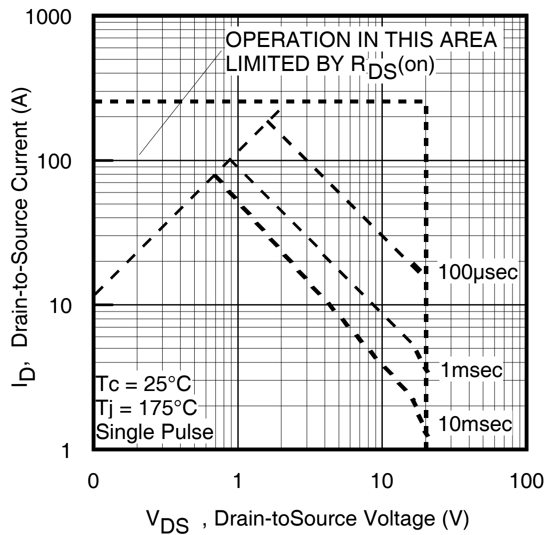


**Fig 8.** Maximum Safe Operating Area



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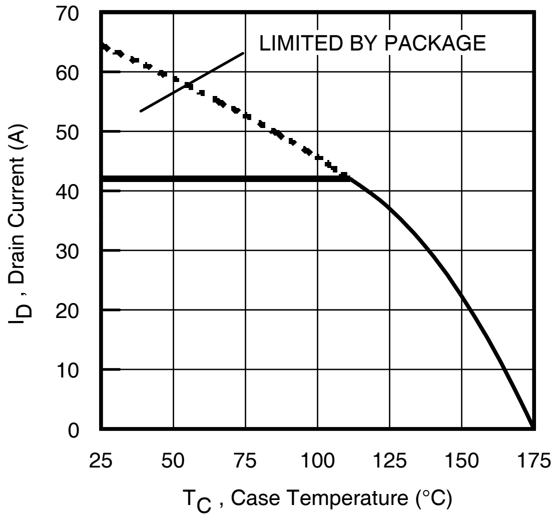



**Fig 9.** Maximum Drain Current vs. Case Temperature

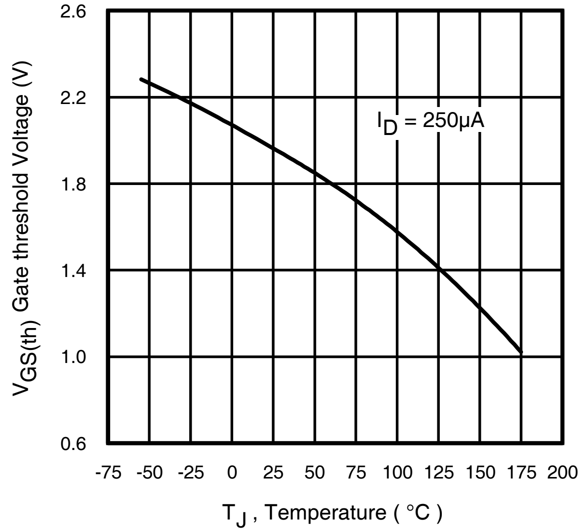
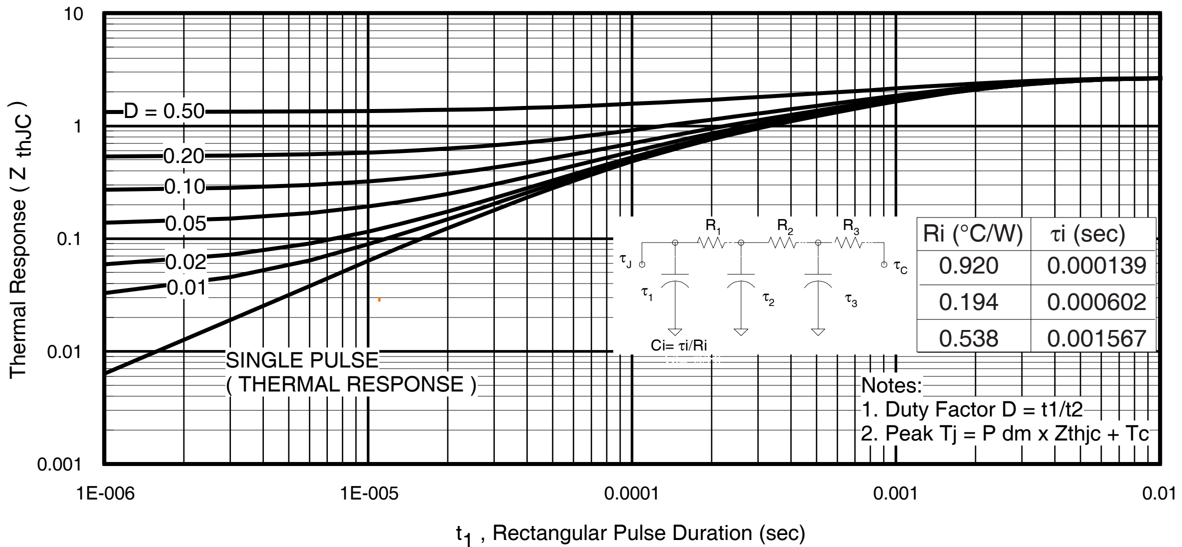



**Fig 10.** Threshold Voltage vs. Temperature




| Ri (°C/W) | τi (sec) |
|---|---|
| 0.920 | 0.000139 |
| 0.194 | 0.000602 |
| 0.538 | 0.001567 |

**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



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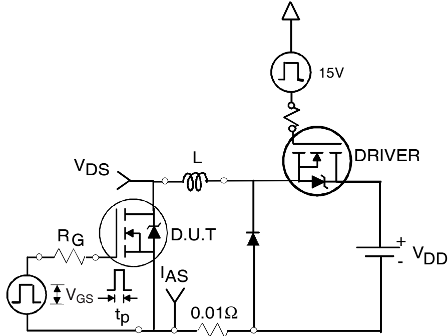


**Fig 12a.** Unclamped Inductive Test Circuit

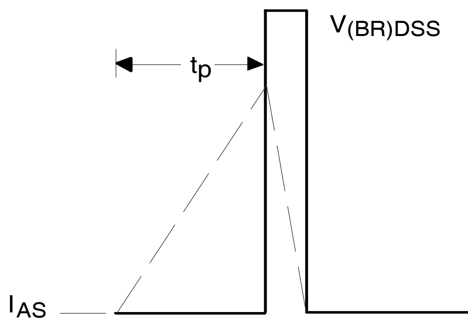


**Fig 12b.** Unclamped Inductive Waveforms

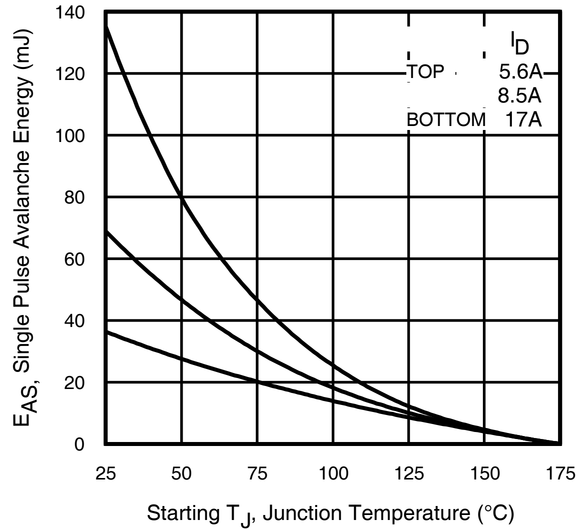


**Fig 12c.** Maximum Avalanche Energy vs. Drain Current

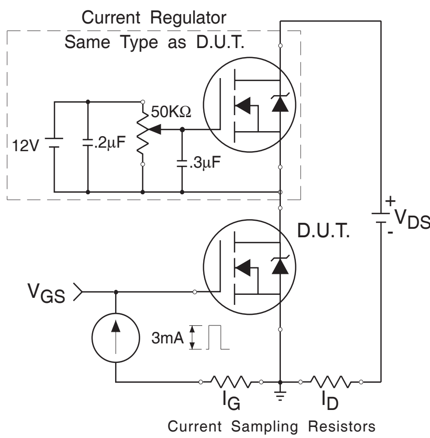


**Fig 13.** Gate Charge Test Circuit

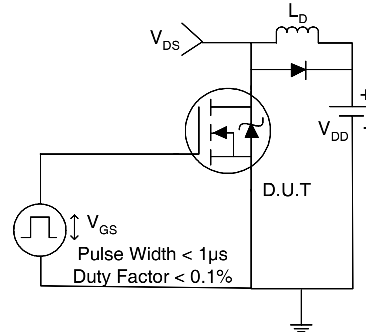


**Fig 14a.** Switching Time Test Circuit

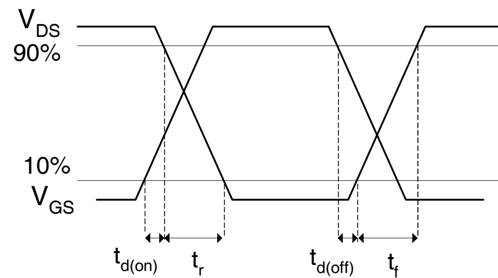


**Fig 14b.** Switching Time Waveforms



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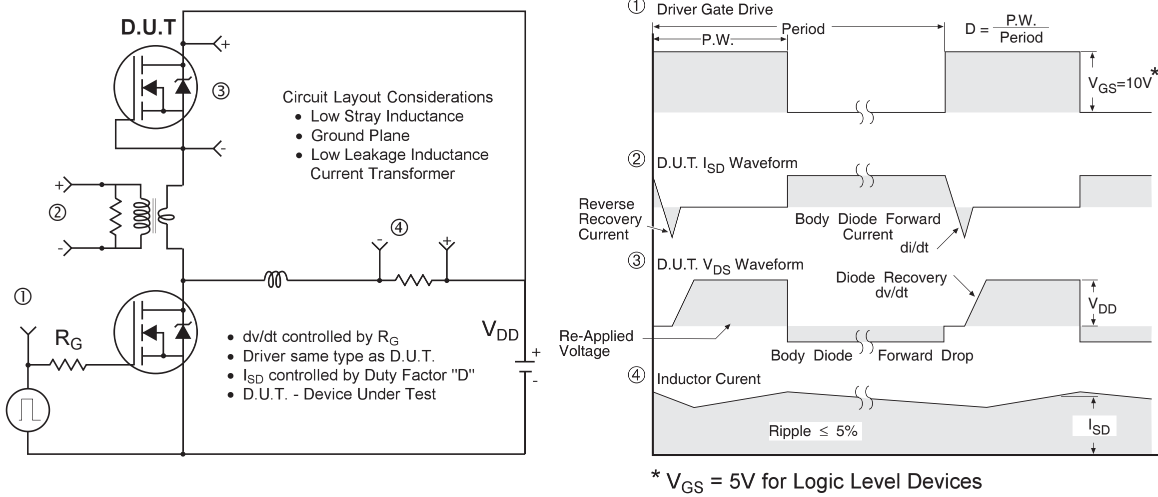


* $V_{GS}$ = 5V for Logic Level Devices

**Fig 15.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

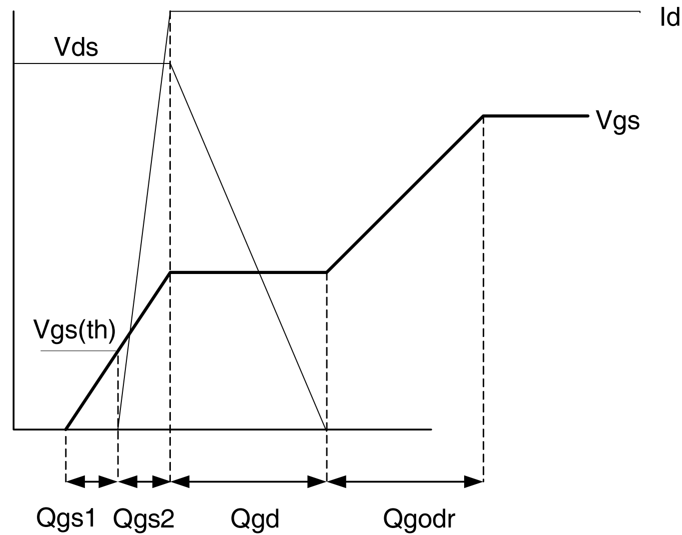


**Fig 16.** Gate Charge Waveform



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## Power MOSFET Selection for Non-Isolated DC/DC Converters

### Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}{}^{2} \times R_{ds(on)}\right) + \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f\right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right)$$

This simplified loss equation includes the terms $Q_{gs2}$ and $Q_{oss}$ which are new to Power MOSFET data sheets.

$Q_{gs2}$ is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, $Q_{gs1}$ and $Q_{gs2}$, can be seen from Fig 16.

$Q_{gs2}$ indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to $I_{dmax}$ at which time the drain voltage begins to change. Minimizing $Q_{gs2}$ is a critical factor in reducing switching losses in Q1.

$Q_{oss}$ is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how $Q_{oss}$ is formed by the parallel combination of the voltage dependant (non-linear) capacitance's $C_{ds}$ and $C_{dg}$ when multiplied by the power supply input buss voltage.

### Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P^{*}_{output}$$

$$P_{loss} = \left(I_{rms}{}^{2} \times R_{ds(on)}\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right) + \left(Q_{rr} \times V_{in} \times f\right)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge $Q_{oss}$ and reverse recovery charge $Q_{rr}$ both generate losses that are transfered to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and $V_{in}$. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current . The ratio of $Q_{gd}/Q_{gs1}$ must be minimized to reduce the potential for Cdv/dt turn on.

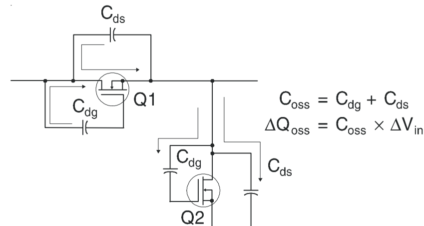


Figure A: $Q_{oss}$ Characteristic



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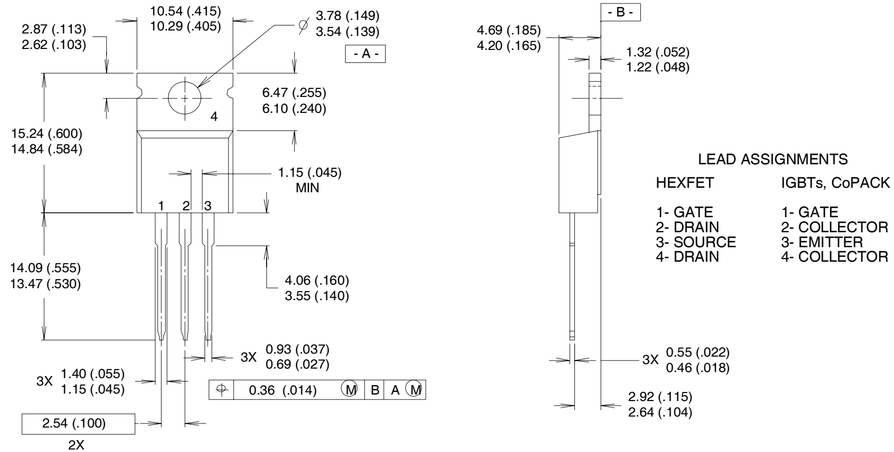
## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

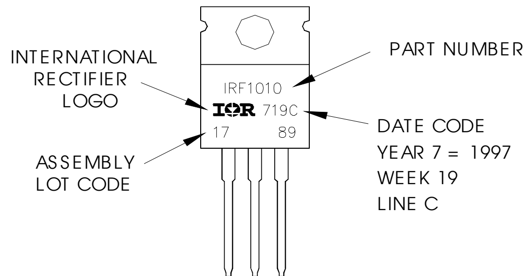



NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

**Note:** "P" in assembly line position indicates "Lead-Free"



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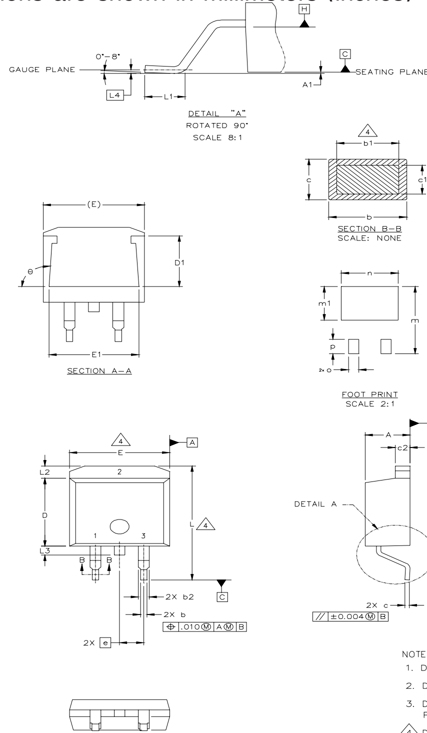
# D2Pak Package Outline

Dimensions are shown in millimeters (inches)




| SYMBOL | DIMENSIONS | | | | NOTES |
|---|---|---|---|---|---|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4.06 | 4.83 | .160 | .190 | |
| A1 | | 0.127 | | .005 | |
| b | 0.51 | 0.99 | .020 | .039 | |
| b1 | 0.51 | 0.89 | .020 | .035 | 4 |
| b2 | 1.14 | 1.40 | .045 | .055 | |
| c | 0.43 | 0.63 | .017 | .025 | |
| c1 | 0.38 | 0.74 | .015 | .029 | 4 |
| c2 | 1.14 | 1.40 | .045 | .055 | |
| D | 8.51 | 9.65 | .335 | .380 | 3 |
| D1 | 5.33 | | .210 | | |
| E | 9.65 | 10.67 | .380 | .420 | 3 |
| E1 | 6.22 | | .245 | | |
| e | 2.54 BSC | | .100 BSC | | |
| L | 14.61 | 15.88 | .575 | .625 | |
| L1 | 1.78 | 2.79 | .070 | .110 | |
| L2 | | 1.65 | | .065 | |
| L3 | 1.27 | 1.78 | .050 | .070 | |
| L4 | 0.25 BSC | | .010 BSC | | |
| m | 17.78 | | .700 | | |
| m1 | 8.89 | | .350 | | |
| n | 11.43 | | .450 | | |
| o | 2.08 | | .082 | | |
| p | 3.81 | | .150 | | |
| θ | 90° | 93° | 90° | 93° | |

LEAD ASSIGNMENTS

| HEXFET | IGBTs, CoPACK | DIODES |
|---|---|---|
| 1.– GATE | 1.– GATE | 1.– ANODE * |
| 2.– DRAIN | 2.– COLLECTOR | 2.– CATHODE |
| 3.– SOURCE | 3.– EMITTER | 3.– ANODE |

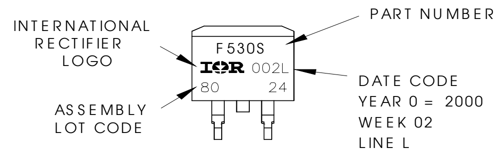
* PART DEPENDENT.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

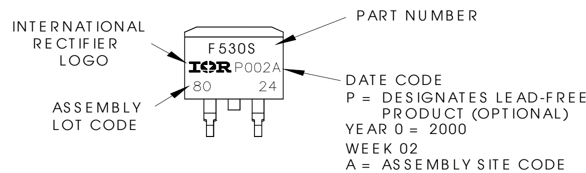
# D2Pak Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF530S WITH LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead-Free"




OR



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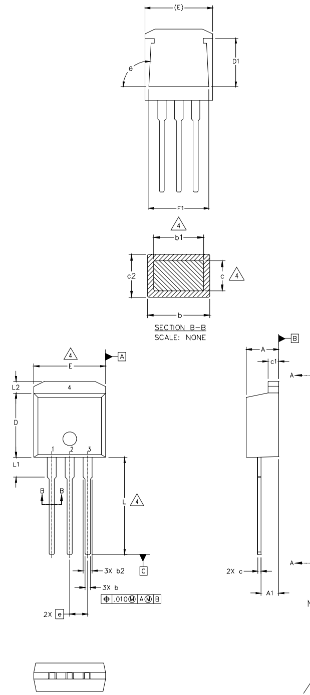
## TO-262 Package Outline



| SYMBOL | DIMENSIONS | | | | NOTES |
|---|---|---|---|---|---|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4.06 | 4.83 | .160 | .190 | |
| A1 | 2.03 | 2.92 | .080 | .115 | |
| b | 0.51 | 0.99 | .020 | .039 | |
| b1 | 0.51 | 0.89 | .020 | .035 | 4 |
| b2 | 1.14 | 1.40 | .045 | .055 | |
| c | 0.38 | 0.63 | .015 | .025 | 4 |
| c1 | 1.14 | 1.40 | .045 | .055 | |
| c2 | 0.43 | .063 | .017 | .029 | |
| D | 8.51 | 9.65 | .335 | .380 | 3 |
| D1 | 5.33 | | .210 | | |
| E | 9.65 | 10.67 | .380 | .420 | 3 |
| E1 | 6.22 | | .245 | | |
| e | 2.54 BSC | | .100 BSC | | |
| L | 13.46 | 14.09 | .530 | .555 | |
| L1 | 3.56 | 3.71 | .140 | .146 | |
| L2 | | 1.65 | | .065 | |

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBT

1- GATE
2- COLLECTOR
3- EMITTER

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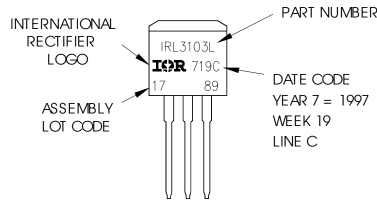
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

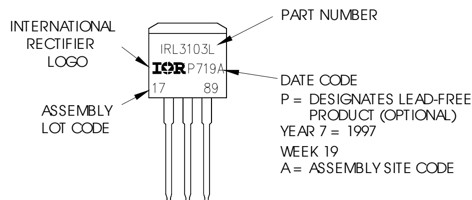
## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"




OR



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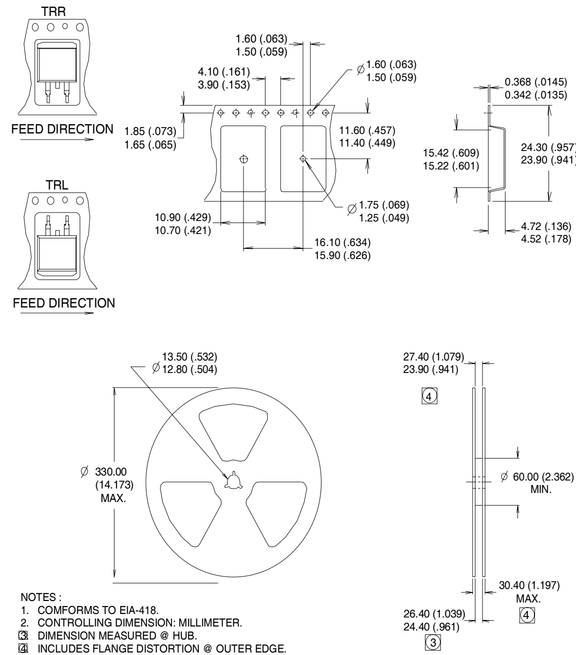
## $D^2$Pak Tape & Reel Infomation




**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting $T_J = 25°C$, L = 0.25mH, $R_G = 25\Omega$, $I_{AS} = 17A$.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ This is only applied to TO-220AB pakcage.

⑤ This is applied to $D^2$Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 42A.

⑦ $R_\theta$ is measured at $T_J$ approximately 90°C

**TO-220AB package is not recommended for Surface Mount Application.**

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
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**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information. 3/04



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Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/

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