

HEXFET® Power MOSFET

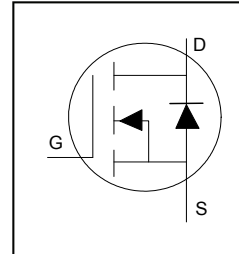
Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free
- Halogen-Free

| | |
|--------------------------|--------------|
| V_{DSS} | 60V |
| $R_{DS(on)}$ typ. | 3.3mΩ |
| max. | 4.2mΩ |
| I_D | 71A |



| | | |
|------|-------|--------|
| G | D | S |
| Gate | Drain | Source |

| Base Part Number | Package Type | Standard Pack | | Orderable Part Number |
|------------------|-----------------|---------------|----------|-----------------------|
| | | Form | Quantity | |
| IRFI3306GPbF | TO-220 Full-Pak | Tube | 50 | IRFI3306GPbF |

Absolute Maximum Ratings

| Symbol | Parameter | Max. | Units |
|---------------------------------|---|---|-------|
| $I_D @ T_C = 25^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ | 71 | A |
| $I_D @ T_C = 100^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ | 50 | |
| I_{DM} | Pulsed Drain Current ① | 300 | |
| $P_D @ T_C = 25^\circ\text{C}$ | Maximum Power Dissipation | 46 | W |
| | Linear Derating Factor | 0.31 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| E_{AS} | Single Pulse Avalanche Energy (Thermally Limited) ② | 311 | mJ |
| T_J | Operating Junction and Storage Temperature Range | -55 to + 175 | °C |
| T_{STG} | | | |
| | | Soldering Temperature, for 10 seconds (1.6mm from case) | |
| | Mounting torque, 6-32 or M3 screw | 10lb•in (1.1N•m) | |

Thermal Resistance

| Symbol | Parameter | Typ. | Max. | Units |
|-----------------|-----------------------------------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case ④ | — | 3.23 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB Mount) ④ | — | 65 | |

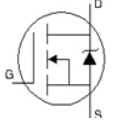
Static Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|--|--------------------------------------|------|-------|------|-------|---|
| V _{(BR)DSS} | Drain-to-Source Breakdown Voltage | 60 | — | — | V | V _{GS} = 0V, I _D = 250μA |
| ΔV _{(BR)DSS} /ΔT _J | Breakdown Voltage Temp. Coefficient | — | 0.068 | — | V/°C | Reference to 25°C, I _D = 5.0mA ^③ |
| R _{DS(on)} | Static Drain-to-Source On-Resistance | — | 3.3 | 4.2 | mΩ | V _{GS} = 10V, I _D = 43A ^③ |
| V _{GS(th)} | Gate Threshold Voltage | 2.0 | — | 4.0 | V | V _{DS} = V _{GS} , I _D = 150μA |
| I _{DSS} | Drain-to-Source Leakage Current | — | — | 20 | μA | V _{DS} = 60V, V _{GS} = 0V |
| | | — | — | 250 | | V _{DS} = 60V, V _{GS} = 0V, T _J = 125°C |
| I _{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | V _{GS} = 20V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | V _{GS} = -20V |
| R _{G(int)} | Internal Gate Resistance | — | 0.72 | — | Ω | |

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------------------------|---|------|------|------|-------|---|
| g _{fs} | Forward Transconductance | 89 | — | — | S | V _{DS} = 25V, I _D = 43A |
| Q _g | Total Gate Charge | — | 90 | 135 | nC | I _D = 43A |
| Q _{gs} | Gate-to-Source Charge | — | 22 | — | | V _{DS} = 30V |
| Q _{gd} | Gate-to-Drain ("Miller") Charge | — | 26 | — | | V _{GS} = 10V ^③ |
| Q _{sync} | Total Gate Charge Sync. (Q _g - Q _{gd}) | — | 116 | — | | I _D = 43A, V _{DS} = 0V, V _{GS} = 10V |
| t _{d(on)} | Turn-On Delay Time | — | 15 | — | ns | V _{DD} = 39V |
| t _r | Rise Time | — | 30 | — | | I _D = 43A |
| t _{d(off)} | Turn-Off Delay Time | — | 45 | — | | R _G = 2.7Ω |
| t _f | Fall Time | — | 33 | — | | V _{GS} = 10V ^③ |
| C _{iss} | Input Capacitance | — | 4685 | — | pF | V _{GS} = 0V |
| C _{oss} | Output Capacitance | — | 506 | — | | V _{DS} = 50V |
| C _{rss} | Reverse Transfer Capacitance | — | 310 | — | | f = 1.0 MHz |
| C _{oss} eff. (ER) | Effective Output Capacitance (Energy Related) ^⑥ | — | 733 | — | | V _{GS} = 0V, V _{DS} = 0V to 48V ^⑥ |
| C _{oss} eff. (TR) | Effective Output Capacitance (Time Related) ^⑤ | — | 822 | — | | V _{GS} = 0V, V _{DS} = 0V to 48V ^⑤ |

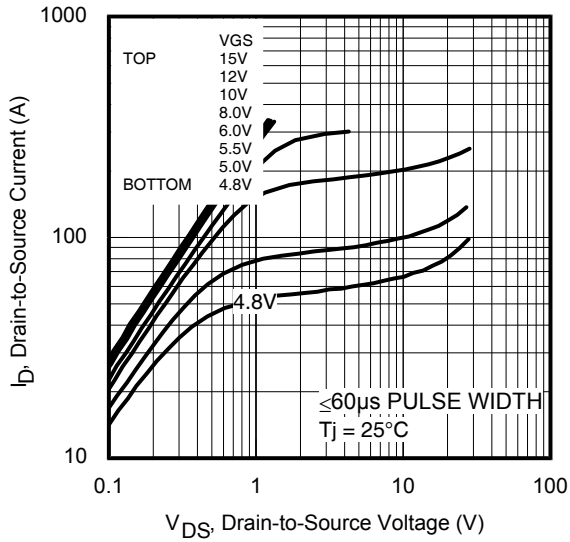
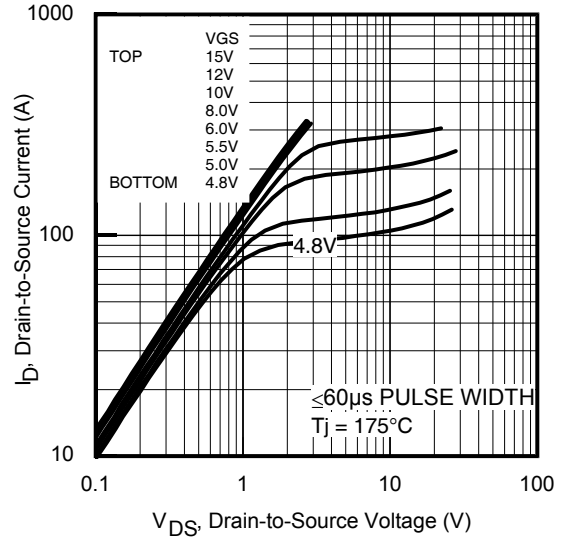
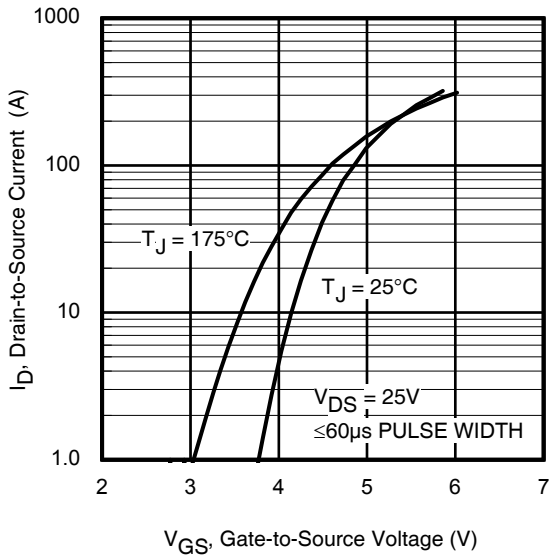
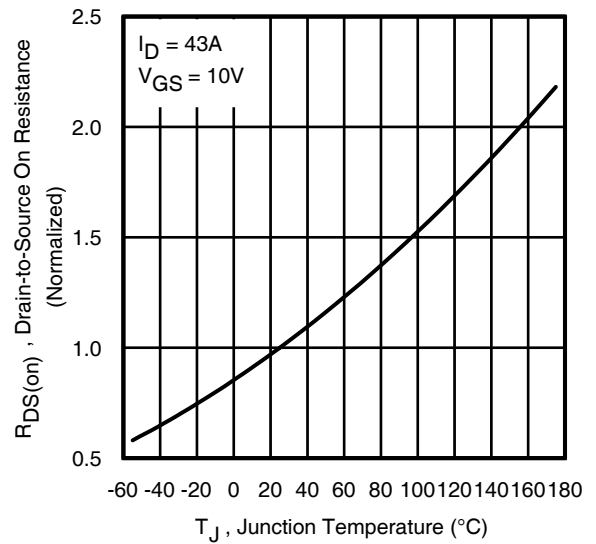
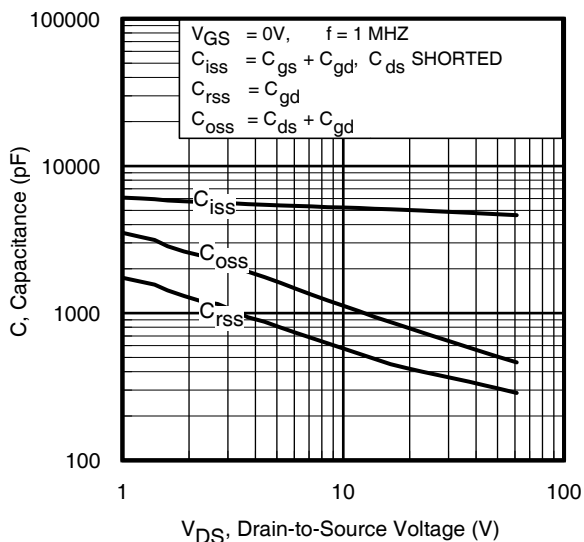
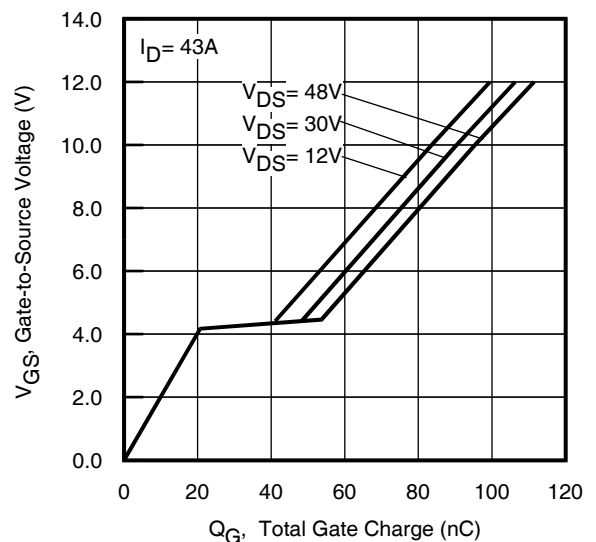
Diode Characteristics

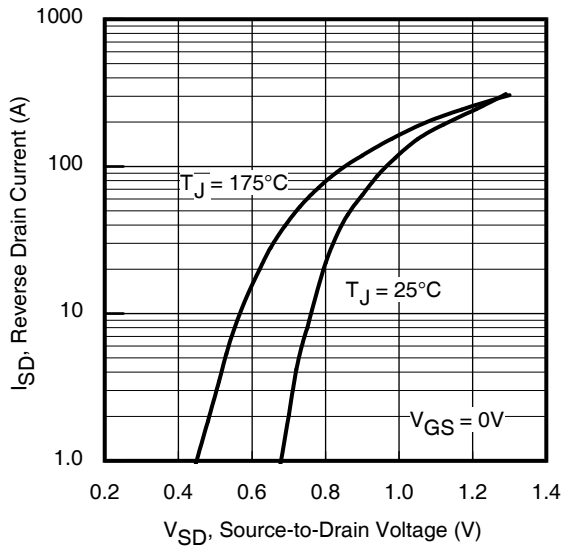
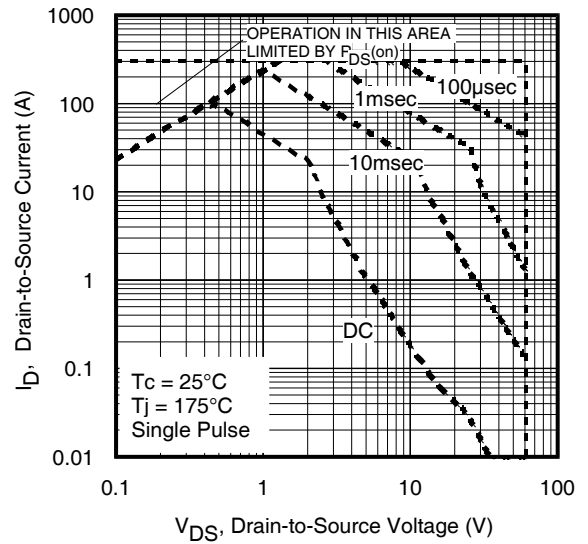
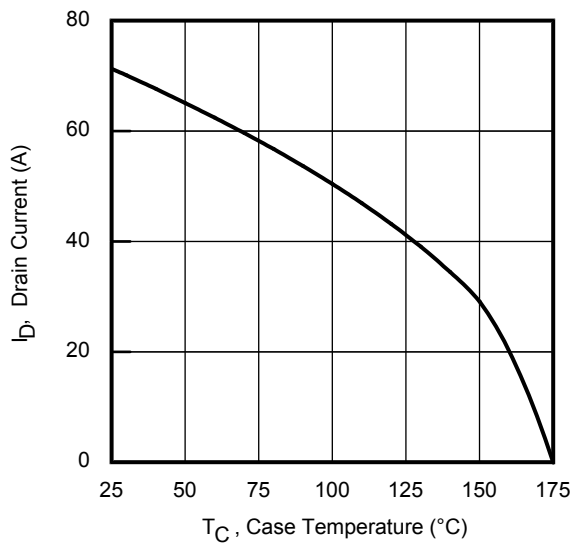
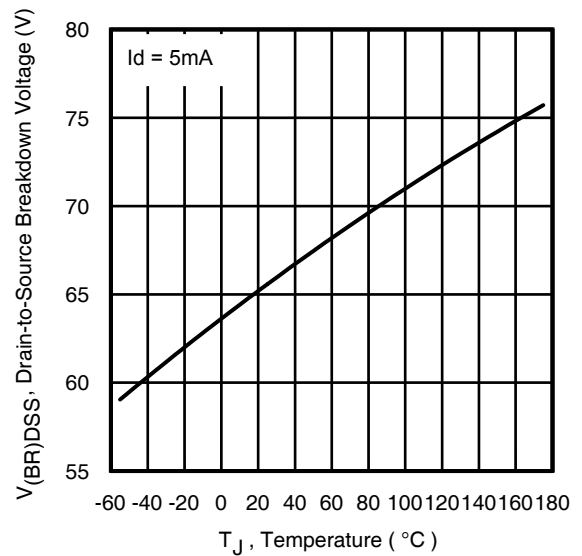
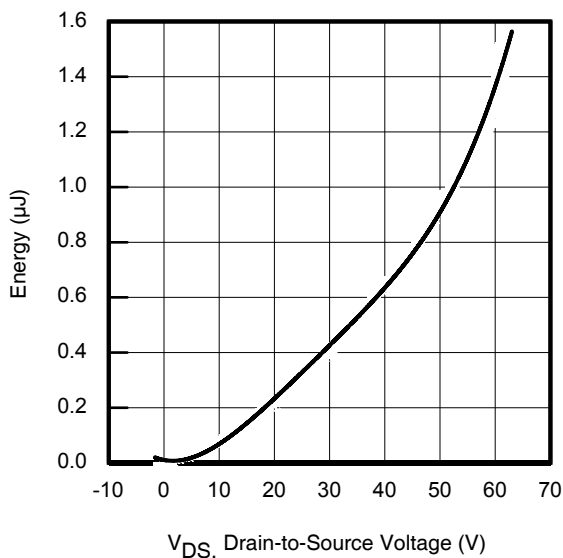
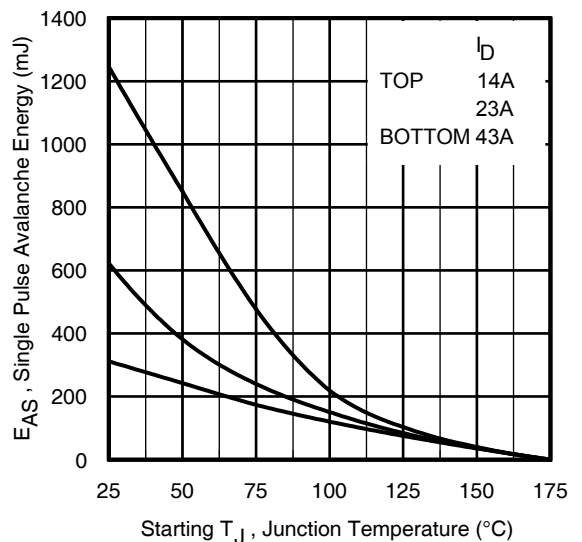
| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|-----------------|---|------|------|------|-------|--|
| I _S | Continuous Source Current (Body Diode) | — | — | 71 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| I _{SM} | Pulsed Source Current (Body Diode) ^② | — | — | 300 | A | |
| V _{SD} | Diode Forward Voltage | — | — | 1.3 | V | T _J = 25°C, I _S = 43A, V _{GS} = 0V ^③ |
| dv/dt | Peak Diode Recovery ^④ | — | 2.3 | — | V/ns | |
| t _{rr} | Reverse Recovery Time | — | 43 | — | ns | T _J = 25°C — V _R = 51V |
| | | — | 47 | — | | T _J = 125°C — I _F = 43A |
| Q _{rr} | Reverse Recovery Charge | — | 63 | — | nC | T _J = 25°C — di/dt = 100A/μs ^③ |
| | | — | 78 | — | | T _J = 125°C — |
| I _R | Reverse Recovery Current | — | 2.5 | — | A | T _J = 25°C |

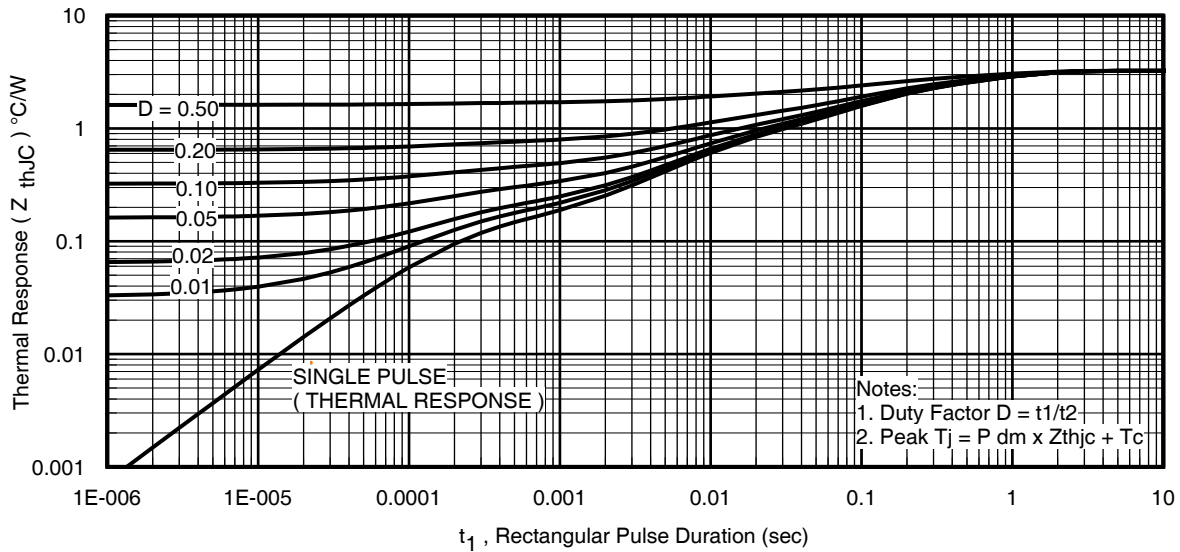
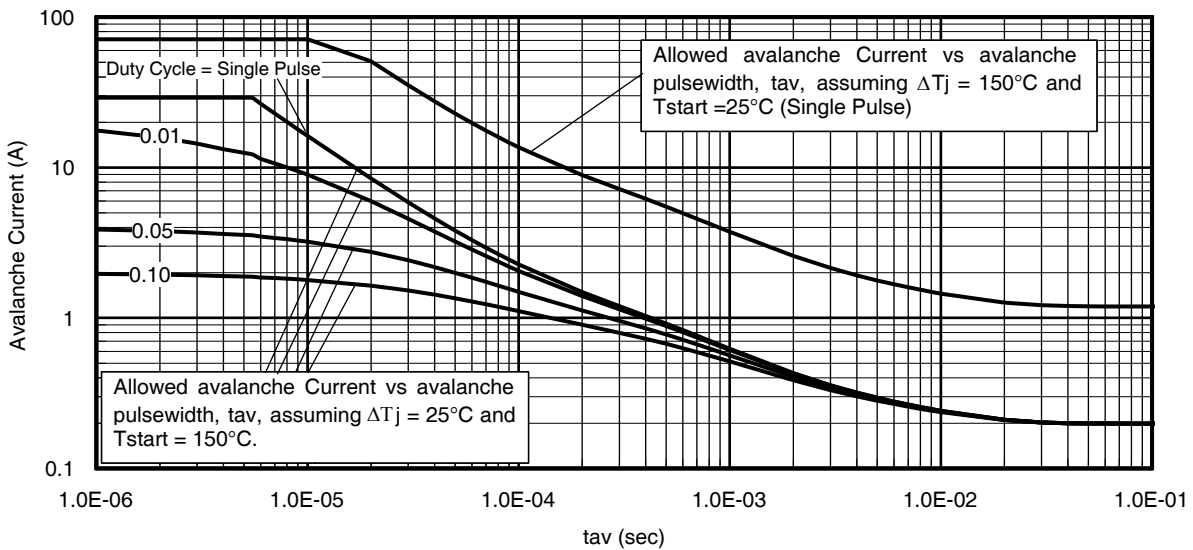
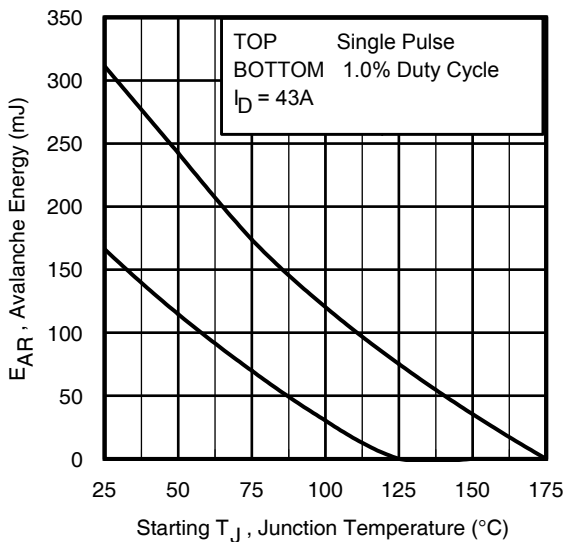
Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.34mH
R_G = 50Ω, I_{AS} = 43A, V_{GS} = 10V. Part not recommended for use above this value.
- ③ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ④ R_θ is measured at T_J approximately 90°C.

- ⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.


Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics

Fig. 3 Typical Transfer Characteristics

Fig. 4 Normalized On-Resistance vs. Temperature

Fig. 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig. 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

Fig. 8. Maximum Safe Operating Area

Fig. 9. Maximum Drain Current vs. Case Temperature

Fig. 10. Drain-to-Source Breakdown Voltage

Fig. 11. Typical Coss Stored Energy

Fig. 12. Maximum Avalanche Energy vs. Drain Current


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 14. Typical Avalanche Current vs. Pulsewidth

Notes on Repetitive Avalanche Curves, Figures 13, 14:
(For further info, see AN-1005 at www.irf.com)

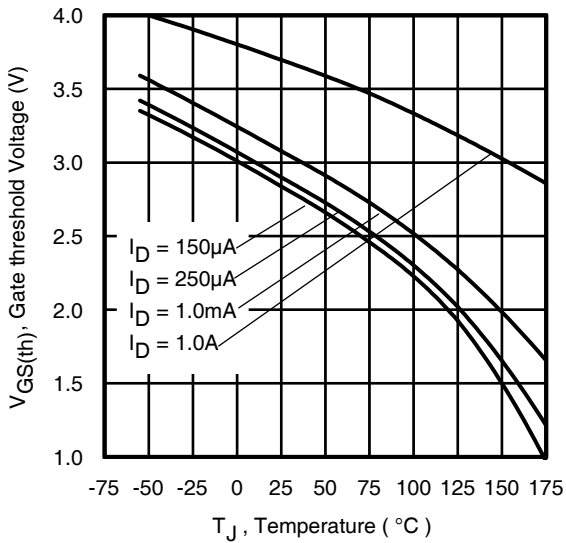
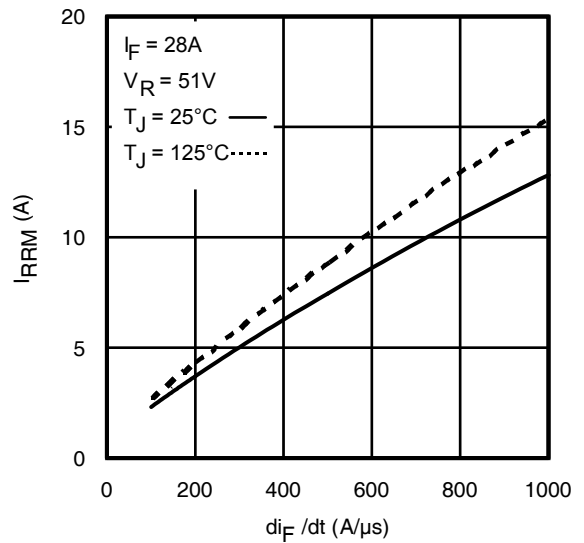
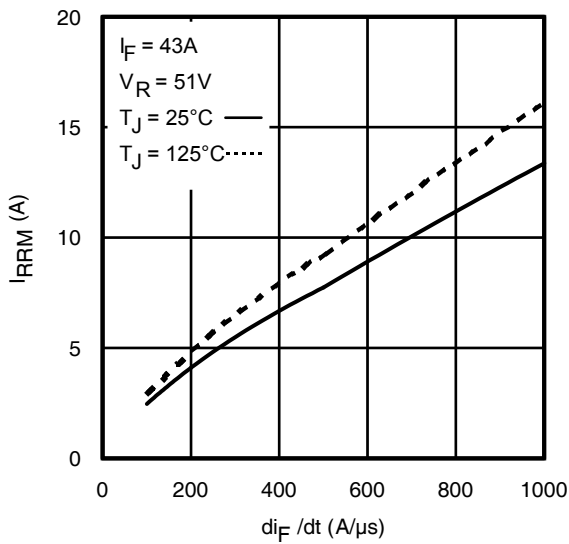
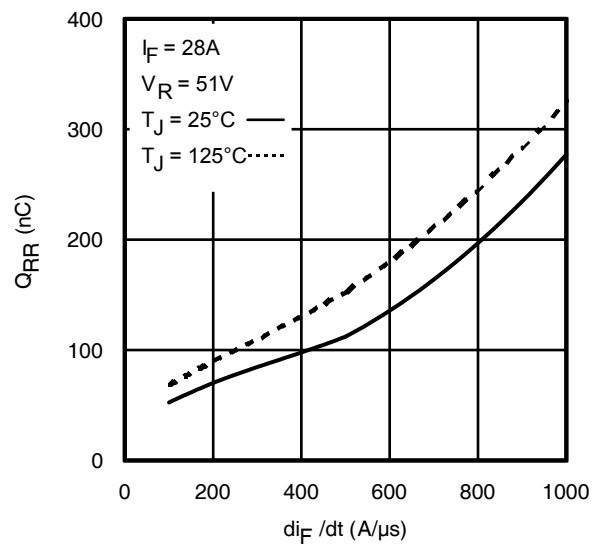
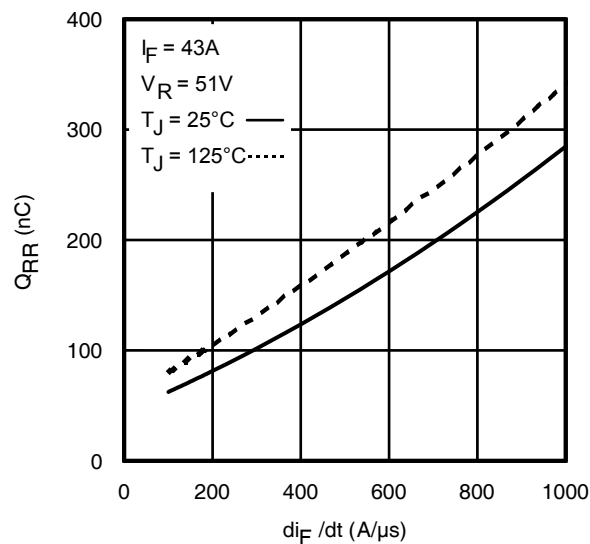
1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

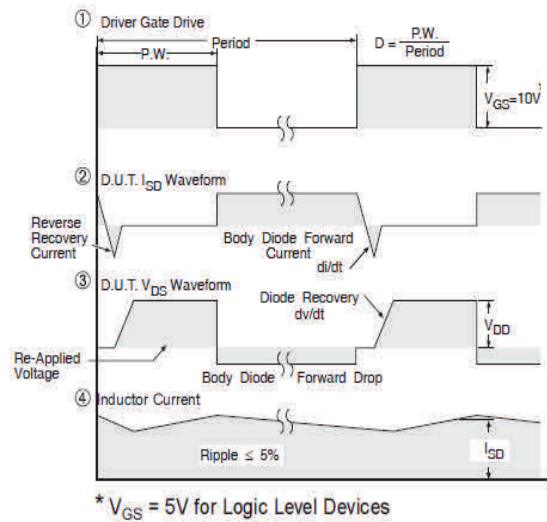
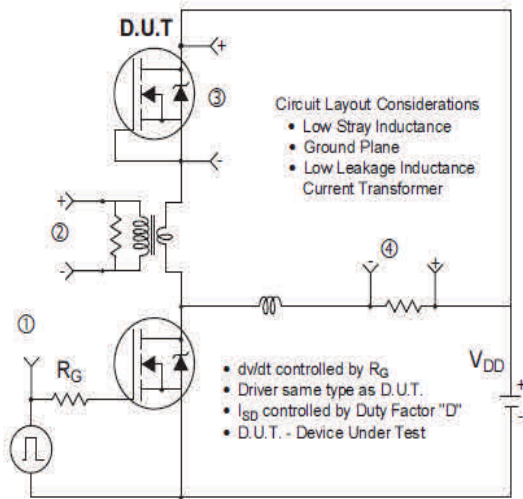
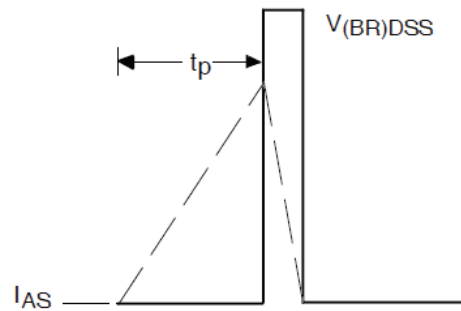
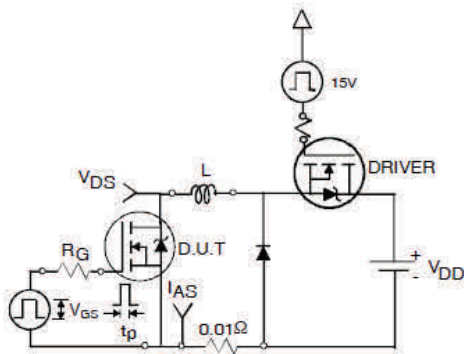
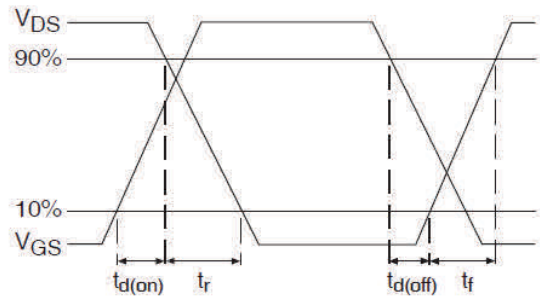
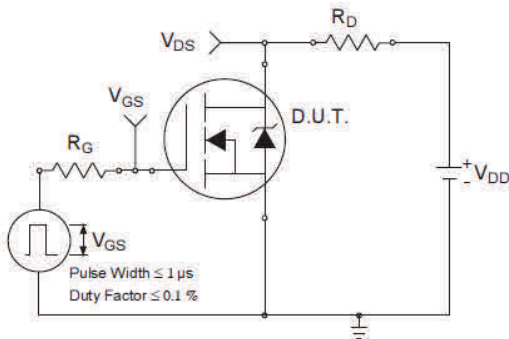
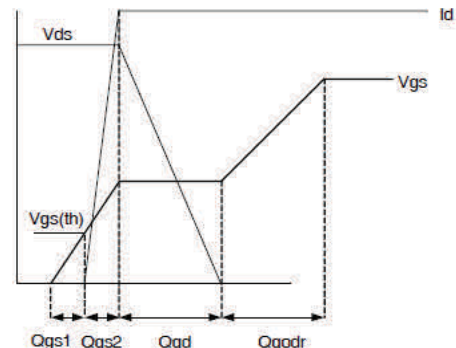
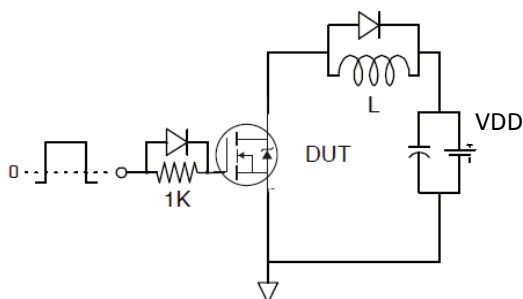
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

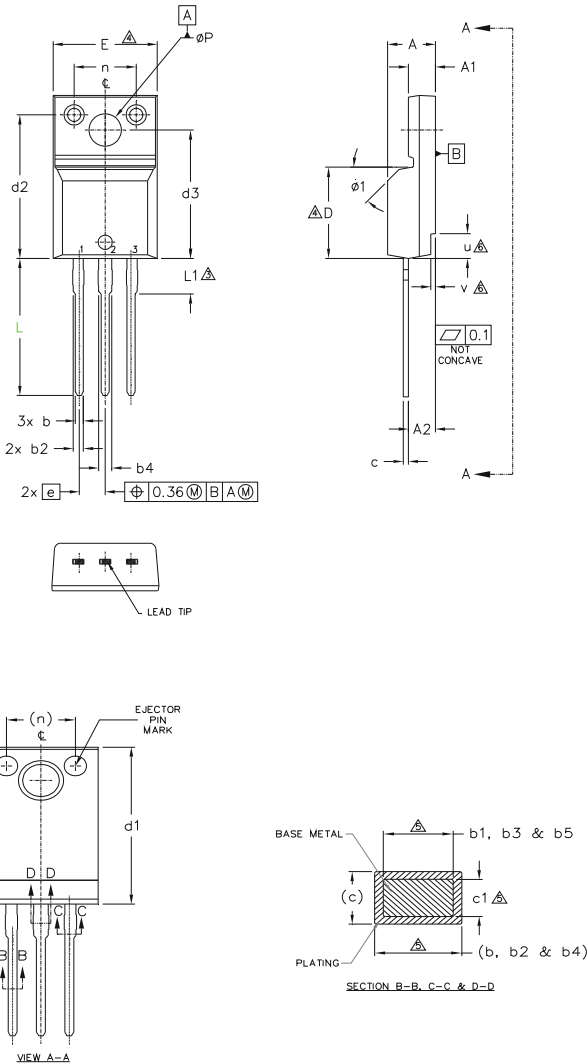
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature


Fig 16. Threshold Voltage vs. Temperature

Fig 17. Typical Recovery Current vs. di_F/dt

Fig. 18 - Typical Recovery Current vs. di_F/dt

Fig. 19 - Typical Stored Charge vs. di_F/dt

Fig. 20 - Typical Stored Charge vs. di_F/dt


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

Fig 22a. Unclamped Inductive Test Circuit
Fig 22b. Unclamped Inductive Waveforms

Fig 23a. Switching Time Test Circuit
Fig 23b. Switching Time Waveforms

Fig 24a. Gate Charge Test Circuit
Fig 24b. Gate Charge Waveform

TO-220 Full-Pak Package Outline (Dimensions are shown in millimeters (inches))

NOTES:

- 1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.
- 5.0 DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY.
- 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
- 7.0 CONTROLLING DIMENSION : INCHES.

| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|-------|----------|------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4.57 | 4.83 | .180 | .190 | |
| A1 | 2.57 | 2.82 | .101 | .111 | |
| A2 | 2.51 | 2.92 | .099 | .115 | |
| b | 0.61 | 0.94 | .024 | .037 | |
| b1 | 0.61 | 0.89 | .024 | .035 | |
| b2 | 0.76 | 1.27 | .030 | .050 | |
| b3 | 0.76 | 1.22 | .030 | .048 | |
| b4 | 1.02 | 1.52 | .040 | .060 | |
| b5 | 1.02 | 1.47 | .040 | .058 | |
| c | 0.33 | 0.63 | .013 | .025 | |
| c1 | 0.33 | 0.58 | .013 | .023 | |
| D | 8.66 | 9.80 | .341 | .386 | |
| d1 | 15.80 | 16.13 | .622 | .635 | |
| d2 | 13.97 | 14.22 | .550 | .560 | |
| d3 | 12.29 | 12.93 | .484 | .509 | |
| E | 9.63 | 10.74 | .379 | .423 | |
| e | 2.54 BSC | | .100 BSC | | |
| L | 13.21 | 13.72 | .520 | .540 | 3 |
| L1 | 3.10 | 3.68 | .122 | .145 | |
| n | 6.05 | 6.60 | .238 | .260 | |
| phi P | 3.05 | 3.45 | .120 | .136 | 6 |
| u | 2.39 | 2.49 | .094 | .098 | |
| v | 0.41 | 0.51 | .016 | .020 | |
| phi 1 | - | 45* | - | 45* | 6 |

LEAD ASSIGNMENTS
HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

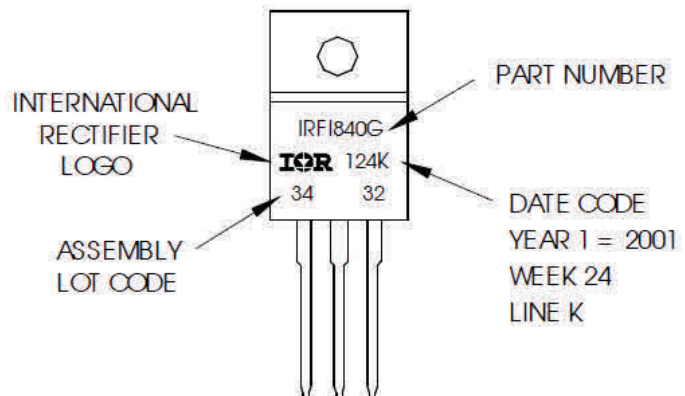
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G
 WITH ASSEMBLY
 LOT CODE 3432
 ASSEMBLED ON WW 24, 2001
 IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position
 indicates "Lead-Free"



TO-220AB Full-Pak packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification information

| | | |
|----------------------------|-----------------------------------|-------------------------|
| Qualification level | Industrial | |
| | (per JEDEC JESD47F † guidelines) | |
| Moisture Sensitivity Level | TO-220 Full-Pak | N/A |
| | | (per JEDEC J-STD-020D†) |
| RoHS compliant | Yes | |

† Applicable version of JEDEC standard at the time of product release.

Revision History

| Date | Comments |
|------------|---|
| 10/07/2013 | <ul style="list-style-type: none"> Removed the “Silicon Limited” from the ID rating, on page 1. |
| 04/27/2017 | <ul style="list-style-type: none"> Changed datasheet with Infineon logo - all pages. Corrected Package Outline on page 8. Added disclaimer on last page. |

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