

IRS2109/IRS21094(S)PbF

HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V, 5 V, and 15 V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- High-side output in phase with IN input
- Logic and power ground +/- 5 V offset.
- Internal 540 ns deadtime, and programmable up to 5 μ s with one external R_{DT} resistor (IRS21094)
- Lower di/dt gate driver for better noise immunity
- Shutdown input turns off both channels.
- RoHS compliant

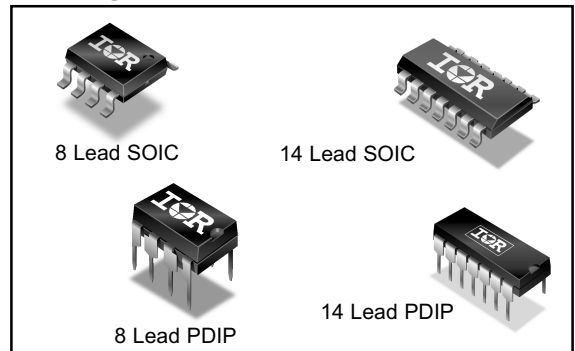
Description

The IRS2109/IRS21094 are high voltage, high speed power MOSFET and IGBT drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

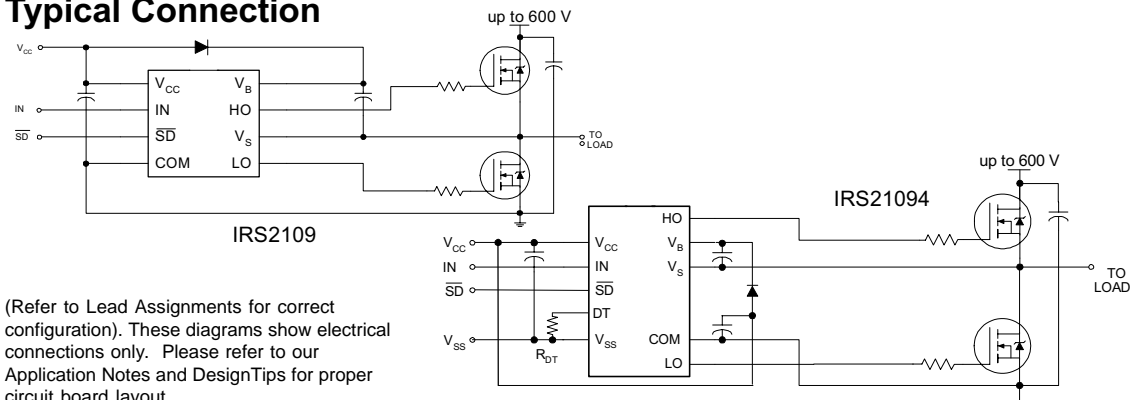
Product Summary

| | |
|---------------------|---|
| V_{OFFSET} | 600 V max. |
| $I_{O+/-}$ | 120 mA / 250 mA |
| V_{OUT} | 10 V - 20 V |
| $t_{on/off}$ (typ.) | 750 ns & 200 ns |
| Deadtime | 540 ns (programmable up to 5 μ s for IRS21094) |

Packages



Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | Min. | Max. | Units | |
|---------------------|---|-----------------------|-----------------------|-------|------|
| V _B | High-side floating absolute voltage | -0.3 | 625 | V | |
| V _S | High-side floating supply offset voltage | V _B - 25 | V _B + 0.3 | | |
| V _{HO} | High-side floating output voltage | V _S - 0.3 | V _B + 0.3 | | |
| V _{CC} | Low-side and logic fixed supply voltage | -0.3 | 25 | | |
| V _{LO} | Low-side output voltage | -0.3 | V _{CC} + 0.3 | | |
| DT | Programmable deadtime pin voltage (IRS21094 only) | V _{SS} - 0.3 | V _{CC} + 0.3 | | |
| V _{IN} | Logic input voltage (IN & \overline{SD}) | V _{SS} - 0.3 | V _{CC} + 0.3 | | |
| V _{SS} | Logic ground (IRS21094/IRS21894 only) | V _{CC} - 25 | V _{CC} + 0.3 | | |
| dV _S /dt | Allowable offset supply voltage transient | — | 50 | V/ns | |
| PD | Package power dissipation @ T _A ≤ +25 °C | (8 Lead PDIP) | — | 1.0 | W |
| | | (8 Lead SOIC) | — | 0.625 | |
| | | (14 lead PDIP) | — | 1.6 | |
| | | (14 lead SOIC) | — | 1.0 | |
| R _{thJA} | Thermal resistance, junction to ambient | (8 Lead PDIP) | — | 125 | °C/W |
| | | (8 Lead SOIC) | — | 200 | |
| | | (14 lead PDIP) | — | 75 | |
| | | (14 lead SOIC) | — | 120 | |
| T _J | Junction temperature | — | 150 | °C | |
| T _S | Storage temperature | -50 | 150 | | |
| T _L | Lead temperature (soldering, 10 seconds) | — | 300 | | |

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at a 15 V differential.

| Symbol | Definition | Min. | Max. | Units |
|----------|---|------------|------------|-------|
| V_B | High-side floating supply absolute voltage | $V_S + 10$ | $V_S + 20$ | V |
| V_S | High-side floating supply offset voltage | (Note 1) | 600 | |
| V_{HO} | High-side floating output voltage | V_S | V_B | |
| V_{CC} | Low-side and logic fixed supply voltage | 10 | 20 | |
| V_{LO} | Low-side output voltage | 0 | V_{CC} | |
| V_{IN} | Logic input voltage (IN & \overline{SD}) | V_{SS} | V_{CC} | |
| DT | Programmable deadtime pin voltage (IRS21094 only) | V_{SS} | V_{CC} | |
| V_{SS} | Logic ground (IRS21094 only) | -5 | 5 | °C |
| T_A | Ambient temperature | -40 | 125 | |

Note 1: Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$, $V_{SS} = \text{COM}$, $C_L = 1000\text{ pF}$, $T_A = 25\text{ °C}$, $DT = V_{SS}$ unless otherwise specified.

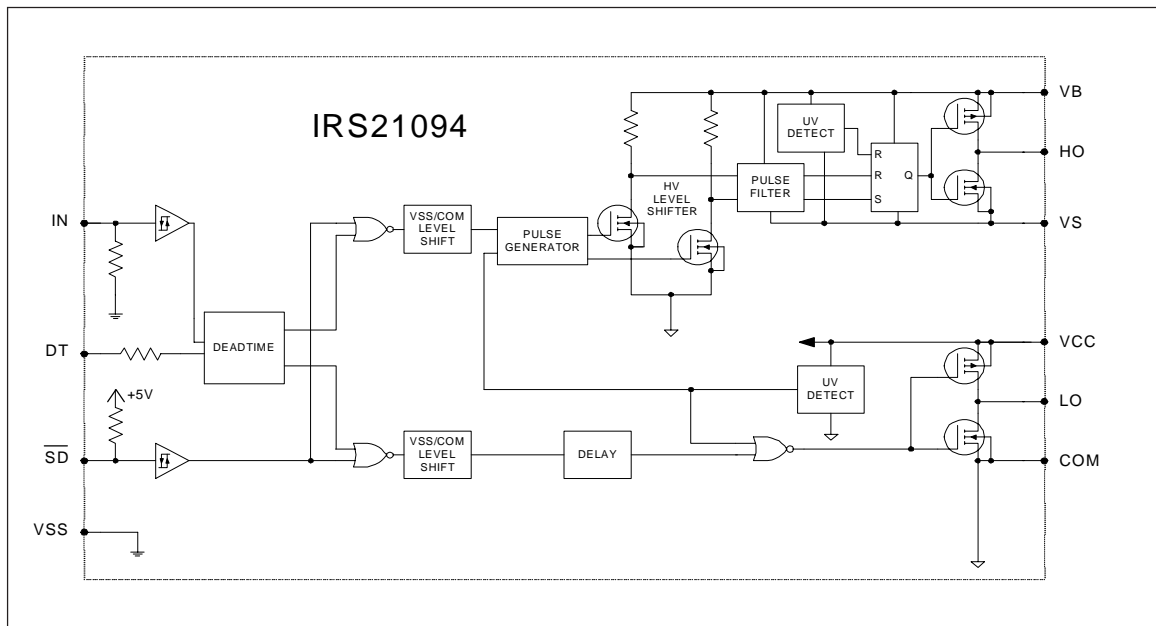
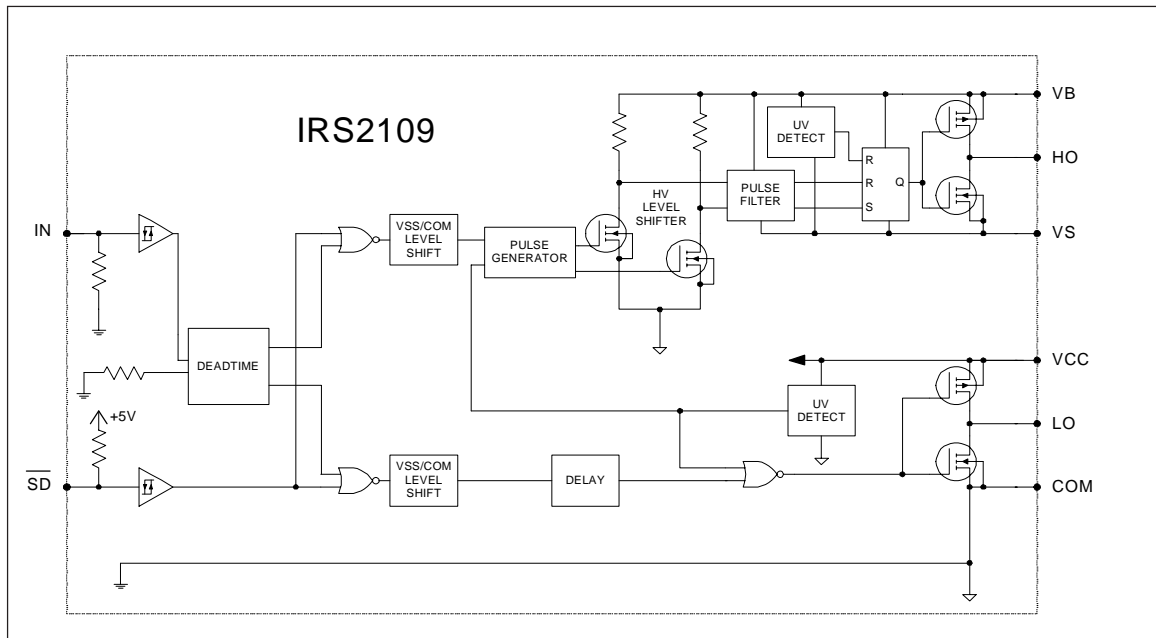
| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|-----------|---|------|------|------|---------------|--|
| t_{on} | Turn-on propagation delay | — | 750 | 950 | ns | $V_S = 0\text{ V}$ |
| t_{off} | Turn-off propagation delay | — | 200 | 280 | | $V_S = 0\text{ V or } 600\text{ V}$ |
| t_{sd} | Shutdown propagation delay | — | 200 | 280 | | $V_S = 0\text{ V}$ |
| MT | Delay matching, HS & LS turn-on/off | — | 0 | 70 | | |
| t_r | Turn-on rise time | — | 100 | 220 | | |
| t_f | Turn-off fall time | — | 35 | 80 | | $R_{DT} = 0\ \Omega$ |
| DT | Deadtime: LO turn-off to HO turn-on (DT _{LO-HO}) & HO turn-off to LO turn-on (DT _{HO-LO}) | 400 | 540 | 680 | μs | $R_{DT} = 200\text{ k}\Omega$ (IRS21094) |
| | | 4 | 5 | 6 | | $R_{DT} = 0\ \Omega$ |
| MDT | Deadtime matching = DT _{LO-HO} - DT _{HO-LO} | — | 0 | 60 | ns | $R_{DT} = 0\ \Omega$ |
| | | — | 0 | 600 | | $R_{DT} = 200\text{ k}\Omega$ (IRS21094) |

Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15 V, V_{SS} = COM, $DT = V_{SS}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified. The V_{IL} , V_{IH} , and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads: IN and \overline{SD} . The V_O , I_O , and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|----------------------------|--|------|------|------|---------------|---|
| V_{IH} | Logic "1" input voltage for HO & logic "0" for LO | 2.5 | — | — | V | $V_{CC} = 10\text{ V to }20\text{ V}$ |
| V_{IL} | Logic "0" input voltage for HO & logic "1" for LO | — | — | 0.8 | | |
| $V_{SD,TH+}$ | \overline{SD} input positive going threshold | 2.5 | — | — | | |
| $V_{SD,TH-}$ | \overline{SD} input negative going threshold | — | — | 0.8 | | |
| V_{OH} | High level output voltage, $V_{BIAS} - V_O$ | — | 0.05 | 0.2 | | |
| V_{OL} | Low level output voltage, V_O | — | 0.02 | 0.1 | | $I_O = 2\text{ mA}$ |
| I_{LK} | Offset supply leakage current | — | — | 50 | μA | $V_B = V_S = 600\text{ V}$ |
| I_{QBS} | Quiescent V_{BS} supply current | 20 | 75 | 130 | | $V_{IN} = 0\text{ V or }5\text{ V}$ |
| I_{QCC} | Quiescent V_{CC} supply current | 0.4 | 1.0 | 1.6 | mA | $V_{IN} = 0\text{ V or }5\text{ V}$ $R_{DT} = 0\ \Omega$ |
| I_{IN+} | Logic "1" input bias current | — | 5 | 20 | μA | $IN = 5\text{ V}, \overline{SD} = 0\text{ V}$ |
| I_{IN-} | Logic "0" input bias current | — | — | 2 | | $IN = 0\text{ V}, \overline{SD} = 5\text{ V}$ |
| V_{CCUV+} V_{BSUV+} | V_{CC} and V_{BS} supply undervoltage positive going threshold | 8.0 | 8.9 | 9.8 | V | |
| V_{CCUV-} V_{BSUV-} | V_{CC} and V_{BS} supply undervoltage negative going threshold | 7.4 | 8.2 | 9.0 | | |
| V_{CCUVH} V_{BSUVH} | Hysteresis | 0.3 | 0.7 | — | | |
| I_{O+} | Output high short circuit pulsed current | 120 | 290 | — | mA | $V_O = 0\text{ V}, PW \leq 10\ \mu\text{s}$ |
| I_{O-} | Output low short circuit pulsed current | 250 | 600 | — | | $V_O = 15\text{ V}, PW \leq 10\ \mu\text{s}$ |

Functional Block Diagrams



Lead Definitions

| Symbol | Description |
|-----------------|---|
| IN | Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO (referenced to COM for IRS2109 and VSS for IRS21094) |
| \overline{SD} | Logic input for shutdown (referenced to COM for IRS2109 and VSS for IRS21094) |
| DT | Programmable deadtime lead, referenced to VSS. (IRS21094 only) |
| VSS | Logic ground (IRS21094 only) |
| V_B | High-side floating supply |
| HO | High-side gate drive output |
| V_S | High-side floating supply return |
| V_{CC} | Low-side and logic fixed supply |
| LO | Low-side gate drive output |
| COM | Low-side return |

Lead Assignments

| | |
|--------------------|--------------------|
| <p>8 Lead PDIP</p> | <p>8 Lead SOIC</p> |
| IRS2109PbF | IRS2109SPbF |

| | |
|---------------------|---------------------|
| <p>14 Lead PDIP</p> | <p>14 Lead SOIC</p> |
| IRS21094PbF | IRS21094SPbF |

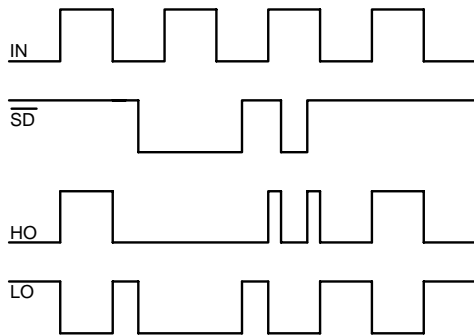


Figure 1. Input/Output Timing Diagram

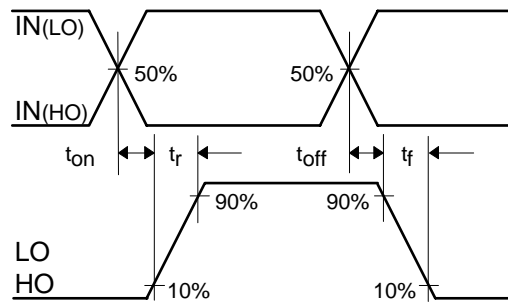


Figure 2. Switching Time Waveform Definitions

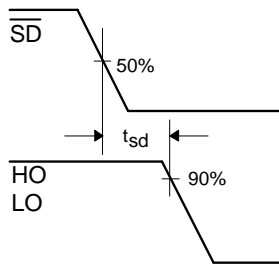


Figure 3. Shutdown Waveform Definitions

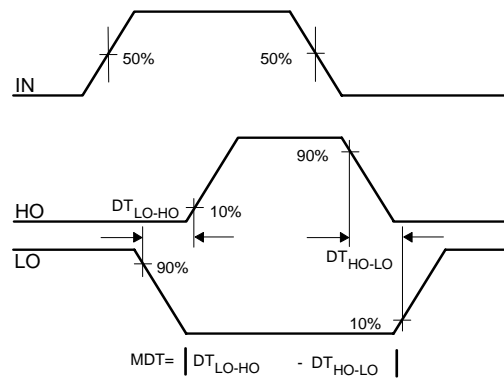


Figure 4. Deadtime Waveform Definitions

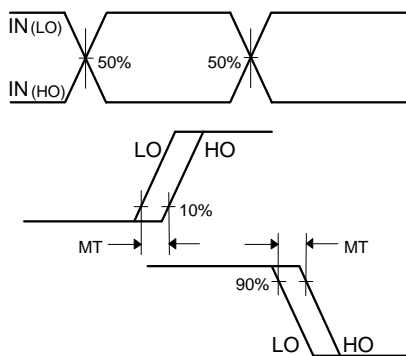


Figure 5. Delay Matching Waveform Definitions

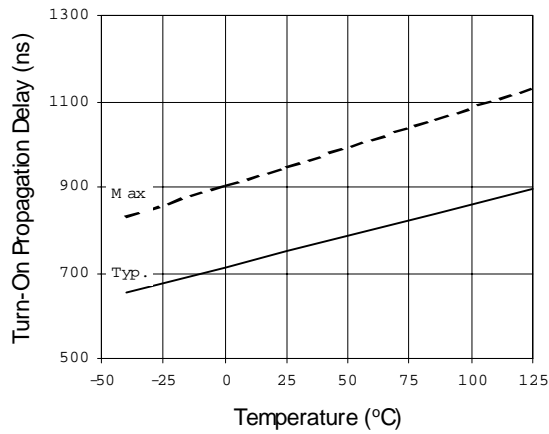


Figure 6A. Turn-On Propagation Delay vs. Temperature

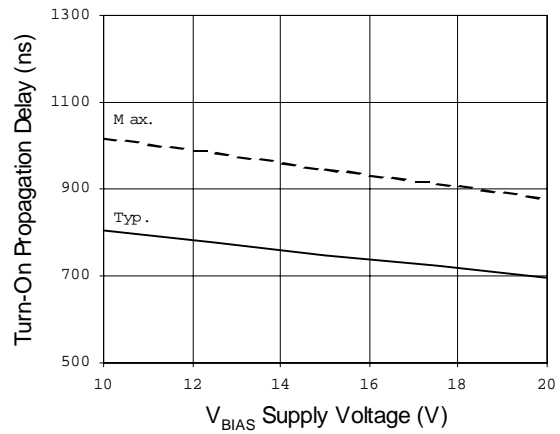


Figure 6B. Turn-On Propagation Delay vs. Supply Voltage

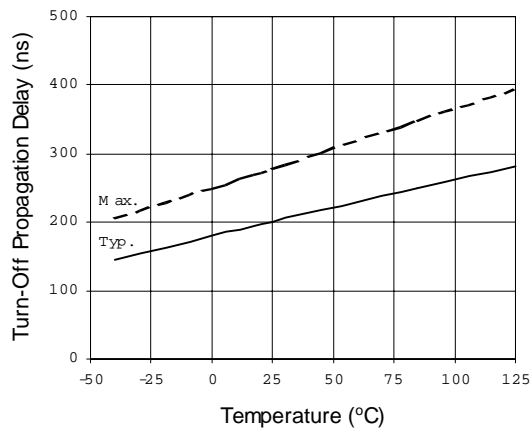


Figure 7A. Turn-Off Propagation Delay vs. Temperature

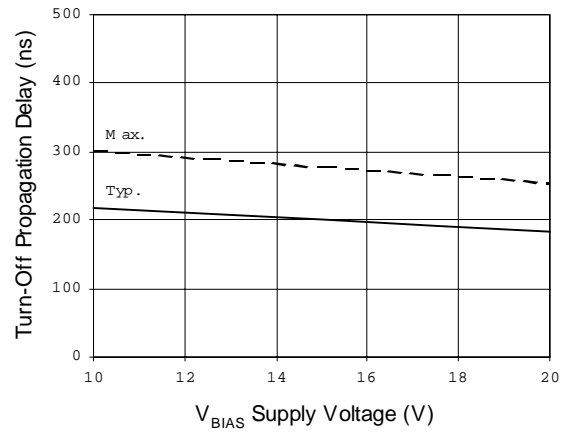


Figure 7B. Turn-Off Propagation Delay vs. Supply Voltage

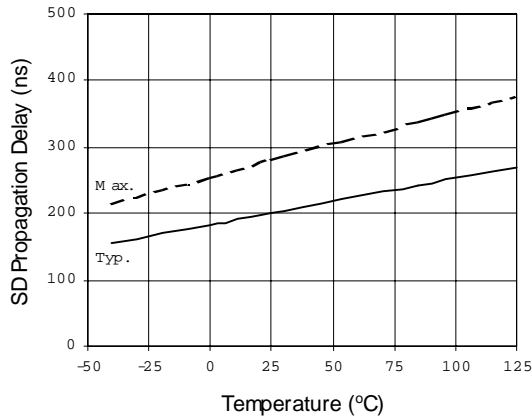


Figure 8A. SD Propagation Delay vs. Temperature

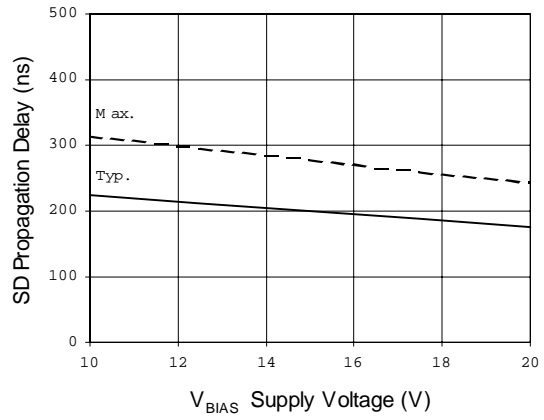


Figure 8B. SD Propagation Delay vs. Supply Voltage

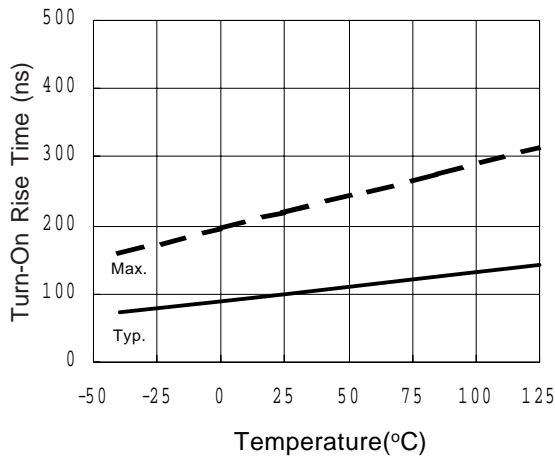


Figure 9A. Turn-On Rise Time vs. Temperature

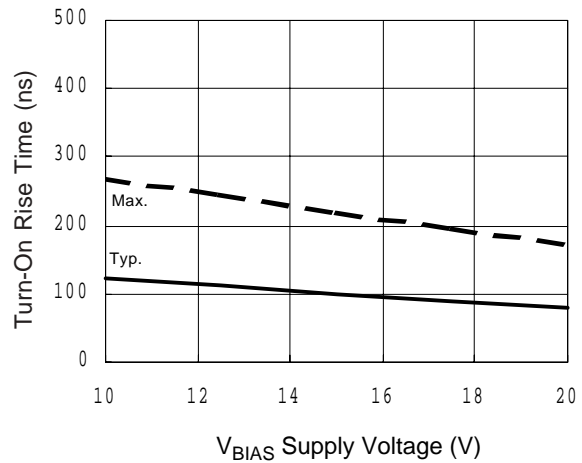


Figure 9B. Turn-On Rise Time vs. Supply Voltage

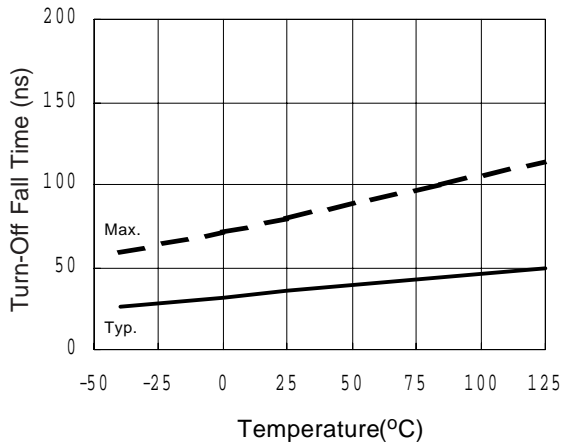


Figure 10A. Turn-Off Fall Time vs. Temperature

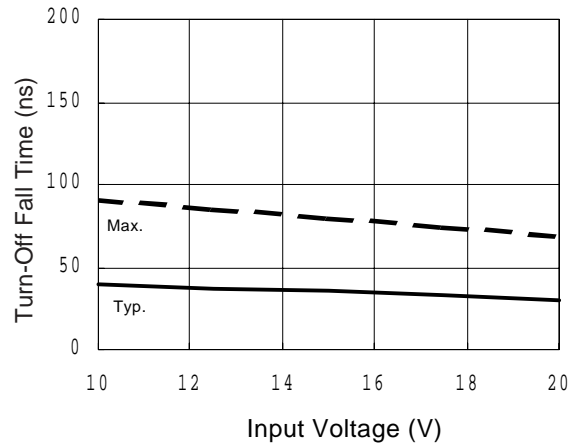


Figure 10B. Turn-Off Fall Time vs. Supply Voltage

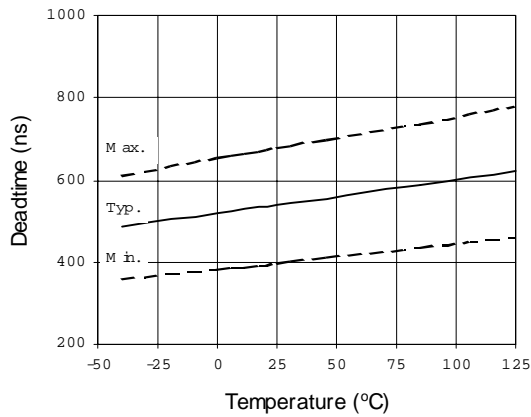


Figure 11A. Deadtime vs. Temperature

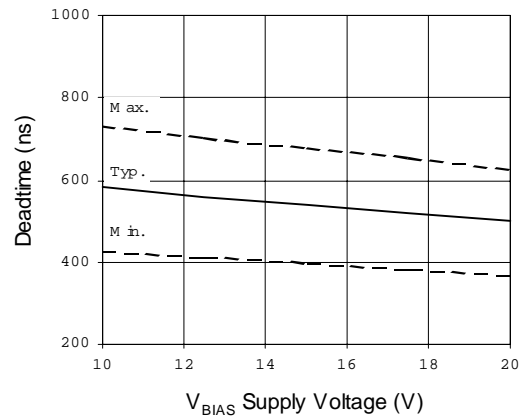
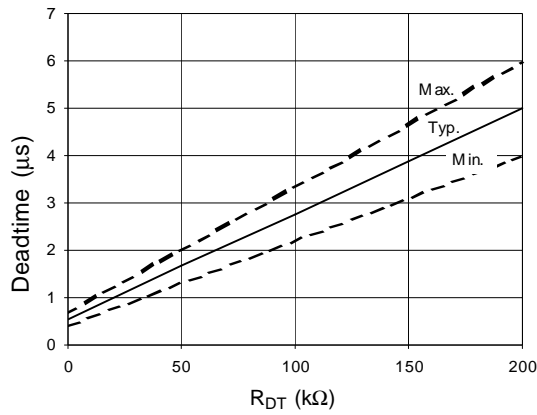
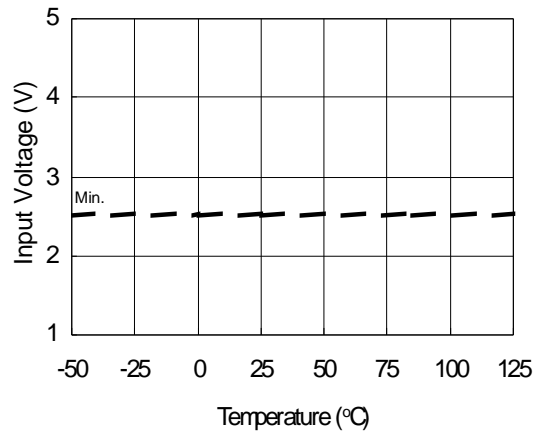


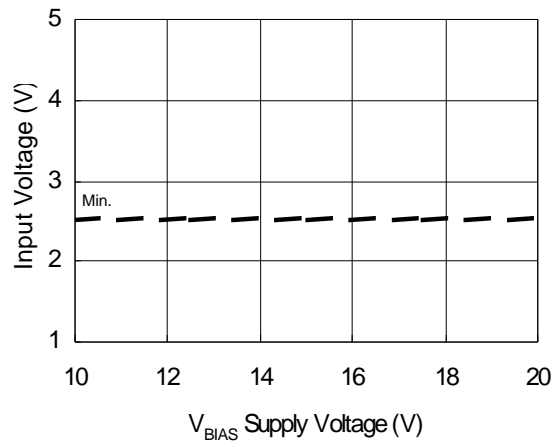
Figure 11B. Deadtime vs. Supply Voltage



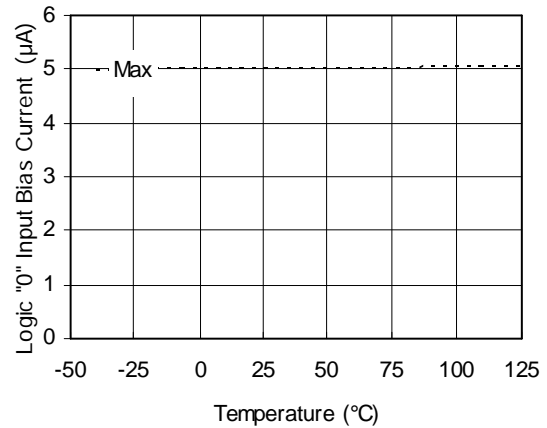
**Figure 11C. Deadtime vs. R_{DT}
 (IR21094 only)**



**Figure 12A. Logic "1" Input Voltage
 vs. Temperature**



**Figure 12B. Logic "1" Input Voltage
 vs. Supply Voltage**



**Figure 13A. Logic "0" Input Bias Current
 vs. Temperature**

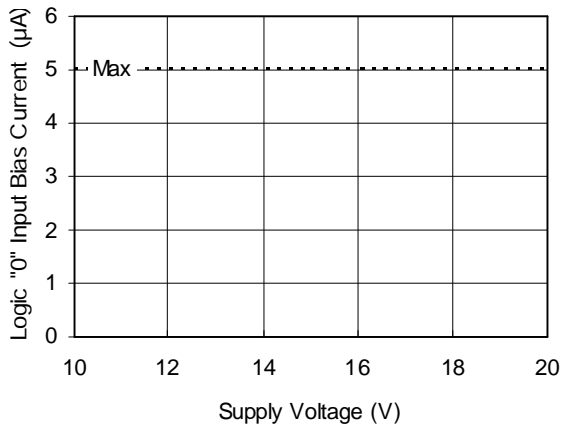


Figure 13B. Logic "0" Input Bias Current vs. Voltage

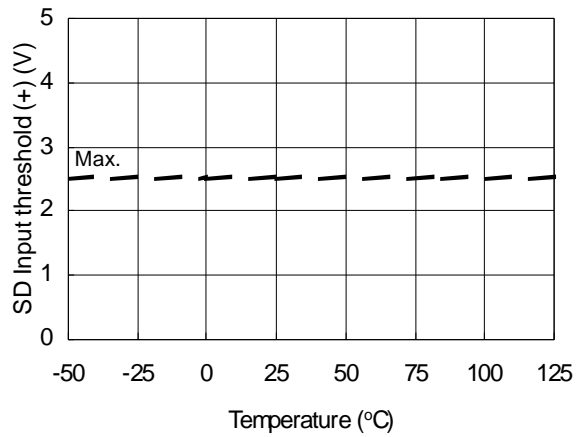


Figure 14A. SD Input Positive Going Threshold (+) vs. Temperature

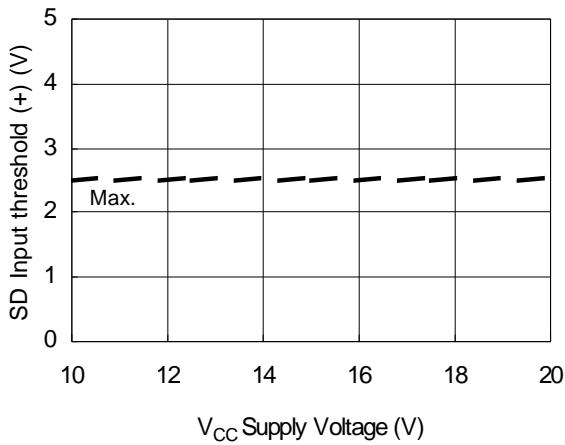


Figure 14B. SD Input Positive Going Threshold (+) vs. Supply Voltage

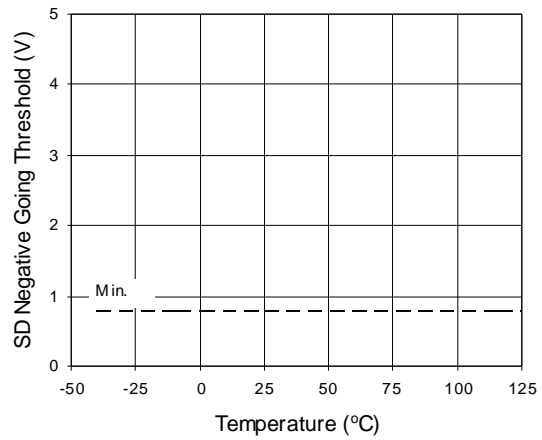


Figure 15A. SD Negative Going Threshold vs. Temperature

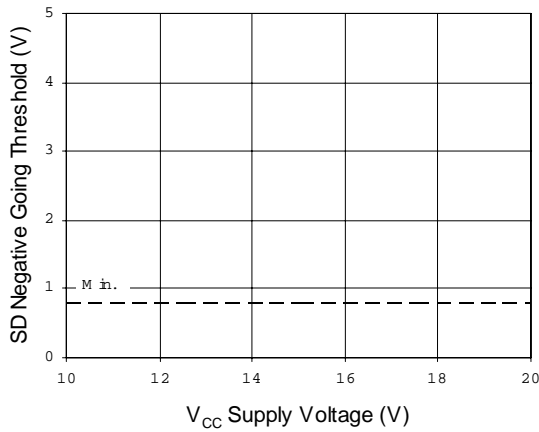


Figure 15B. SD Negative Going Threshold vs. Supply Voltage

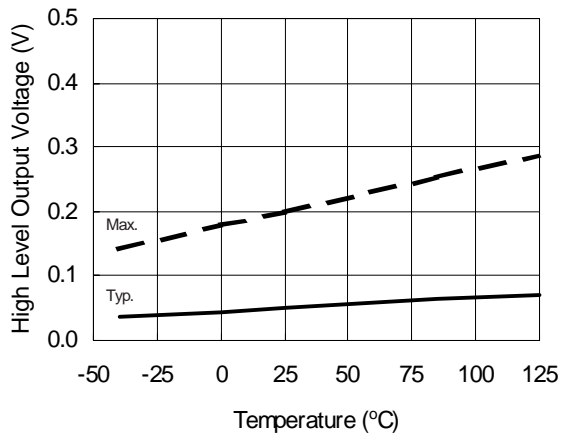


Figure 16A. High Level Output Voltage vs. Temperature

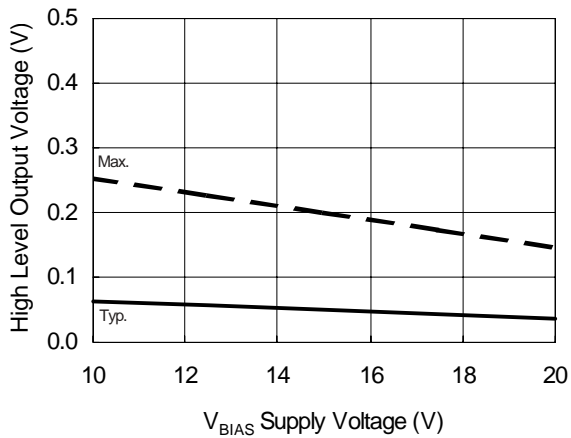


Figure 16B. High Level Output Voltage vs. Supply Voltage

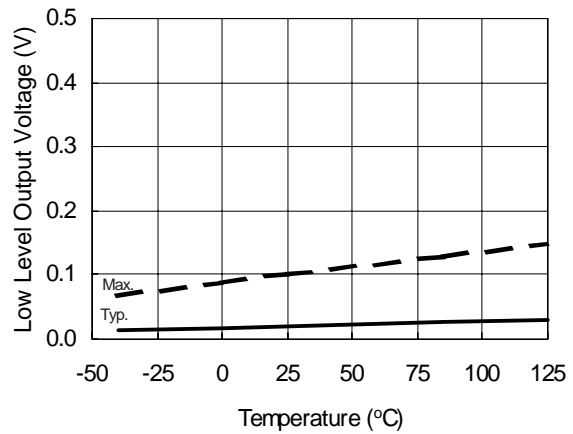


Figure 17A. Low Level Output Voltage vs. Temperature

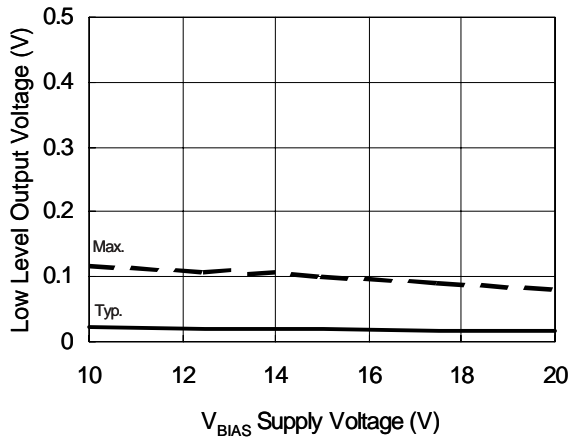


Figure 17B. Low Level Output Voltage vs. Supply Voltage

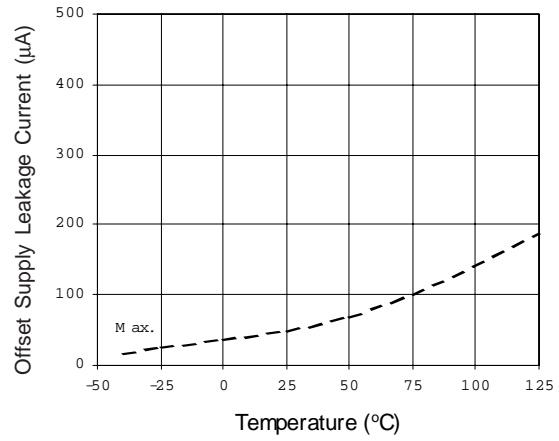


Figure 18A. Offset Supply Leakage Current vs. Temperature

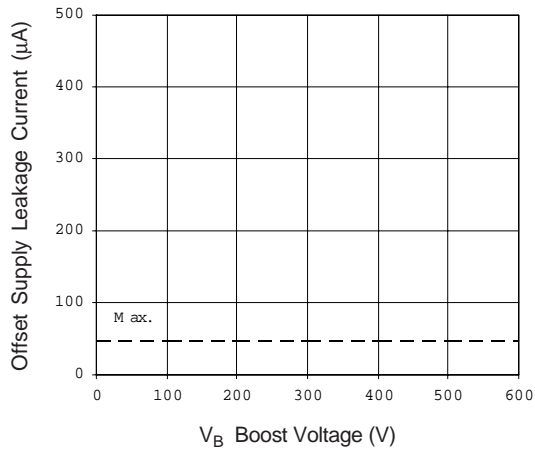


Figure 18B. Offset Supply Leakage Current vs. Boost Voltage

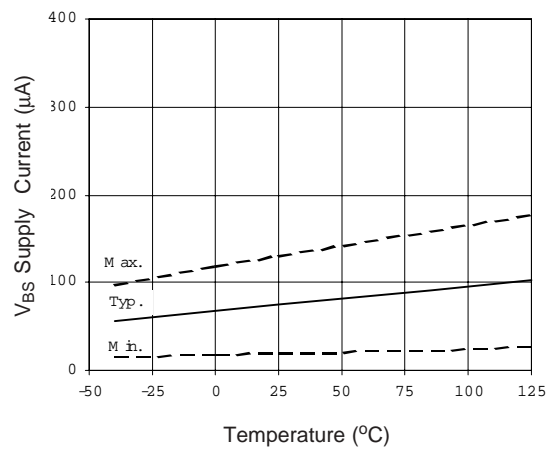


Figure 19A. V_{BS} Supply Current vs. Temperature

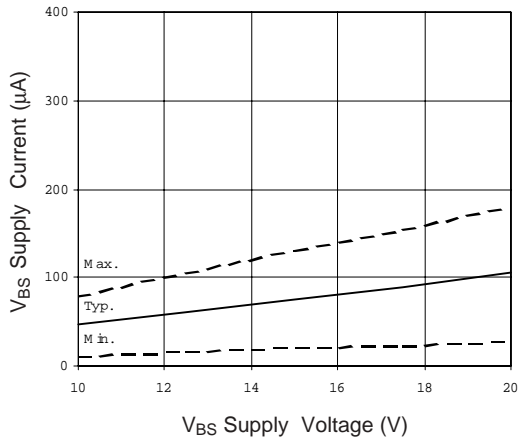


Figure 19B. VBS Supply Current vs. Supply Voltage

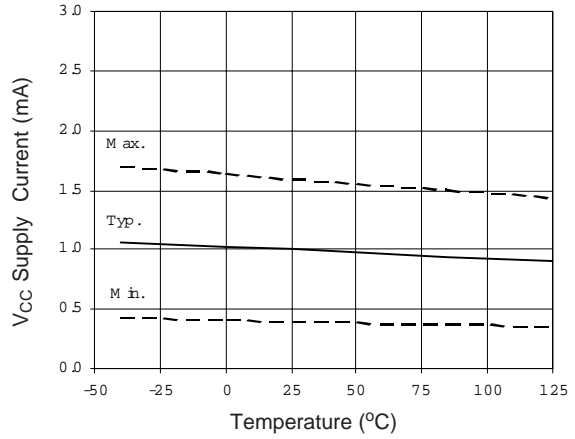


Figure 20A. VCC Supply Current vs. Temperature

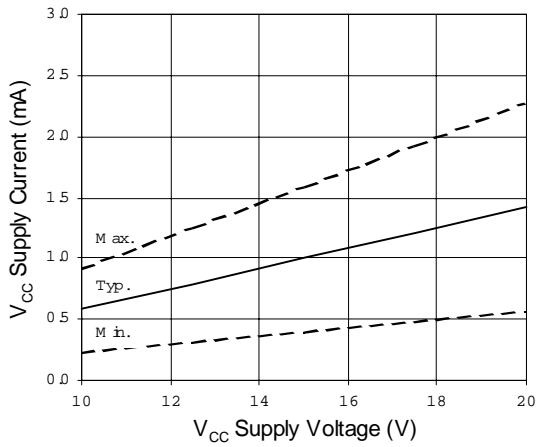


Figure 20B. VCC Supply Current vs. VCC Supply Voltage

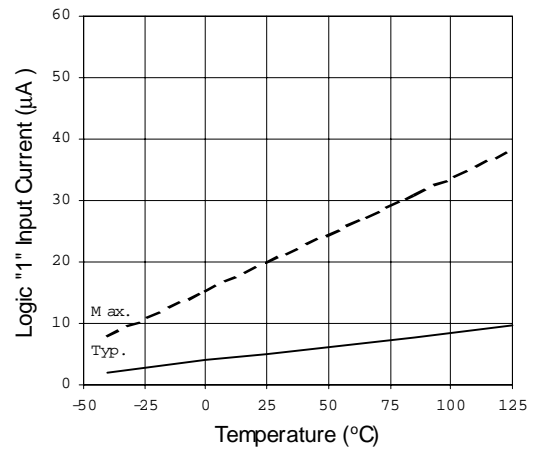


Figure 21A. Logic "1" Input Current vs. Temperature

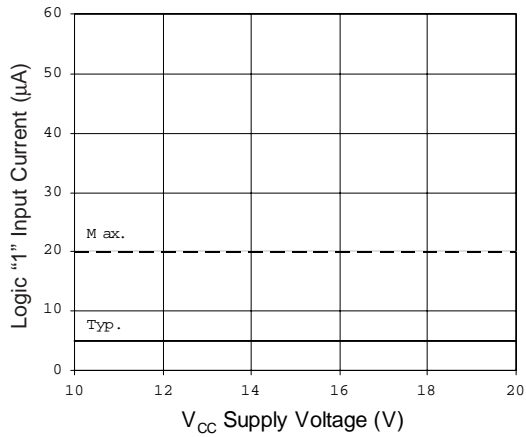


Figure 21B. Logic "1" Input Current vs. Supply Voltage

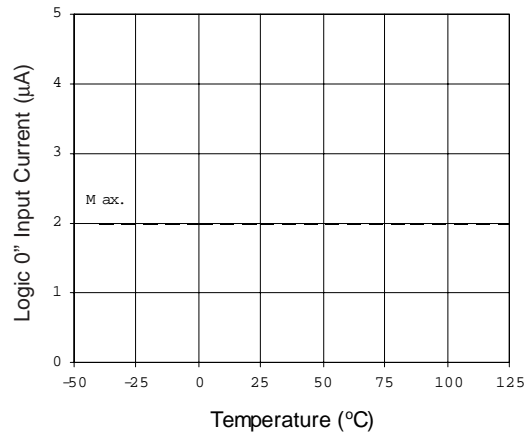


Figure 22A. Logic "0" Input Current vs. Temperature

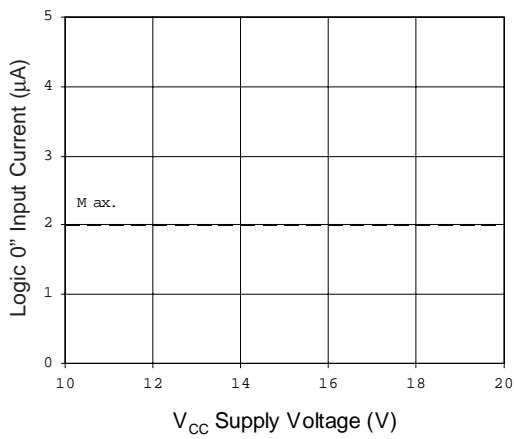


Figure 22B. Logic "0" Input Current vs. Supply Voltage

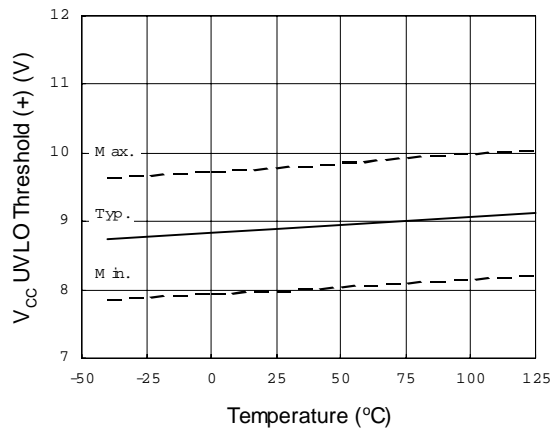


Figure 23. V_{CC} Undervoltage Threshold (+) vs. Temperature

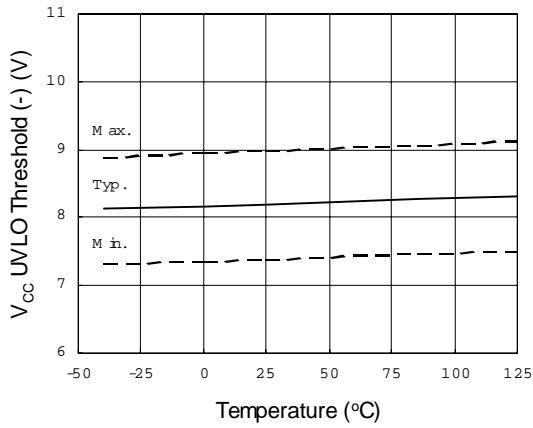


Figure 24. VCC Undervoltage Threshold (-) vs. Temperature

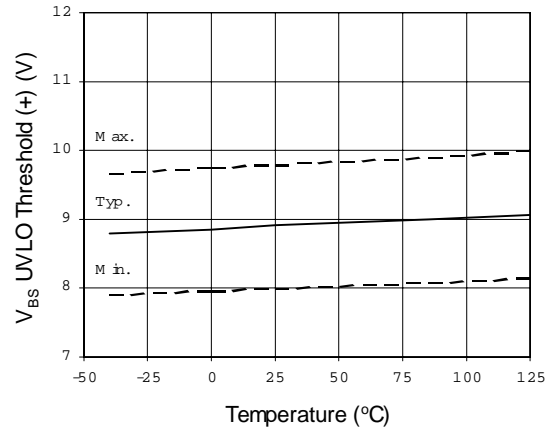


Figure 25. VBS Undervoltage Threshold (+) vs. Temperature

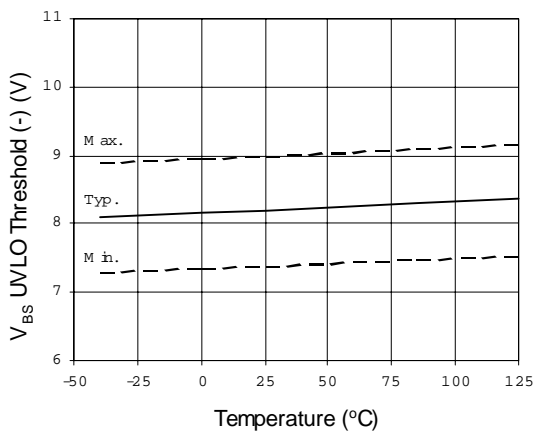


Figure 26. VBS Undervoltage Threshold (-) vs. Temperature

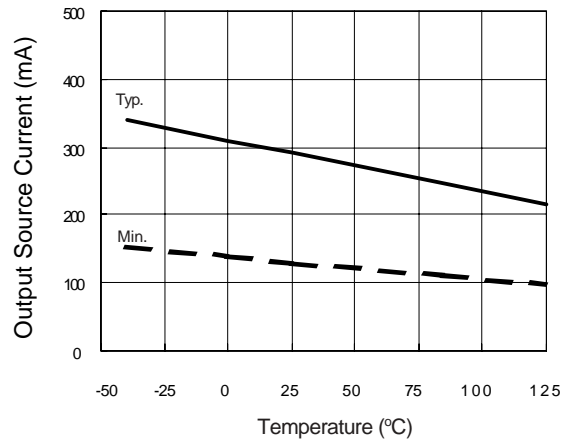


Figure 27A. Output Source Current vs. Temperature

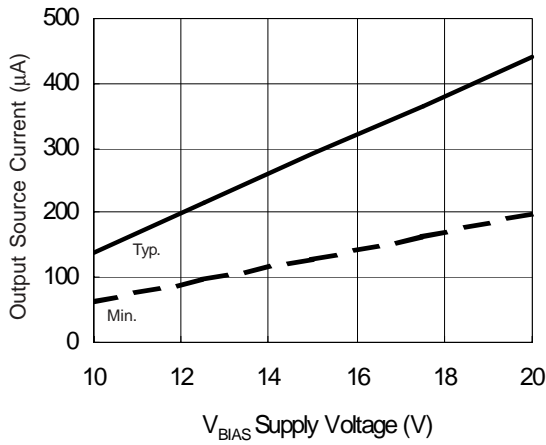


Figure 27B. Output Source Current vs. Supply Voltage

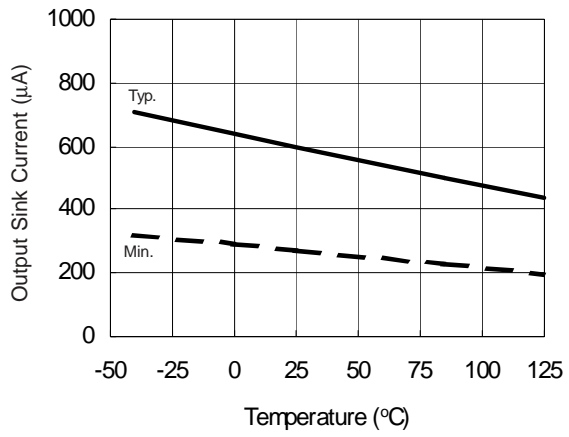


Figure 28A. Output Sink Current vs. Temperature

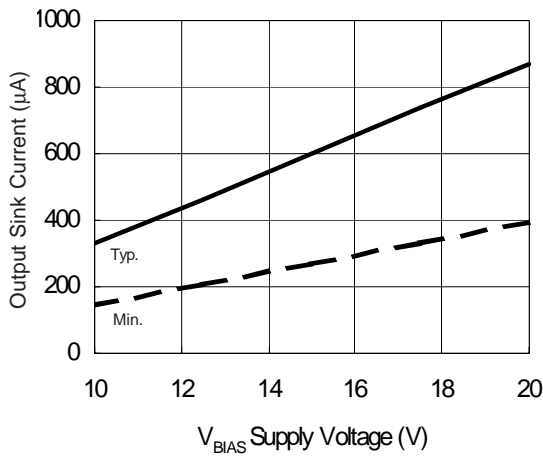


Figure 28B. Output Sink Current vs. Supply Voltage

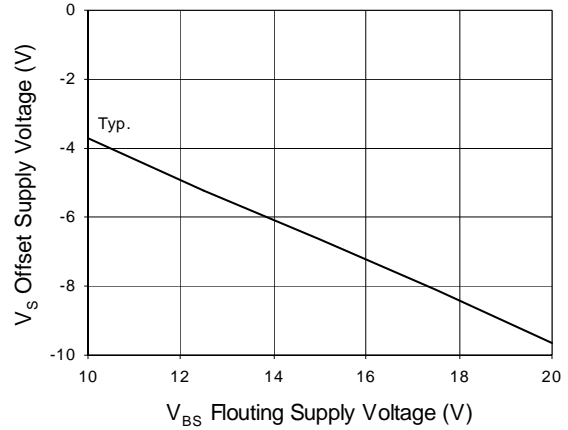


Figure 29. Maximum V_S Negative Offset vs. Supply Voltage

IRS2109/IRS21094(S)PbF

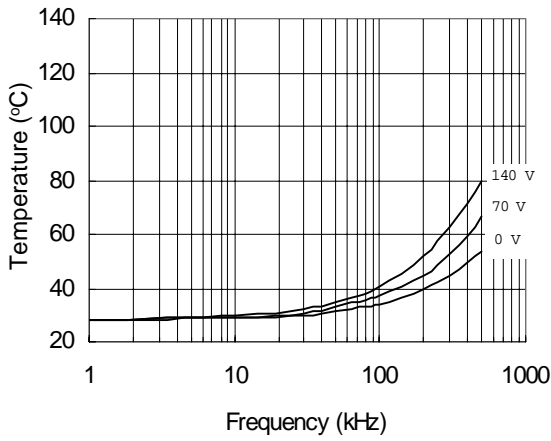


Figure 30. IRS2109 vs Frequency (IRFBC20)
 $R_{gate} = 33 \Omega$, $V_{CC} = 15 V$

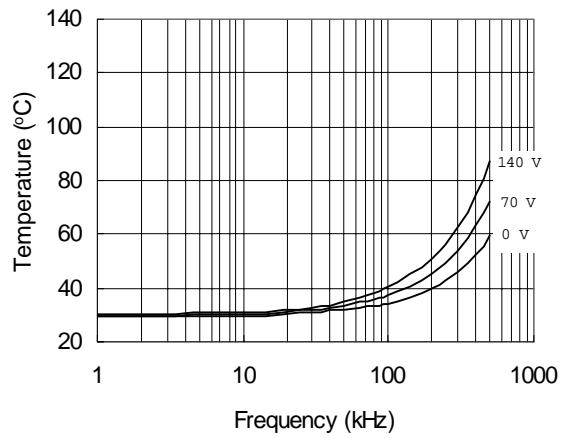


Figure 31. IRS2109 vs Frequency (IRFBC30)
 $R_{gate} = 22 \Omega$, $V_{CC} = 15 V$

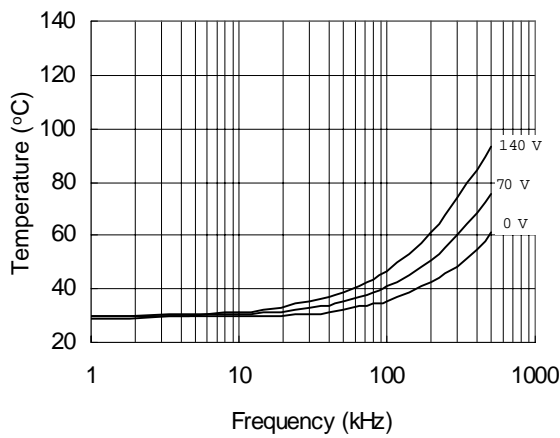


Figure 32. IRS2109 vs Frequency (IRFBC40)
 $R_{gate} = 15 \Omega$, $V_{CC} = 15 V$

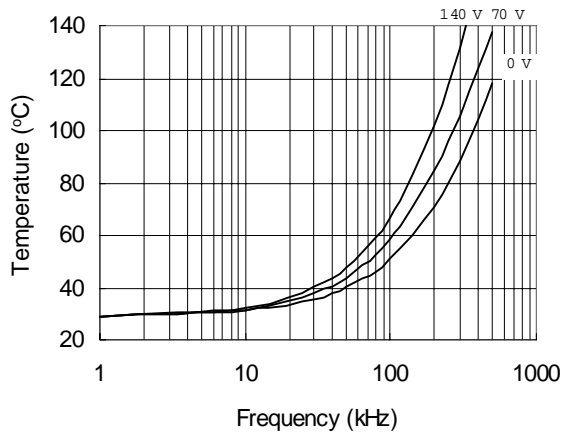
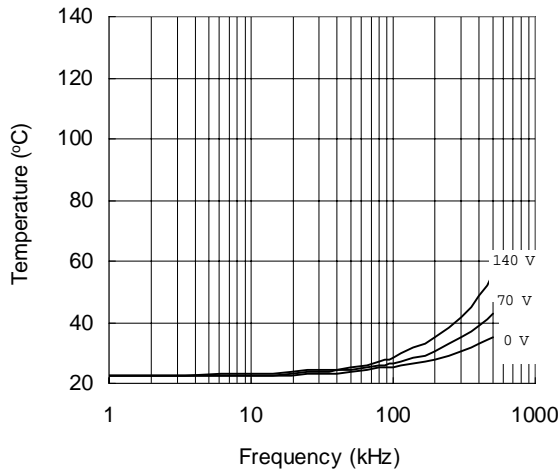
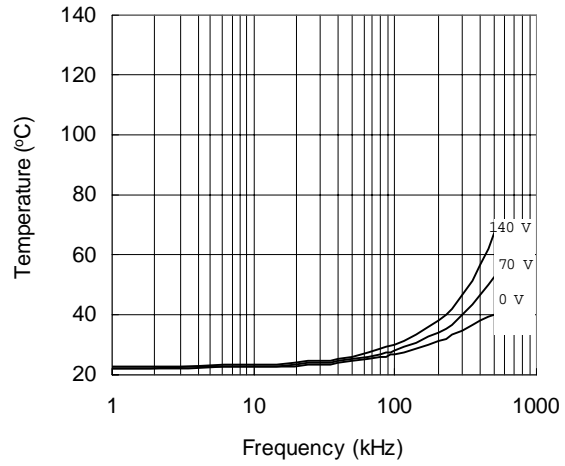


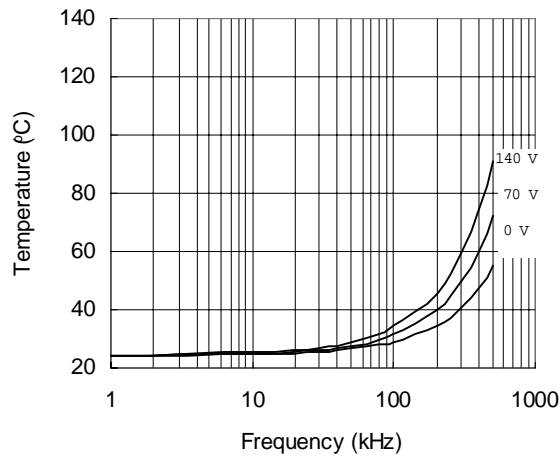
Figure 33. IRS2109 vs Frequency (IRFPE50)
 $R_{gate} = 10 \Omega$, $V_{CC} = 15 V$



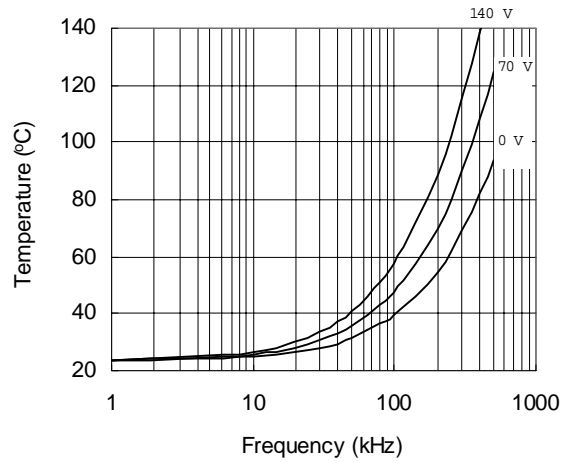
**Figure 34. IRS21094 vs. Frequency (IRFBC20),
 $R_{gate}=33 \Omega$, $V_{CC}=15 \text{ V}$**



**Figure 35. IRS21094 vs. Frequency (IRFBC30),
 $R_{gate}=22 \Omega$, $V_{CC}=15 \text{ V}$**

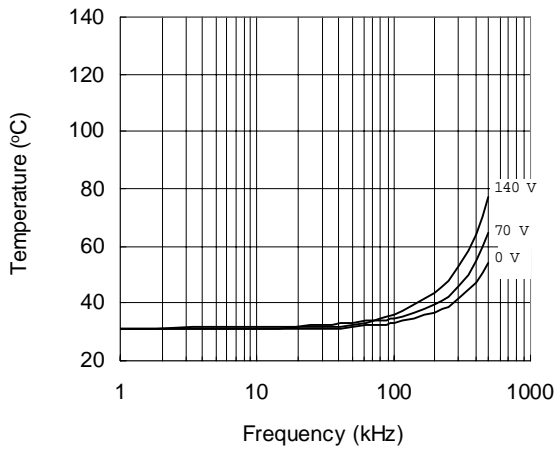


**Figure 36. IRS21094 vs. Frequency (IRFBC40),
 $R_{gate}=15 \Omega$, $V_{CC}=15 \text{ V}$**

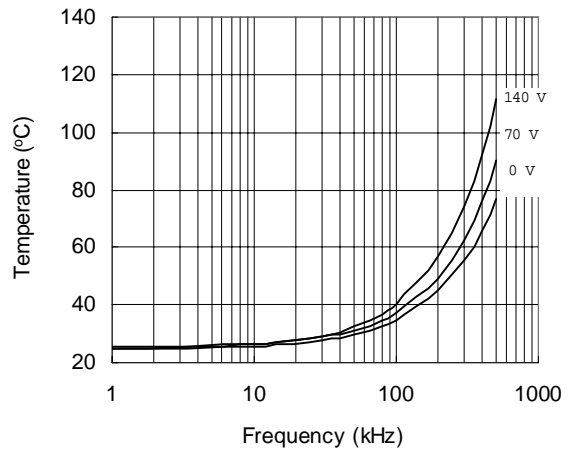


**Figure 37. IRS21094 vs. Frequency (IRFPE50),
 $R_{gate}=10 \Omega$, $V_{CC}=15 \text{ V}$**

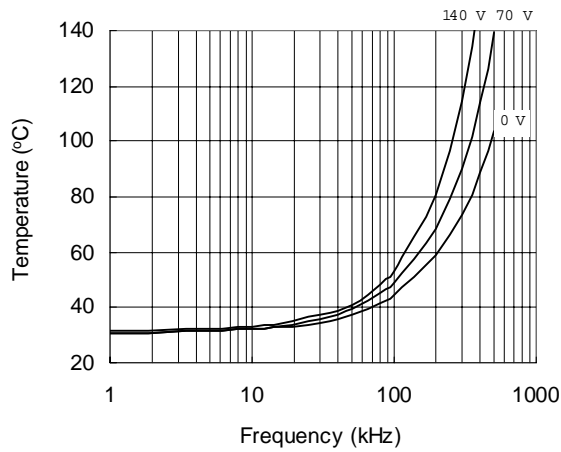
IRS2109/IRS21094(S)PbF



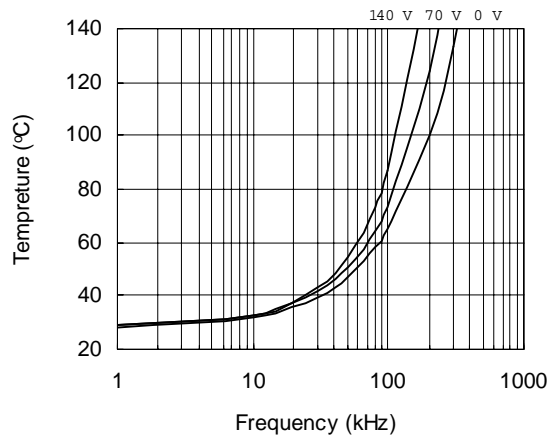
**Figure 38. IRS2109S vs. Frequency (IRFBC20),
 $R_{gate}=33 \Omega$, $V_{CC}=15 V$**



**Figure 39. IRS2109S vs. Frequency (IRFBC30),
 $R_{gate}=22 \Omega$, $V_{CC}=15 V$**



**Figure 40. IRS2109S vs. Frequency (IRFBC40),
 $R_{gate}=15 \Omega$, $V_{CC}=15 V$**



**Figure 41. IRS2109S vs. Frequency (IRFPE50),
 $R_{gate}=10 \Omega$, $V_{CC}=15 V$**

IRS2109/IRS21094(S)PbF

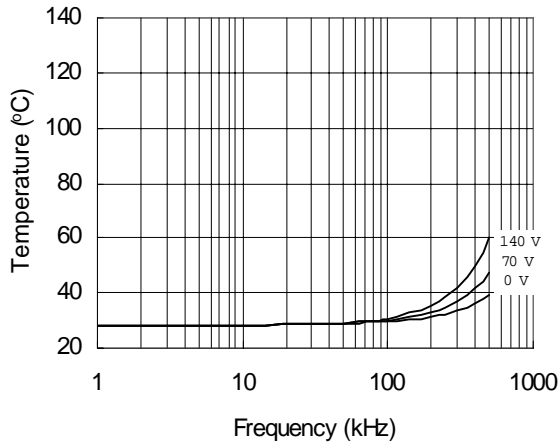


Figure 42. IRS21094S vs. Frequency (IRFBC20),
 $R_{gate}=33 \Omega$, $V_{cc}=15 V$

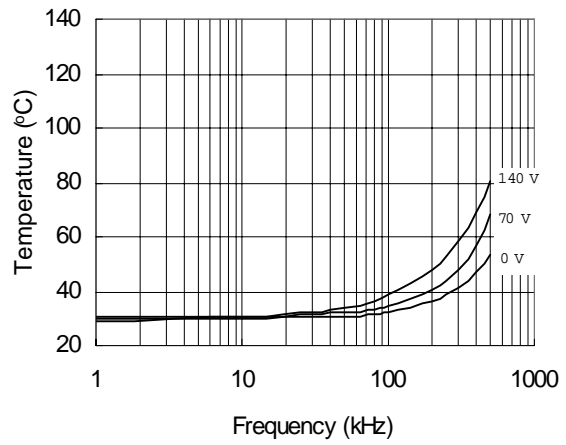


Figure 43. IRS21094S vs. Frequency (IRFBC30),
 $R_{gate}=22 \Omega$, $V_{cc}=15 V$

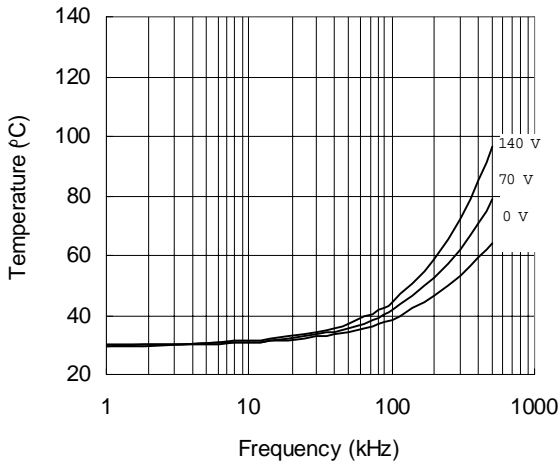


Figure 44. IRS21094S vs. Frequency (IRFBC40),
 $R_{gate}=15 \Omega$, $V_{cc}=15 V$

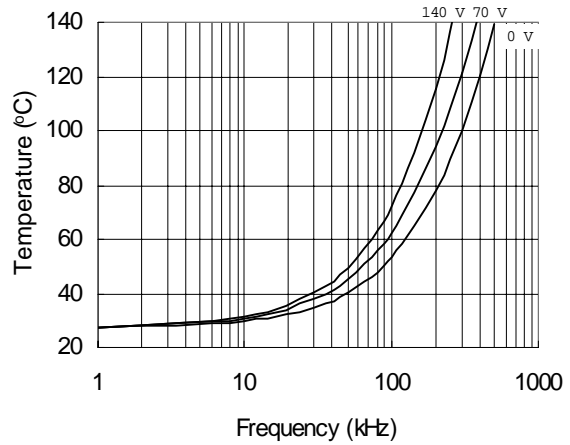
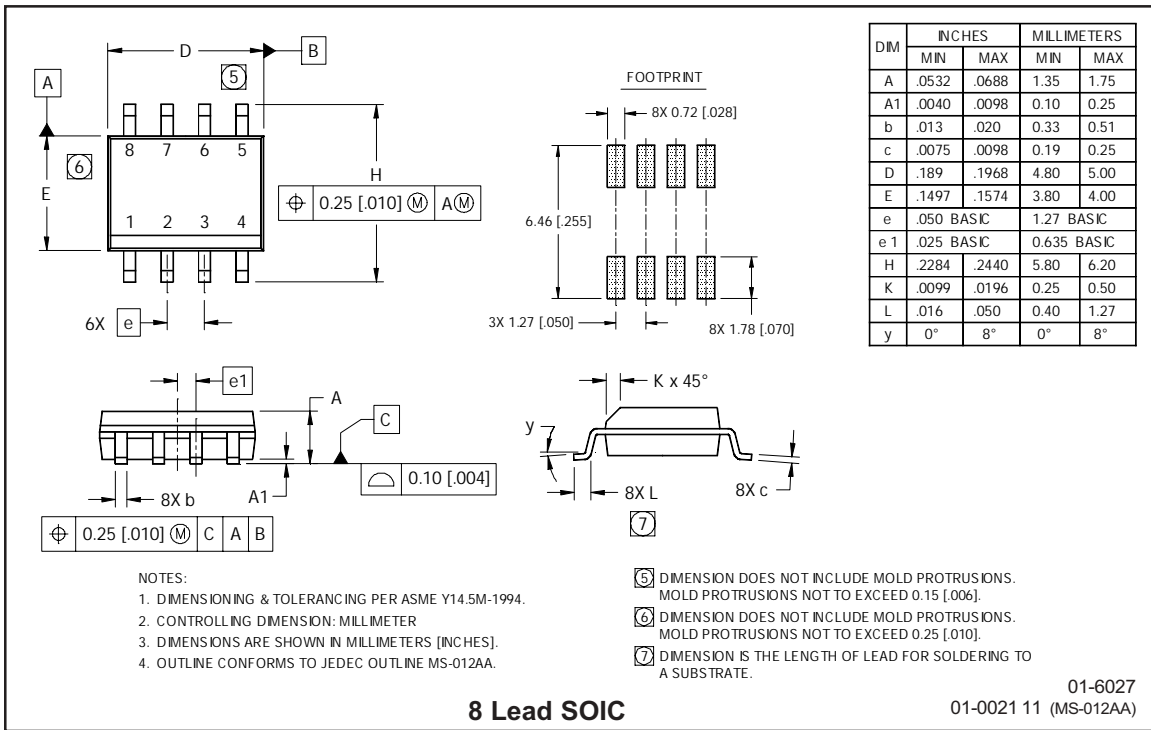
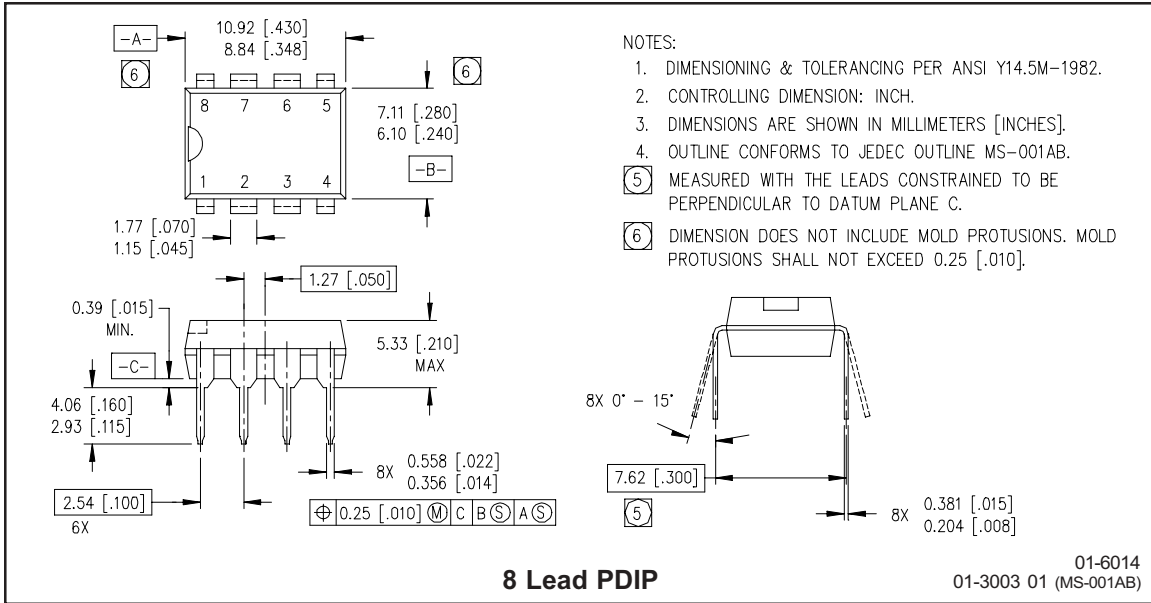


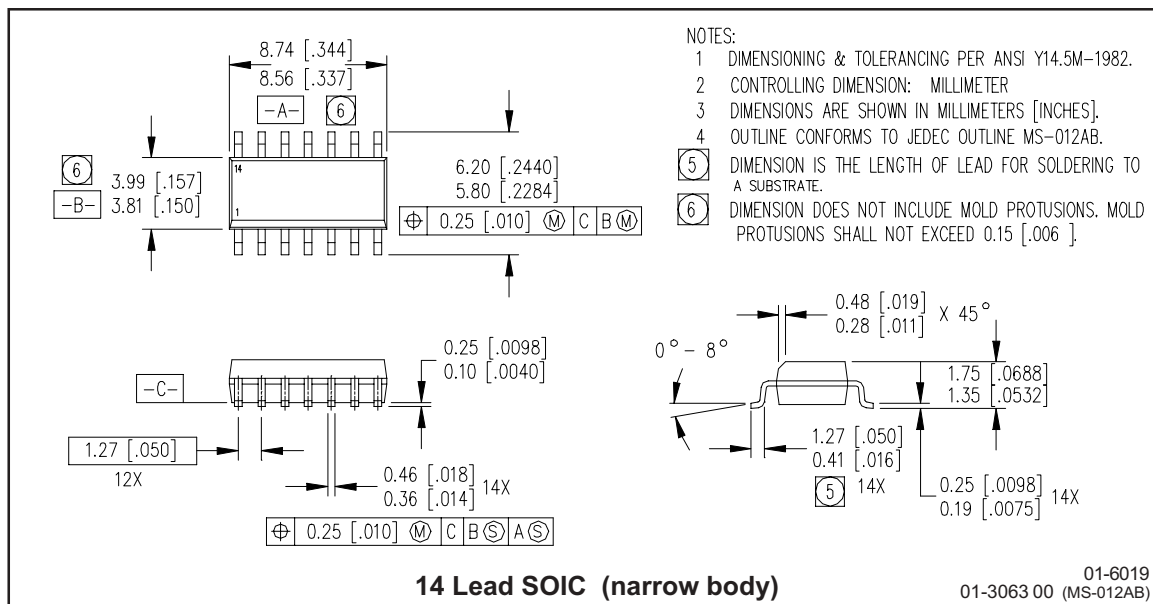
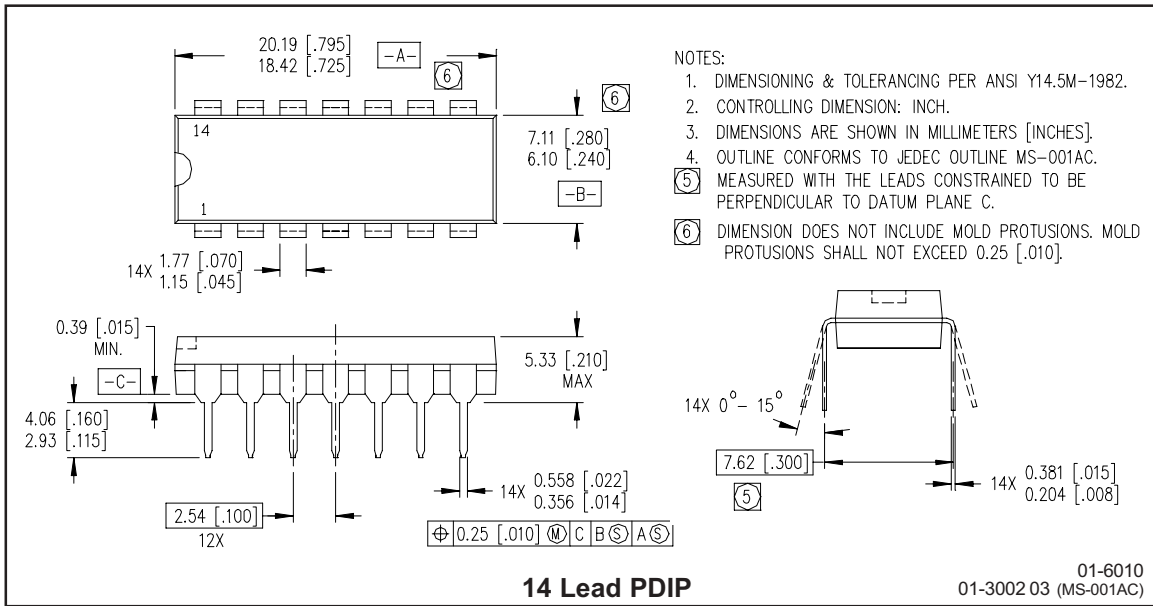
Figure 45. IRS21094S vs. Frequency (IRFPE50),
 $R_{gate}=10 \Omega$, $V_{cc}=15 V$

IRS2109/IRS21094(S)PbF

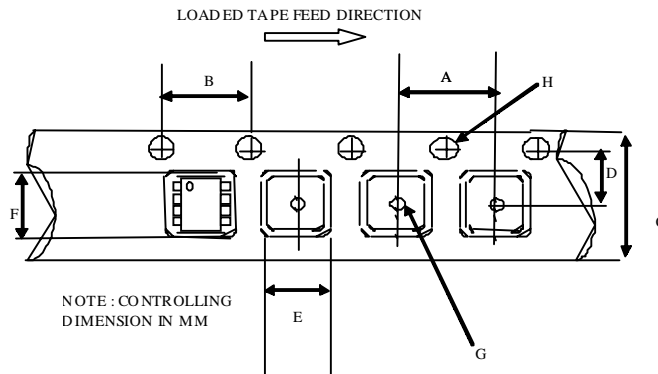
Case Outlines



IRS2109/IRS21094(S)PbF

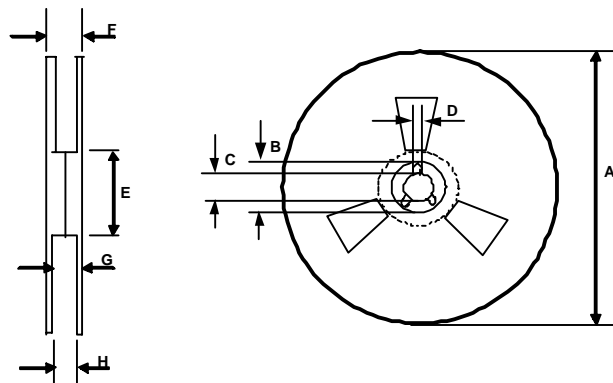


Tape & Reel 8-lead SOIC



CARRIER TAPE DIMENSION FOR 8SOICN

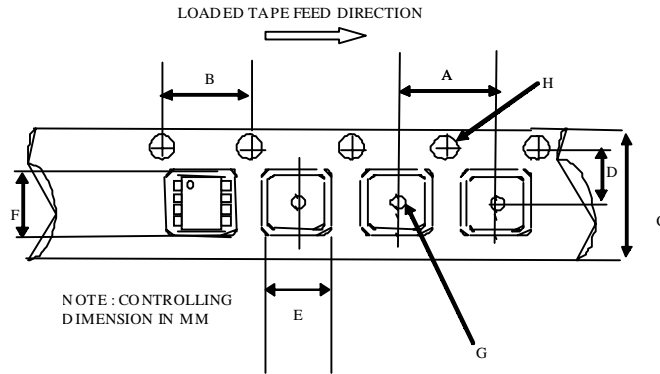
| Code | Metric | | Imperial | |
|------|--------|-------|----------|-------|
| | Min | Max | Min | Max |
| A | 7.90 | 8.10 | 0.311 | 0.318 |
| B | 3.90 | 4.10 | 0.153 | 0.161 |
| C | 11.70 | 12.30 | 0.46 | 0.484 |
| D | 5.45 | 5.55 | 0.214 | 0.218 |
| E | 6.30 | 6.50 | 0.248 | 0.255 |
| F | 5.10 | 5.30 | 0.200 | 0.208 |
| G | 1.50 | n/a | 0.059 | n/a |
| H | 1.50 | 1.60 | 0.059 | 0.062 |



REEL DIMENSIONS FOR 8SOICN

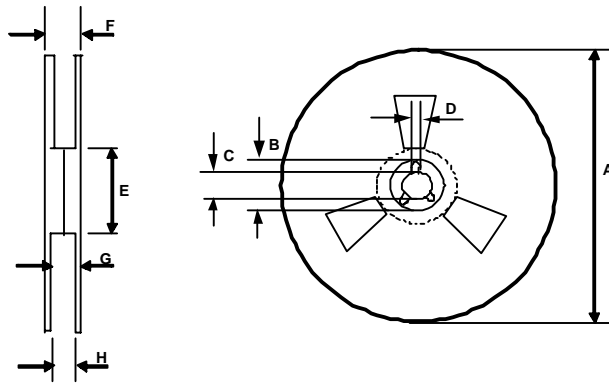
| Code | Metric | | Imperial | |
|------|--------|--------|----------|--------|
| | Min | Max | Min | Max |
| A | 329.60 | 330.25 | 12.976 | 13.001 |
| B | 20.95 | 21.45 | 0.824 | 0.844 |
| C | 12.80 | 13.20 | 0.503 | 0.519 |
| D | 1.95 | 2.45 | 0.767 | 0.096 |
| E | 98.00 | 102.00 | 3.858 | 4.015 |
| F | n/a | 18.40 | n/a | 0.724 |
| G | 14.50 | 17.10 | 0.570 | 0.673 |
| H | 12.40 | 14.40 | 0.488 | 0.566 |

Tape & Reel 14-lead SOIC



CARRIER TAPE DIMENSION FOR 14SOICN

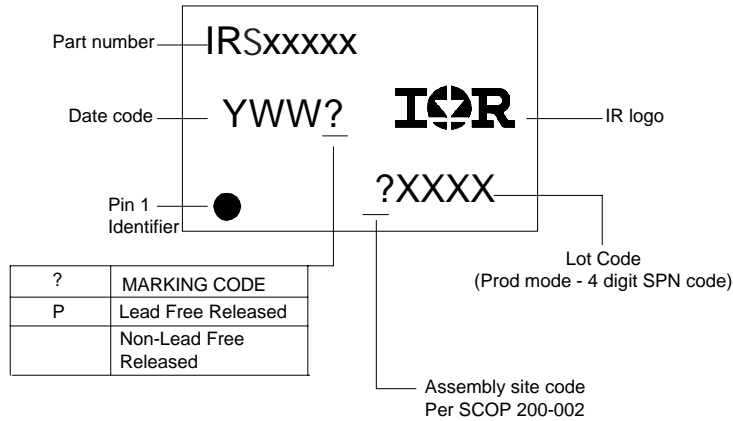
| Code | Metric | | Imperial | |
|------|--------|-------|----------|-------|
| | Min | Max | Min | Max |
| A | 7.90 | 8.10 | 0.311 | 0.318 |
| B | 3.90 | 4.10 | 0.153 | 0.161 |
| C | 15.70 | 16.30 | 0.618 | 0.641 |
| D | 7.40 | 7.60 | 0.291 | 0.299 |
| E | 6.40 | 6.60 | 0.252 | 0.260 |
| F | 9.40 | 9.60 | 0.370 | 0.378 |
| G | 1.50 | n/a | 0.059 | n/a |
| H | 1.50 | 1.60 | 0.059 | 0.062 |



REEL DIMENSIONS FOR 14SOICN

| Code | Metric | | Imperial | |
|------|--------|--------|----------|--------|
| | Min | Max | Min | Max |
| A | 329.60 | 330.25 | 12.976 | 13.001 |
| B | 20.95 | 21.45 | 0.824 | 0.844 |
| C | 12.80 | 13.20 | 0.503 | 0.519 |
| D | 1.95 | 2.45 | 0.767 | 0.096 |
| E | 98.00 | 102.00 | 3.858 | 4.015 |
| F | n/a | 22.40 | n/a | 0.881 |
| G | 18.50 | 21.10 | 0.728 | 0.830 |
| H | 16.40 | 18.40 | 0.645 | 0.724 |

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

- 8-Lead PDIP IRS2109PbF
- 8-Lead SOIC IRS2109SPbF
- 8-Lead SOIC Tape & Reel IRS2109STRPbF

- 14-Lead PDIP IRS21094PbF
- 14-Lead SOIC IRS21094SPbF
- 14-Lead SOIC Tape & Reel IRS21094STRPbF

SOIC8 &14 are MSL2 qualified.
 This product has been designed and qualified for the industrial level.
 Qualification standards can be found at www.irf.com

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
 Data and specifications subject to change without notice. 12/4/2006

单击下面可查看定价，库存，交付和生命周期等信息

[>>Infineon Technologies\(英飞凌\)](#)