

**Radiation Hardended,
 Solid-State Relay
 with Buffered Inputs**

**RDHA710SE10A2FK
 Dual, 100V, 10A**

Product Summary ⑤

Part Number	Breakdown Voltage	Current	tr / tf	Logic Drive Voltage
RDHA710SE10A2FK	100V	10A	Fast	3.3V



Description

The RDHA710SE10A2FK is a radiation hardened dual solid-state relay in a hermetic package. It is configured as a dual, single-pole-single-throw (SPST) normally open relay with common input supply. This device is characterized for 100 krad(Si) total ionizing dose and neutron fluence level of $1.8E^{12}$ n/cm². The input and output MOSFETs utilize International Rectifier's R5 technology. The RDHA710SE10A2FK is optically coupled and actuated by standard logic inputs.

Features:

- Total Dose Capability to 100 krad(Si)
- Neutron Fluence Level of $1.8E^{12}$ n/cm²
- Optically Coupled
- 1000V_{DC} Input to Output Isolation
- Buffered Input Stage
- 3.3V Compatible Logic Level Input
- Controlled Switching Times
- Hermetically Sealed Package

Absolute Maximum Ratings per Channel @ T_j=25°C (unless otherwise specified)

Parameter	Symbol	Value	Units
Output Maximum Voltage ⑥	V _S	100	V
Output Current ④ ⑤	I _O	12	A
Input Buffer Voltage - (pins 4 & 6) ③	V _{IN}	±7.5	V
Input Buffer Current	I _{IN}	±10	mA
Input Supply Voltage (pin 5) ⑦	V _{DD}	5.25	V
Input Supply Current ⑦	I _{DD}	25	mA
Power Dissipation ④⑤	P _{DISS}	60	W
Operating Temperature Range	T _J	-55 to +125	°C
Storage Temperature Range	T _S	-65 to +150	
Lead Temperature	T _L	300	

For notes, please refer to page 3

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General Characteristics per Channel @ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ (Unless Otherwise Specified)

Parameter	Group A Subgroups	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Input Buffer Threshold Voltage ^{①②}		$V_{DD} = 5.0\text{V}$, $I_O = 10\text{A}$	$V_{IN(TH)}$	3.0	--	--	V
Input-to-Output Leakage Current	1	$V_{I-O} = 1.0\text{KVdc}$, dwell = 5.0s	I_{I-O}	--	--	1.0	μA
Output Capacitance ^①		$V_{IN} = 0.1\text{V}$, $f = 1.0\text{MHz}$, $V_S = 25\text{V}$ $T_C = 25^{\circ}\text{C}$	C_{OSS}	--	365	--	pF
Thermal Resistance ^①		$V_{IN} = 3.3\text{V}$, $V_{DD} = 5.0\text{V}$ ①,②	R_{THJC}	--	--	1.7	$^{\circ}\text{C/W}$
MTBF (Per Channel)		MIL-HDBK-217F, SF@ $T_C = 25^{\circ}\text{C}$		6.0	--	--	MHrs

Pre-Irradiation**Electrical Characteristics per Channel @ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ (Unless Otherwise Specified)**

Parameter	Group A Subgroups	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Output On-Resistance	1	$V_{IN} = 3.3\text{V}$	$R_{DS(ON)}$	--	0.070	0.100	Ω
	2	$V_{DD} = 5.0\text{V}$, $I_O = 10\text{A}$		--	0.125	0.165	
Output Leakage Current	1	$V_{IN} = 0.1\text{V}$, $V_S = 100\text{V}$	I_O	--	--	25	μA
	2	$V_{IN} = 0.1\text{V}$, $V_S = 80\text{V}$		--	--	250	
Input Supply Current	1,2,3	$V_{DD} = 5.0\text{V}$, $I_O = 10\text{A}$	I_{DD}	--	18	25	mA
Input Buffer Current	1	$V_{IN} = 3.3\text{V}$	I_{IN}	--	--	1.0	μA
	2,3			--	--	3.0	
Turn-On Delay ^⑥	1,2,3	$V_{IN} = 3.3\text{V}$, $V_{DD} = 5.0\text{V}$, $V_S = 30\text{V}$ $RC = 7.0\Omega/100\mu\text{F}$, $PW = 50\text{ms}$	t_{on}	--	0.18	0.45	ms
Turn-Off Delay ^⑥	1,2,3	$V_{IN} = 0.1\text{V}$, $V_{DD} = 5.0\text{V}$, $V_S = 30\text{V}$ $RC = 7.0\Omega/100\mu\text{F}$, $PW = 50\text{ms}$	t_{off}	--	0.50	0.75	
Rise Time ^{②,⑥}	1,2,3	$V_{IN} = 3.3\text{V}$, $V_{DD} = 5.0\text{V}$, $V_S = 30\text{V}$ $RC = 7.0\Omega/100\mu\text{F}$, $PW = 50\text{ms}$	t_r	--	0.25	0.40	
Fall Time ^{②,⑥}	1,2,3	$V_{IN} = 0.1\text{V}$, $V_{DD} = 5.0\text{V}$, $V_S = 30\text{V}$ $RC = 7.0\Omega/100\mu\text{F}$, $PW = 50\text{ms}$	t_f	--	1.50	1.80	

For notes, please refer to page 3

Post Total Dose Irradiation ⑦,⑧,⑨

Electrical Characteristics per Channel @ 25°C (Unless Otherwise Specified)

Parameter	Group A Subgroups	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Output On-Resistance	1	$V_{IN} = 3.3V, V_{DD} = 5.0V, I_O = 10A$	$R_{DS(ON)}$	--	0.070	0.100	Ω
Input Supply Current	1	$V_{DD} = 5.0V, I_O = 10A$	I_{DD}	--	18	25	mA
Output Leakage Current	1	$V_{IN} = 0.1V, V_S = 100V$	I_O	--	--	25	μA
Input Buffer Current	1	$V_{IN} = 3.3V$	I_{IN}	--	--	1.0	
Turn-On Delay④	1	$V_{IN} = 3.3V, V_{DD} = 5.0V, V_S = 30V$ $RC = 7.0\Omega/100\mu F, PW = 50ms$	t_{on}	--	0.18	0.45	ms
Turn-Off Delay④	1	$V_{IN} = 0.1V, V_{DD} = 5.0V, V_S = 30V$ $RC = 7.0\Omega/100\mu F, PW = 50ms$	t_{off}	--	0.50	0.75	
Rise Time②⑥	1	$V_{IN} = 3.3V, V_{DD} = 5.0V, V_S = 30V$ $RC = 7.0\Omega/100\mu F, PW = 50ms$	t_r	--	0.25	0.40	
Fall Time②⑥	1	$V_{IN} = 0.1V, V_{DD} = 5.0V, V_S = 30V$ $RC = 7.0\Omega/100\mu F, PW = 50ms$	t_f	--	1.50	1.80	

Notes for Maximum Ratings and Electrical Characteristic Tables

- ① Specification is guaranteed by design
- ② Rise and fall times are controlled internally
- ③ Inputs protected for $V_{IN} < 1.0V$ and $V_{IN} > 7.5V$
- ④ Optically coupled Solid State Relays (SSRs) have relatively slow turn on and turn off times. Care must be taken to insure that transient currents do not cause violation of SOA. If transient conditions are present, IR recommends a complete simulation to be performed by the end user to insure compliance with SOA requirements as specified in the IRHNJ57130 data sheet
- ⑤ While the SSR design meets the design requirements specified in MIL-PRF-38534, the end user is responsible for product derating, as required for the application
- ⑥ Reference Figures 3 & 4 for Switching Test Circuits and Wave Form
- ⑦ Total Dose Irradiation with Input Bias. 10mA I_{DD} applied and $V_{DS} = 0$ during Irradiation
- ⑧ Total Dose Irradiation with Output Bias. 80 Volts V_{DS} applied and $I_{DD} = 0$ during Irradiation
- ⑨ International Rectifier does not currently have a DSCC certified Radiation Hardness Assurance Program

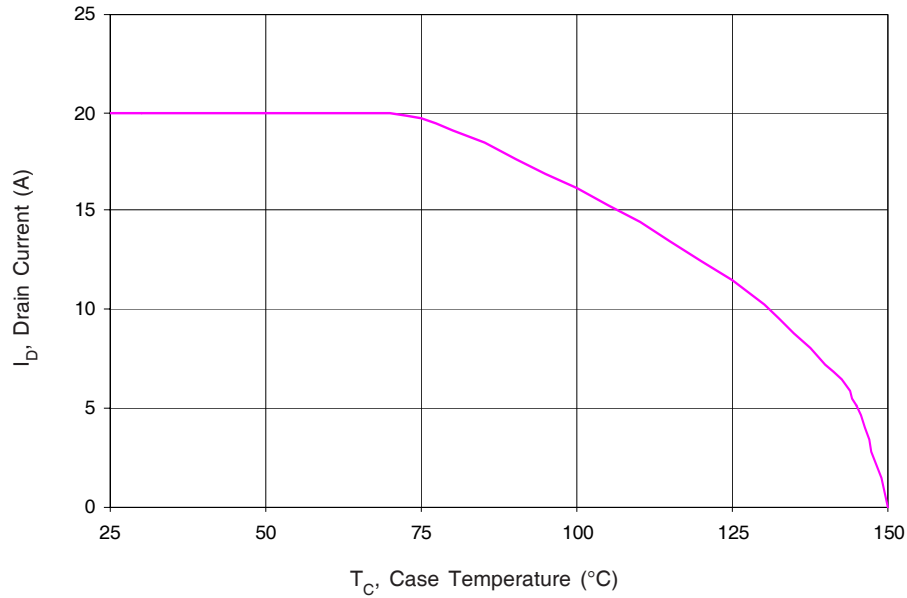


Fig 1: Maximum Drain Current Vs Case Temperature per Channel

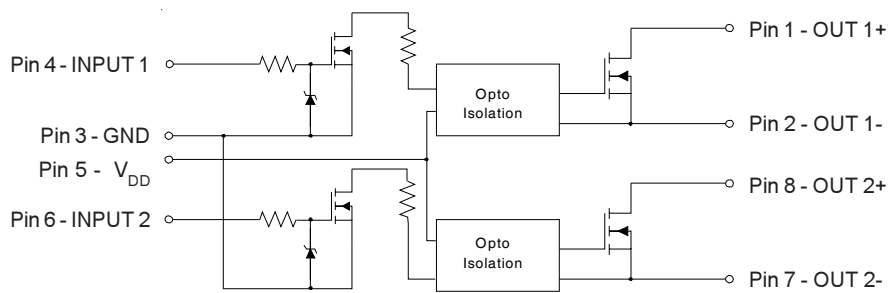


Fig 2: Typical Application

Radiation Performance

International Rectifier Radiation Hardened Solid State Relays are tested to verify their hardness capability. The hardness assurance program at IR uses a Cobalt-60 (⁶⁰Co) Source and heavy ion irradiation. Both pre- and post- irradiation performance are tested and specified using the same drive circuitry and test conditions to provide a direct comparison.

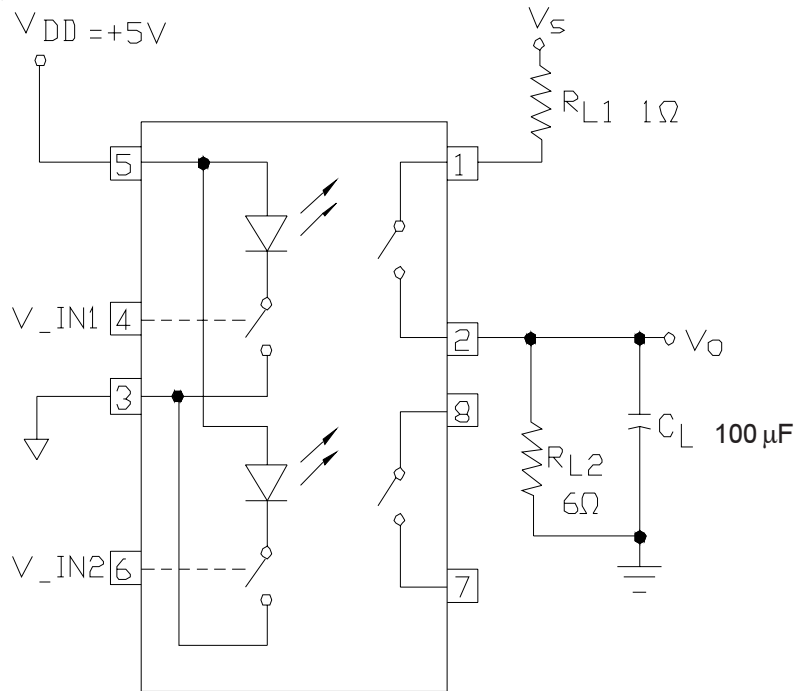


Fig 3: Switching Test Circuit (Only one channel shown)

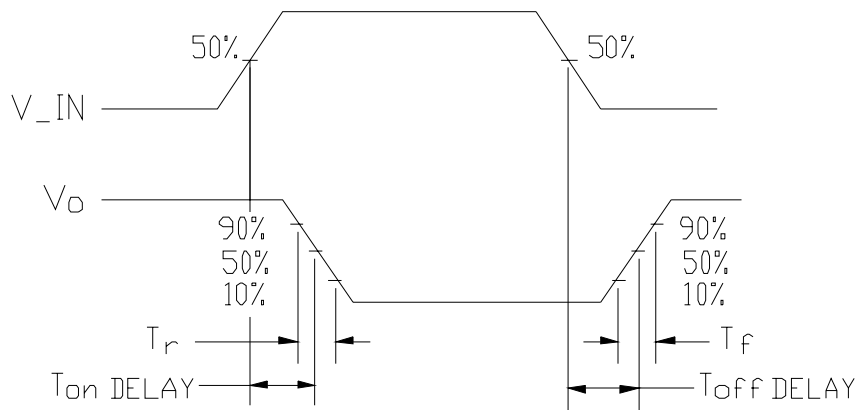
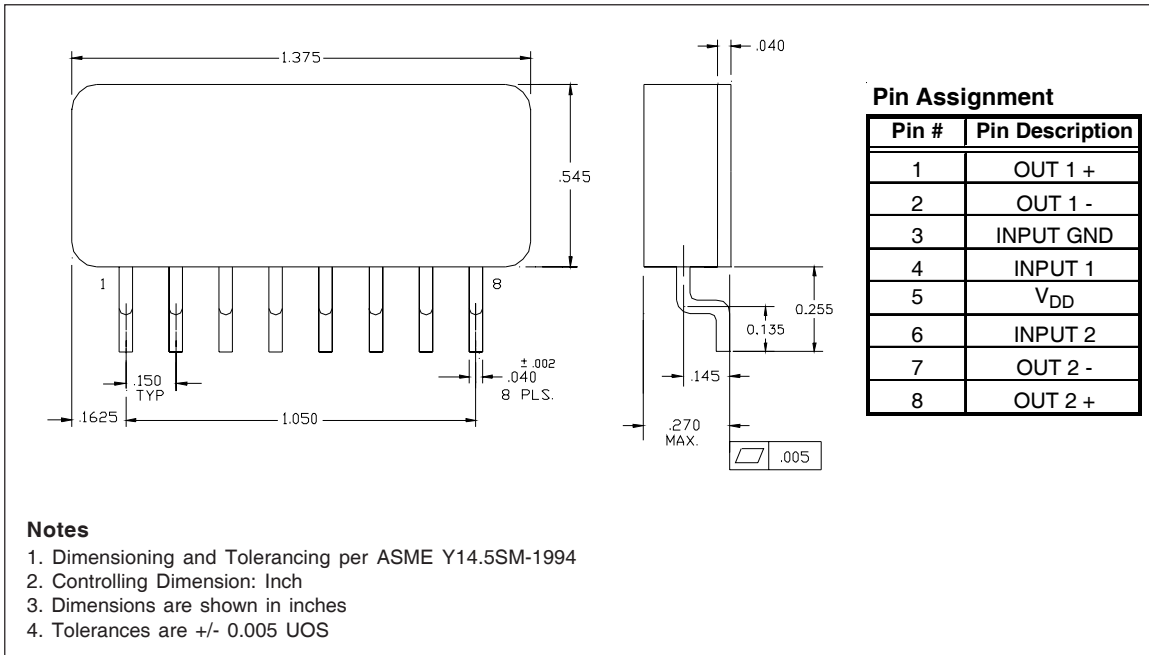
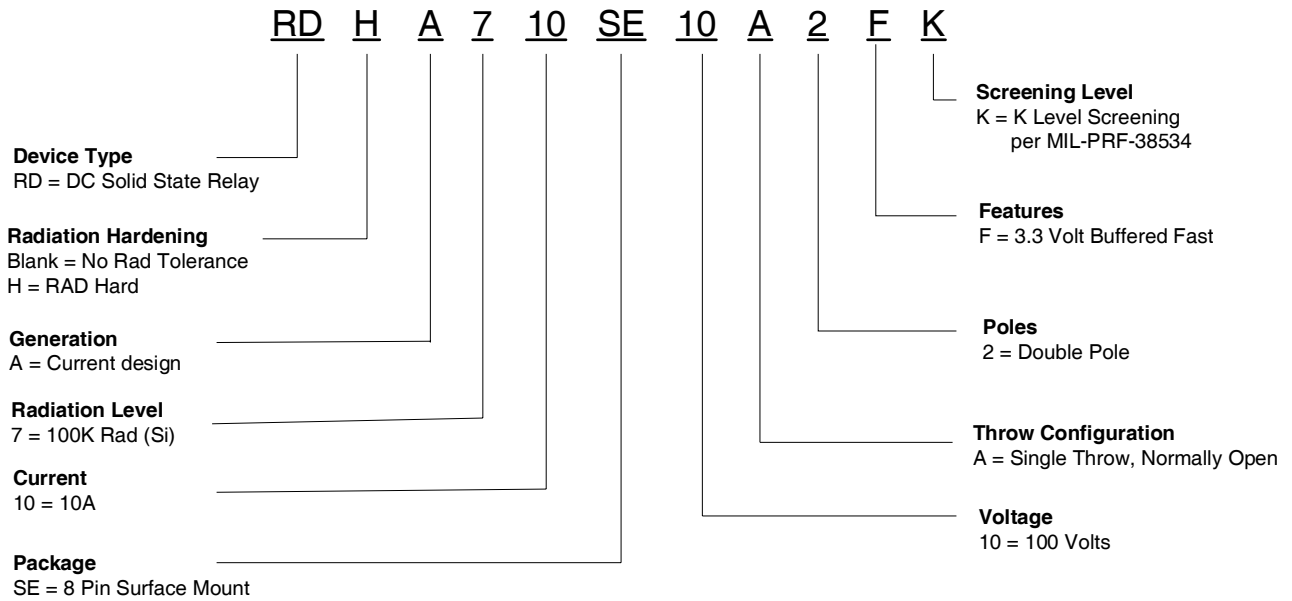


Fig 4: Switching Test Waveform

Case Outline and Dimensions — 8 Pin Surface Mount Package



Part Numbering Nomenclature



单击下面可查看定价，库存，交付和生命周期等信息

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