IR HiRel
An Infineon Technologies Company

IRHQ57110

RADIATION HARDENED POWER MOSFET SURFACE MOUNT (LCC-28)

100V, Quad N-CHANNEL
R5 TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	I_D
IRHQ57110	100 kRads(Si)	0.27Ω	4.6A
IRHQ53110	300 kRads(Si)	0.27Ω	4.6A
IRHQ55110	500 kRads(Si)	0.29Ω	4.6A
IRHQ58110	1000 kRads(Si)	0.29Ω	4.6A

LCC-28

Description

IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm2)). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Features

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Ceramic Package
- Light Weight
- ESD Rating: Class 1A per MIL-STD-750, Method 1020

Absolute Maximum Ratings (Per Die) — Pre-Irradiation

Symbol	Parameter	Value	Units
I_{D1} @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	4.6	
I_{D2} @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	2.9	A
I_{DM} @T_C = 25°C	Pulsed Drain Current ①	18.4	
P_D @T_C = 25°C	Maximum Power Dissipation	12	W
	Linear Derating Factor	0.1	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	47	mJ
I_{AR}	Avalanche Current ①	4.6	A
E_{AR}	Repetitive Avalanche Energy ①	1.2	mJ
dv/dt	Peak Diode Recovery dv/dt ③	6.1	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Package. Mounting Surface Temperature.	300 (for 5s)	
	Weight	0.89 (Typical)	g

For Footnotes, refer to the page 2.

Electrical Characteristics For Each N-Channel Device @ Tj = 25°C(Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.13	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.31	Ω	V_{GS} = 12V, I_{D2} = 4.6A ④
		—	—	0.27		V_{GS} = 12V, I_{D2} = 2.9A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
Gfs	Forward Transconductance	3.3	—	—	S	V_{DS} = 15V, I_{D2} = 2.9A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	10	µA	V_{DS} = 80V, V_{GS} = 0V
		—	—	25		V_{DS} = 80V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_G	Total Gate Charge	—	—	13	nC	I_{D1} = 4.6A
Q_{GS}	Gate-to-Source Charge	—	—	4.0		V_{DS} = 50V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	3.9		V_{GS} = 12V
$t_{d(on)}$	Turn-On Delay Time	—	—	20	ns	V_{DD} = 50V
tr	Rise Time	—	—	24		I_{D1} = 4.6A
$t_{d(off)}$	Turn-Off Delay Time	—	—	32		R_G = 7.5Ω
t_f	Fall Time	—	—	90		V_{GS} = 12V
$L_S + L_D$	Total Inductance	—	6.1	—	nH	Measured from the center of drain pad to center of source pad
C_{iss}	Input Capacitance	—	371	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	108	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	3.0	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics (Per Die)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	4.6	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	18.4		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J = 25°C, I_S = 4.6A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	173	ns	T_J = 25°C, I_F = 4.6A, V_{DD} ≤ 25V
Q_{rr}	Reverse Recovery Charge	—	—	863	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Thermal Resistance (Per Die)

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	11.8	°C/W
$R_{\theta JA}$	Junction-to-Ambient (Typical socket mount)	—	—	60	

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 25V, starting T_J = 25°C, L = 4.4mH, Peak I_L = 4.6A, V_{GS} = 12V

③ $I_{SD} \leq$ 4.6A, di/dt ≤ 300A/µs, $V_{DD} \leq$ 100V, $T_J \leq$ 150°C

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

⑤ Total Dose Irradiation with V_{GS} Bias. 10 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

⑥ Total Dose Irradiation with V_{DS} Bias. 80 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Symbol	Parameter	Up to 500 kRads (Si)[1]		1000 kRads (Si)[2]		Units	Test Conditions
		Min.	Max.	Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	——	100	——	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	1.5	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	——	100	——	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	——	-100	——	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	——	10	——	10	µA	V_{DS} = 80V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	——	0.27	——	0.29	Ω	V_{GS} = 12V, I_{D2} = 2.9A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-254AA)	——	0.27	——	0.29	Ω	V_{GS} = 12V, I_{D2} = 2.9A
V_{SD}	Diode Forward Voltage	——	1.2	——	1.2	V	V_{GS} = 0V, I_S = 4.6A

1. Part number IRHQ57110, IRHQ53110, IRHQ55110
2. Part numbers IRHQ58110

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm²))	Energy (MeV)	Range (µm)	VDS (V)				
			@ VGS = 0V	@ VGS = -5V	@ VGS = -10V	@ VGS = -15V	@ VGS = -20V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	100	100	100	100	100
61 ± 5%	330 ± 7.5%	31 ± 7.5%	100	100	100	35	25
84 ± 5%	350 ± 10%	28 ± 7.5%	100	100	80	25	——

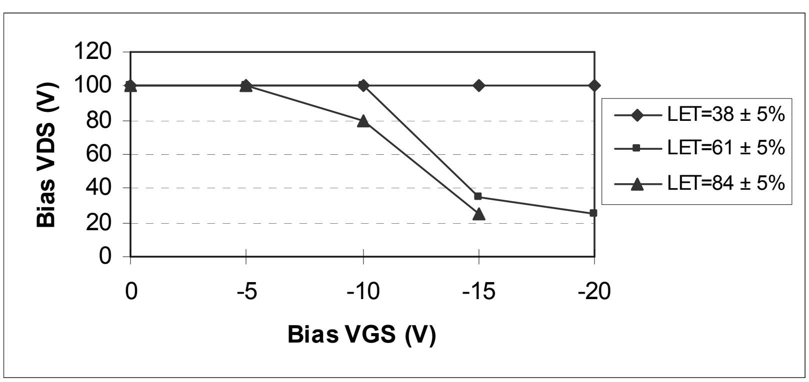


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

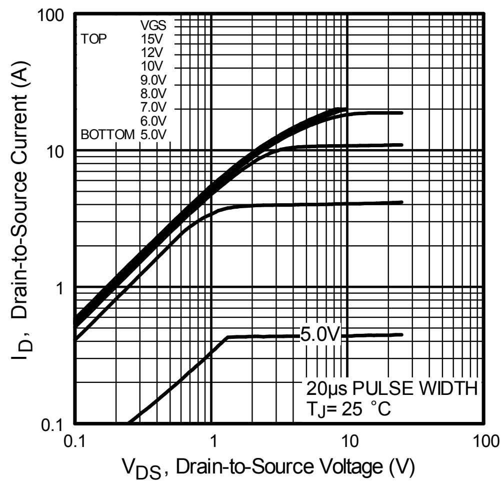


Fig 1. Typical Output Characteristics

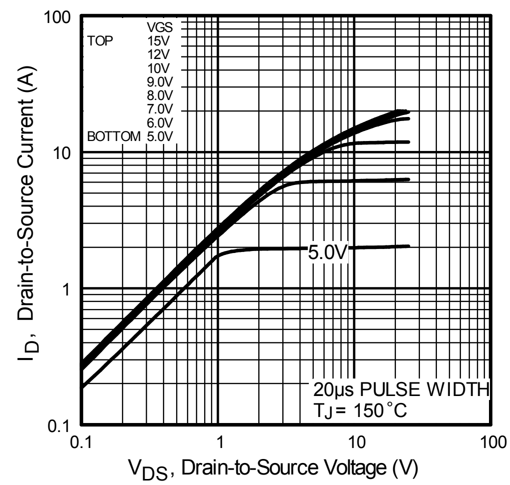


Fig 2. Typical Output Characteristics

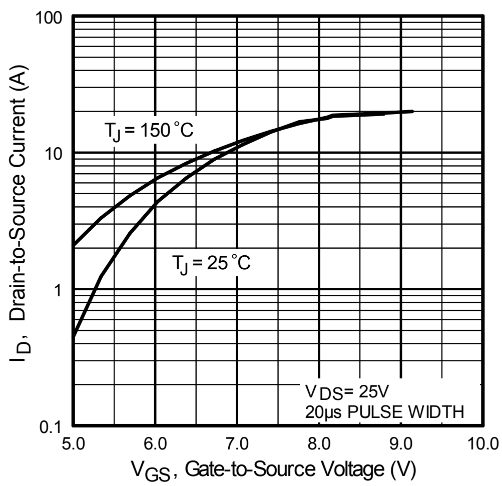


Fig 3. Typical Transfer Characteristics

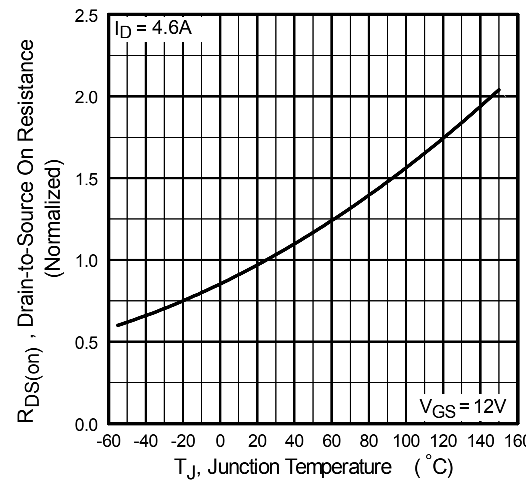


Fig 4. Normalized On-Resistance Vs. Temperature

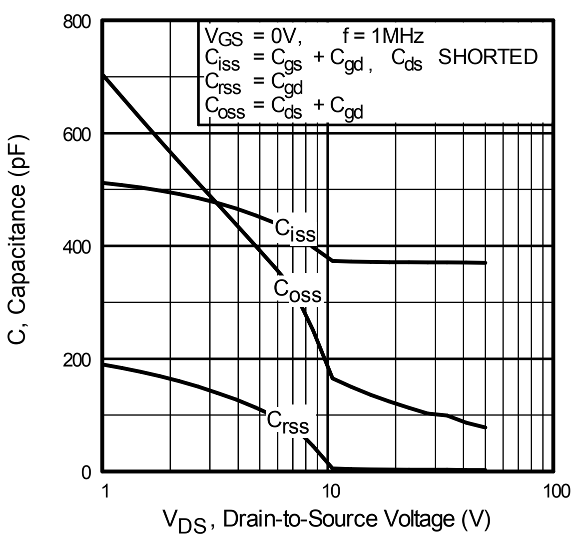


Fig 5. Typical Capacitance Vs. Drain-to-Source

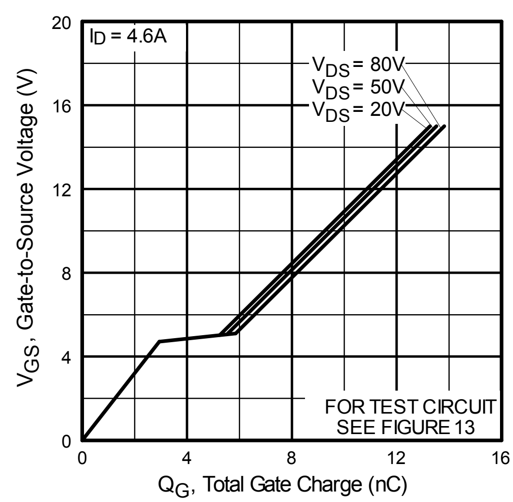


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

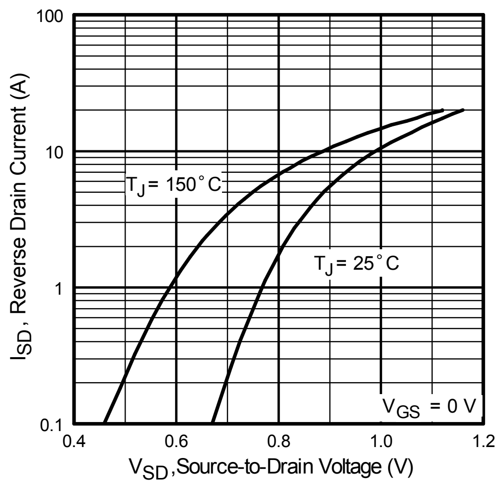


Fig 7. Typical Source-Drain Diode Forward Voltage

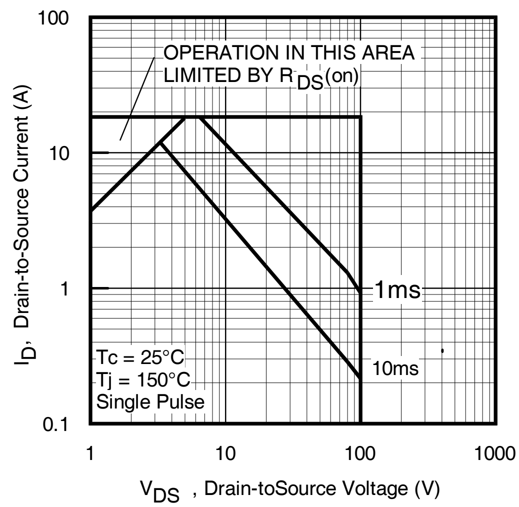


Fig 8. Maximum Safe Operating Area

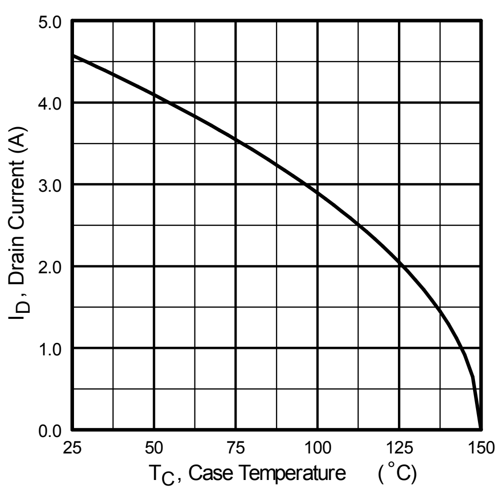


Fig 9. Maximum Drain Current Vs. Case Temperature

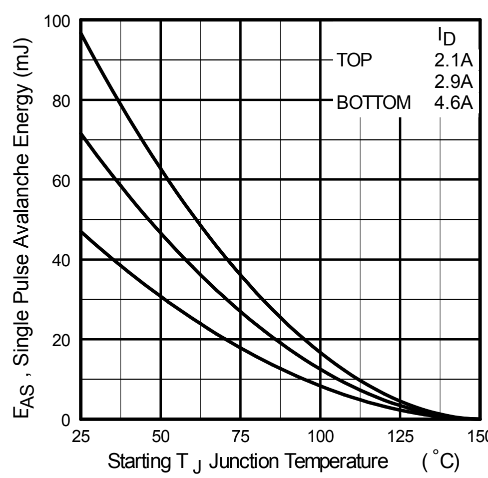


Fig 10. Maximum Avalanche Energy Vs. Drain Current

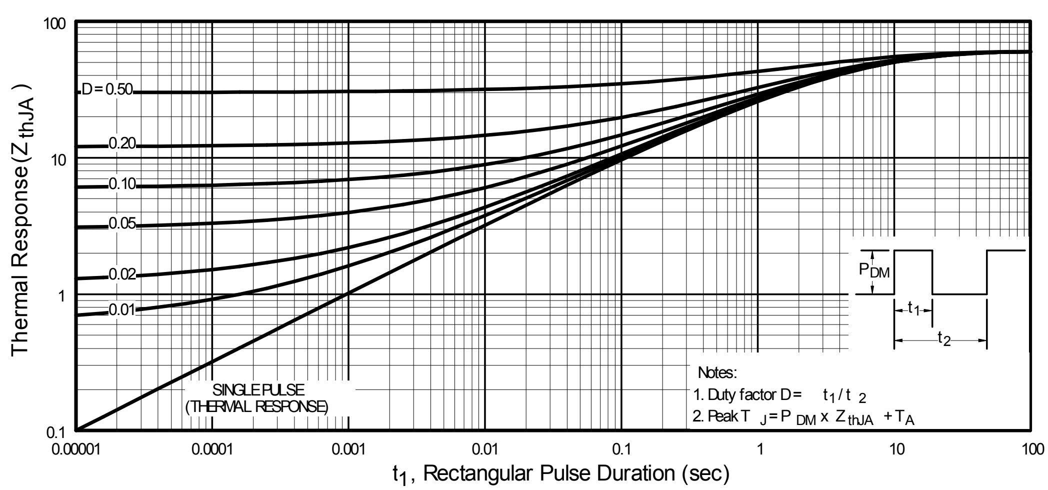


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

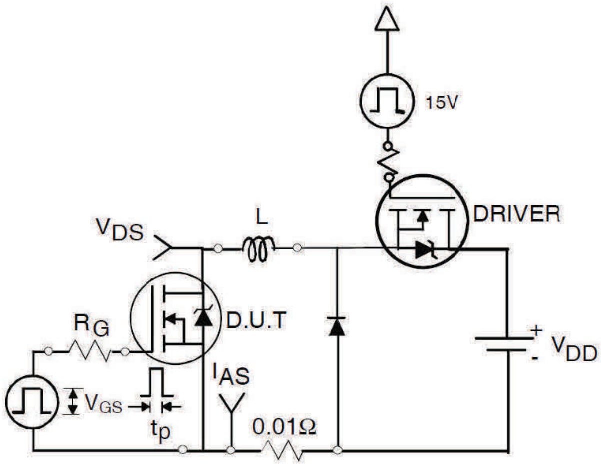


Fig 12a. Unclamped Inductive Test Circuit

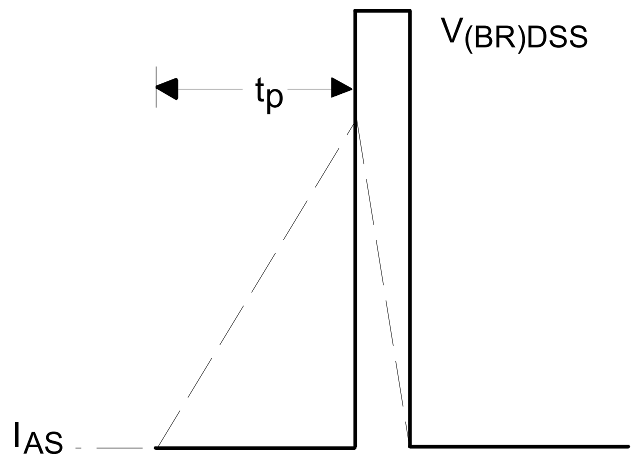


Fig 12b. Unclamped Inductive Waveforms

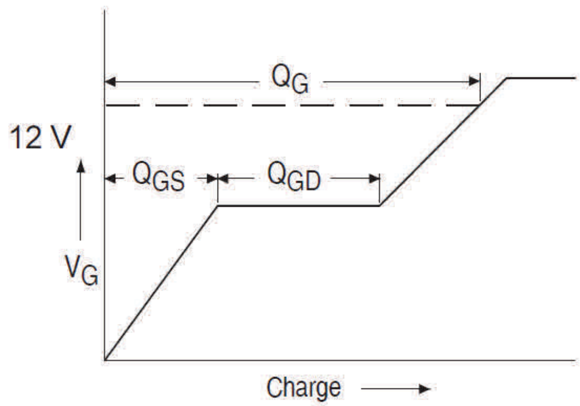


Fig 13a. Gate Charge Waveform

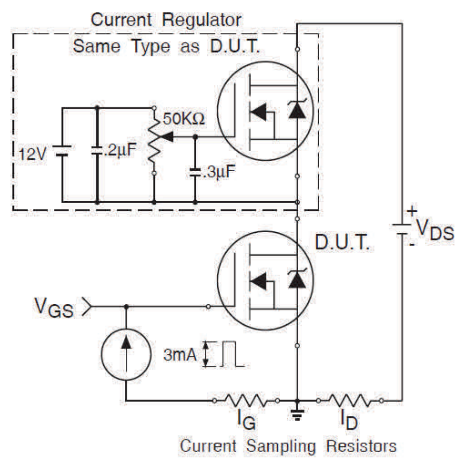


Fig 13b. Gate Charge Test Circuit

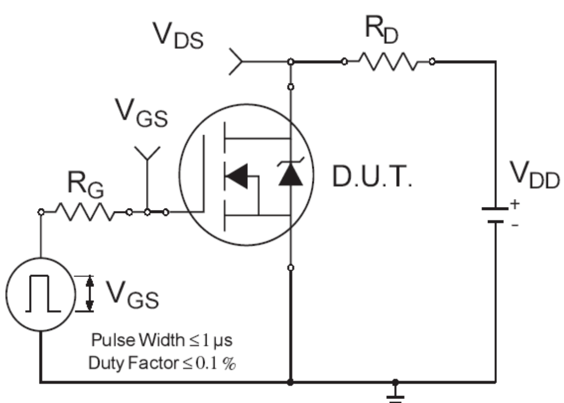


Fig 14a. Switching Time Test Circuit

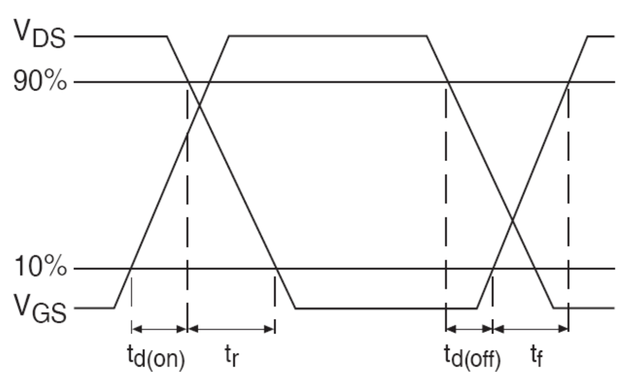
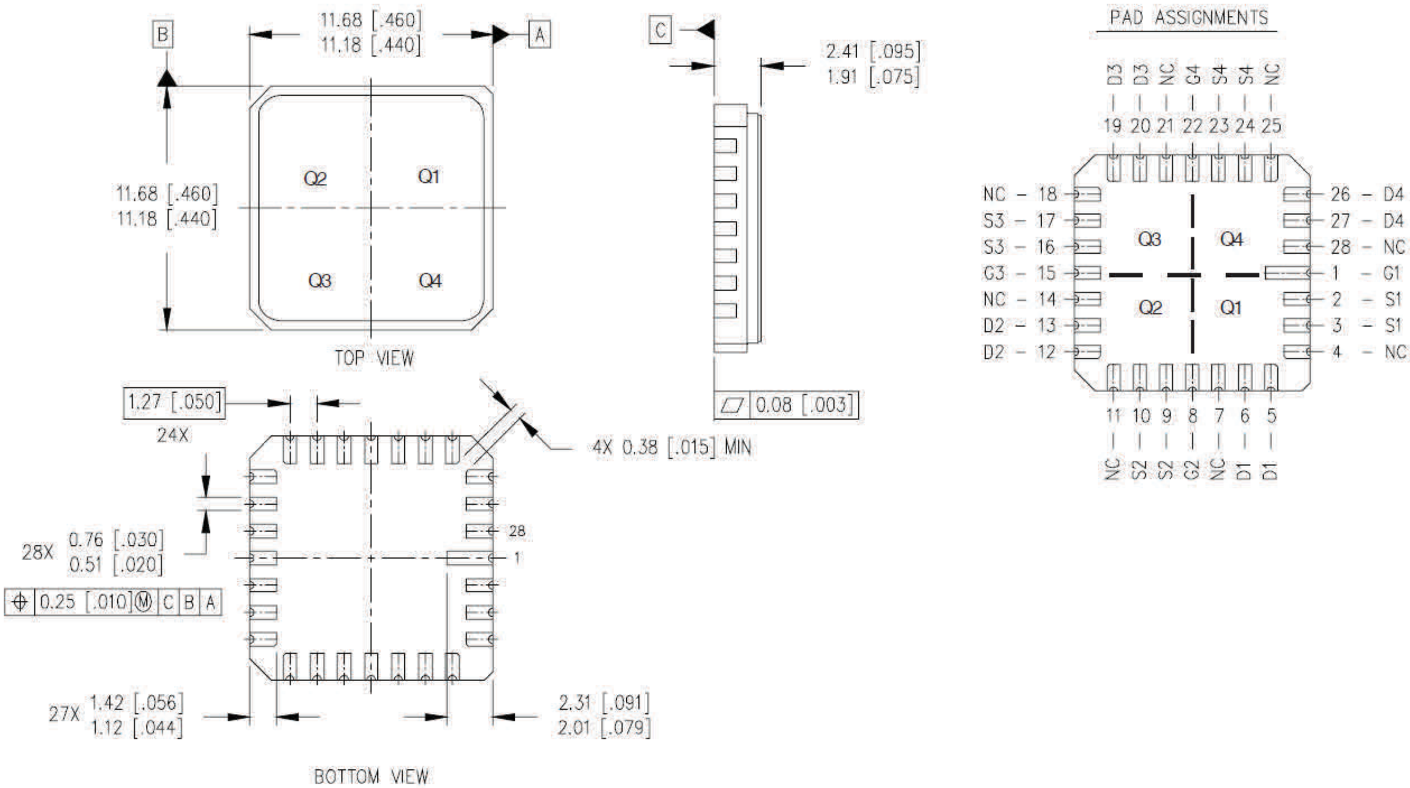


Fig 14b. Switching Time Waveforms

Case Outline and Dimensions - LCC-28



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

PAD ASSIGNMENTS

D = DRAIN
G = GATE
S = SOURCE
NC = NO CONNECTION

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