An Infineon Technologies Company

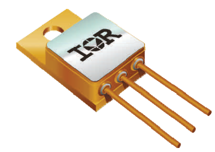
IRHMS57064
JANSR2N7470T1

RADIATION HARDENED POWER MOSFET THRU-HOLE (Low-Ohmic TO-254AA)

60V, N-CHANNEL
REF: MIL-PRF-19500/698
R5 TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	I_D	QPL Part Number
IRHMS57064	100 kRads(Si)	0.0076Ω	45A*	JANSR2N7470T1
IRHMS53064	300 kRads(Si)	0.0076Ω	45A*	JANSF2N7470T1
IRHMS55064	500 kRads(Si)	0.0076Ω	45A*	JANSG2N7470T1
IRHMS58064	1000 kRads(Si)	0.0080Ω	45A*	JANSH2N7470T1



Low-Ohmic TO-254AA

Description

IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm^2)). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Features

- Low RDS(on)
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Ceramic Eyelets
- Electrically Isolated
- Light Weight
- ESD Rating: Class 3B per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Pre-Irradiation

Symbol	Parameter	Value	Units
I_{D1} @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	45*	A
I_{D2} @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	45*	
I_{DM} @ T_C = 25°C	Pulsed Drain Current ①	180	
P_D @T_C = 25°C	Maximum Power Dissipation	208	W
	Linear Derating Factor	1.67	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	824	mJ
I_{AR}	Avalanche Current ①	45	A
E_{AR}	Repetitive Avalanche Energy ①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.3	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 ((0.063in./1.6mm from case for 10s)	
	Weight	9.3 (Typical)	g

*Current is limited by package

For Footnotes refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified) Pre-Irradiation

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.067	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Rsistance	—	—	0.0076	Ω	V_{GS} = 12V, I_{D2} = 45A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
Gfs	Forward Transconductance	42	—	—	S	V_{DS} = 15V, I_{D2} = 45A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	10	µA	V_{DS} = 48V, V_{GS} = 0V
		—	—	25		V_{DS} = 48V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_G	Total Gate Charge	—	—	150	nC	I_{D1} = 45A
Q_{GS}	Gate-to-Source Charge	—	—	75		V_{DS} = 30V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	50		V_{GS} = 12V
$t_{d(on)}$	Turn-On Delay Time	—	—	35	ns	V_{DD} = 30V
tr	Rise Time	—	—	125		I_{D1} = 45A
$t_{d(off)}$	Turn-Off Delay Time	—	—	70		R_G = 2.35Ω
t_f	Fall Time	—	—	50		V_{GS} = 12V
Ls +L_D	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm /0.25in. from package) to Source lead (6mm /0.25in. from package) with Source wires internally bonded from Source Pin to Drain Pad
C_{iss}	Input Capacitance	—	5640	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	2410	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	105	—		f = 100KHz
R_G	Gate Resistance	—	1.04	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	45*	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	180		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J = 25°C, I_S = 45A, V_{GS} = 0V④
t_{rr}	Reverse Recovery Time	—	—	170	ns	T_J = 25°C, I_F = 45A, V_{DD} ≤ 50V
Q_{rr}	Reverse Recovery Charge	—	—	760	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

* Current is limited by package

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.60	°C/W
$R_{\theta JCS}$	Case -to- Sink	—	0.21	—	
$R_{\theta JA}$	Junction-to-Ambient (Typical socket mount)	—	—	48	

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 25V, starting T_J = 25°C, L = 0.81mH, Peak I_L = 45A, V_{GS} = 12V

③ I_{SD} ≤ 45A, di/dt ≤ 390A/µs, V_{DD} ≤ 60V, T_J ≤ 150°C

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

⑤ Total Dose Irradiation with V_{GS} Bias. 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

⑥ Total Dose Irradiation with V_{DS} Bias. 48 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR Hirel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Symbol	Parameter	Up to 500 kRads (Si)[1]		1000 kRads (Si)[2]		Units	Test Conditions
		Min.	Max.	Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	——	60	——	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	1.5	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	——	100	——	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	——	-100	——	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	——	10	——	25	µA	V_{DS} = 48V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	——	0.0061	——	0.0071	Ω	V_{GS} = 12V, I_{D2} = 45A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-254AA)	——	0.0076	——	0.0080	Ω	V_{GS} = 12V, I_{D2} = 45A
V_{SD}	Diode Forward Voltage	——	1.2	——	1.2	V	V_{GS} = 0V, I_S = 45A

1. Part number IRHMS57064 (JANSR2N7470T1),IRHMS53064 (JANSF2N7470T1),IRHMS55064 (JANSG2N7470T1)
2. Part numbers IRHMS58064 (JANSH2N7470T1)

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm²))	Energy (MeV)	Range (µm)	VDS (V)				
			@VGS= 0V	@VGS= -5V	@VGS= -10V	@VGS= -15V	@VGS= -20V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	60	60	60	60	30
61 ± 5%	330 ± 7.5%	31 ± 10%	46	46	35	25	15
84 ± 5%	350 ± 10%	28 ± 7.5%	35	30	25	20	14

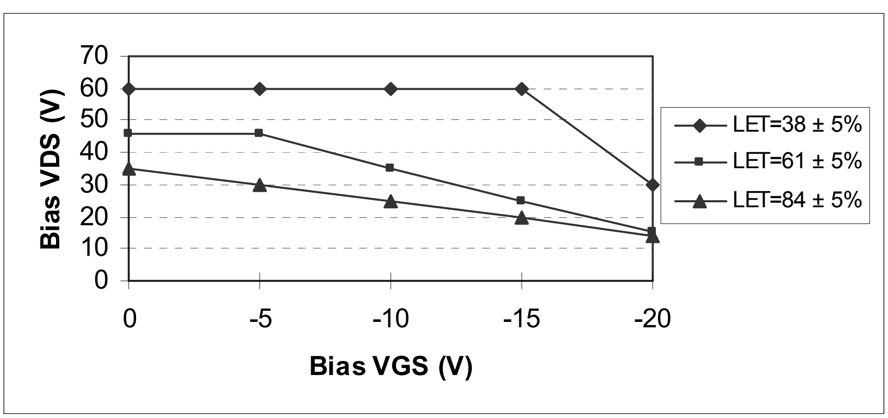


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

Pre-Irradiation

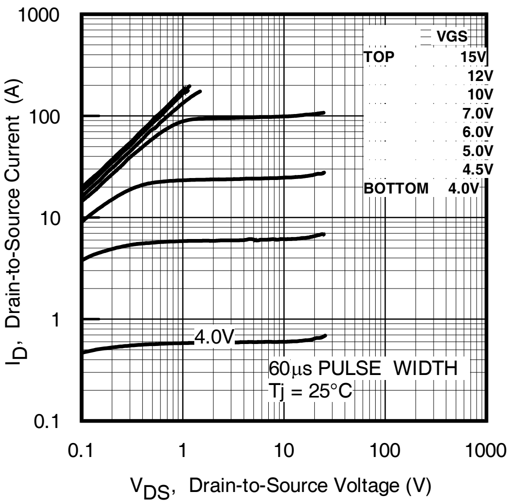


Fig 1. Typical Output Characteristics

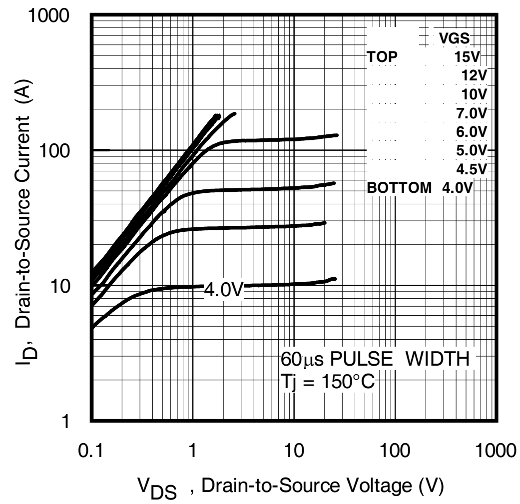


Fig 2. Typical Output Characteristics

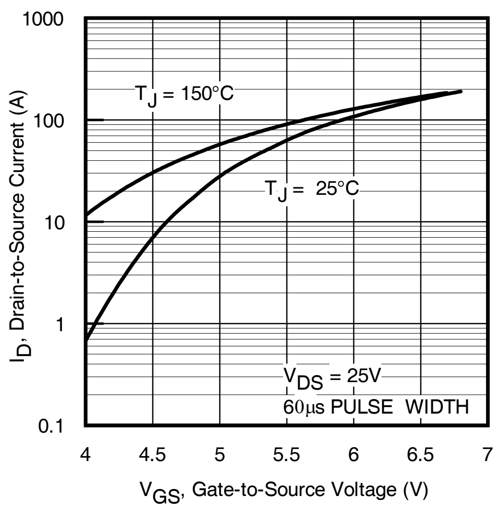


Fig 3. Typical Transfer Characteristics

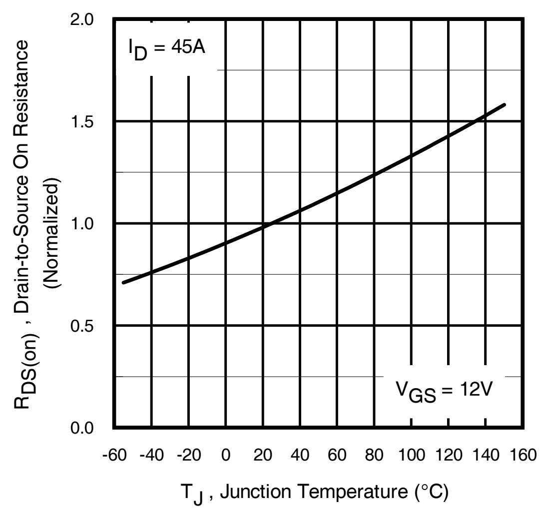


Fig 4. Normalized On-Resistance Vs. Temperature

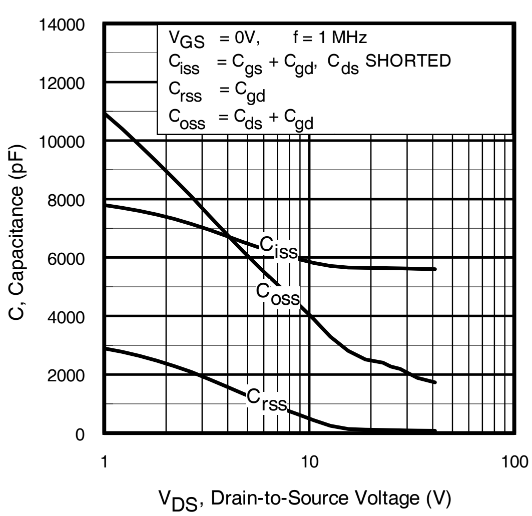


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

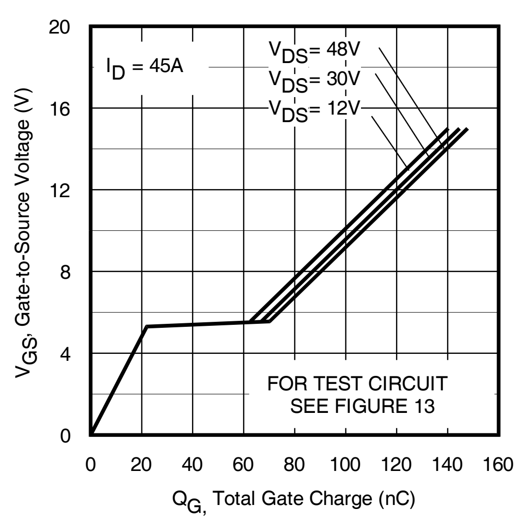


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

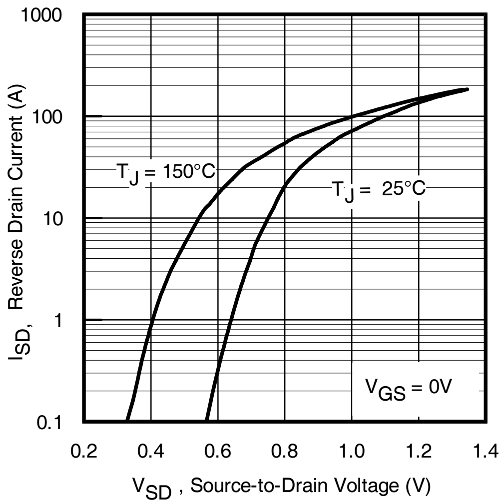


Fig 7. Typical Source-Drain Diode Forward Voltage

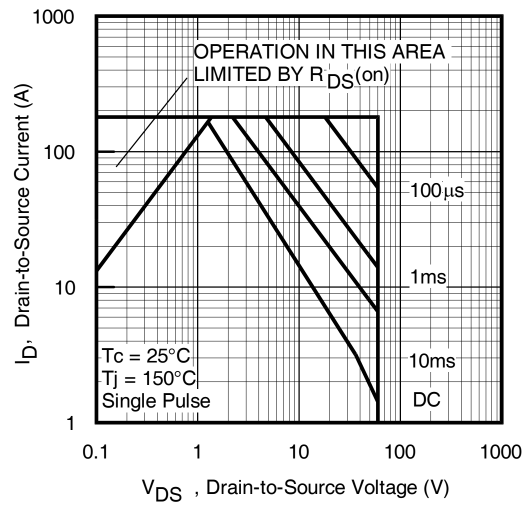


Fig 8. Maximum Safe Operating Area

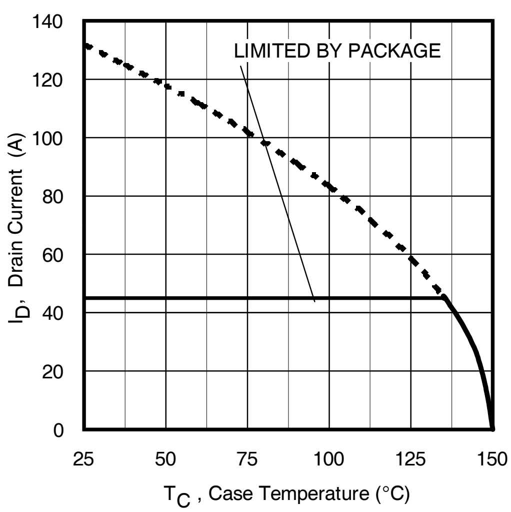


Fig 9. Maximum Drain Current Vs. Case Temperature

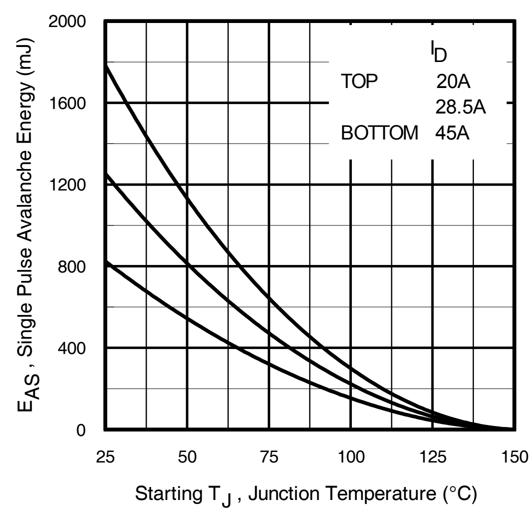


Fig 10. Maximum Avalanche Energy Vs. Drain Current

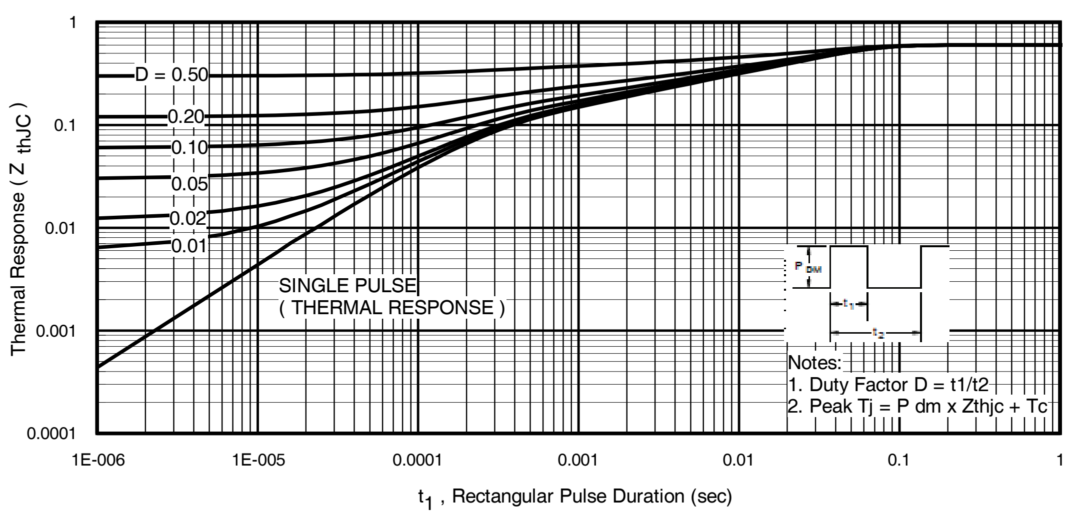


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

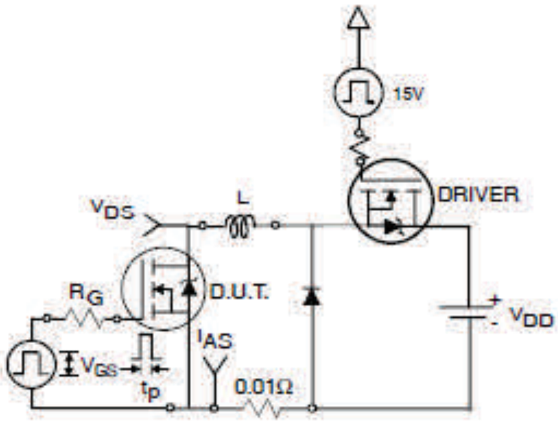


Fig 12a. Unclamped Inductive Test Circuit

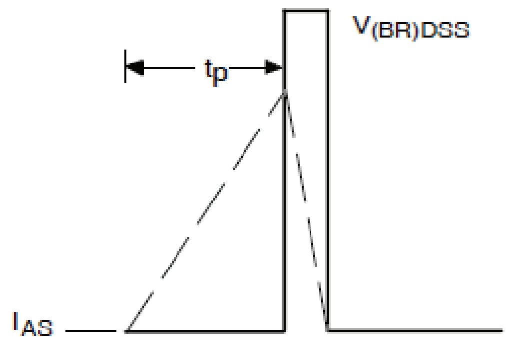


Fig 12b. Unclamped Inductive Waveforms

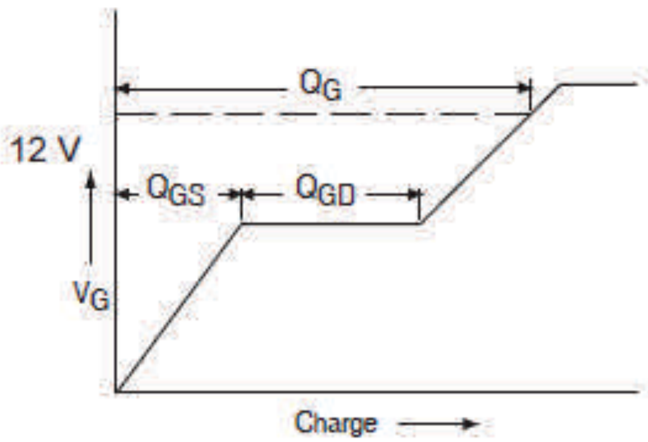


Fig 13a. Gate Charge Waveform

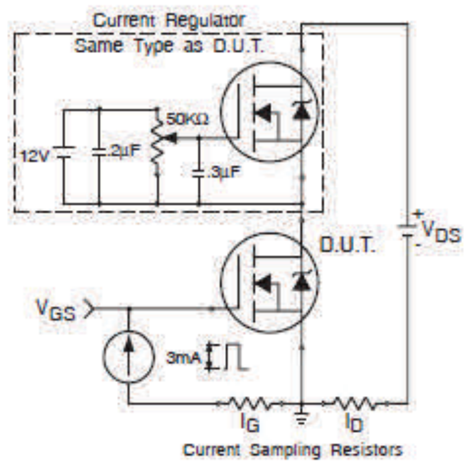


Fig 13b. Gate Charge Test Circuit

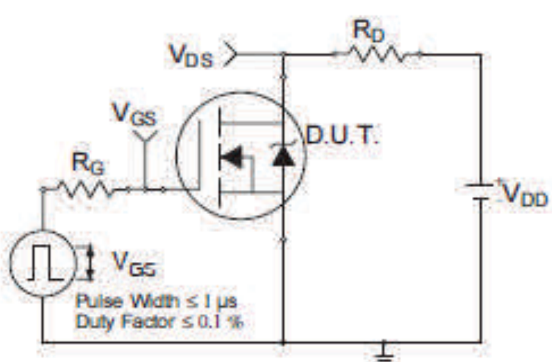


Fig 14a. Switching Time Test Circuit

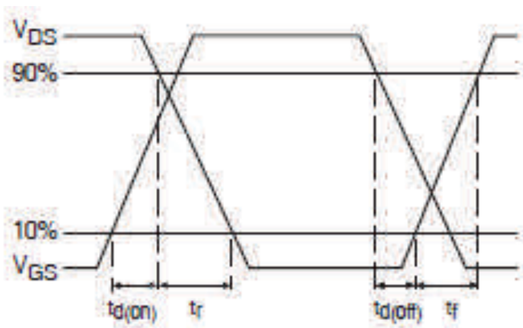
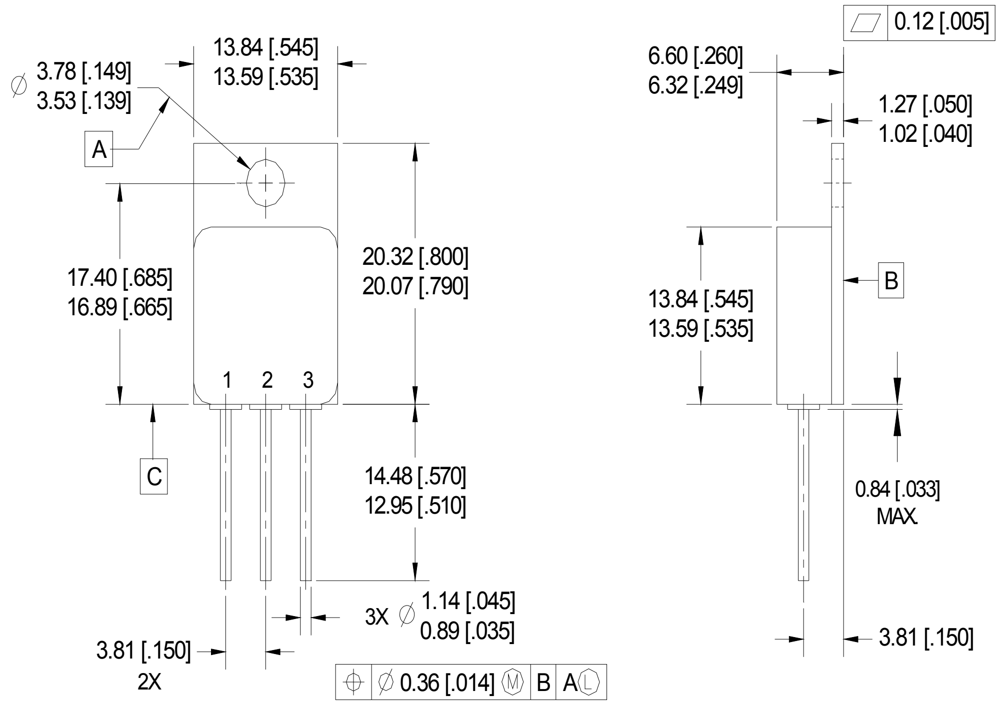


Fig 14b. Switching Time Waveforms

Case Outline and Dimensions - Low-Ohmic TO-254AA



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-254AA.

PIN ASSIGNMENTS

1 = DRAIN
2 = SOURCE
3 = GATE

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

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