# Diode

Emitter Controlled 4 Medium Power Technology

# IDC51D120T8M

## Data Sheet

Industrial Power Control

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# IDC51D120T8M

## Diode Chip in Emitter Controlled 4 Medium Power Technology

**Features:**

- 1200V Emitter Controlled 4 technology 110µm chip
- Soft, fast switching
- Low reverse recovery charge
- Small temperature coefficient

**Recommended for:**

- Low / medium power modules

**Applications:**

- Low / medium power drives


| Chip Type | $V_R$ | $I_{Fn}$ | Die Size | Package |
|---|---|---|---|---|
| IDC51D120T8M | 1200V | 100A | 7.00mm x 7.30mm | Sawn on foil |

**Mechanical Parameters**

| | | | |
|---|---|---|---|
| Die size | | 7.00 x 7.30 | $mm^2$ |
| Area total | | 51.10 | |
| Anode pad size | | 6.026 x 6.346 | |
| Silicon thickness | | 110 | µm |
| Wafer size | | 200 | mm |
| Maximum possible chips per wafer | | 518 | |
| Passivation frontside | | Photoimide | |
| Pad metal | | 3200nm AlSiCu | |
| Backside metal | | Ni Ag – system<br>To achieve a reliable solder connection it is strongly recommended not to consume the Ni layer completely during production process | |
| Die bond | | Electrically conductive epoxy glue and soft solder | |
| Wire bond | | Al, ≤500µm | |
| Reject ink dot size | | ∅ 0.65mm; max 1.2mm | |
| Storage environment (<6 months) | for original and sealed MBB bags | Ambient atmosphere air, temperature 17°C – 25°C | |
| | for open MBB bags | Acc. IEC 62258-3; Section 9.4 Storage Environment. | |

## Maximum Ratings

**In general, from reliability and lifetime point of view, the lower the operation junction temperature and/or the applied voltage, the greater the expected lifetime of any semiconductor device.**

| Parameter | Symbol | Conditions | Value | Unit |
|---|---|---|---|---|
| Repetitive peak reverse voltage | $V_{RRM}$ | $T_{vj}$=25°C | 1200 | V |
| Continuous forward current [1] | $I_F$ | | - | A |
| Maximum repetitive forward current [2] | $I_{FRM}$ | | 200 | |
| Junction temperature | $T_{vj}$ | | -40...+175 | °C |
| Operating junction temperature | $T_{vj\ op}$ | | -40…+150 | °C |

**Static Characteristics** (tested on wafer), $T_{vj}$=25°C

| Parameter | Symbol | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| Reverse leakage current | $I_R$ | $V_R$=1200V | - | - | 18.0 | µA |
| Cathode-anode breakdown voltage | $V_{BR}$ | $I_R$=0.25mA | 1200 | - | - | V |
| Forward voltage drop | $V_F$ | $I_F$=100A | 1.35 | 1.70 | 2.05 | |

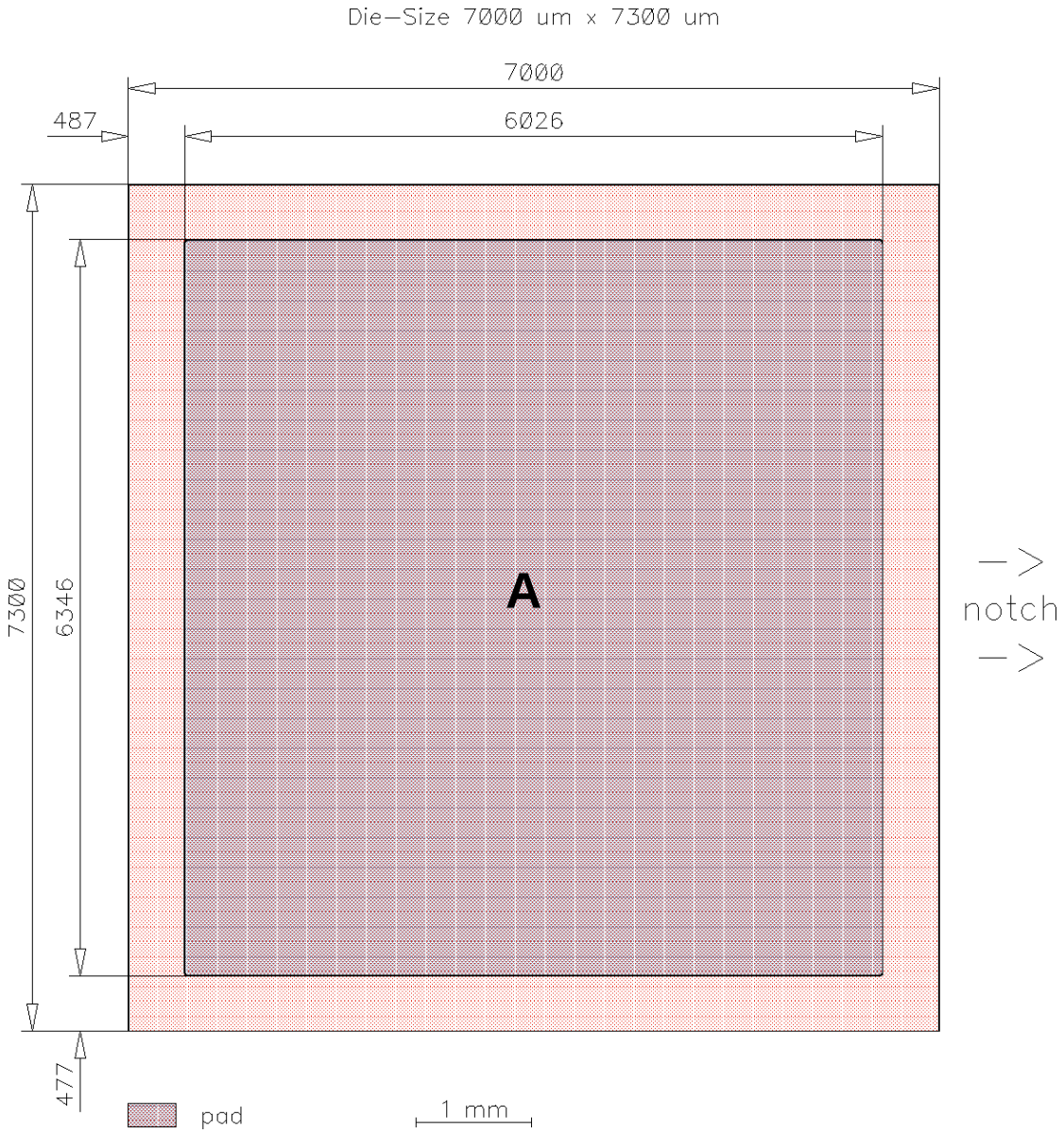
**Further Electrical Characteristics**
Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

| | | |
|---|---|---|
| Application example | FP100R12KT4_B11 | Rev. 3.0 |

[1] Depending on thermal properties of assembly.

[2] Not subject to production test - verified by design/characterization.

**Chip Drawing**




**A** = Anode pad

**Bare Die Product Specifics**
Test coverage at wafer level cannot cover all application conditions. Therefore it is recommended to test all characteristics which are relevant for the application at package level, including RBSOA and SCSOA.

**Description**

| |
|---|
| AQL 0.65 for visual inspection according to failure catalogue |
| Electrostatic Discharge Sensitive Device according to MIL-STD 883 |

**Revision History**

| Revision | Subjects (major changes since last revision) | Date |
|---|---|---|
| 2.0 | Final data sheet | 22.08.2016 |
| | | |
| | | |

**Relevant Application Notes**

| | |
|---|---|
| | |
| | |

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