

**CoolMOS™ Power Transistor**
**Features**

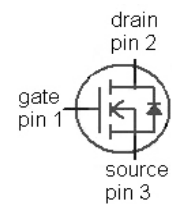
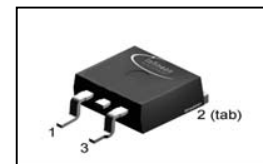
- Lowest figure of merit  $R_{ON} \times Q_g$
- Ultra low gate charge
- Extreme dv/dt rated
- High peak current capability
- Pb-free lead plating; RoHS compliant; Halogen free for mold compound
- Qualified for industrial grade applications according to JEDEC<sup>1)</sup>

**Product Summary**

$V_{DS} @ T_{jmax}$	550	V
$R_{DS(on),max}$	0.140	$\Omega$
$Q_{g,typ}$	48	nC

**CoolMOS CP is designed for:**

- Hard & soft switching SMPS topologies
- CCM PFC for ATX Notebook adapter, PDP and LCD TV
- PWM for ATX, Notebook adapter, PDP and LCD TV

**PG-TO263**


Type	Package	Marking
IPB50R140CP	PG-TO263	5R140P

**Maximum ratings, at  $T_j=25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$T_C=25\text{ }^\circ\text{C}$	23	A
		$T_C=100\text{ }^\circ\text{C}$	15	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C=25\text{ }^\circ\text{C}$	56	
Avalanche energy, single pulse	$E_{AS}$	$I_D=9.3\text{ A}, V_{DD}=50\text{ V}$	616	mJ
Avalanche energy, repetitive $t_{AR}$ <sup>2),3)</sup>	$E_{AR}$	$I_D=9.3\text{ A}, V_{DD}=50\text{ V}$	0.93	
Avalanche current, repetitive $t_{AR}$ <sup>2),3)</sup>	$I_{AR}$		9	A
MOSFET dv/dt ruggedness	dv/dt	$V_{DS}=0\dots400\text{ V}$	50	V/ns
Gate source voltage	$V_{GS}$	static	$\pm 20$	V
		AC (f>1 Hz)	$\pm 30$	
Power dissipation	$P_{tot}$	$T_C=25\text{ }^\circ\text{C}$	192	W
Operating and storage temperature	$T_j, T_{stg}$		-55 ... 150	$^\circ\text{C}$
Mounting torque		M3 and M3.5 screws	60	Ncm

**Maximum ratings, at  $T_j=25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous diode forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	14	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$		56	
Reverse diode $dv/dt$ <sup>4)</sup>	$dv/dt$		15	V/ns

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - case	$R_{thJC}$		-	-	0.65	K/W
Thermal resistance, junction - ambient	$R_{thJA}$	SMD version, device on PCB, minimal footprint	-	-	62	
		SMD version, device on PCB, 6 cm <sup>2</sup> cooling area <sup>5)</sup>	-	35	-	
Soldering temperature, wave & reflow soldering allowed	$T_{sold}$	reflow MSL 1	-	-	260	°C

**Electrical characteristics, at  $T_j=25\text{ }^\circ\text{C}$ , unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=250\text{ }\mu\text{A}$	500	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=0.93\text{ mA}$	2.5	3	3.5	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=500\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$	-	-	2	$\mu\text{A}$
		$V_{DS}=500\text{ V}, V_{GS}=0\text{ V}, T_j=150\text{ }^\circ\text{C}$	-	20	-	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=14\text{ A}, T_j=25\text{ }^\circ\text{C}$	-	0.13	0.14	$\Omega$
		$V_{GS}=10\text{ V}, I_D=14\text{ A}, T_j=150\text{ }^\circ\text{C}$	-	0.32	-	
Gate resistance	$R_G$	$f=1\text{ MHz}, \text{open drain}$	-	2.2	-	$\Omega$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
<b>Dynamic characteristics</b>						
Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=100\text{ V},$ $f=1\text{ MHz}$	-	2540	-	pF
Output capacitance	$C_{oss}$		-	110	-	
Effective output capacitance, energy related <sup>6)</sup>	$C_{o(er)}$	$V_{GS}=0\text{ V}, V_{DS}=0\text{ V}$ to 400 V	-	110	-	
Effective output capacitance, time related <sup>7)</sup>	$C_{o(tr)}$		-	230	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=400\text{ V},$ $V_{GS}=10\text{ V}, I_D=14\text{ A},$ $R_G=12.2\ \Omega$	-	35	-	ns
Rise time	$t_r$		-	14	-	
Turn-off delay time	$t_{d(off)}$		-	80	-	
Fall time	$t_f$		-	8.0	-	
<b>Gate Charge Characteristics</b>						
Gate to source charge	$Q_{gs}$	$V_{DD}=400\text{ V}, I_D=14\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	11	-	nC
Gate to drain charge	$Q_{gd}$		-	15	-	
Gate charge total	$Q_g$		-	48	64	
Gate plateau voltage	$V_{plateau}$		-	5.2	-	V
<b>Reverse Diode</b>						
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=14\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.9	1.2	V
Reverse recovery time	$t_{rr}$	$V_R=400\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	400	-	ns
Reverse recovery charge	$Q_{rr}$		-	5.6	-	$\mu\text{C}$
Peak reverse recovery current	$I_{rrm}$		-	26	-	A

<sup>1)</sup> J-STD20 and JESD22

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Repetitive avalanche causes additional power losses that can be calculated as  $P_{AV}=E_{AR} \cdot f$ .

<sup>4)</sup>  $I_{SD} \leq I_D, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DClink}=400\text{ V}, V_{peak} < V_{(BR)DSS}, T_j < T_{j,max}$ , identical low and high side switch

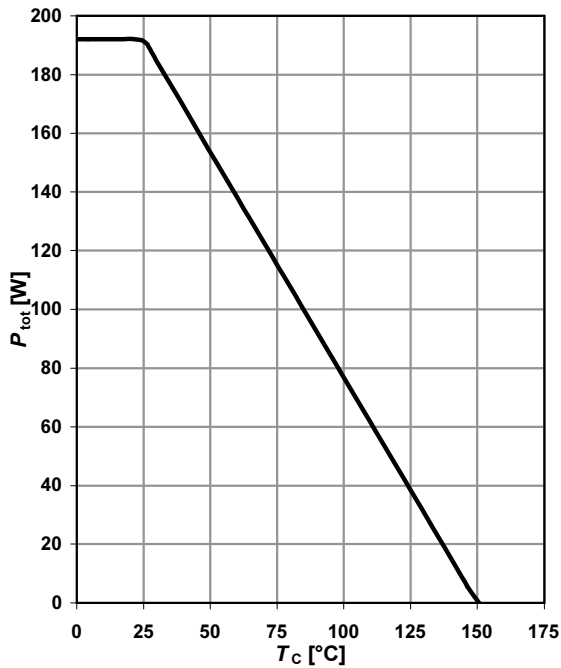
<sup>5)</sup> Device on 40mm\*40mm\*1.5 epoxy PCB FR4 with 6cm<sup>2</sup> (one layer, 70 $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical without blown air

<sup>6)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

<sup>7)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**1 Power dissipation**

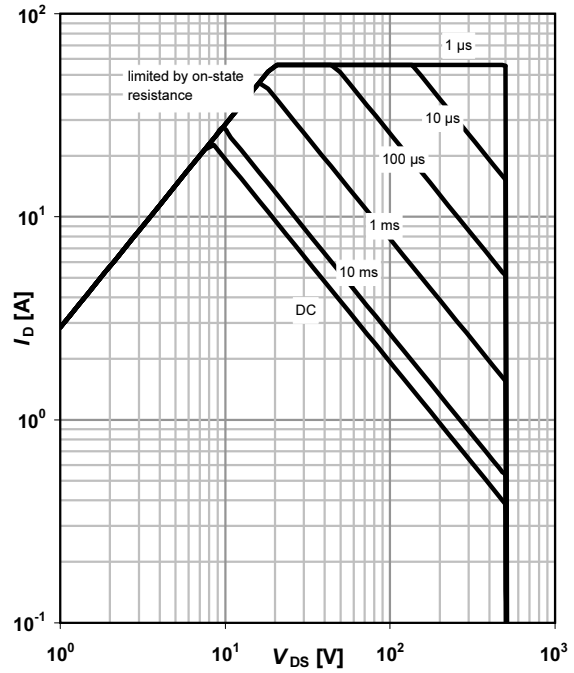
$P_{tot}=f(T_C)$



**2 Safe operating area**

$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$

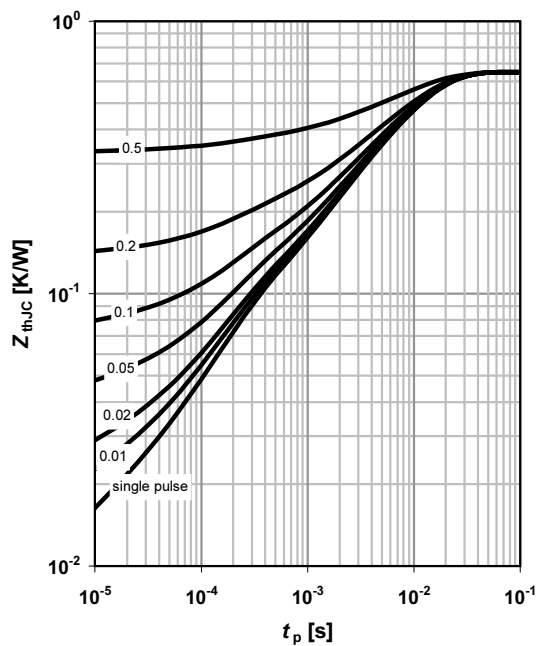
parameter:  $t_p$



**3 Max. transient thermal impedance**

$Z_{(thJC)}=f(t_p)$

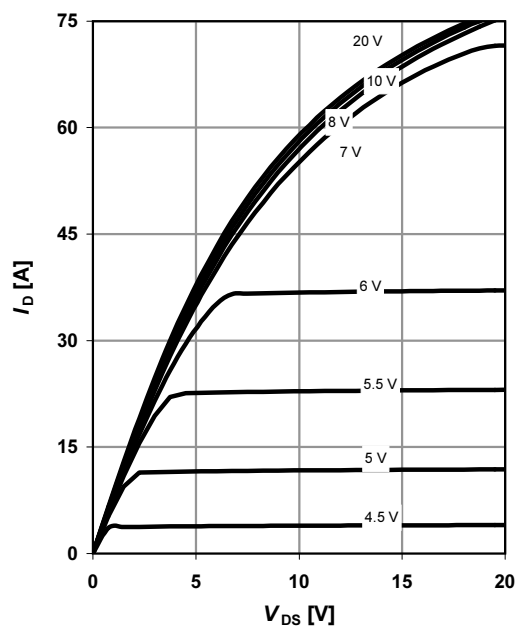
parameter:  $D=t_p/T$



**4 Typ. output characteristics**

$I_D=f(V_{DS}); T_J=25\text{ °C}$

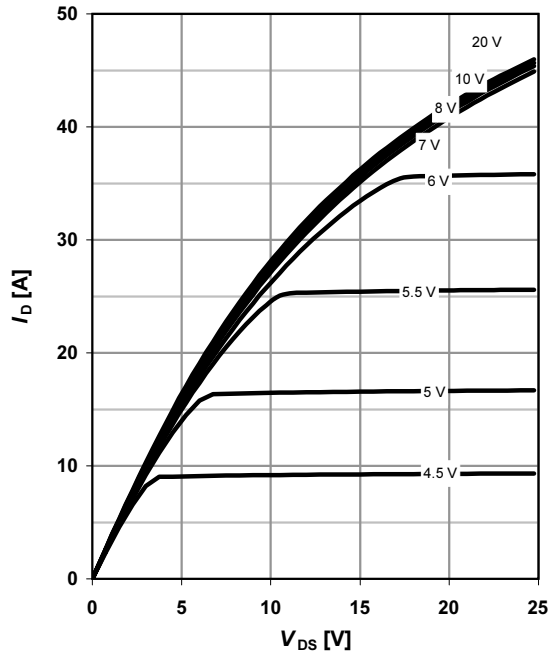
parameter:  $V_{GS}$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 150\text{ }^\circ\text{C}$

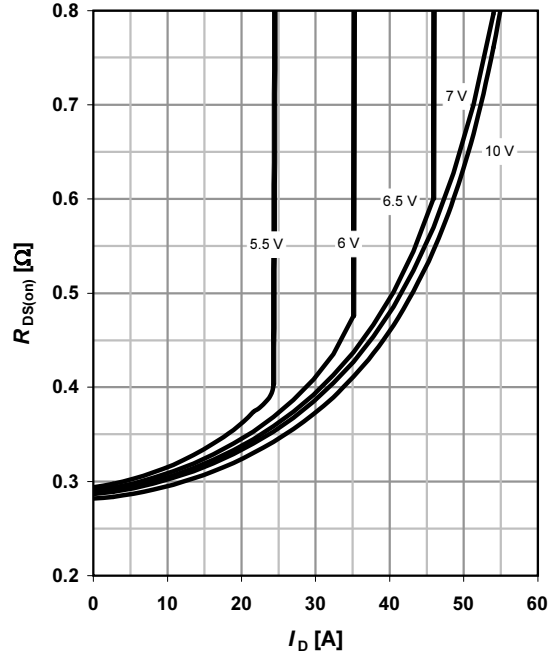
parameter:  $V_{GS}$



**6 Typ. drain-source on-state resistance**

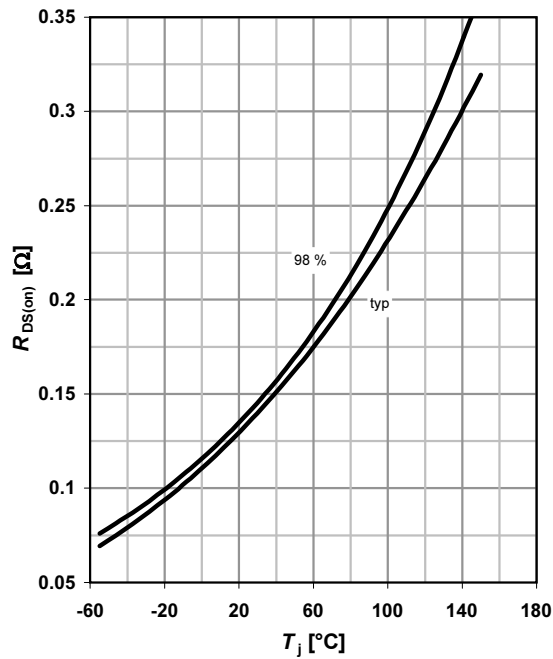
$R_{DS(on)} = f(I_D); T_j = 150\text{ }^\circ\text{C}$

parameter:  $V_{GS}$



**7 Drain-source on-state resistance**

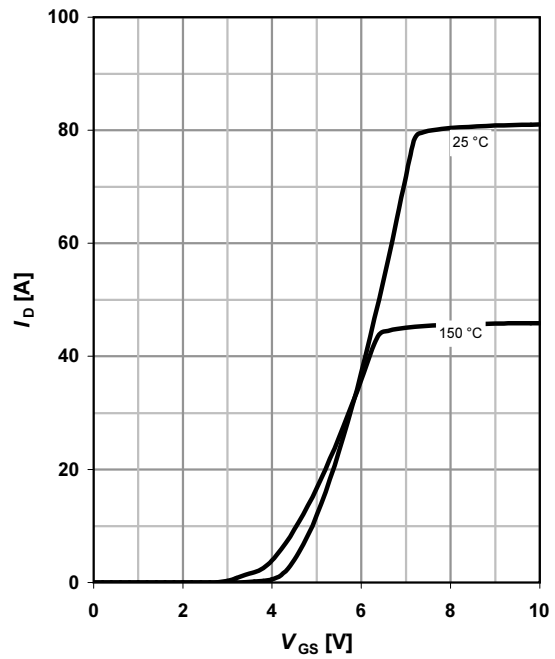
$R_{DS(on)} = f(T_j); I_D = 14\text{ A}; V_{GS} = 10\text{ V}$



**8 Typ. transfer characteristics**

$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

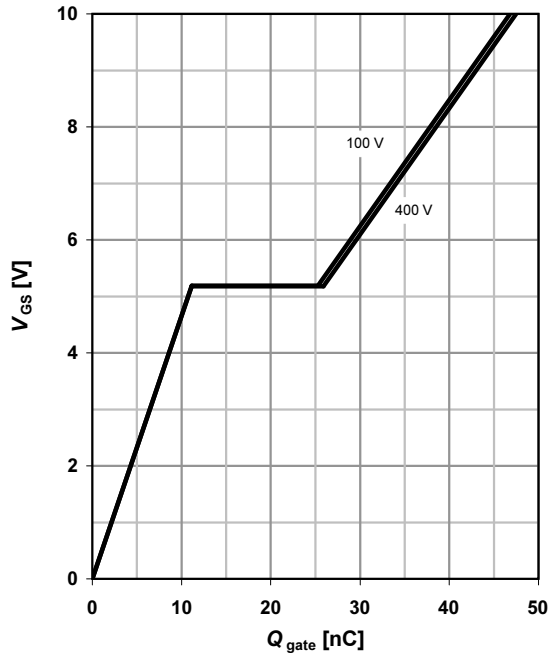
parameter:  $T_j$



**9 Typ. gate charge**

$V_{GS}=f(Q_{gate}); I_D=14\text{ A pulsed}$

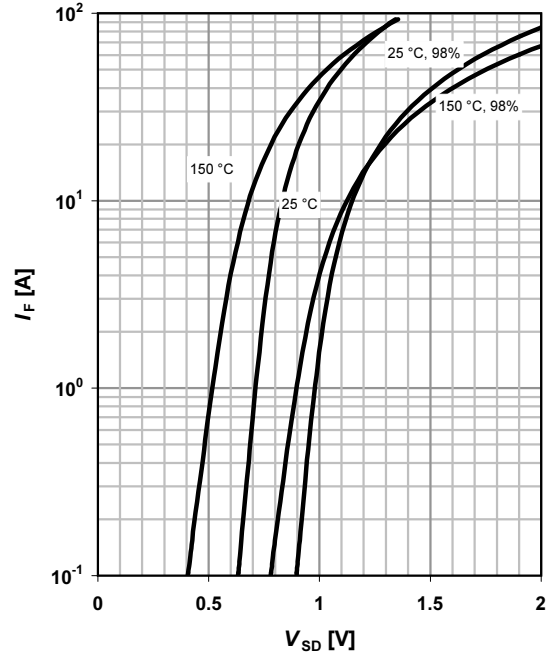
parameter:  $V_{DD}$



**10 Forward characteristics of reverse diode**

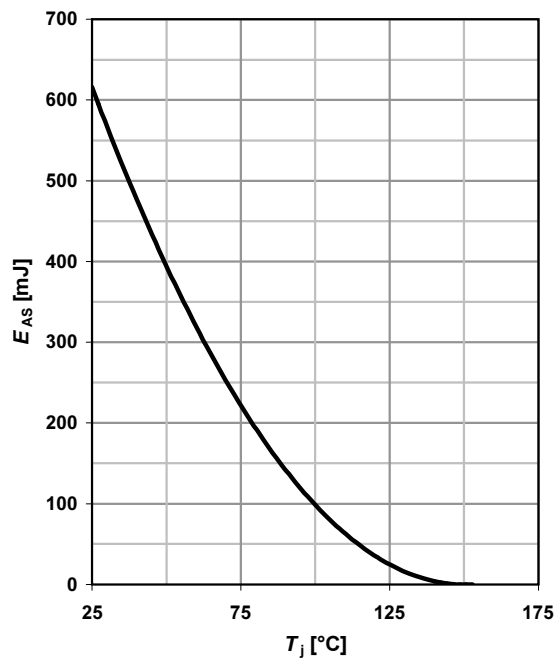
$I_F=f(V_{SD})$

parameter:  $T_j$



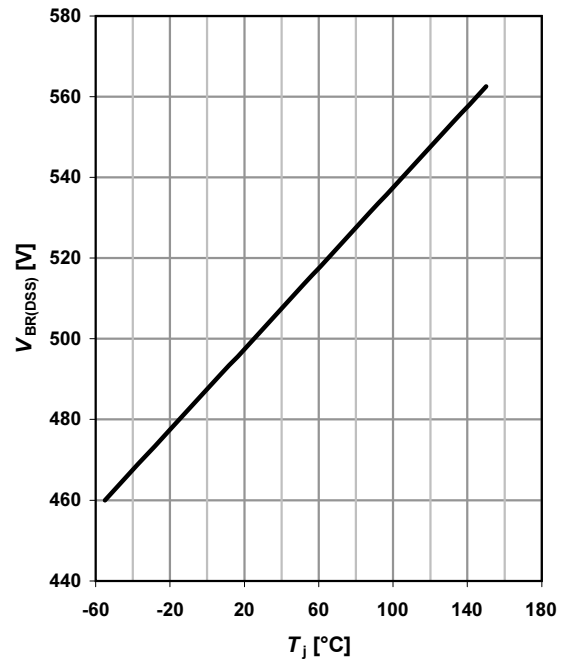
**11 Avalanche energy**

$E_{AS}=f(T_j); I_D=9.3\text{ A}; V_{DD}=50\text{ V}$



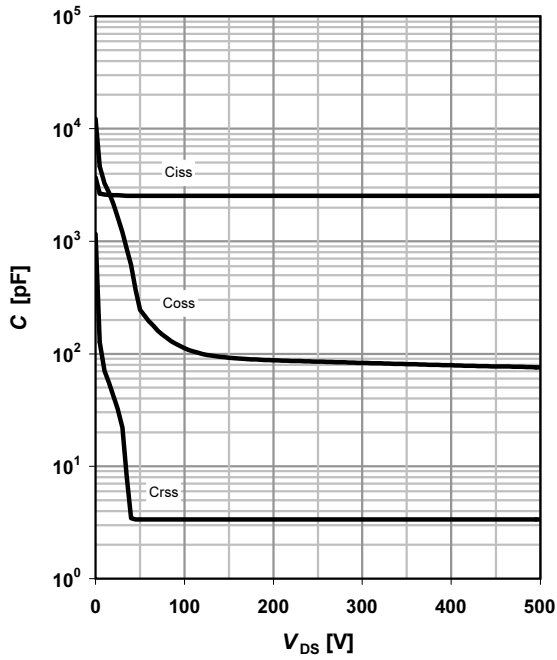
**12 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=0.25\text{ mA}$



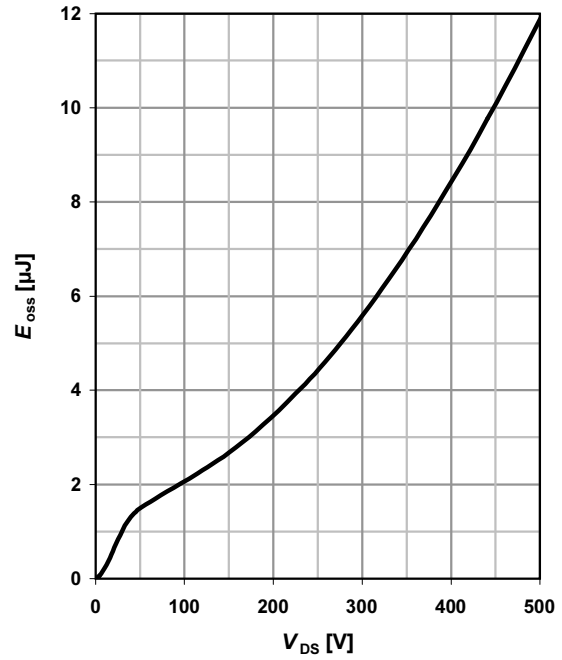
13 Typ. capacitances

$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



14 Typ.  $E_{oss}$  stored energy

$E_{oss} = f(V_{DS})$



Definition of diode switching characteristics







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