

MOSFET

800V CoolMOS™ P7 Power Transistor

The latest 800V CoolMOS™ P7 series sets a new benchmark in 800V super junction technologies and combines best-in-class performance with state of the art ease-of-use, resulting from Infineon's over 18 years pioneering super junction technology innovation.

Features

- Best-in-class FOM $R_{DS(on)} * E_{oss}$; reduced Q_g , C_{iss} , and C_{oss}
- Best-in-class DPAK $R_{DS(on)}$
- Best-in-class $V_{(GS)th}$ of 3V and smallest $V_{(GS)th}$ variation of $\pm 0.5V$
- Integrated Zener Diode ESD protection
- Fully qualified acc. JEDEC for Industrial Applications
- Fully optimized portfolio

Benefits

- Best-in-class performance
- Enabling higher power density designs, BOM savings and lower assembly costs
- Easy to drive and to parallel
- Better production yield by reducing ESD related failures
- Less production issues and reduced field returns
- Easy to select right parts for fine tuning of designs

Potential applications

Recommended for hard and soft switching flyback topologies for LED Lighting, low power Chargers and Adapters, Audio, AUX power and Industrial power. Also suitable for PFC stage in Consumer applications and Solar.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

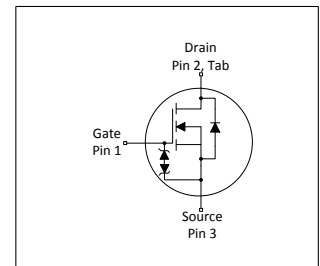


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_j=25^\circ C$	800	V
$R_{DS(on),max}$	1.4	Ω
$Q_{g,typ}$	10	nC
I_D	4	A
$E_{oss} @ 500V$	0.9	μJ
$V_{GS(th),typ}$	3	V
ESD class (HBM)	2	-

Type / Ordering Code	Package	Marking	Related Links
IPA80R1K4P7	PG-TO 220 FullPAK	80R1K4P7	see Appendix A

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	4 2.7	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	8.9	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	8	mJ	$I_D=0.6\text{A}$; $V_{DD}=50\text{V}$
Avalanche energy, repetitive	E_{AR}	-	-	0.07	mJ	$I_D=0.6\text{A}$; $V_{DD}=50\text{V}$
Avalanche current, repetitive	I_{AR}	-	-	0.6	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS}=0$ to 400V
Gate source voltage	V_{GS}	-20 -30	-	20 30	V	static; AC ($f>1$ Hz)
Power dissipation	P_{tot}	-	-	24	W	$T_C=25^\circ\text{C}$
Operating and storage temperature	T_j, T_{stg}	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	50	Ncm	M2.5 screw
Continuous diode forward current	I_S	-	-	3	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	8.9	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	1	V/ns	$V_{DS}=0$ to 400V, $I_{SD}\leq 0.7\text{A}$, $T_j=25^\circ\text{C}$
Maximum diode commutation speed ³⁾	di/dt	-	-	50	A/ μs	$V_{DS}=0$ to 400V, $I_{SD}\leq 0.7\text{A}$, $T_j=25^\circ\text{C}$
Insulation withstand voltage	V_{ISO}	-	-	2500	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	5.1	$^\circ\text{C/W}$	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	$^\circ\text{C/W}$	leaded
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	$^\circ\text{C/W}$	n.a.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	$^\circ\text{C}$	1.6 mm (0.063 in.) from case for 10s

¹⁾ TO220 equivalent. Limited by $T_{j,max}$. Maximum duty cycle $D=0.5$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ $V_{DClink}=400\text{V}$; $V_{DS,peak}<V_{(BR)DSS}$; identical low side and high side switch with identical R_G ; $t_{cond}<2\mu\text{s}$

3 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	800	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5	V	$V_{DS}=V_{GS}, I_D=0.07mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=800V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=800V, V_{GS}=0V, T_j=150^\circ C$
Gate-source leakage current incl. zener diode	I_{GSS}	-	-	1	μA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.2	1.4	Ω	$V_{GS}=10V, I_D=1.4A, T_j=25^\circ C$ $V_{GS}=10V, I_D=1.4A, T_j=150^\circ C$
Gate resistance	R_G	-	1.5	-	Ω	$f=250kHz, \text{open drain}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	250	-	pF	$V_{GS}=0V, V_{DS}=500V, f=250kHz$
Output capacitance	C_{oss}	-	6.5	-	pF	$V_{GS}=0V, V_{DS}=500V, f=250kHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	8	-	pF	$V_{GS}=0V, V_{DS}=0 \text{ to } 500V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	97	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0 \text{ to } 500V$
Turn-on delay time	$t_{d(on)}$	-	10	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=1.4A, R_G=22\Omega$
Rise time	t_r	-	8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=1.4A, R_G=22\Omega$
Turn-off delay time	$t_{d(off)}$	-	40	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=1.4A, R_G=22\Omega$
Fall time	t_f	-	20	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=1.4A, R_G=22\Omega$

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	1	-	nC	$V_{DD}=640V, I_D=1.4A, V_{GS}=0 \text{ to } 10V$
Gate to drain charge	Q_{gd}	-	5	-	nC	$V_{DD}=640V, I_D=1.4A, V_{GS}=0 \text{ to } 10V$
Gate charge total	Q_g	-	10	-	nC	$V_{DD}=640V, I_D=1.4A, V_{GS}=0 \text{ to } 10V$
Gate plateau voltage	$V_{plateau}$	-	4.5	-	V	$V_{DD}=640V, I_D=1.4A, V_{GS}=0 \text{ to } 10V$

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 500V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 500V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V, I_F=1.4A, T_i=25^\circ C$
Reverse recovery time	t_{rr}	-	800	-	ns	$V_R=400V, I_F=0.7A, di_F/dt=50A/\mu s$
Reverse recovery charge	Q_{rr}	-	5	-	μC	$V_R=400V, I_F=0.7A, di_F/dt=50A/\mu s$
Peak reverse recovery current	I_{rrm}	-	9	-	A	$V_R=400V, I_F=0.7A, di_F/dt=50A/\mu s$

4 Electrical characteristics diagrams

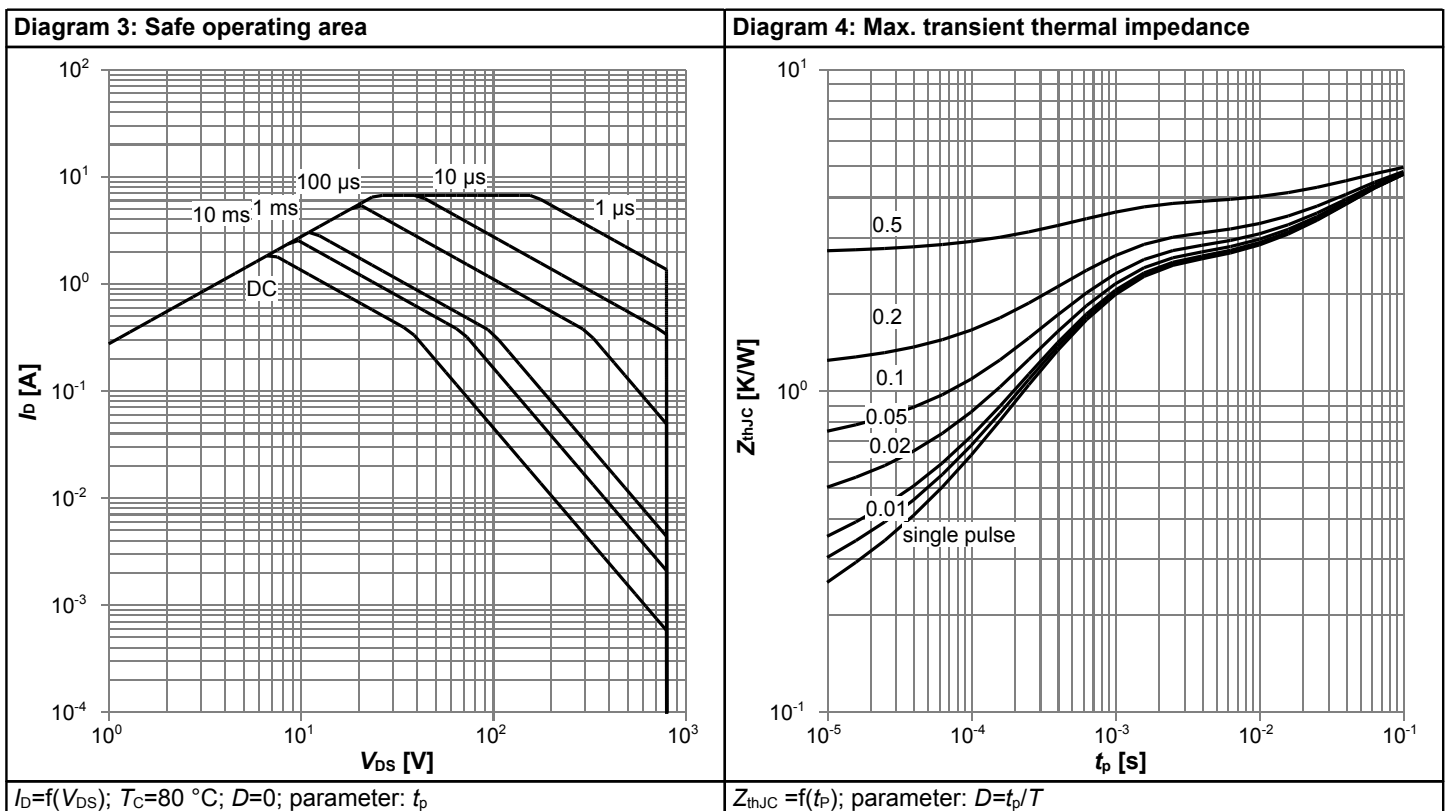
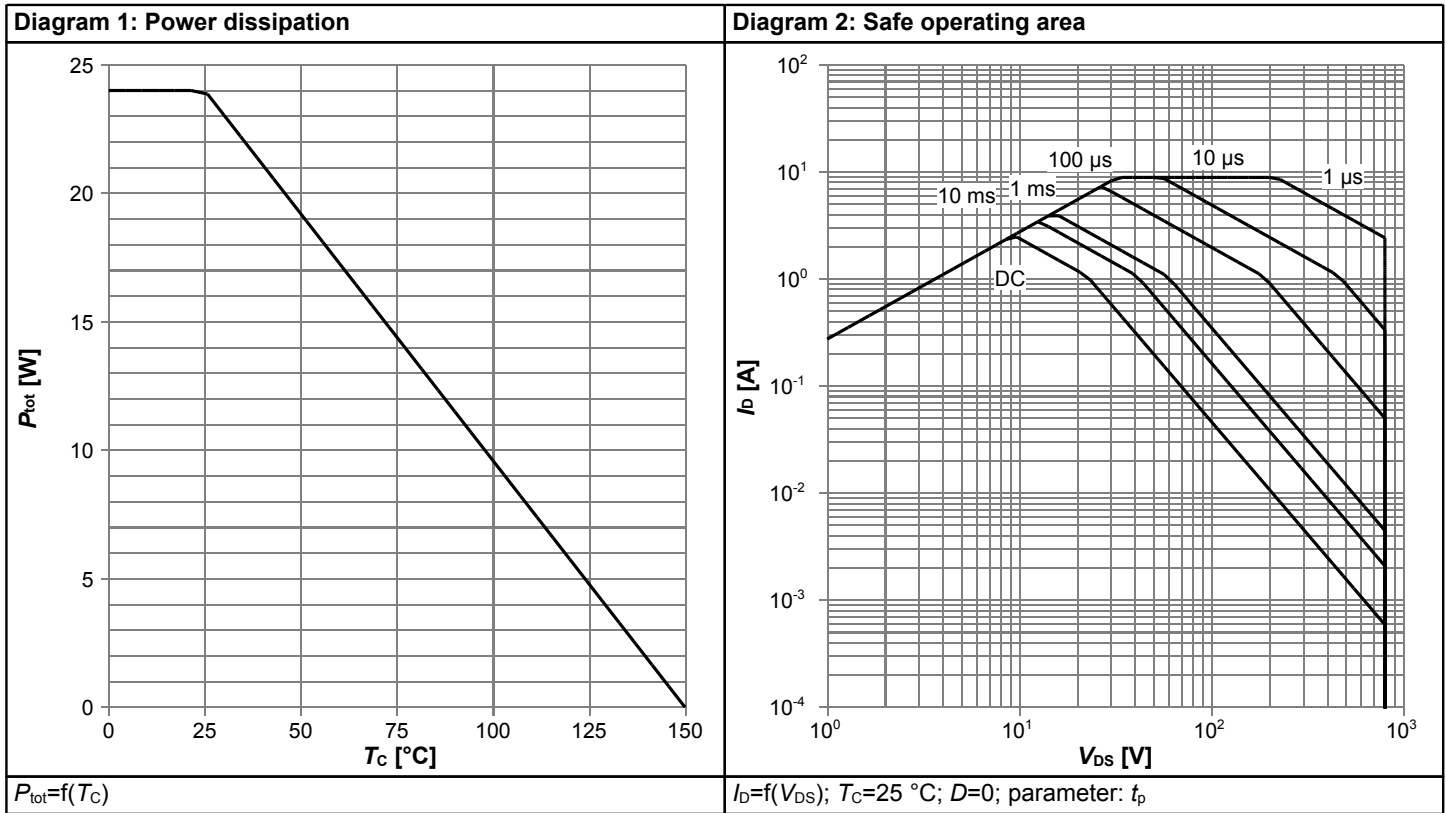
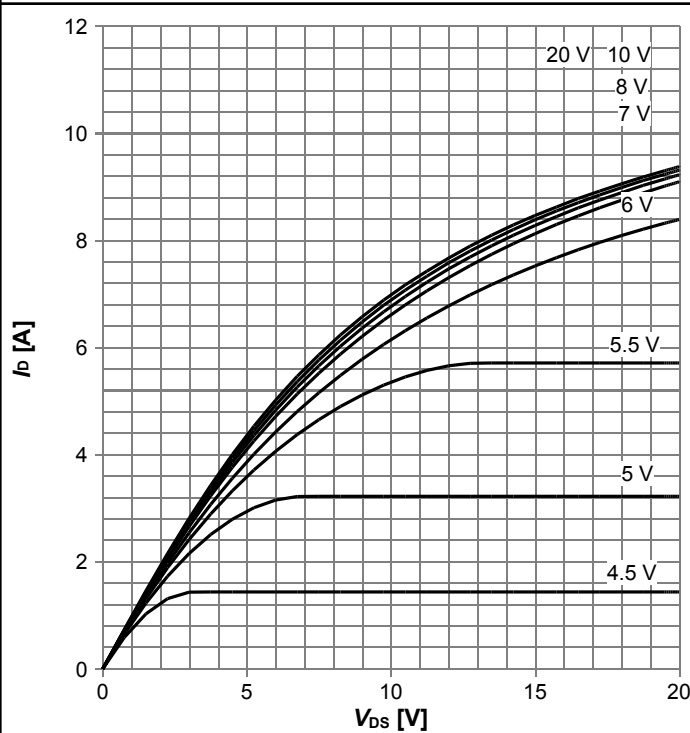
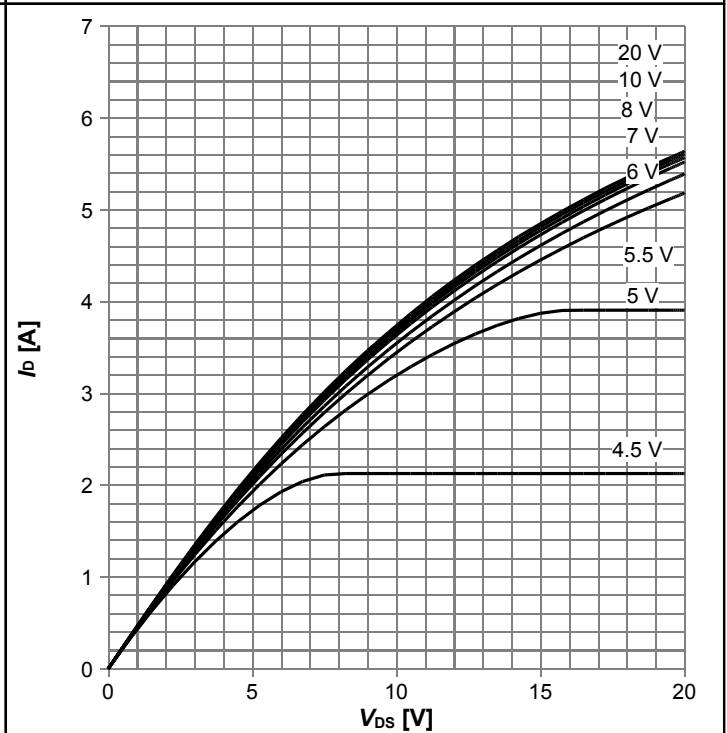


Diagram 5: Typ. output characteristics



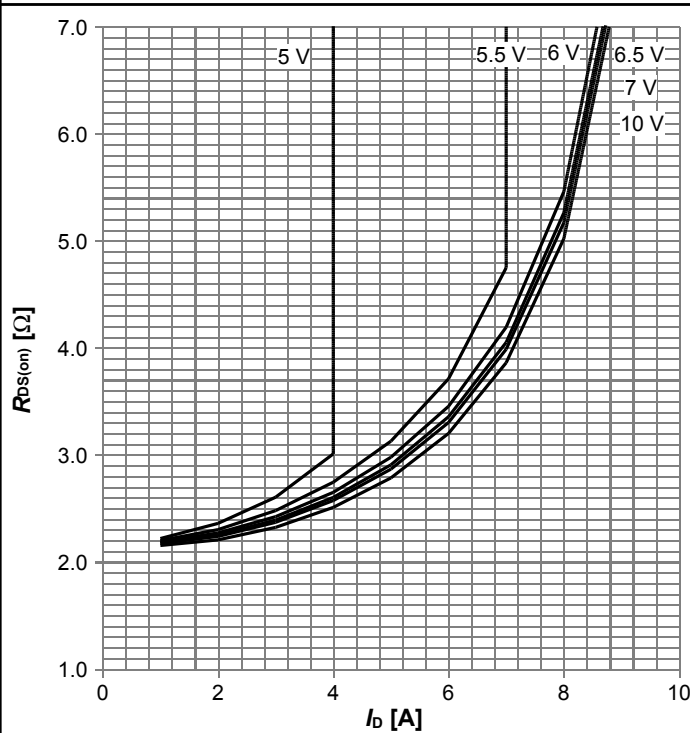
$I_D=f(V_{DS})$; $T_j=25\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



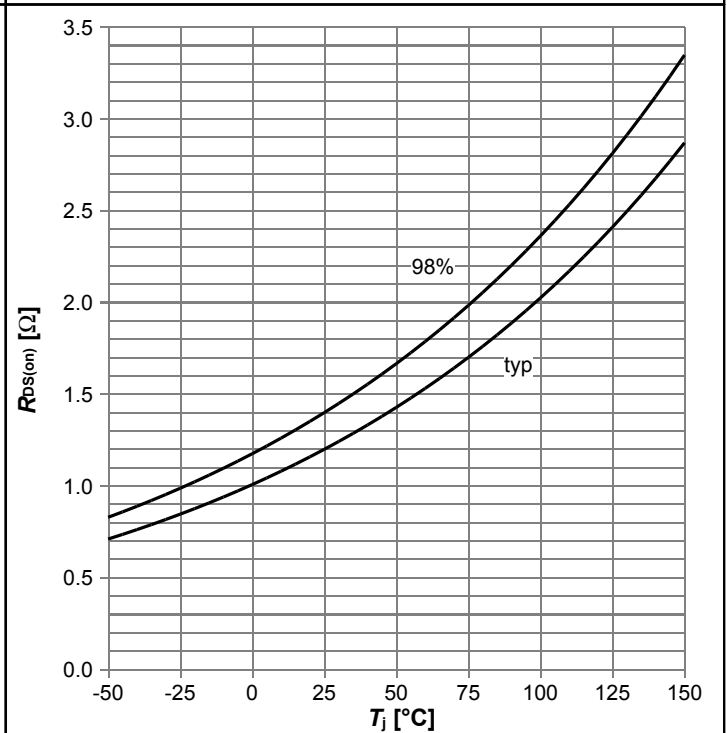
$I_D=f(V_{DS})$; $T_j=125\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



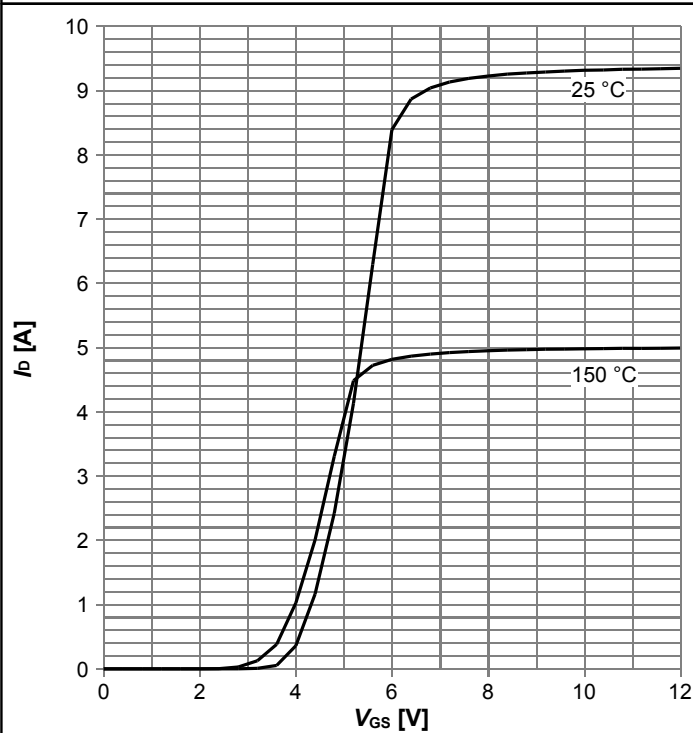
$R_{DS(on)}=f(I_D)$; $T_j=125\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



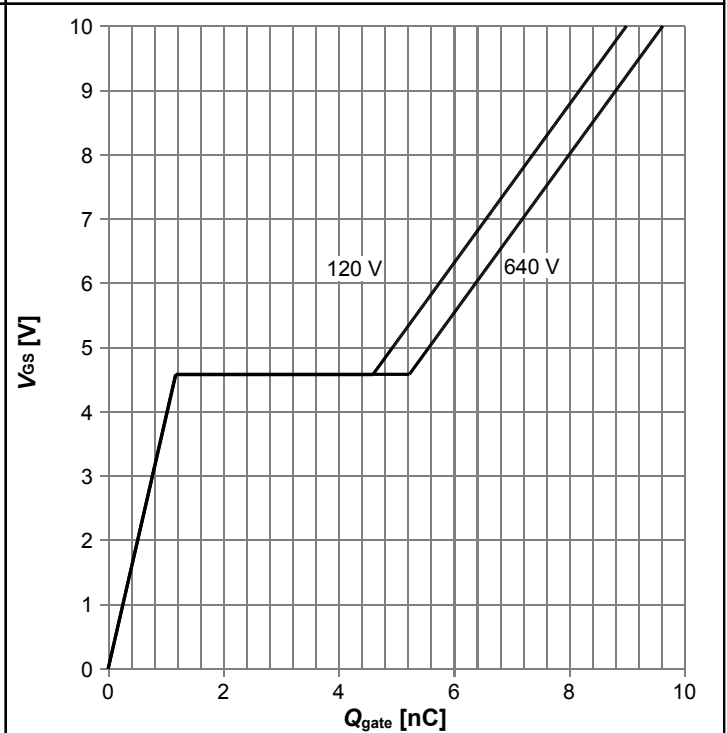
$R_{DS(on)}=f(T_j)$; $I_D=1.4\text{ A}$; $V_{GS}=10\text{ V}$

Diagram 9: Typ. transfer characteristics



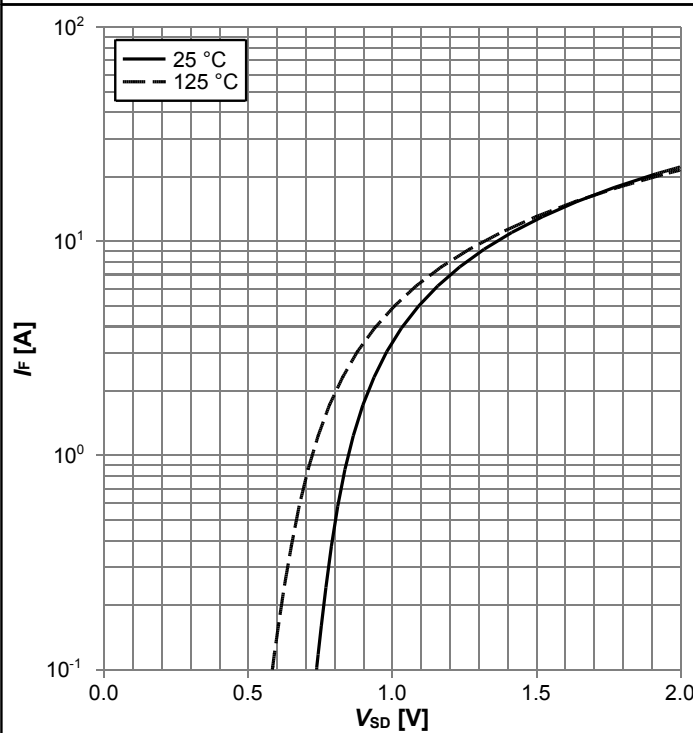
$I_D = f(V_{GS})$; $V_{DS} = 20V$; parameter: T_j

Diagram 10: Typ. gate charge



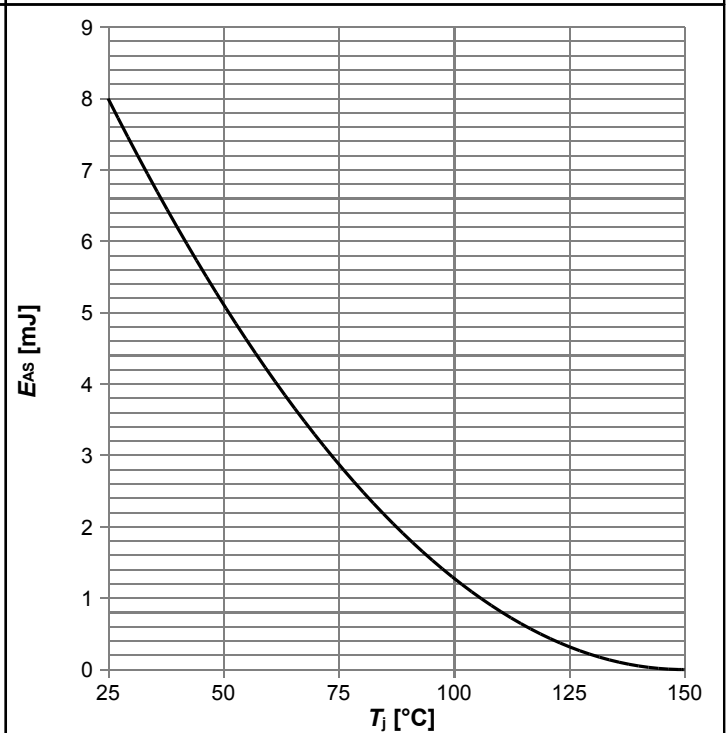
$V_{GS} = f(Q_{gate})$; $I_D = 1.4 A$ pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



$I_F = f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



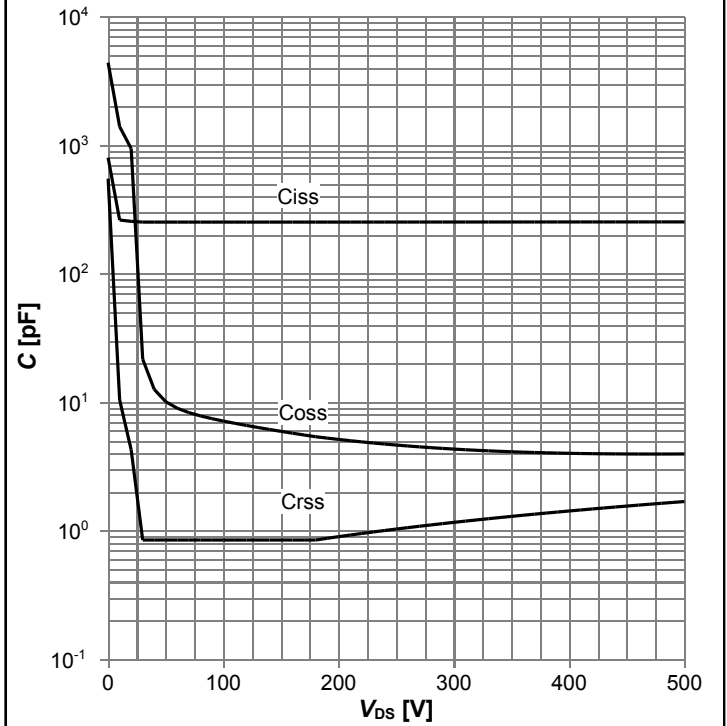
$E_{AS} = f(T_j)$; $I_D = 0.6 A$; $V_{DD} = 50 V$

Diagram 13: Drain-source breakdown voltage



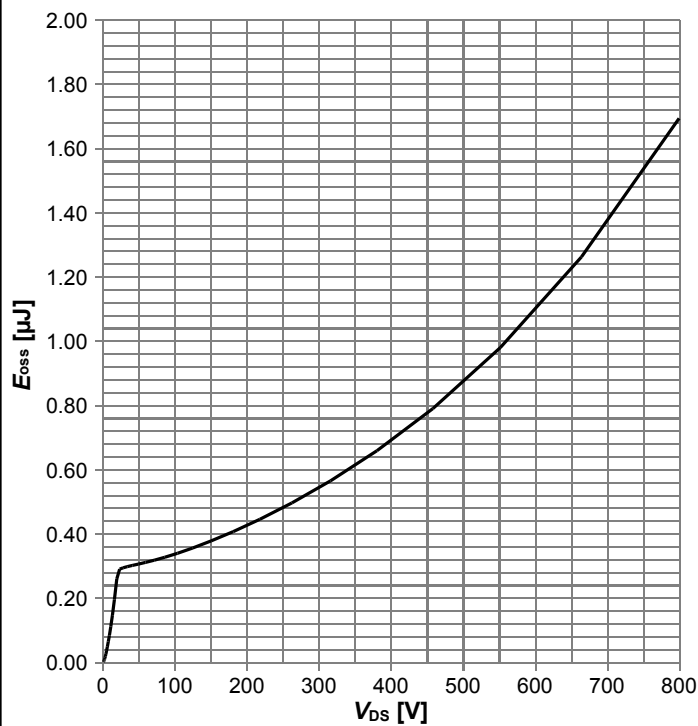
$V_{BR(DSS)}=f(T_j); I_D=1\text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=250\text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics

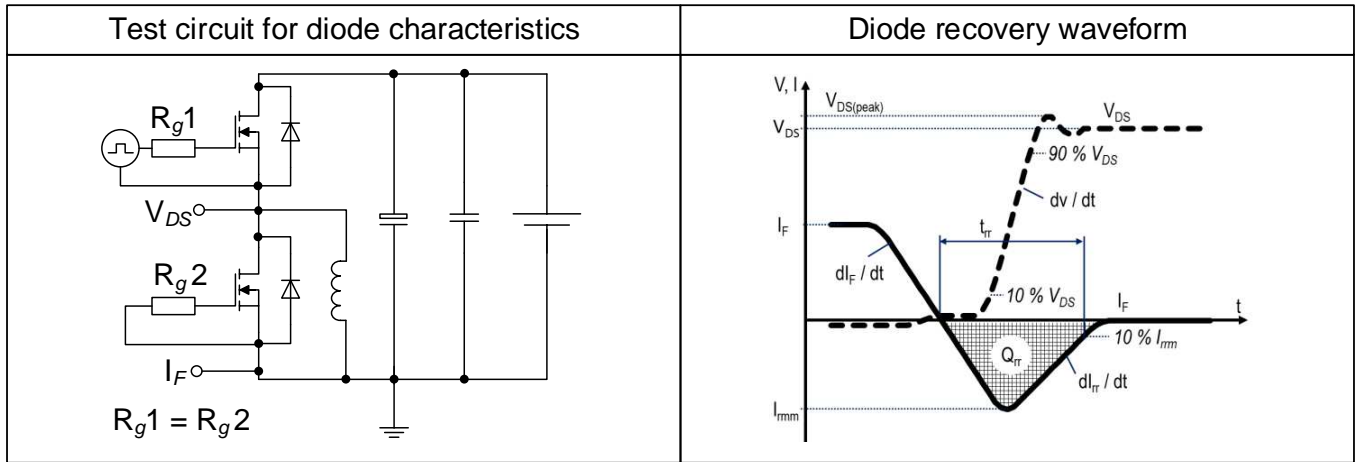


Table 9 Switching times

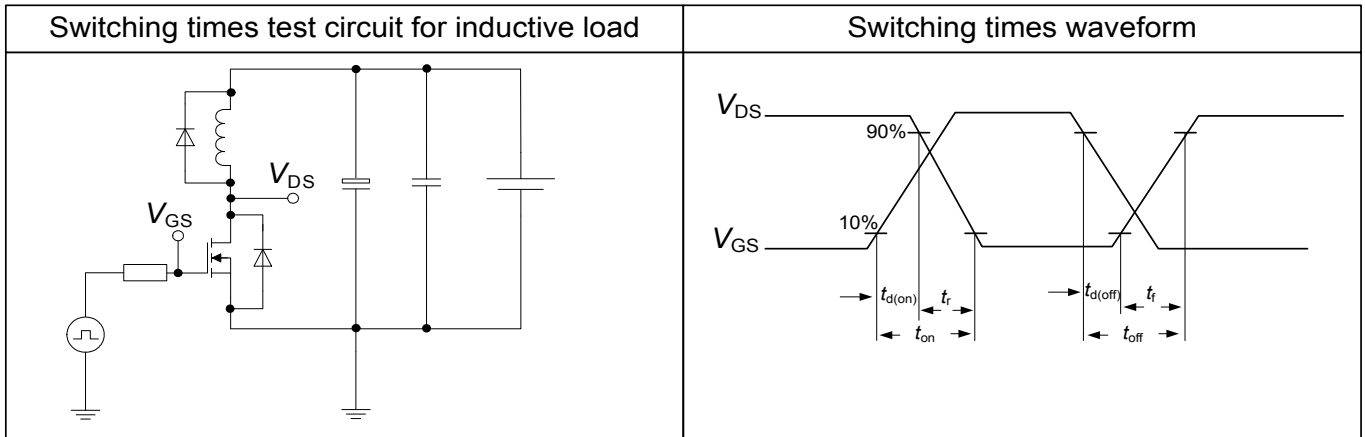
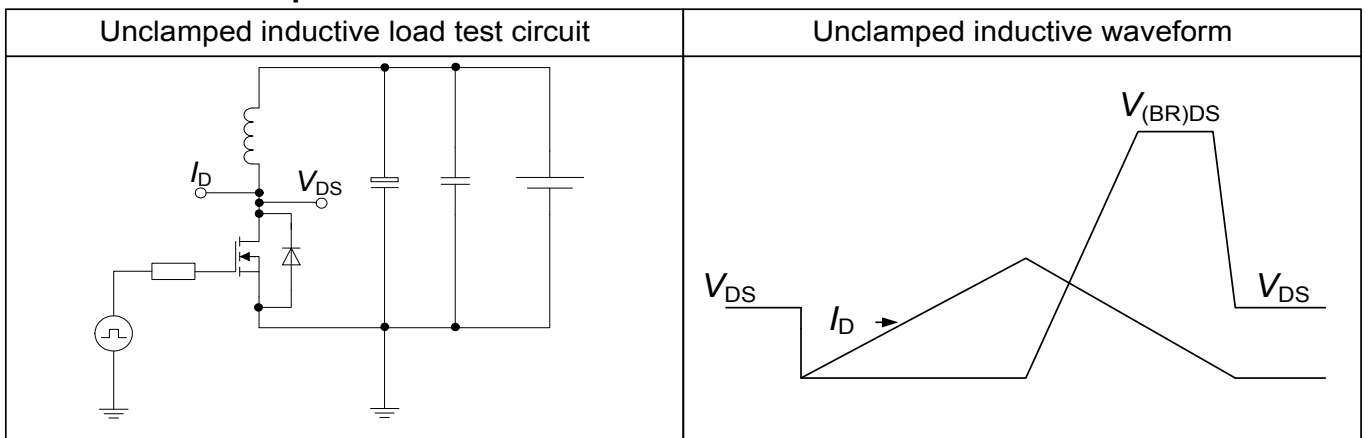


Table 10 Unclamped inductive load



6 Package Outlines



- NOTES:
- INDUSTRIAL QUALITY GRADE
 - ALL DIMENSIONS REFER TO JEDEC STANDARD TO-261 NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS

DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.85	0.092	0.112
A2	2.42	2.86	0.095	0.113
b	0.65	0.90	0.026	0.035
b1	0.95	1.38	0.037	0.054
b2	0.95	1.51	0.037	0.059
b3	0.65	1.38	0.026	0.054
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.67	16.15	0.617	0.636
D1	8.97	9.83	0.353	0.387
E	10.00	10.65	0.394	0.419
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	3		3	
H	28.70	29.75	1.130	1.171
L	12.78	13.75	0.503	0.541
L1	2.83	3.45	0.111	0.136
øP	2.95	3.38	0.116	0.133
Q	3.15	3.50	0.124	0.138

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SCALE

EUROPEAN PROJECTION

ISSUE DATE
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REVISION
06

Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- IFX CoolMOS Webpage: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPA80R1K4P7

Revision: 2018-02-07, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-07-05	Release of final version
2.1	2018-02-07	Corrected front page text

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