

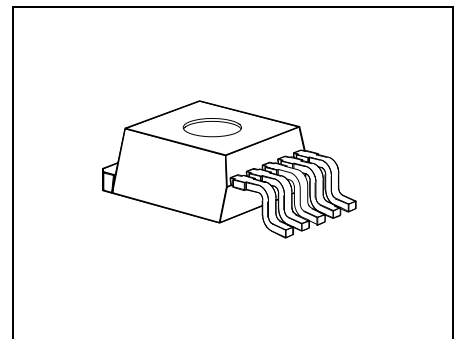
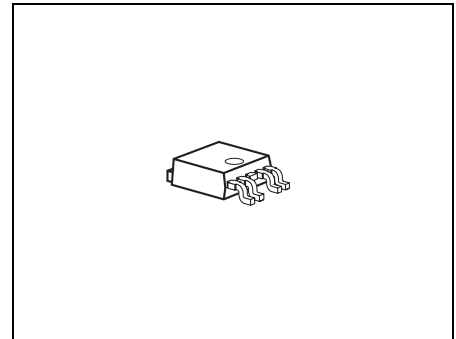


## Features

- Output voltage  $5\text{ V} \pm 2\%$
- Very low current consumption
- 450 mA current capability
- Power Good Feature
- Very low-drop voltage
- Short-circuit-proof
- Reverse polarity proof
- Suitable for use in automotive electronics
- Green Product (RoHS compliant)
- AEC Qualified

## Functional Description

The TLE 4290 is a monolithic integrated low drop voltage regulator which can supply loads up to 450 mA with power good feature. An input voltage up to 42 V is regulated to  $V_{Q,nom} = 5.0\text{ V}$ . The device is designed to supply  $\mu$ -controllers in the severe environment of automotive applications. Therefore it is protected against overload, short circuit and over temperature conditions. Of course the TLE 4290 can be used also in all other applications, where a stabilized 5 V voltage is required.



Type	Package
TLE 4290 D	PG-TO252-5-11
TLE 4290 G	PG-TO263-5-1

### Power Good

The Power Good PG pin informs e.g. the microcontroller in case the output voltage has fallen below the lower threshold  $V_{Q,pgt-d}$  of typ. 3.65 V. Connecting the regulator to a battery voltage at first the power good signal remains LOW. When the output voltage has reached the higher threshold  $V_{Q,pgt-i}$  the power good output remains still LOW for the power good delay time  $t_{rd}$ . Afterwards the power good output turns HIGH. The delay time can be set by the user with an external capacitor at pin D according to the requirements of the application.

The Power Good circuitry supervises the output voltage. In case  $V_Q$  falls below the lower Power Good switching threshold  $V_{Q,pgt-d}$  the PG output is set LOW after the Power Good reaction time. The Power Good LOW signal is generated down to an output voltage  $V_Q$  to 1 V. A LOW signal at the Power Good pin informs that the battery was lost and memory is no longer valid.

The feature should be used in combination with a microcontroller with internal reset.

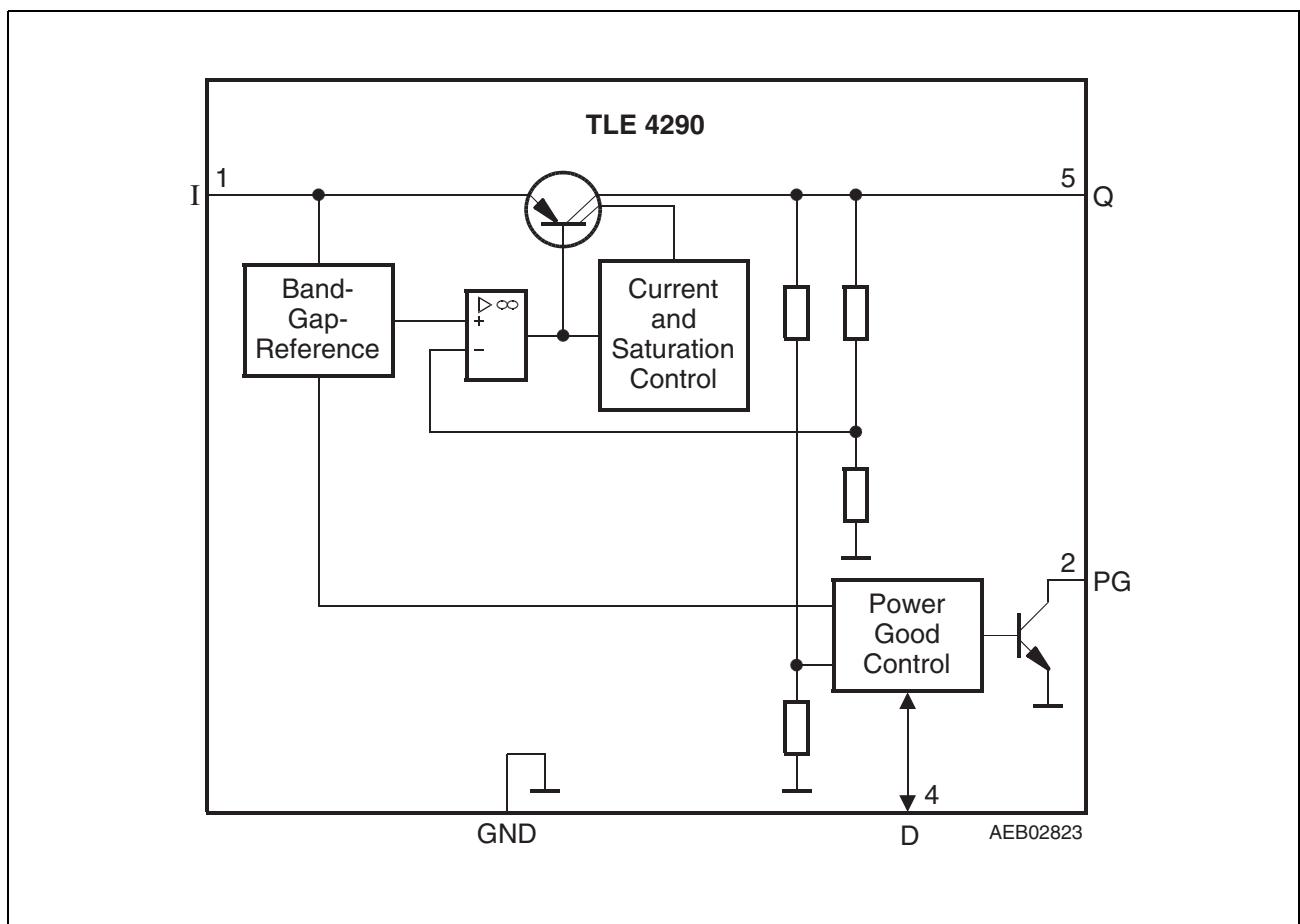
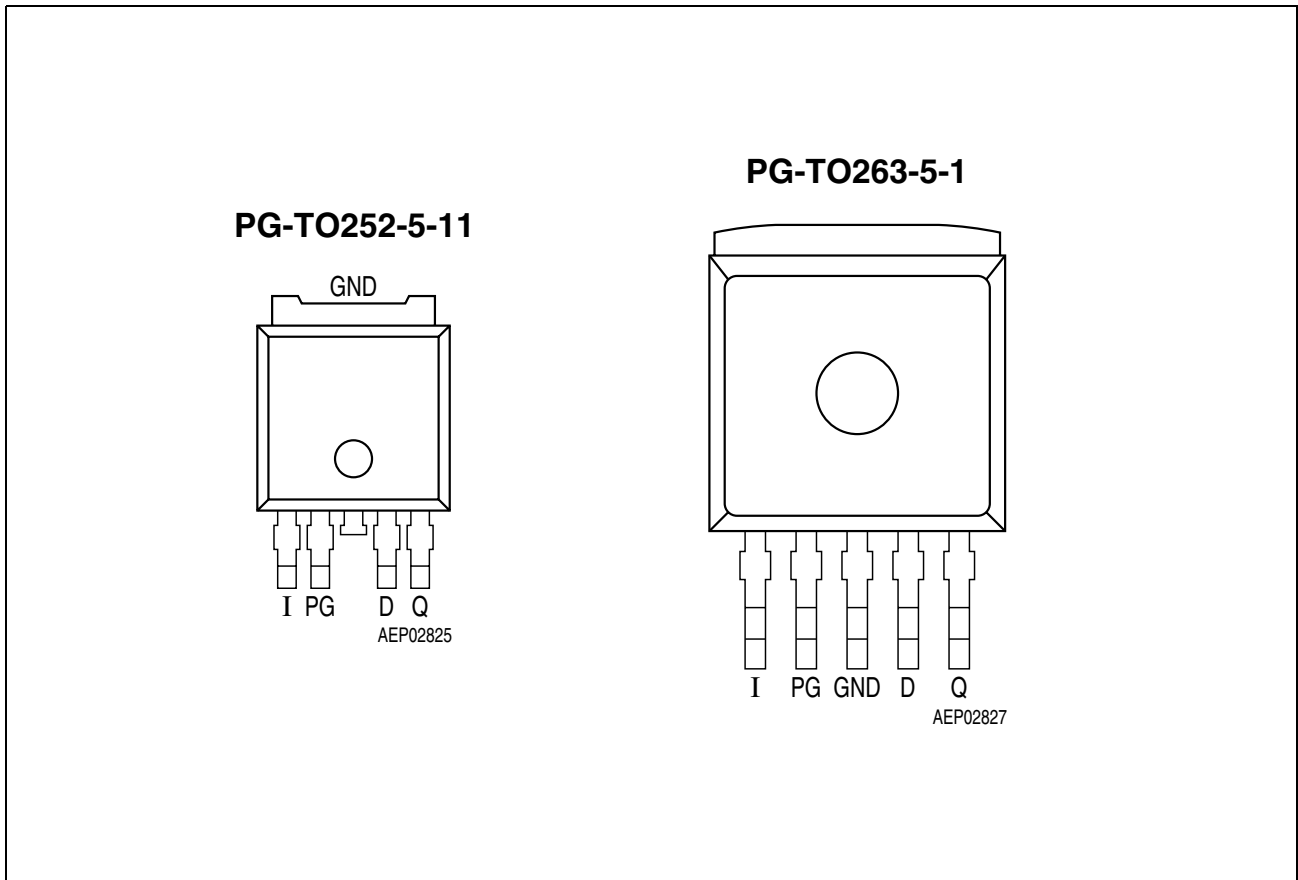


Figure 1 Block Diagram



**Figure 2** Pin Configuration (top view)

**Table 1** Pin Definitions and Functions

Pin No.	Symbol	Function
1	I	<b>Input;</b> block to ground directly at the IC with a ceramic capacitor.
2	PG	<b>Power Good;</b> open collector output. Add a pull-up resistor of > 5 kΩ to pin Q.
3	GND	<b>Ground;</b> Pin 3 internally connected to heatsink.
4	D	<b>Delay;</b> connect a capacitor to GND for setting power good delay time.
5	Q	<b>Output;</b> block to ground with a capacitor, $C \geq 22 \mu\text{F}$ ESR < 5 Ω at 10 kHz.

**Table 2 Absolute Maximum Ratings**

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
<b>Input I</b>					
Voltage	$V_I$	-42	45	V	–
Current	$I_I$	–	–	–	Internally limited
<b>Output Q</b>					
Voltage	$V_Q$	-1.0	16	V	–
Current	$I_Q$	–	–	–	Internally limited
<b>Power Good Output PG</b>					
Voltage	$V_{PG}$	-0.3	25	V	–
Current	$I_{PG}$	-5	5	mA	–
<b>Delay D</b>					
Voltage	$V_D$	-0.3	7	V	–
Current	$I_D$	-2	2	mA	–
<b>Temperature</b>					
Junction temperature	$T_j$	-40	150	°C	–
Storage temperature	$T_{stg}$	-50	150	°C	–

*Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**Table 3 Operating Range**

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input voltage	$V_I$	5.5	42	V	–
Junction temperature	$T_j$	-40	150	°C	–

**Thermal Resistance**

Junction case	$R_{thj-c}$	–	4	K/W	–
Junction ambient	$R_{thj-a}$	–	53	K/W	TO263 <sup>1)</sup>
Junction ambient	$R_{thj-a}$	–	78	K/W	TO252 <sup>1)</sup>

1) Worst case, regarding peak temperature; zero airflow; mounted on a PCB FR4, 80 × 80 × 1.5 mm<sup>3</sup>, heat sink area 300 mm<sup>2</sup>

*Note: In the operating range, the functions given in the circuit description are fulfilled.*

**Table 4 Characteristics**
 $V_I = 13.5 \text{ V}; -40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$  (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		Min.	Typ.	Max.		
<b>Output</b>						
Output voltage	$V_Q$	4.9	5.0	5.1	V	$5 \text{ mA} < I_Q < 400 \text{ mA};$ $6 \text{ V} < V_I < 28 \text{ V}$
Output voltage	$V_Q$	4.9	5.0	5.1	V	$5 \text{ mA} < I_Q < 200 \text{ mA};$ $6 \text{ V} < V_I < 40 \text{ V}$
Output current limitation	$I_Q$	450	700	–	mA	1)
Current consumption; $I_q = I_I - I_Q$	$I_q$	–	200	230	$\mu\text{A}$	$I_Q = 1 \text{ mA};$ $T_j = 25 \text{ }^\circ\text{C}$
Current consumption; $I_q = I_I - I_Q$	$I_q$	–	200	255	$\mu\text{A}$	$I_Q = 1 \text{ mA};$ $T_j \leq 85 \text{ }^\circ\text{C}$
Current consumption; $I_q = I_I - I_Q$	$I_q$	–	5	12	mA	$I_Q = 250 \text{ mA}$
Current consumption; $I_q = I_I - I_Q$	$I_q$	–	12	25	mA	$I_Q = 400 \text{ mA}$
Drop voltage	$V_{dr}$	–	250	500	mV	$I_Q = 300 \text{ mA}$ $V_{dr} = V_I - V_Q$ 1)
Load regulation	$\Delta V_{Q,lo}$	-30	15	30	mV	$V_I = 6 \text{ V};$ $I_Q = 5 \text{ mA to } 400 \text{ mA}$
Line regulation	$\Delta V_{Q,li}$	-15	5	15	mV	$V_I = 8 \text{ V to } 32 \text{ V};$ $I_Q = 5 \text{ mA}$
Power supply ripple rejection	$PSRR$	–	60	–	dB	$f_r = 100 \text{ Hz};$ $V_r = 0.5 \text{ Vpp}$
Temperature output voltage drift	$dV_Q/dT$	–	0.5	–	mV/K	–
Output Capacitor	$C_Q$	22	–	–	$\mu\text{F}$	ESR < 5 $\Omega$ in the operation range

**Power Good Output PG and Delay Timing D**

Power Good switching threshold	$V_{Q,pgt-i}$	4.45	4.65	4.80	V	$V_Q$ increasing
Power Good switching threshold	$V_{Q,pgt-d}$	3.50	3.65	3.80	V	$V_Q$ decreasing

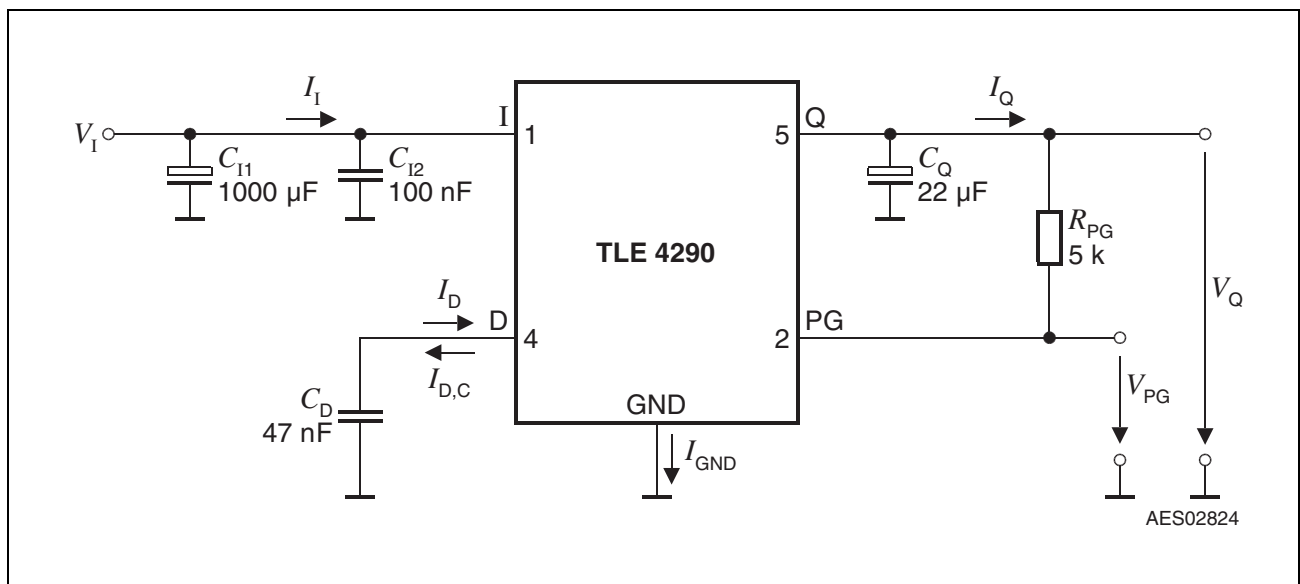
**Table 4 Characteristics (cont'd)**

$V_1 = 13.5\text{ V}$ ;  $-40\text{ }^\circ\text{C} < T_j < 150\text{ }^\circ\text{C}$  (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		Min.	Typ.	Max.		
Power Good output low voltage	$V_{PGL}$	–	0.2	0.4	V	$R_{PG} \geq 5\text{ k}\Omega$ ; $V_Q > 1\text{ V}$
Power Good output leakage current	$I_{PGH}$	–	0	2	$\mu\text{A}$	$V_{PG} > 4.5\text{ V}$
Power Good charging current	$I_{D,c}$	3	6	9	$\mu\text{A}$	$V_D = 1\text{ V}$
Upper timing threshold	$V_{DU}$	1.5	1.8	2.2	V	–
Lower timing threshold	$V_{DL}$	0.60	0.85	1.10	V	–
Power Good delay time	$t_{rd}$	10	16	22	ms	$C_D = 47\text{ nF}$
Power Good reaction time	$t_{rr}$	0.2	0.5	2.0	$\mu\text{s}$	$C_D = 47\text{ nF}$

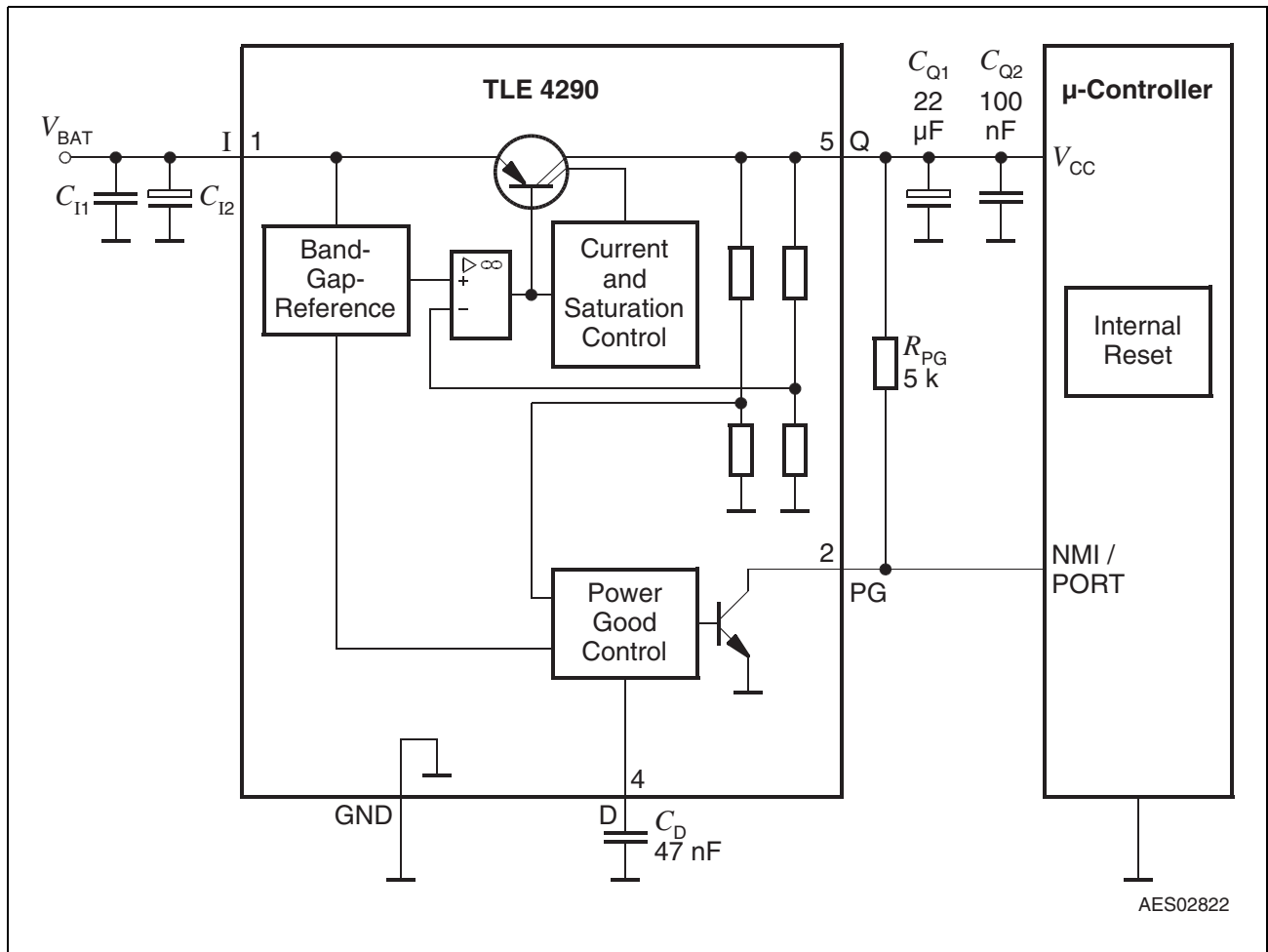
1) Measured when the output voltage  $V_Q$  has dropped 100 mV from the nominal value obtained at  $V_1 = 13.5\text{ V}$ .

*Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_a = 25\text{ }^\circ\text{C}$  and the given supply voltage.*



**Figure 3 Test Circuit**

### Application Information



**Figure 4 Application Diagram**

#### Input, Output

An input capacitor is necessary for damping line influences. A resistor of approx. 1  $\Omega$  in series with  $C_I$ , can damp the LC of the input inductivity and the input capacitor.

The TLE 4290 requires an output capacitor of at least 22  $\mu$ F with an ESR below 5  $\Omega$  for stability.

#### Power Good

The Power Good pin informs e.g. the micro-controller in case the output voltage has fallen below a threshold of typ. 3.65 V. When the battery voltage is supplied the Power Good signal indicates a loss of memory due to missing power. After the Memory Good switching threshold is reached the Power Good output remains low for the Power Good delay time. This time can be set by the user with an external capacitor at pin D according to the requirements of the application, e.g. the time until the microcontroller is initialized and ready to receive any information.



The power good circuit supervises the output voltage. In case  $V_Q$  falls below the Power Good switching threshold the Power Good output PG is set LOW after the power good reaction time. The power good LOW signal is generated down to an output voltage  $V_Q$  to 1 V. A LOW signal at the power good pin informs that the battery was lost and memory is no longer valid.

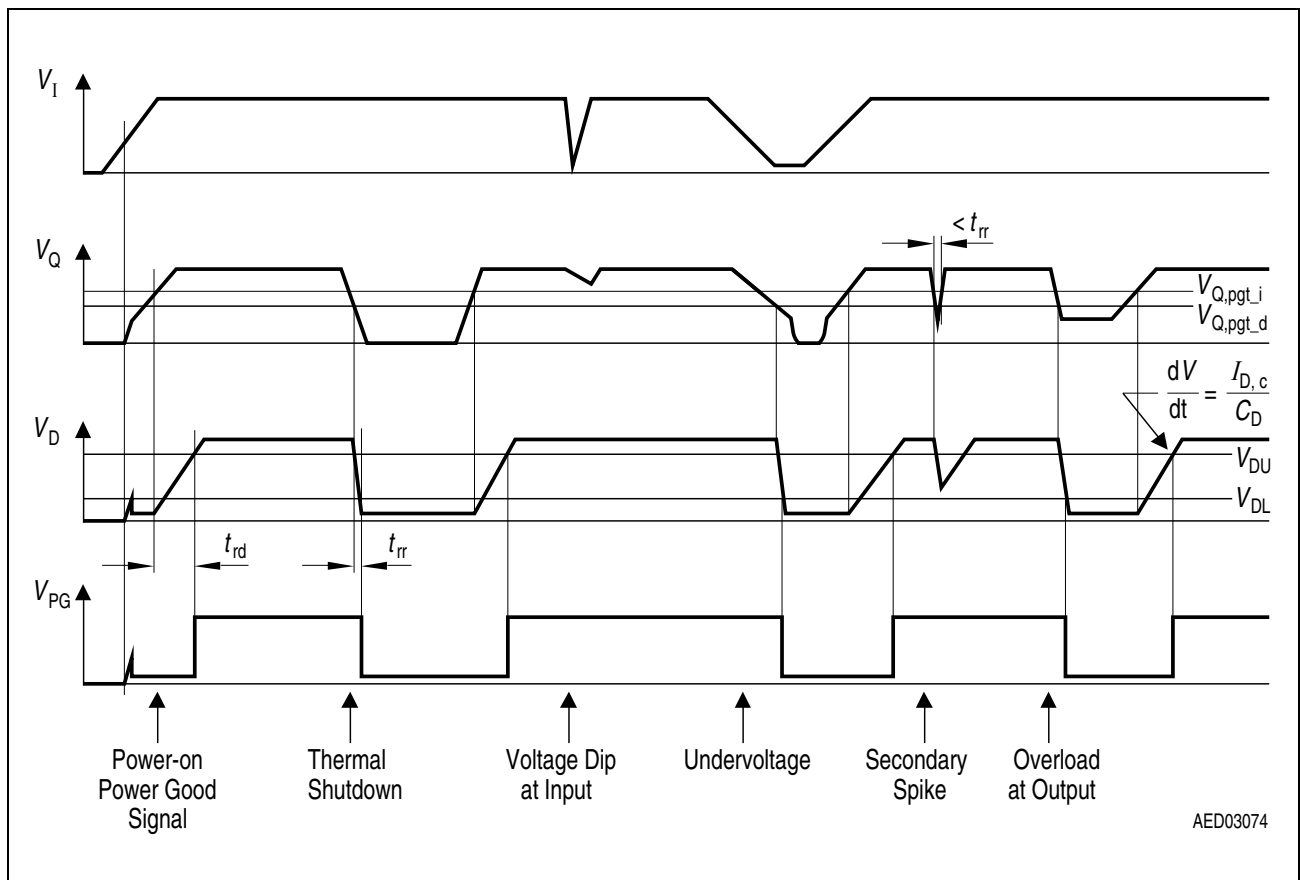
The feature should only be used in combination to a microcontroller with internal reset. For the power good delay time after the output voltage of the regulator is above the reset threshold, the reset signal is set High again. The reset delay time is defined by the reset delay capacitor  $C_D$  at pin D.

The Power Good delay time is defined by the charging time of an external delay capacitor  $C_D$ .

$$C_D = (t_{rd} \times I_{D,c}) / \Delta V \tag{1}$$

With:

- $C_D$  = Power Good delay capacitor
- $t_{rd}$  = Power Good delay time
- $\Delta V = V_{DU}$ , typical 1.8 V
- $I_{D,c}$  = Charge current typical 6  $\mu A$



**Figure 5 Power Good Timing**

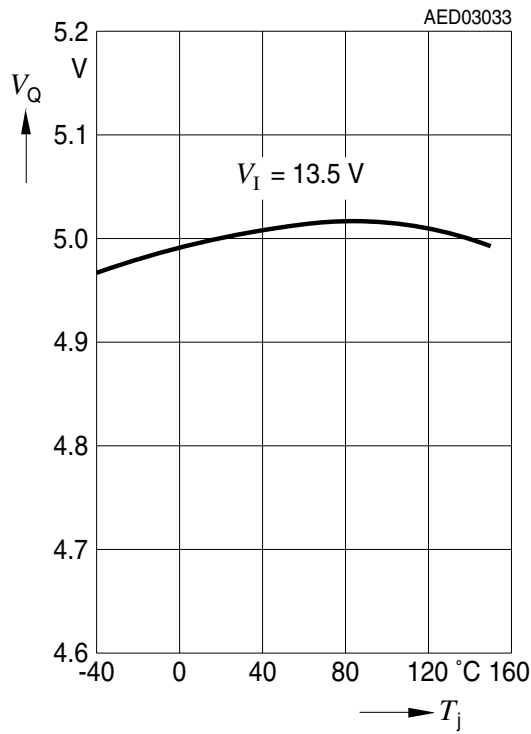
The power good reaction time  $t_{rr}$  is the time it takes the voltage regulator to set power good output PG LOW after the output voltage has dropped below the power good switching threshold. It is typically 0.5  $\mu$ s for delay capacitor of 47 nF. For other values for  $C_D$  the reaction time can be estimated using the following equation:

$$t_{rr} = 10 \text{ ns/nF} \times C_D \quad (2)$$

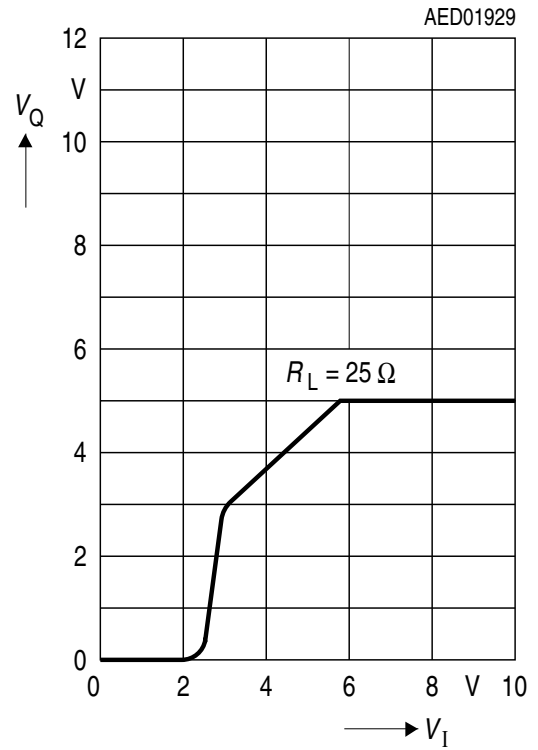
The Power Good output is an open collector output. It requires externally a pull-up resistor of at least 5 k $\Omega$  to Q.

Typical Performance Characteristics

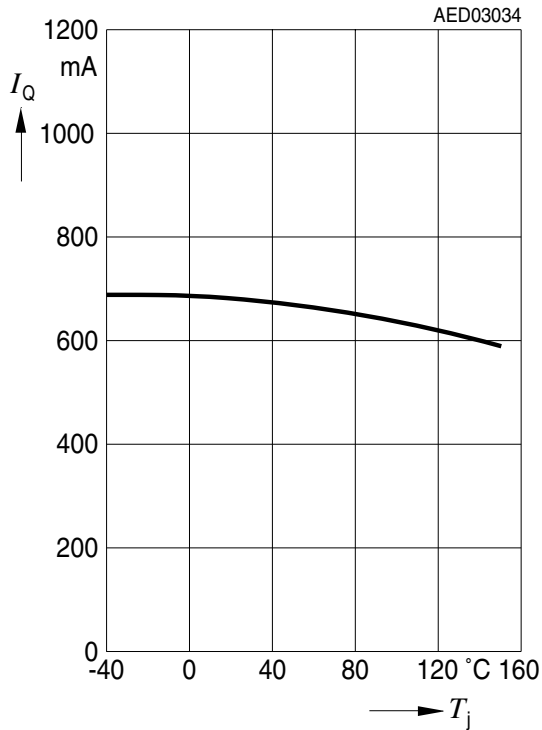
Output Voltage  $V_Q$  versus Temperature  $T_j$



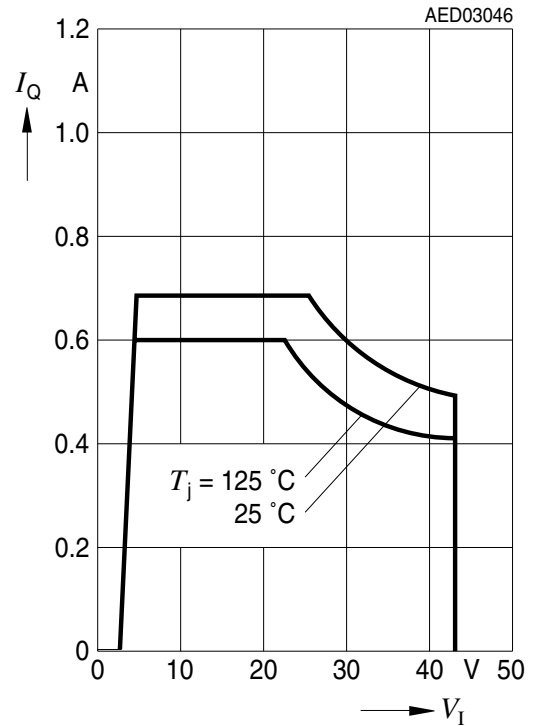
Output Voltage  $V_Q$  versus Input Voltage  $V_I$



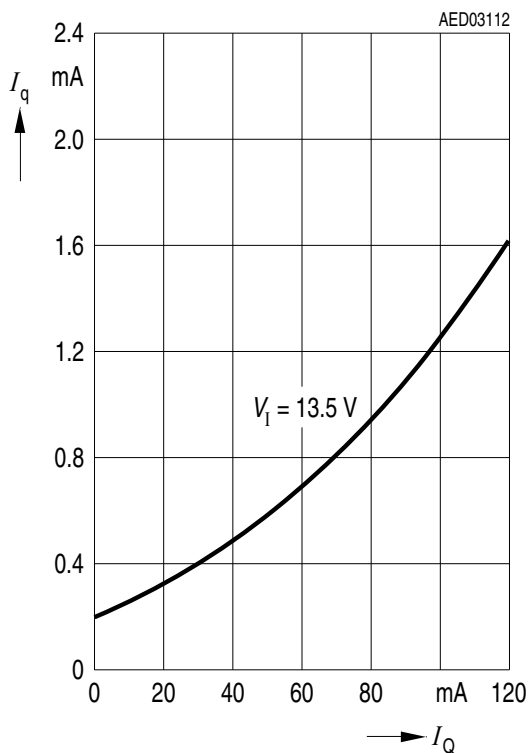
**Output Current  $I_Q$  versus Temperature  $T_j$**



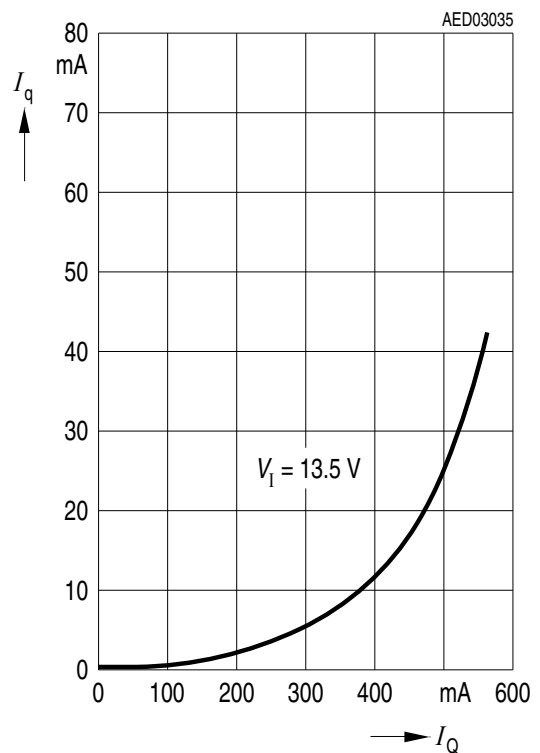
**Output Current  $I_Q$  versus Input Voltage  $V_I$**



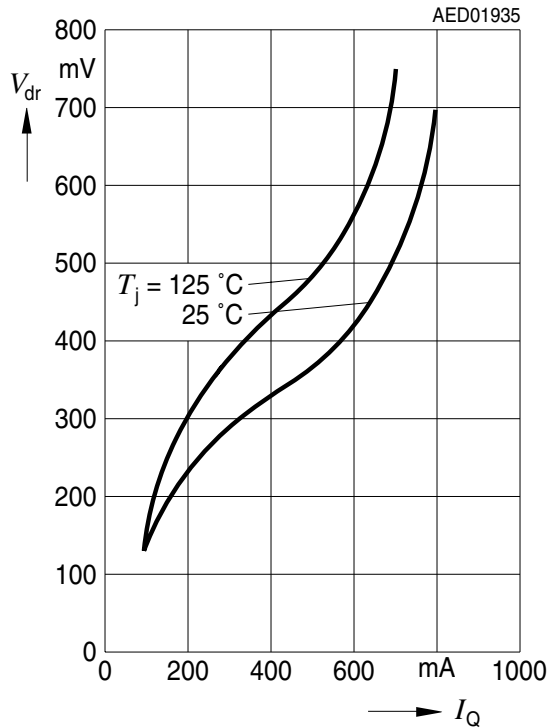
**Current Consumption  $I_q$  versus Output Current  $I_Q$ ;  $T_j = 25$  °C**



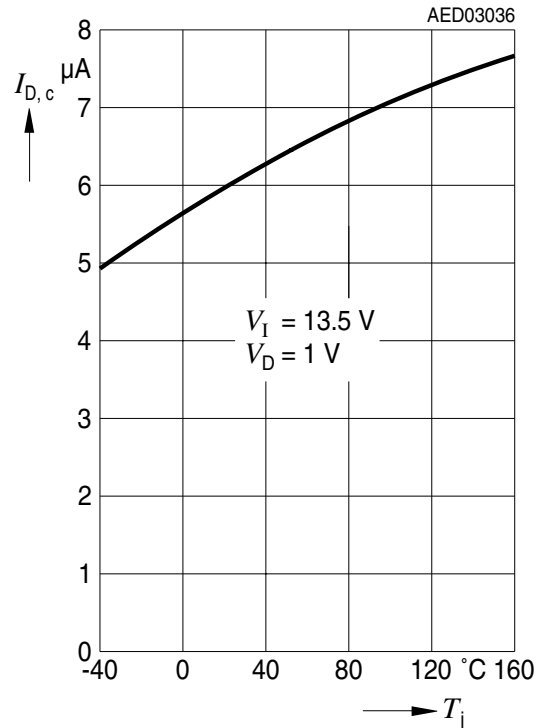
**Current Consumption  $I_q$  versus Output Current  $I_Q$**



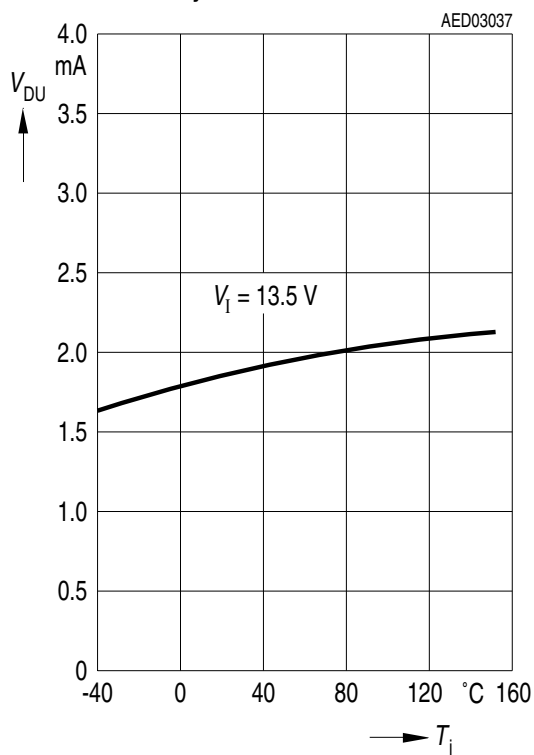
**Drop Voltage  $V_{dr}$  versus Output Current  $I_Q$**



**Charge Current  $I_{D,c}$  versus Temperature  $T_j$**



**Upper Timing Threshold  $V_{DU}$  versus Temperature  $T_j$**



Package Outlines

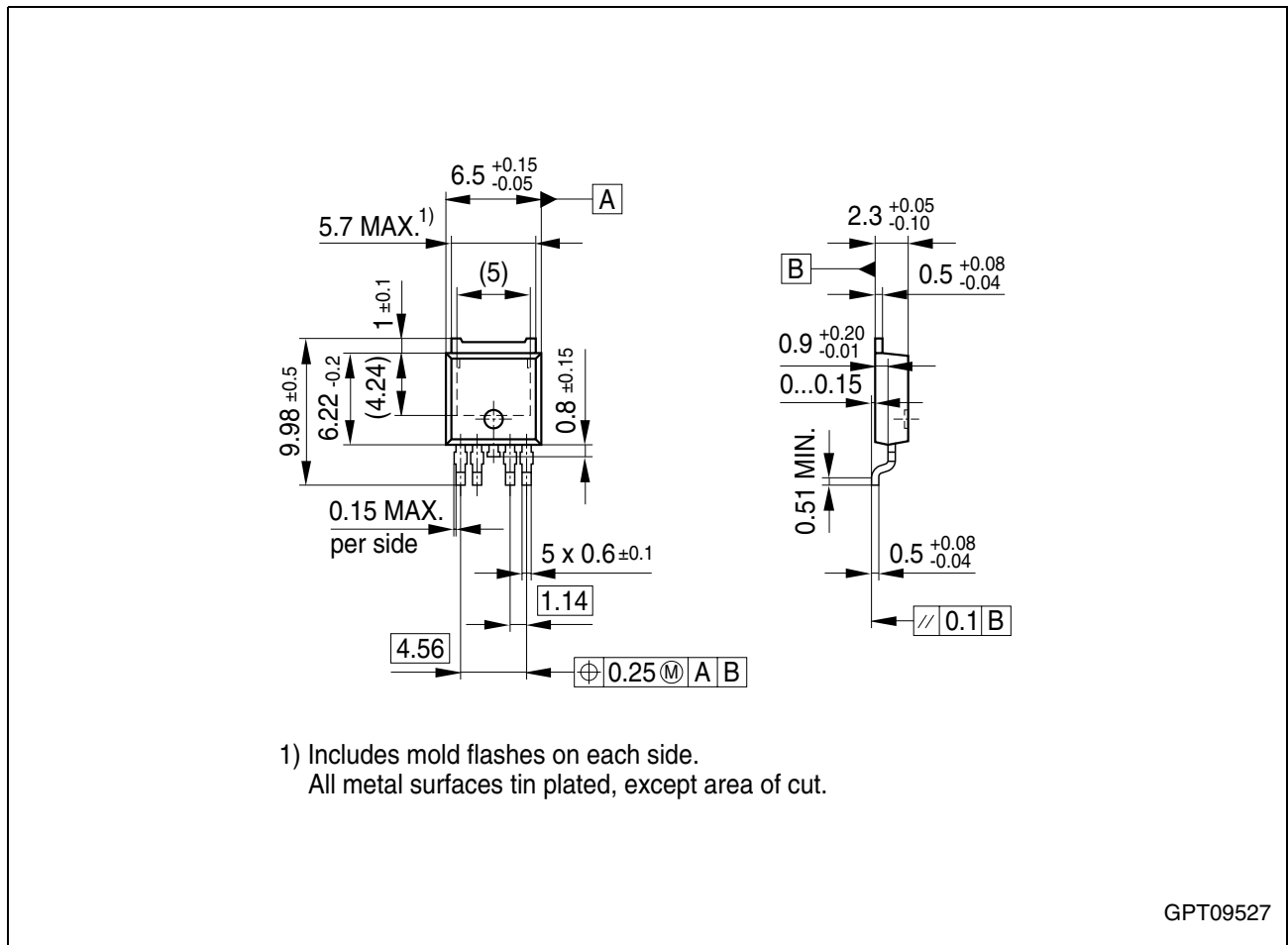


Figure 6 PG-TO252-5-11 (Plastic Transistor Single Outline)

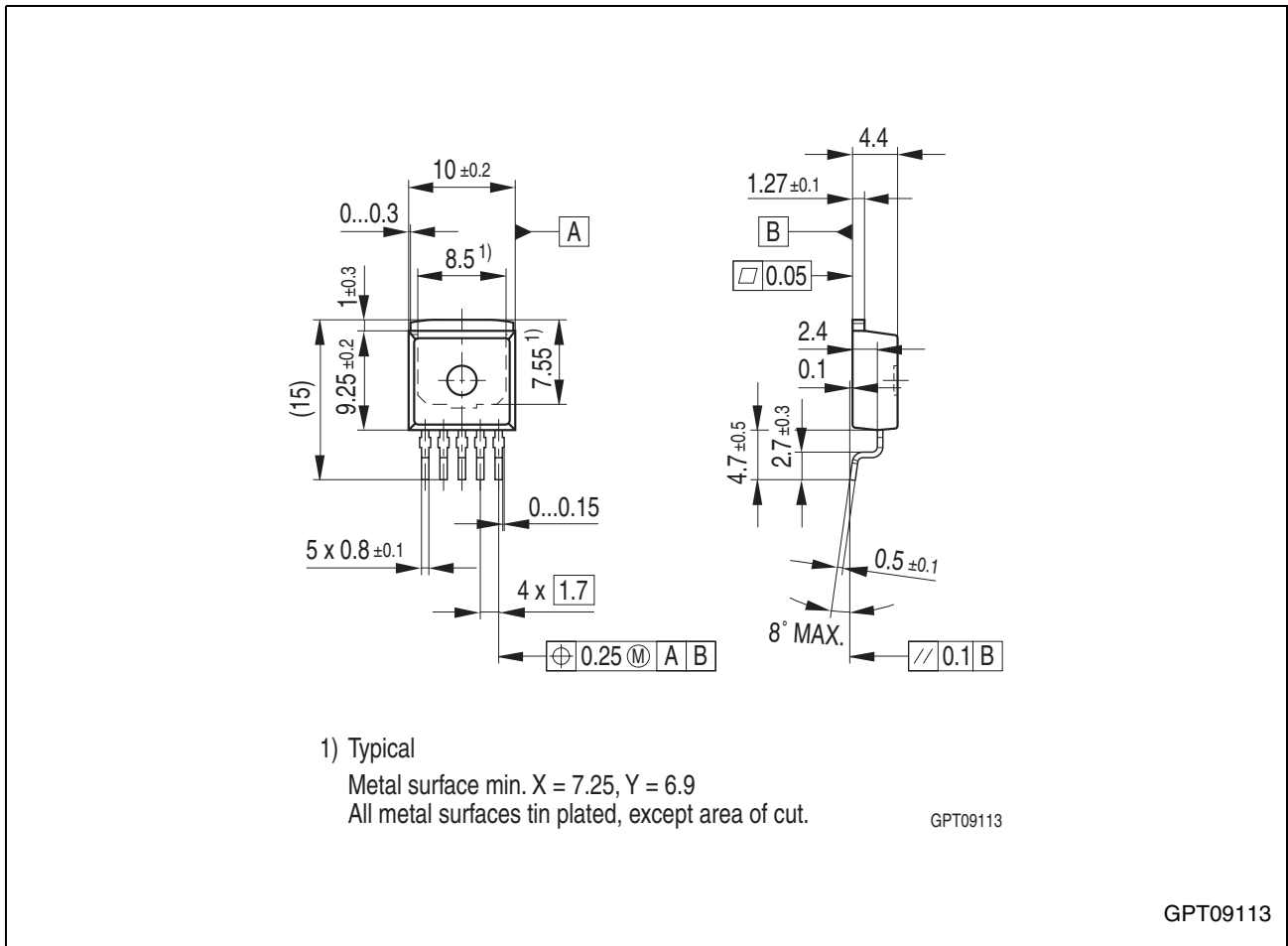
Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

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SMD = Surface Mounted Device

Dimensions in mm



**Figure 7 PG-TO263-5-1 (Plastic Transistor Single Outline)**

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SMD = Surface Mounted Device

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**Revision History**

<b>Version</b>	<b>Date</b>	<b>Changes</b>
Rev. 1.7	2007-03-20	Initial version of RoHS-compliant derivate of TLE 4290 <b>Page 1</b> : AEC certified statement added <b>Page 1</b> and <b>Page 14</b> : RoHS compliance statement and Green product feature added <b>Page 1</b> and <b>Page 14</b> : Package changed to RoHS compliant version Legal Disclaimer updated



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