TLE 8108 EM

Smart 8-Channel Low Side Relay Driver with SPI Interface

coreFLEX TLE8108EM

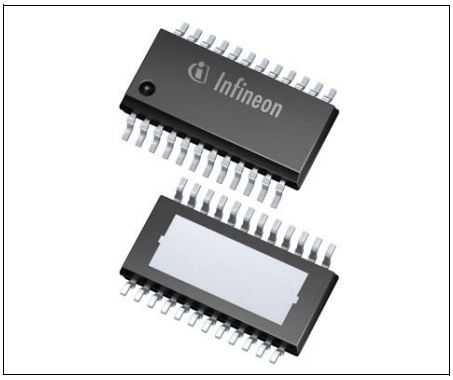
Data Sheet

Rev. 1.0, 2011-03-23

Automotive Power

Table of Contents

1 Overview



PG-SSOP-24

Features

- 4 input pins providing flexible PWM configuration
- Active Clamping
- Low Power Consumption Mode (Standby)
- 16 bit SPI for diagnostics and control
- Daisy chain capability also compatible with 8bit SPI devices
- Green product (RoHS compliant)
- AEC qualified

Description

The TLE8108EM is an 8-Channel Low Side Switch in PG-SSOP-24 package providing embedded protective functions.

It is especially designed as relay driver for powertrain automotive applications.

A serial peripheral interface (SPI) is implemented for control and diagnosis of the device and the load.

Four configurable direct inputs are available to control the outputs in PWM.

The device is monolithically integrated. The internal switches are power n-MOSFETs.

Table 1 Basic Electrical Data

Supply voltage	V_{DD}	4.5V ... 5.5V
Max. ON State resistance at T_j = 150°C for each channel	$R_{DS(ON,max)}$	1.7Ω
Continuos load current	$I_{L\ (cont)}$	400mA
Overload switch off threshold	$I_{D\ (OVL,min)}$	500mA
Output leakage current per channel	$I_{D\ (STB,max)}$	5µA
Minimal drain to source clamping voltage	$V_{DS(CL)}$	41V
Maximum SPI clock frequency	$f_{SCLK,max}$	5MHz

Type	Package	Marking
TLE8108EM	PG-SSOP-24	

Diagnostic Feedback Information

- Latched diagnostic information via SPI register
- Overtemperature detection (DOT)
- Overload detection corresponding Short Circuit to Battery (SCB) in ON state.
- Open load detection in OFF state (OL)
- Short Circuit to GND detection in OFF state (SCG)

Protection Functions

- Overload switch off
- Overtemperature switch off
- Electrostatic discharge (ESD)

Application

- Resistive, inductive and capacitive loads
- Especially designed for driving relays in automotive applications

General Information

The TLE8108EM is an 8-Channel Low Side Relay Switch designed for typical automotive relays, providing embedded protective functions. The PG-SSOP-24 package is used to get a footprint optimized solution. The 16 bit serial peripheral interface (SPI) is utilized for control and diagnosis of the device and the loads. The SPI interface provides daisy chain capability.

The TLE8108EM is equipped with 4 input pins that can be used to directly control their dedicated channels thus offering flexibility in design and PCB layout. The input multiplexer is controlled via SPI.

The device provides full diagnosis of the load, which is open load, short circuit to ground, as well as a short circuit to battery detection. The SPI diagnosis bits indicate latched fault conditions that may have occurred.

Each output stage is protected against short circuit. In case of Overload, the affected channel switches off. There are temperature sensors for each channel to protect the device in case of Overtemperature.

The device is supplied by a single power supply. It is operating at 5V nominal value.

The internal switches are power n-MOSFETs. The inputs are ground referenced CMOS compatible. The device is monolithically integrated in Smart Power Technology.

All output pins are available at one side of the device while the other side bundles the signals to the microcontroller, thus facilitating the PCB layout.

It is possible to set each channel in a Clear Mode (CLR) in order to clear Diagnosis flags; in CLR state output is switched off and diagnosis currents are disabled.

A Standby mode of the Device (STB) can be entered if all the channels are set into CLR state; in STB mode the power consumpiton is reduced to the minimum.

2 Block Diagram

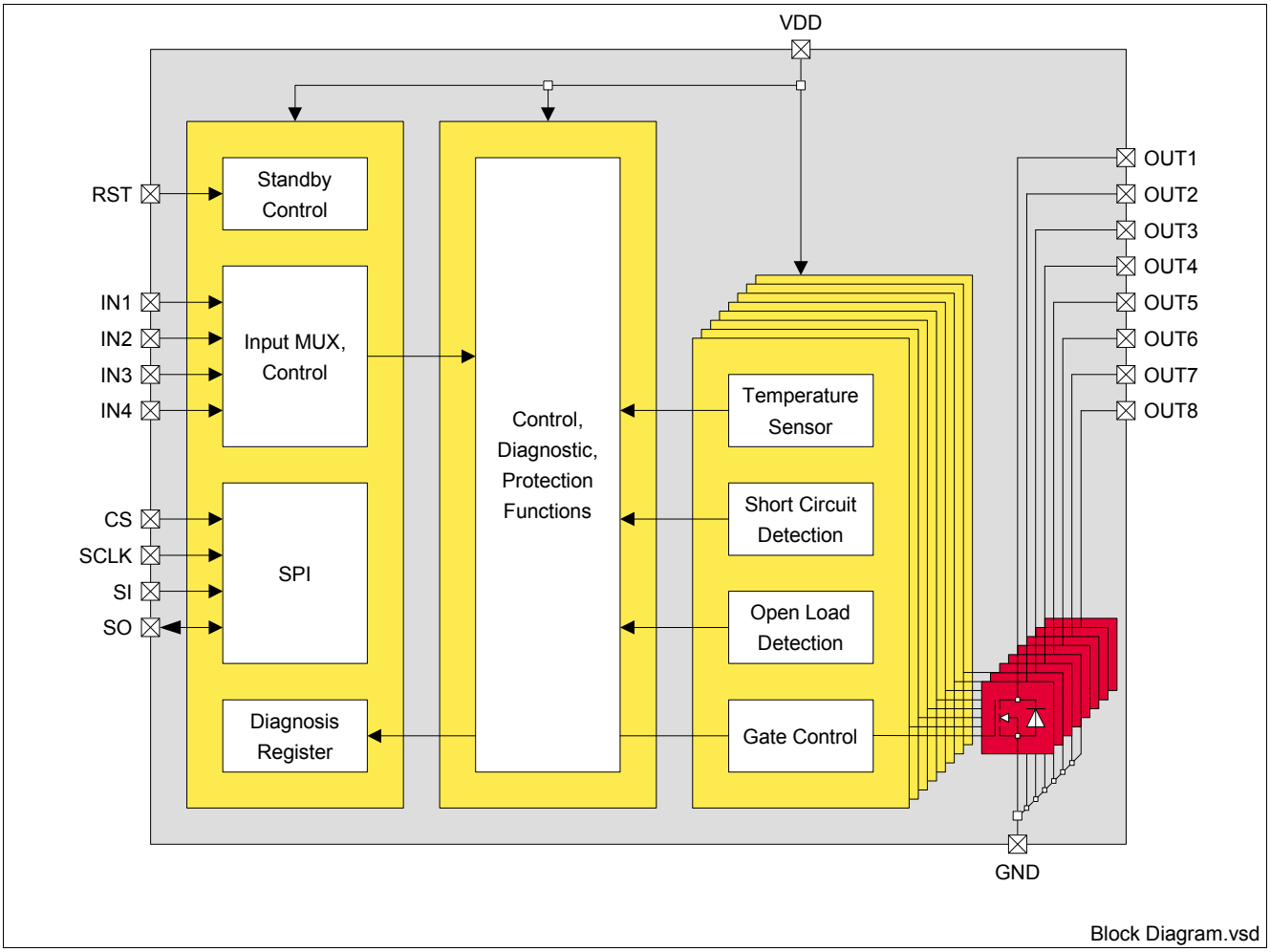


Figure 1 Block Diagram for the TLE8108EM

3 Pin Configuration

3.1 Pin Assignment

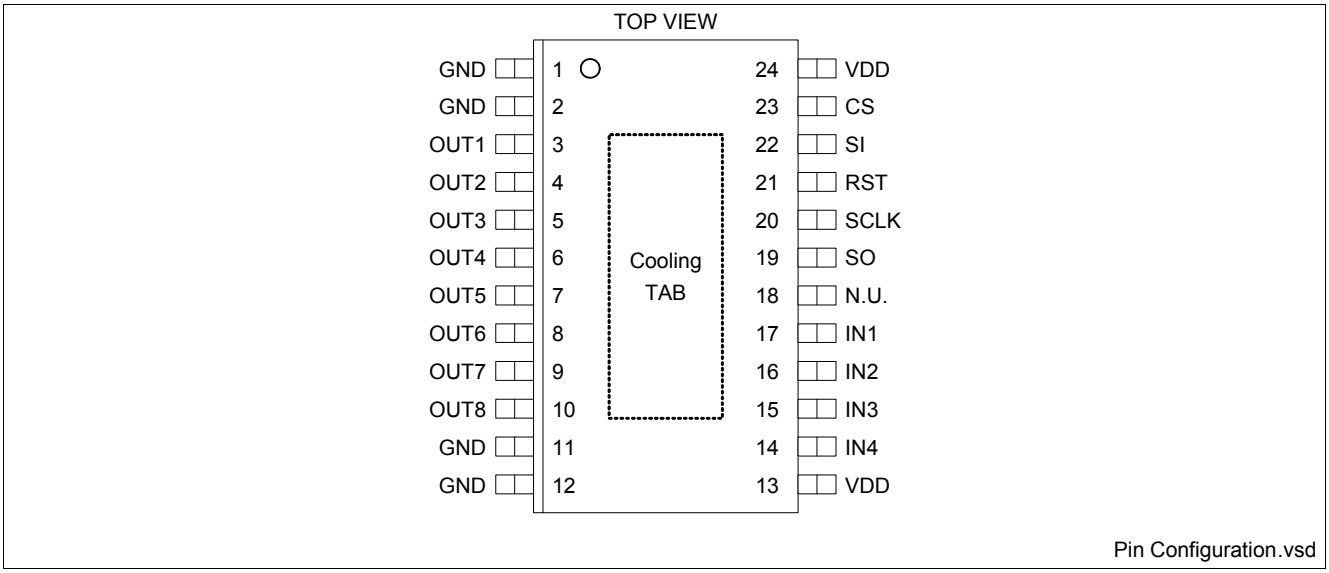


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	I/O [1]		Function
Power Supply				
13,24	VDD	-		Supply voltage; Connected to 5V voltage with reverse protection diode and filter against EMC; Both pins must be connected to the supply without parasitic resistors
1,2,11,12	GND	-		Ground; common ground for digital, analog and power; Pins must be connected together without parasitic resistors
Cooling TAB	GND	-		Cooling TAB (bottom side); Internally connected to ground; Pin must be connected externally to ground without parasitic resistors
Power Stages				
3	OUT1	O		Output channel 1; Drain of power transistor channel 1
4	OUT2	O		Output channel 2; Drain of power transistor channel 2
5	OUT3	O		Output channel 3; Drain of power transistor channel 3
6	OUT4	O		Output channel 4; Drain of power transistor channel 4
7	OUT5	O		Output channel 5; Drain of power transistor channel 5
8	OUT6	O		Output channel 6; Drain of power transistor channel 6
9	OUT7	O		Output channel 7; Drain of power transistor channel 7
10	OUT8	O		Output channel 8; Drain of power transistor channel 8
Inputs				
17	IN1	I	PD	Active Low; Control input; Digital input 3.3V or 5V; If not used, pin must be connected to GND

Pin	Symbol	I/O [1]		Function
16	IN2	I	PD	Active Low; Control input; Digital input 3.3V or 5V; If not used, pin must be connected to GND
15	IN3	I	PD	Active Low; Control input; Digital input 3.3V or 5V; If not used, pin must be connected to GND
14	IN4	I	PD	Active Low; Control input; Digital input 3.3V or 5V; If not used, pin must be connected to GND
18	N.C.	I	PD	Not Connected; pin must be tied to GND
21	RST	I	PD	Active Low; Reset input pin; Digital input 3.3V or 5V
SPI				
23	CS	I	PU	Active Low; SPI chip select; Digital input 3.3V or 5V
20	SCLK	I	PD	Active Low; Serial clock; Digital input 3.3V or 5V
22	SI	I	PD	Active Low; Serial data in; Digital input 3.3V or 5V.
19	SO	O[2]		Serial data out; Digital output with voltage level referring to VDD

1) O=Output;
I=Input;
PD=integrated pull-down resistor;
PU=integrated pull-up resistor

2) SO is set to tristate if SPI is inactive (CS is high or RST is low)

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

Unless otherwise specified: T_j = -40°C to +150°C; V_{DD} = 4.5V to 5.5V

All voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Power Supply						
4.1.1	Supply voltage	V_{DD}	-0.3	5.5	V	-
4.1.2	Output voltage for short circuit protection (single pulse)	V_{DS_SC}	0	36	V	-
Power Stages						
4.1.3	Load current	I_D	-0.5	0.5	A	-
4.1.4	Voltage at power transistor	V_{DS}	-0.3	41	V	Active Clamped
Clamping Energy - Singel Pulse [2)]						
4.1.5	Single Clamping Energy per Channel	E_{AS}	-	20	mJ	I_D = 0.18A 1 Single Pulse
Logic Pins						
4.1.6	IN1 to IN4; Voltage at input pins	V_{IN}	-0.3	V_{DD} + 0.3	V	3)
4.1.7	RST; Voltage at reset pin	V_{RST}	-0.3	V_{DD} + 0.3	V	3)
4.1.8	CS; Voltage at chip select	V_{CS}	-0.3	V_{DD} + 0.3	V	3)
4.1.9	SCLK; Voltage at serial clock pin	V_{SCLK}	-0.3	V_{DD} + 0.3	V	3)
4.1.10	SI; Voltage at serial input pin	V_{SI}	-0.3	V_{DD} + 0.3	V	3)
4.1.11	SO; Voltage at serial output pin	V_{SO}	-0.3	V_{DD} + 0.3	V	3)
Temperatures						
4.1.12	Junction Temperature	T_j	-40	150	°C	-
4.1.13	Junction Temperature	T_j	-40	165	°C	Dynamic Conditions, 100h max total
4.1.14	Storage Temperature	T_{stg}	-55	150	°C	-
ESD Susceptibility						
4.1.15	ESD Resistivity	V_{ESD}	-4	4	kV	HBM[4)]

1) Not subject to production test, specified by design.

2) Triangular Pulse Shape (Inductance Discharge): $I_D(t) = I_D(0) \times (1 - t / t_{pulse})$; $0 < t < t_{pulse}$.

3) Level must not exceed V_{DD}+0.3V < 5.5V

4) ESD susceptibility, HBM according to EIA/JESD 22-A114-F

Note: Stress above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

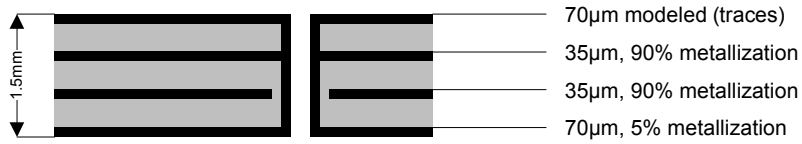
4.2 Thermal Resistance

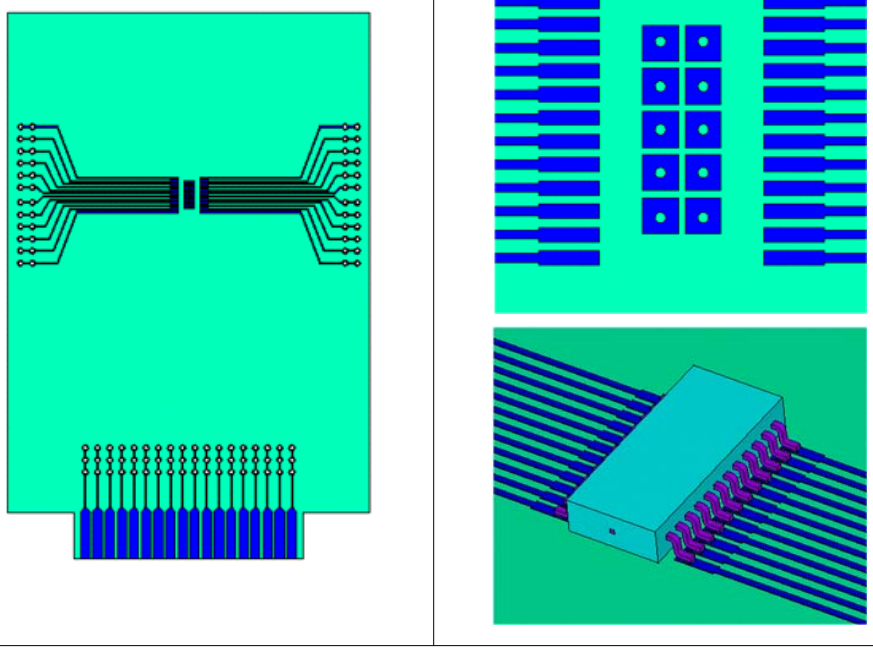
Note: This thermal data was generated in accordance with JEDEC JESD51 standards.
*For more information go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.2.1	Junction to Case	R_{thJC}	-	-	7	K/W	P_{TOT} = 1W 1) 2) 3)
4.2.2	Junction to Ambient (2s2p)	R_{thJA}	-	40	-	K/W	P_{TOT} = 1W 1) 2) 3)

1) Not subject to production test, specified by design.
2) Homogenous power distrubution over all channels (all power stages equally heated), dependent on cooling setup.
3) Refer to **Figure 3** for the setup.

Dimensions:	76.2 x 114.3 x 1.5 mm³ , FR4
Metallization:	JEDEC 2s2p (JESD 51-7) + (JESD 51-5)
Thermal Vias:	F =0.3mm; plating 25µm; 10 pcs. for PG-SSOP-24





Rth PCB setup.vsd

Figure 3 PG-SSOP-24 PCB setup

5 Electrical and functional Description of the Device

The TLE8108EM is a 8-Channel Low Side Relay Switch.

The power stages are composed of n-MOSFET transistors.

5.1 Functional Description of Supply and Input Pins

5.1.1 Power Supply and Reset

The TLE8108EM is supplied by a single power supply line V_{DD} with two input pins which must be connected together. After power supply start-up, the input registers of the device are programmed to OFF mode for all channels. The output registers must be reset to their default values by programming the Clear mode for all channels once.

Capacitors at the supply pins V_{DD} to GND are recommended.

There is a reset pin available. Low level at this pin causes all registers to be set to their default values and the quiescent supply currents are minimized. This is also true for the Standby Mode in case all channels are programmed to Clear. **Figure 4** shows the timing requirements for the RST pin to be enabled and for the device to wake up.

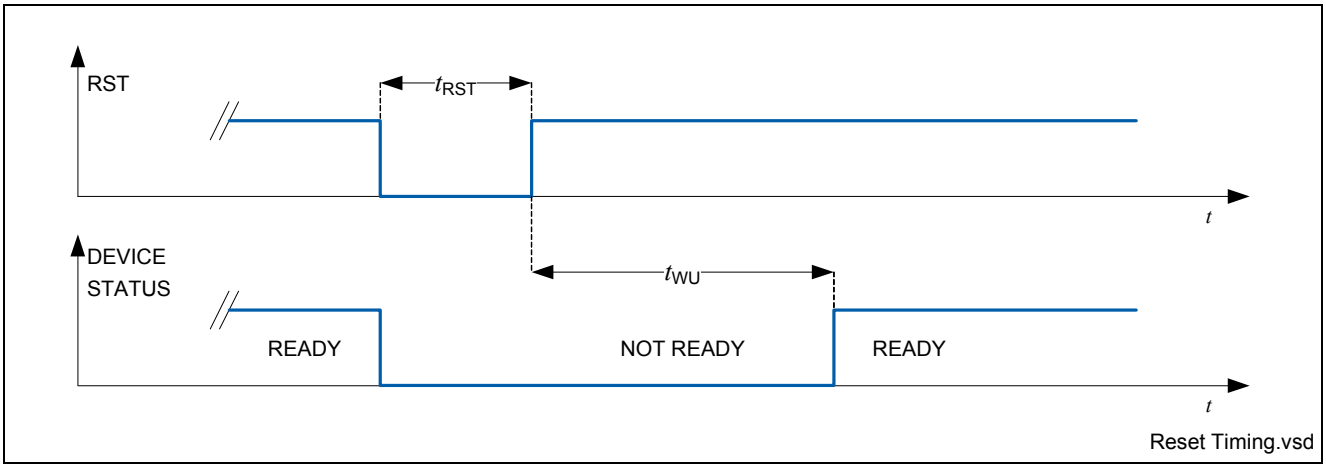


Figure 4 Reset Timings

5.1.2 Switching Inputs IN1 to IN4

There are four input pins available at TLE8108EM, which can be configured to be used for control of the output stages. The SPI INn parameter selects the input pin to be used. **Figure 5** shows the input circuit of TLE8108EM.

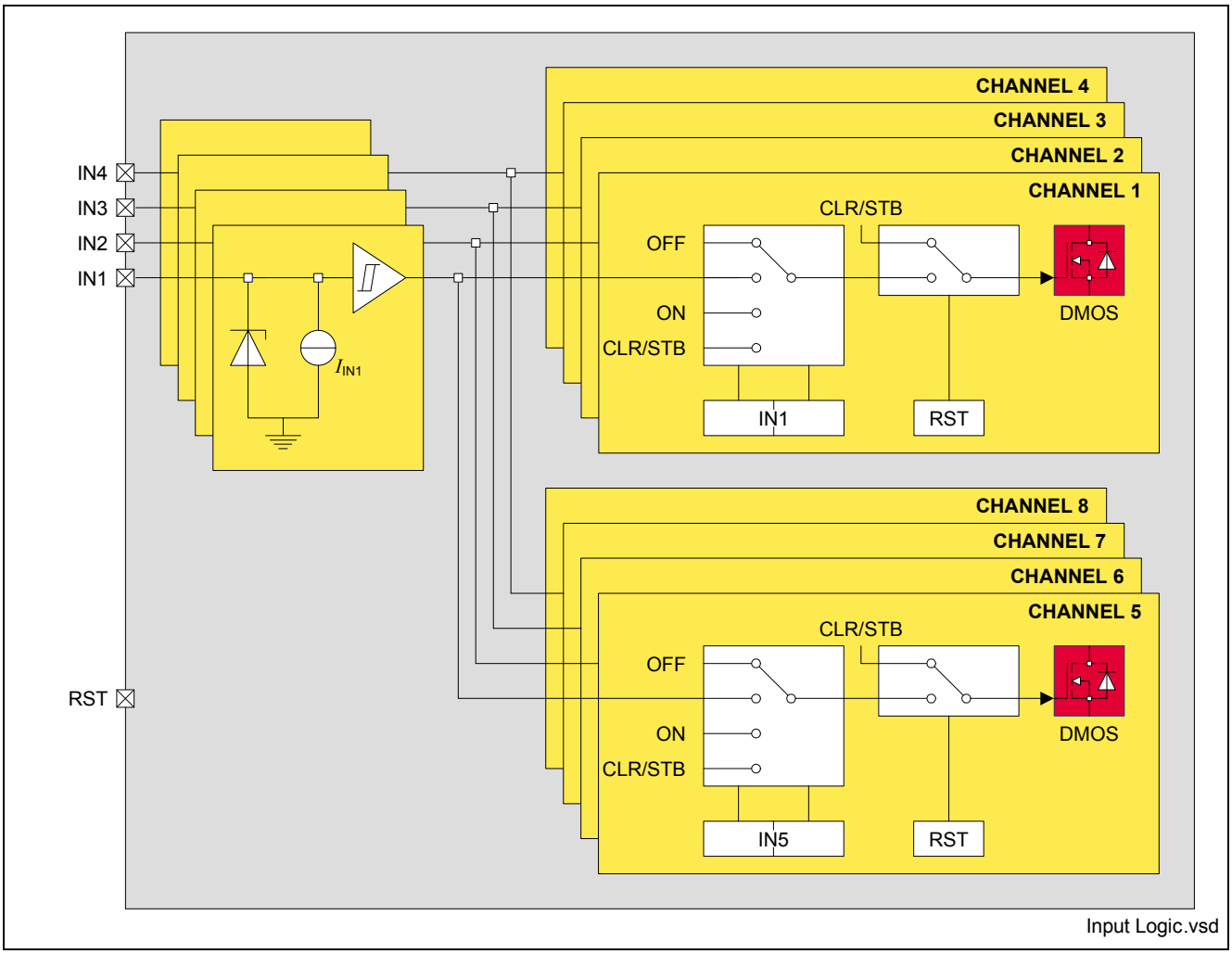


Figure 5 Input Matrix and Logic

The current sink to ground ensures that the channels switch off in case of an open input pin. The zener diode protects the input circuit against ESD pulses. After power-on reset or after an external reset the device enters the OFF mode for all channels. During an external reset or a power-on reset, the output stages are set to Clear mode.

5.2 Power Outputs

5.2.1 Inductive Output Clamp

When switching off inductive loads, the potential at pin OUT rises to $V_{DS(CL)}$ potential, because the inductance intends to continue driving the current. The voltage clamping is necessary to prevent destruction of the device. See **Figure 6** for more details. Nevertheless, the maximum allowed load inductance is limited. If a dedicated output enters clamping mode, the channel can be turned on again after clamping has disappeared.

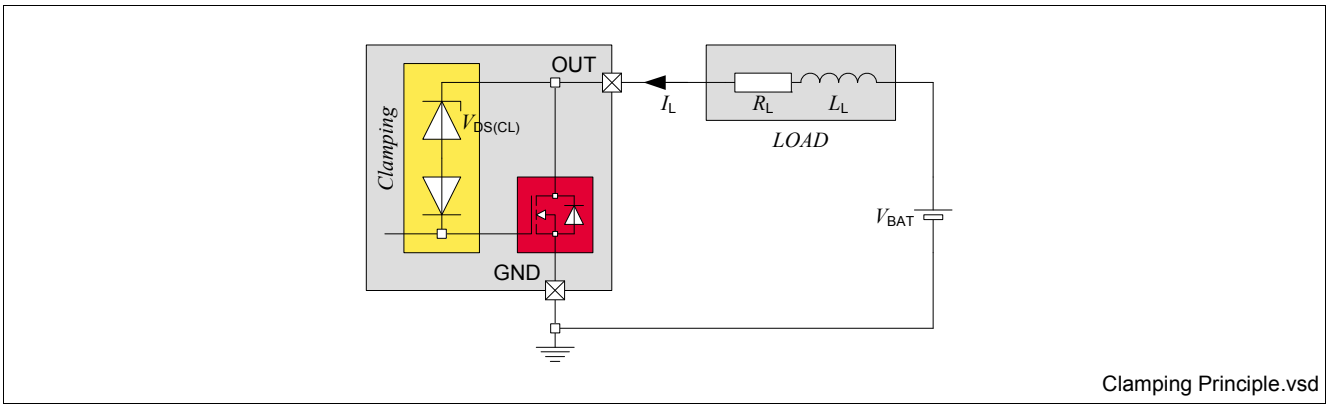


Figure 6 Internal Clamping Principle

Clamping Energy

During demagnetization of inductive loads, energy has to be dissipated in the TLE8108EM. This energy can be calculated with following equation:

$$E = V_{DS(CL)} \cdot \frac{L_L}{R_L} \cdot \left[I_L - \frac{V_{DS(CL)} - V_{BAT}}{R_L} \cdot \ln\left(1 + \frac{R_L \cdot I_L}{V_{DS(CL)} - V_{BAT}}\right)\right] \quad (1)$$

The maximum energy which is converted into heat, is limited by the thermal design of the component.

- Application hint: It is recommended to consider the real behavior of the load (R_L and L_L vs. temperature and vs. current) at each operating condition. Typical small signal parameters provided in the Datasheet of the load (actuator) might not represent the real behavior under operating conditions.

5.2.2 Timing Diagrams

The power transistors are switched on and off with a dedicated slope via the IN bits of the serial peripheral interface SPI or by the dedicated input pins and the input mode which is also programmed by SPI. The switching times t_{ON} and t_{OFF} are designed equally. If all channels are programmed into Clear mode together, the overall power consumption is reduced to a minimum. To switch the channel on again, OFF mode must be programmed and a wake up time $t_{wu(Stdby)}$ has to expire before sending the ON command. This procedure is shown in **Figure 7**.

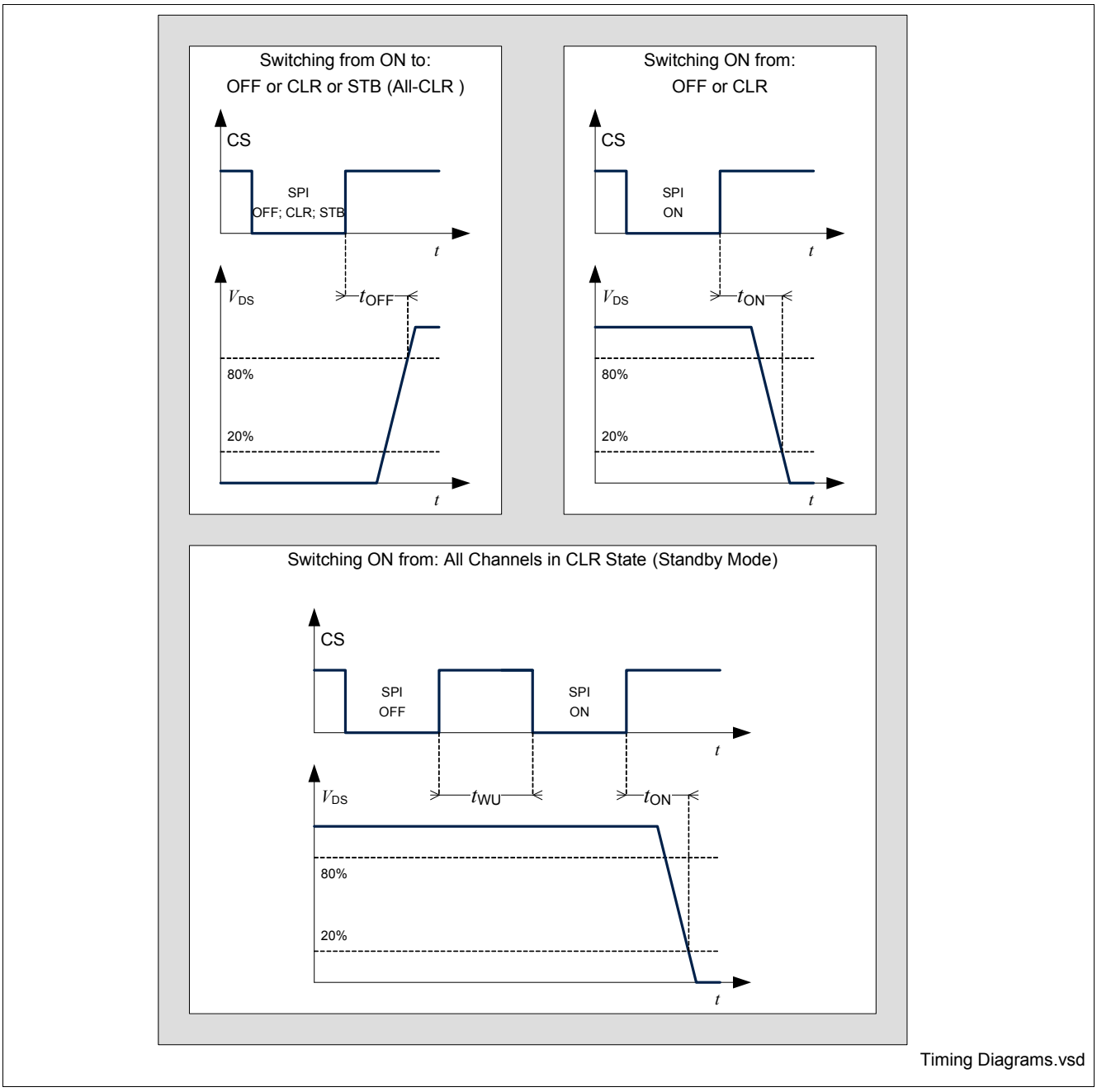


Figure 7 Timing Diagrams (Resistive Load)

In Input Mode, a high signal at the input pin is equivalent to a SPI ON command and a low signal to SPI OFF command respectively. Please refer to **Chapter 8.3** for details on operation modes.

5.3 Electrical Characteristics

Note: Characteristics show the deviation of parameters at given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.

Electrical Characteristics: Supply, Inputs, Reset and Power Stages

All voltages with respect to ground, positive currents are flowing into pin unless otherwise specified: V_{DD} = 4.5V to 5.5V, T_j = -40°C to +150°C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Power Supply							
5.3.1	Supply voltage	V_{DD}	4.5	-	5.5	V	
5.3.2	Supply current all channels on	$I_{DD(ON)}$	-	-	5.5	mA	
5.3.3	Supply standby current all channels in Clear mode	$I_{DD(STB)}$	-	-	80	µA	$V_{CS} = V_{DD}$ V_{SI} = 0V V_{SCLK} = 0V
5.3.4	Supply reset current	$I_{DD(RST)}$	-	-	40	µA	V_{RST} = 0V
5.3.5	Power-on reset threshold voltage	$V_{DD(PO)}$	-	-	4.0	V	
Output Characteristics							
5.3.6	On-state resistance per channel	$R_{DS(ON)}$	-	0.8	-	Ω	I_L = 400mA [1] T_j = 25°C
			-	-	1.7	Ω	I_L = 400mA T_j = 150°C
5.3.7	Continuous load current	$I_{L(cont)}$	-	-	400	mA	[1] All Channels ON
5.3.8	Output leakage current in Standby Mode (per channel)	$I_{D(STB)}$	-	-	5	µA	V_{DS} = 13.5V
5.3.9	Output clamping voltage	$V_{DS(CL)}$	41	-	50	V	I_{DS} = 20mA
Input Characteristics							
5.3.10	L level of pins IN1..IN4	$V_{IN(L)}$	0	-	0.6	V	-
5.3.11	H level of pins IN1..IN4	$V_{IN(H)}$	2.0	-	5.5	V	-
5.3.12	L input pull-down current through pin IN	$I_{IN(L)}$	1	10	40	µA	V_{IN} = 0.6V [1]
5.3.13	H input pull-down current through pin IN	$I_{IN(H)}$	10	40	80	µA	$V_{IN} = V_{DD}$ = 5V
Reset Characteristics							
5.3.14	L level of pin RST	$V_{RST(L)}$	0.3	-	0.2* V_{DD}	V	-
5.3.15	H level of pin RST	$V_{RST(H)}$	0.4* V_{DD}	-	V_{DD}	V	-
5.3.16	L input pull-down current through pin RST	$I_{RST(L)}$	1	10	40	µA	V_{RST} = 0.6V [1]
5.3.17	H input pull-down current through pin RST	$I_{RST(H)}$	10	40	80	µA	$V_{RST} = V_{DD}$ = 5V
Timings							
5.3.18	Reset wake up time (**Figure 4**)	t_{wu}	-	-	200	µs	[1]

Electrical Characteristics: Supply, Inputs, Reset and Power Stages (cont'd)

All voltages with respect to ground, positive currents are flowing into pin
unless otherwise specified: V_{DD} = 4.5V to 5.5V, T_j = -40°C to +150°C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.19	Reset signal duration (**Figure 4**)	t_{RST}	50	-	-	µs	1)
5.3.20	Turn on time V_{DS} = 20% V_{BAT} (**Figure 7**) all channels	t_{ON}	5	15	50	µs	V_{BAT} = 13.5V resistive load I_{DS} = 180mA
5.3.21	Turn off time V_{DS} = 80% V_{BAT} (**Figure 7**)	t_{OFF}	5	15	50	µs	V_{BAT} = 13.5V resistive load
5.3.22	Standby Mode wake up time (All channels in CLR state) (**Figure 7**)	$t_{wu(Stdby)}$	-	-	200	ms	1)
Clamping Energy - Repetitive 1) 2) 3) 4)							
5.3.23	Repetitive Clamping Energy per Channel	E_{AR}	-	-	13	mJ	I_D = 0.17A 10^6 cycles
			-	-	18	mJ	I_D = 0.2A 10^4 cycles

1) Not subject to production test, specified by design.

2) Either one of the values has to be considered as worst case limitation.

3) This lifetime statement is an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.

4) Triangular Pulse Shape (Inductance Discharge): $I_D(t) = I_D(0) \times (1 - t / t_{pulse})$; $0 < t < t_{pulse}$.

6 Protection Functions

The device provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in this Data Sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

6.1 Overload Protection

The TLE8108EM is protected in case of Overload or short circuit of the load. After time $t_{OFF(OVL)}$, the overloaded channel n switches off and the according diagnosis information is stored into the corresponding diagnosis register. The channel can be switched on again with the corresponding command after programming the Clear mode to reset the diagnosis register. Please refer to the example from **Figure 8** for details.

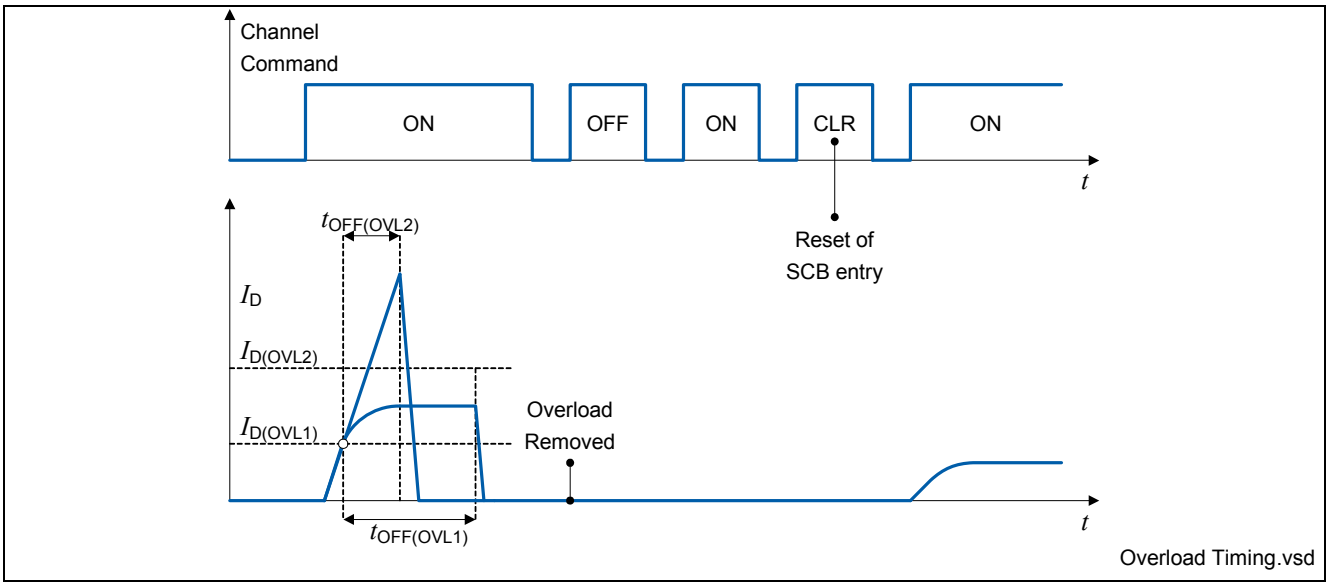


Figure 8 Shutdown at Overload

6.2 Overtemperature Protection

In case of Overload, a temperature sensor for each channel causes an overheated channel n to switch off to prevent destruction and the according diagnosis information is stored into the corresponding diagnosis register. The channel can be switched on again after programming the Clear mode and sending the ON command afterwards. Please refer to **Chapter 7** for information on diagnosis features.

6.3 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diode of the n-MOSFET generates power to be dissipated. The reverse current through the intrinsic body diode of the power transistor has to be limited by the connected load. The VDD supply pins must be protected against reverse polarity externally.

6.4 Protection Characteristics

Note: Characteristics show the deviation of parameters at given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.

Electrical Characteristics: Protection

All voltages with respect to ground, positive currents are flowing into pin unless otherwise specified: V_{DD} = 4.5V to 5.5V, T_j = -40°C to +150°C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Overload Protection							
6.4.1	Overload current Threshold Low all channels (**Figure 8**)	$I_{D(OVL1)}$	0.5		0.95	A	-
6.4.2	Overload current Threshold High all channels (**Figure 8**)	$I_{D(OVL2)}$	-	2.8* $I_{D(OVL1)}$	-	A	1)
6.4.3	Overload shut-down delay time Long	$t_{OFF(OVL1)}$	11	-	50	µs	Valid for Overload current Threshold Low
6.4.4	Overload shut-down delay time Short	$t_{OFF(OVL2)}$	1.5	-	35	µs	Valid for Overload current Threshold High 1)
Overtemperature Protection							
6.4.5	Thermal shut down temperature	$T_{j(SC)}$	165	-	-	°C	1)

1) Not subject to production test, specified by design

7 Diagnosis Features

The SPI of TLE8108EM provides diagnosis information about the device and about the load. The following diagnosis states are implemented:

- Short circuit to battery (SCB): Can be detected if stages are turned on
- Short circuit to ground (SCG): Can be detected if stages are turned off (channel either in OFF or in input mode with the dedicated input low)
- Open load (OL): Can be detected if stages are turned off (channel either in OFF or in input mode with dedicated input low)
- Diagnosis of Overtemperature (DOT): Is set in case the thermal shut down temperature $T_{j(SC)}$ is reached, if the output is turned on (either ON-state or input mode and channel turned on via parallel INx). In case the thermal shut down temperature $T_{j(SC)}$ is reached during clamping in OFF state, DOT is set and the dedicated channel can only be switched on again after a Clear mode is programmed, the temperature got below the shut down threshold and the clamping has vanished. In case the thermal shut down temperature $T_{j(SC)}$ is reached in OFF state without clamping, there is no diagnosis entry and the channel can be switched on again after the thermal shut down temperature $T_{j(SC)}$ falls below the threshold.

In Clear mode (CLR) there is no diagnostic function.

For each output channel there are 2 bits in the diagnosis register coding the different failures; Refer to **Chapter 8.3** for encoding details.

A short circuit to ground (SCG) will overwrite an open load (OL), but an open load (OL) will not overwrite a short circuit to ground (SCG). In order to detect an open load (OL) after a short circuit to ground (SCG), the output has to be programmed in Clear mode and again in either OFF mode or input mode with low input level.

Failure Mode	Comment
Open load or short circuit to ground	• No diagnosis when channel n is switched on (either channel in ON mode or channel in input mode and corresponding input signal is H) • No diagnosis when channel n is in Clear mode • Diagnosis when channel n is in input mode and corresponding input signal is L: According to the voltage level at the output pin, the corresponding failure is latched into the diagnosis register after the filtering time t_d has expired. • Diagnosis when channel n is in OFF mode: According to voltage level at the output pin, the corresponding failure is latched into the diagnosis register after the filtering time t_d has expired.

Failure Mode	Comment
Overtemperature	• In OFF state without clamping an Overtemperature will not be recognized. The channel can be switched on after the event vanishes without any diagnosis entry. • In OFF state when the output voltage is limited to the clamping voltage, an Overtemperature event will be recognized immediately at occurrence. Switching the channel(s) on is possible when the Overtemperature and the clamping events disappear and the dedicated channel(s) is (are) programmed to Clear mode. • In ON state when overtemperature occurs, the corresponding failure is stored into the diagnosis register and the affected channel(s) is(are) switched off. To switch the channel on again, the overtemperature event must disappear and the dedicated channel(s) must be programmed to Clear mode
Overload (Short Circuit to battery)	• Diagnosis in ON state when the dedicated channel(s) is (are) programmed to ON mode or input mode with input H. When Overload is detected, the affected channel(s) is (are) switched off after time $t_{OFF(OVL)}$ and the corresponding failure is latched into the diagnosis register. To switch the channel(s) ON again, the Overload event must disappear and the dedicated channel(s) must be programmed to Clear mode.

If, when the output stage is on, a SCB is detected the device turns the output stage off and the output stage can not be turned on again unless Clear mode is entered for the corresponding channel.

It could happen that when the SCB is detected another failure has already been stored in the corresponding register (OL or SCG); In this case the previous failure information, if not already been read, is lost.

If SCB is stored in the corresponding register and the output detects an OL or SCG, this OL or SCG will not be stored until the previous SCB has been cleared by entering Clear Mode (CLR). In order to detect OL or SCG then, an active OFF command needs to be adressed or, while a low input value is set on the dedicated input, input mode has to be programmed. The final OL or SCG diagnosis information can be obtained when the next SPI command is transmitted.

After power on sequence, the device must be programmed into Standby Mode, that means all channels in Clear mode, to have proper diagnosis information afterwards.

7.1 Diagnosis Characteristics

In order to detect the failures in OFF status, there are 2 thresholds ($V_{DS(SCG)}$ and $V_{DS(OL)}$) and an internal voltage regulating mechanism with 2 diagnosis currents with current limits for each output.

In OFF state, the internal mechanism tends to regulate the output to the middle value between $V_{DS(SCG)}$ and $V_{DS(OL)}$ achieving it only in case of OL. In case of SCG the output is pulled to GND by the short-circuit. In case of normal function, in OFF state, the output voltage is above $V_{DS(OL)}$

The diagnosis currents are switched off in case the output is in CLR mode.

The OL, SCB, SCG and DOT fault conditions are not stored until an integrated filter time has expired

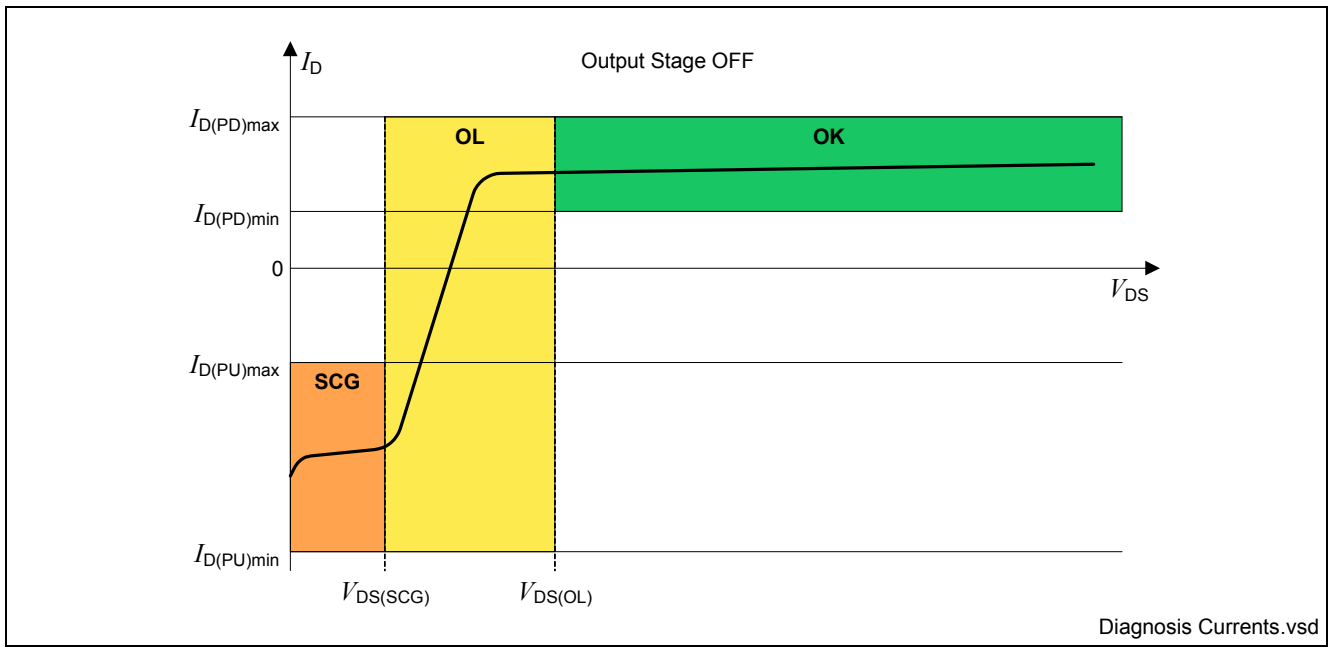


Figure 9 SCG and OL diagnosis function (overview only)

Note: Characteristics show the deviation of parameters at given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.

Electrical Characteristics: Diagnosis

All voltages with respect to ground, positive currents are flowing into pin unless otherwise specified: V_{DD} = 4.5V to 5.5V, T_j = -40°C to +150°C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
OFF State Diagnosis							
7.1.1	Open load detection threshold voltage	$V_{DS(OL)}$	V_{DD} * 0.45	-	V_{DD} * 0.62	V	-
7.1.2	Short circuit to Ground threshold voltage	$V_{DS(SCG)}$	V_{DD} * 0.13	-	V_{DD} * 0.25	V	-
7.1.3	Output pull-down diagnosis current per channel	$I_{D(PD)}$	30	-	80	µA	V_{DS} = 13.5V
7.1.4	Output pull-up diagnosis current per channel	$I_{D(PU)}$	-150	-	-50	µA	V_{DS} = 0V
7.1.5	Diagnosis filter time for diagnosis of SCG and OL states	t_d	30	-	200	µs	

8 Serial Peripheral Interface (SPI)

The diagnosis and control interface is based on a serial peripheral interface (SPI).

The SPI is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and CS. Data is transferred by the lines SI and SO at the data rate given by SCLK. The falling edge of CS indicates the beginning of a data access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of CS. A modulo 8 counter ensures that data is taken only, when a multiple of 8 bit has been transferred, while the minimum of 16 bit is also taken into consideration. Therefore the interface provides daisy chain capability even with 8 bit SPI devices.

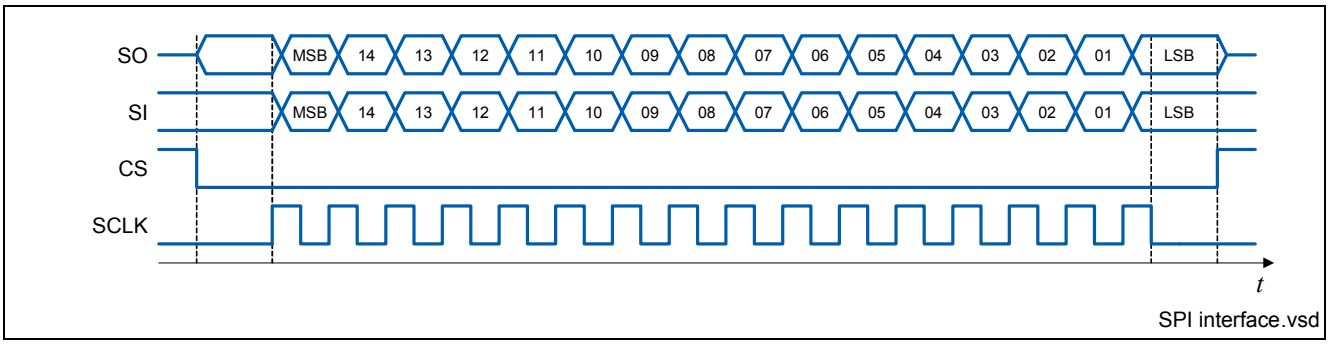


Figure 10 Serial peripheral Interface

The SPI protocol is described in **Section 8.3**. It is reset to the default values after programming the device into Standby mode (all the channels in Clear mode).

8.1 SPI Signal Description

There is one internal register where the diagnosis information is stored and a shift register used for transmitting the information via SO.

CS - Chip Select:

The system microcontroller selects the TLE8108EM by means of the CS pin. Whenever the pin is in low state, data transfer can take place. When CS is in high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

CS High to Low transition:

- The information which is stored in the internal diagnosis register is transferred into the shift register.
- SO changes from high impedance state to high or low state depending on the logic OR combination between the transmission error flag (TER) and the signal level at pin SI. The transmission error flag is set after any kind of reset, so a reset between two SPI commands is indicated. For details, please refer to **Figure 11**. This information stays available till the first rising edge of SCLK.

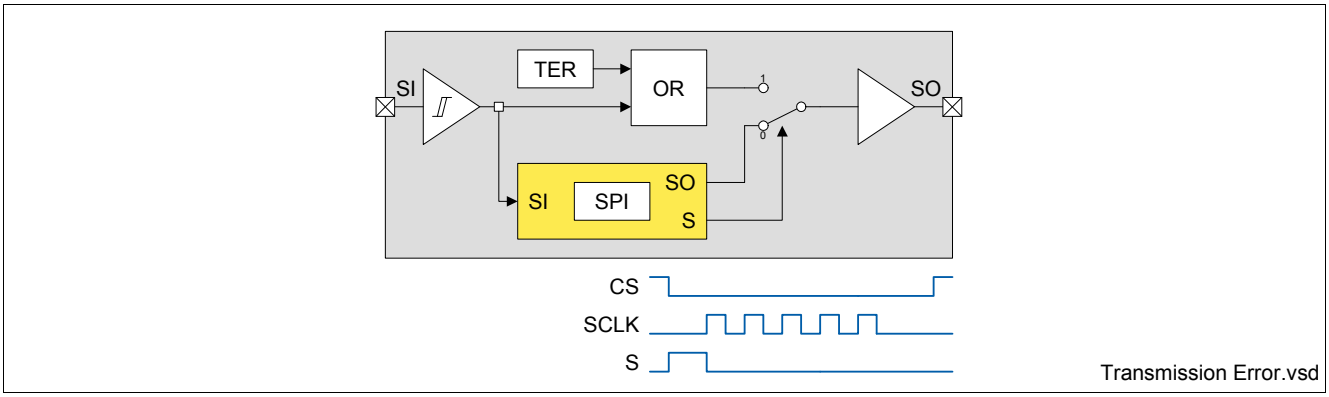


Figure 11 Transmission Error Flag on SO Line

CS Low to High transition:

Data from shift register is transferred into the input matrix register only if a multiple of 8 SCLK signals after the falling edge of CS has been detected, while the minimum valid length of 16 clocks for the 16-bit register TLE8108EM is taken into account.

SCLK - Serial Clock:

This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in low state whenever chip select CS makes any transition.

SI - Serial Input:

Serial input data bits are shifted in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. Please refer to **Section 8.3** for further information.

SO - Serial Output:

Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the CS pin goes to low state. New data will appear at the SO pin following the rising edge of SCLK. Please refer to **Section 8.3** for further information.

8.2 Daisy Chain Capability

The SPI of TLE8108EM provides daisy chain capability. In this configuration several devices are activated by the same CS signal (MCS). The SI line of one device is connected with the SO line of another device (see **Figure 12**), to build a chain. The terminations of the chain are connected with the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK, which is connected to the SCLK line of each device in the chain.

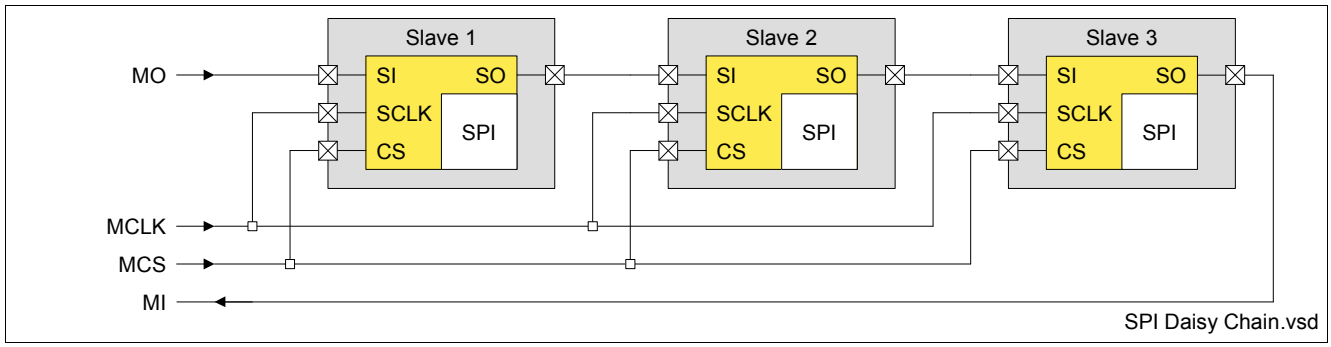


Figure 12 Daisy Chain Configuration

In the SPI block of each device, there is a shift register where one bit from SI line is shifted at each SCLK. The bit shifted out can be seen at SO. After 16 SCLK cycles, the data transfer for one TLE8108EM has been finished. In single chip configuration, the CS line must go high to make the device accepting the transferred data. In daisy chain configuration the data shifted out at device #1 is shifted in at device #2. When using multiple devices in daisy chain, the number of transferred bits must correspond to the number of the register bits of all chained devices. **Figure 13** shows an example with 3 SPI devices, where #1 and #3 are 16-bit SPI and #2 has a 8-bit SPI. To get a successful transmission, there must be (2*16 + 1*8)-bit shifted through the devices. After that, the MCS line can go high.

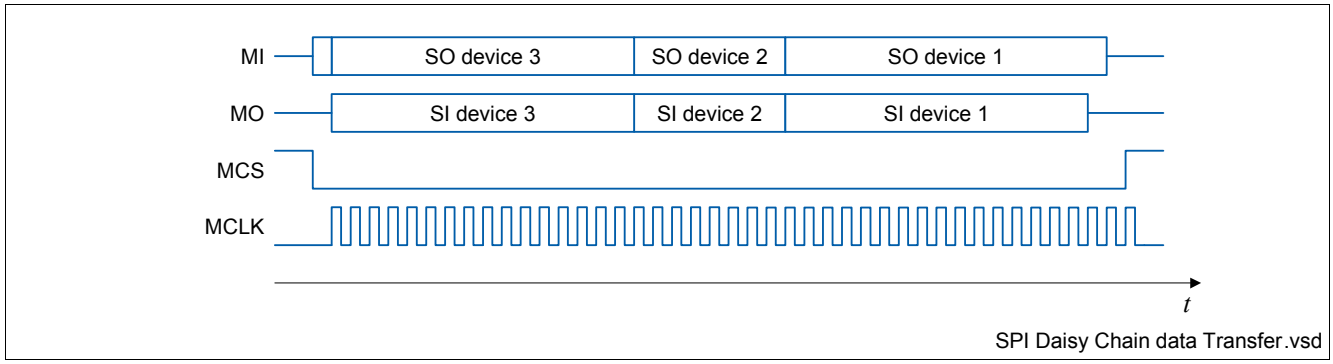


Figure 13 Data Transfer in Daisy Chain Configuration

8.3 SPI Protocol

The SPI protocol of the TLE8108EM provides two registers. The input register and the diagnosis register. The diagnosis register contains 8 pairs of diagnosis flags, the input register contains the input multiplexer configuration. After power-on reset, all input register bits are set to 1 which is the OFF state.

SI **Default: $FFFF_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN8		**IN7**		**IN6**		**IN5**		**IN4**		**IN3**		**IN2**		**IN1**	

Field	Bits	Type	Description
INn (n = 8-1)	15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0	W	**Input Register Channel n** 00_B Clear Mode: Channel switched off. Diagnosis flags are cleared. Diagnosis currents are disabled. 01_B Input Mode: Channel is switched according to signal at input pin. Diagnosis currents are enabled in OFF state. 10_B ON mode: Channel is switched on. Diagnosis currents are disabled. 11_B OFF mode (default state): Channel is switched off. Diagnosis currents are enabled.

If all channels are in Clear Mode, the device enters the Standby Mode a power down status with minimum current consumption.

SO **Reset Value: $FFFF_H$**

16[1]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TER	**OUT8_DIA2**	**OUT8_DIA1**	**OUT7_DIA2**	**OUT7_DIA1**	**OUT6_DIA2**	**OUT6_DIA1**	**OUT5_DIA2**	**OUT5_DIA1**	**OUT4_DIA2**	**OUT4_DIA1**	**OUT3_DIA2**	**OUT3_DIA1**	**OUT2_DIA2**	**OUT2_DIA1**	**OUT1_DIA2**	**OUT1_DIA1**

1) This bit is valid between CS HI-LO and first SCLK LO-HI transition.

OUTn_DIA2	OUTn_DIA1	Description
1	1	Power stage ok
1	0	Short circuit to battery (SCB) or diagnostic overtemperature (DOT)
0	1	Open load (OL)
0	0	Short circuit to GND (SCG)

8.3.1 Timing Diagrams

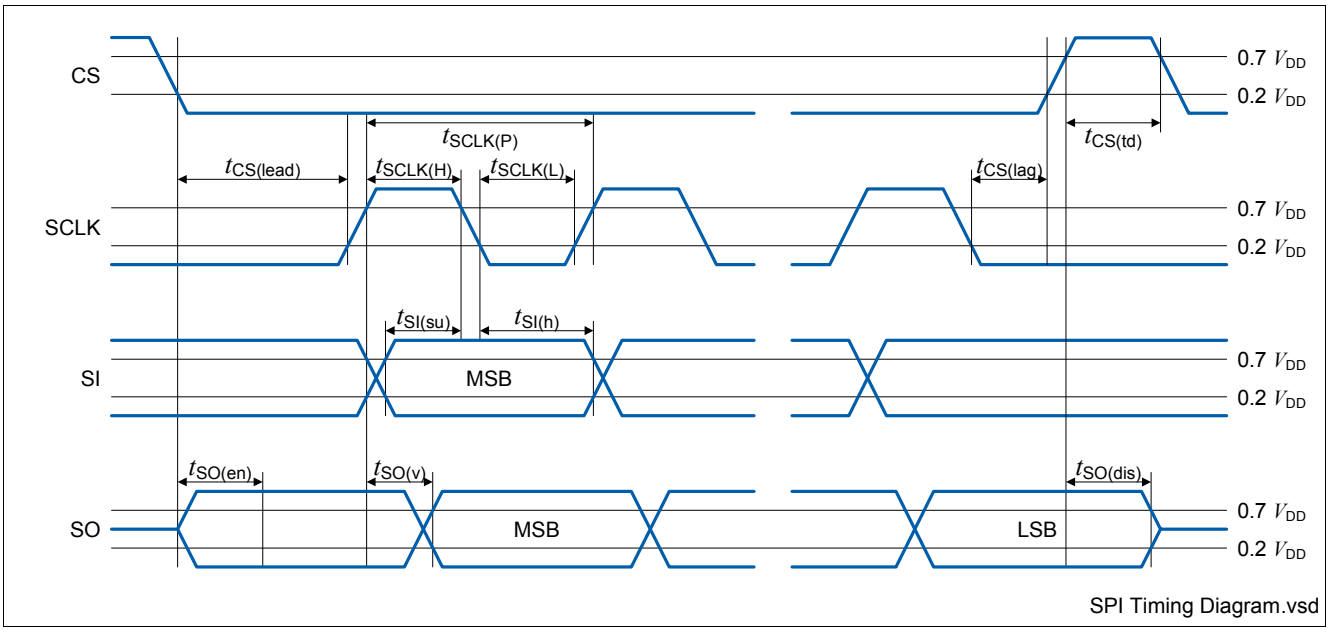


Figure 14 Timing Diagram

8.4 SPI Characteristics

Note: Characteristics show the deviation of parameters at given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.

Electrical Characteristics: Serial Peripheral Interface (SPI)

All voltages with respect to ground, positive currents are flowing into pin
unless otherwise specified: V_{DD} = 4.5V to 5.5V, T_j = -40°C to +150°C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Input Characteristics (CS, SCLK, SI)							
8.4.1	L level of pin CS SCLK SI	 $V_{CS(L)}$ $V_{SCLK(L)}$ $V_{SI(L)}$	0	-	0.2* V_{DD}	V	-
8.4.2	H level of pin CS SCLK SI	 $V_{CS(H)}$ $V_{SCLK(H)}$ $V_{SI(H)}$	0.4* V_{DD}	-	V_{DD}	V	-
8.4.3	L input pull-up current through CS	$I_{CS(L)}$	3	17	40	µA	V_{DD}=5V V_{CS} = 0V
8.4.4	H input pull-up current through CS	$I_{CS(H)}$	3	15	40	µA	V_{DD}=5V V_{CS} = 0.4*V_{DD} [1]
8.4.5	L input pull-down current through pin SCLK SI	 $I_{SCLK(L)}$ $I_{SI(L)}$	1	10	60	µA	[1] V_{SCLK} = 0.6V V_{SI} = 0.6V

Electrical Characteristics: Serial Peripheral Interface (SPI) (cont'd)

All voltages with respect to ground, positive currents are flowing into pin unless otherwise specified: V_{DD} = 4.5V to 5.5V, T_j = -40°C to +150°C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
8.4.6	H-input pull-down current through pin SCLK SI	 $I_{SCLK(H)}$ $I_{SI(H)}$	10	40	80	µA	V_{DD}=5V $V_{SCLK} = V_{DD}$ $V_{SI} = V_{DD}$
Output Characteristics (SO)							
8.4.7	L level output voltage	$V_{SO(L)}$	0	-	0.6	V	I_{SO} = 2mA
8.4.8	H level output voltage	$V_{SO(H)}$	V_{DD} - 0.4	-	V_{DD}	V	I_{SO} = -1.5mA
8.4.9	Output tristate leakage current	$I_{SO(OFF)}$	-10	-	10	µA	$V_{CS} = V_{DD}$
Timings							
8.4.10	Serial clock frequency	f_{SCLK}	0	-	5	MHz	1) C_L = 50pF
8.4.11	Serial clock period	$t_{SCLK(P)}$	200	-	-	ns	1)
8.4.12	Serial clock high time	$t_{SCLK(H)}$	50	-	-	ns	1)
8.4.13	Serial clock low time	$t_{SCLK(L)}$	50	-	-	ns	1)
8.4.14	Enable lead time (falling CS to rising SCLK)	$t_{CS(lead)}$	250	-	-	ns	1)
8.4.15	Enable lag time (falling SCLK to rising CS)	$t_{CS(lag)}$	250	-	-	ns	1)
8.4.16	Transfer delay time (rising CS to falling CS)	$t_{CS(td)}$	250	-	-	ns	1) 2)
8.4.17 a) b)	 Data setup time (SI to falling SCLK) Data hold time (falling SCLK to SI)	 $t_{SI(su)}$ $t_{SI(h)}$	 20 20	 - -	 - -	 ns ns	 1) 1)
8.4.18	Output enable time (falling CS to SO valid)	$t_{SO(en)}$	-	-	200	ns	C_L = 50pF 1)
8.4.19	Output disable time (rising CS to SO tristate)	$t_{SO(dis)}$	-	-	200	ns	C_L = 50pF 1)
8.4.20	Output data valid time with capacitive load	$t_{SO(v)}$	-	-	100	ns	C_L = 50pF 1)

1) Not subject to production test, specified by design.

2) Diagnosis flag update needs the time specified in **Chapter 7.1** to get valid information

9 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

Figure 15 shows a simplified application circuit. V_{DD} needs to be externally reverse polarity protected.

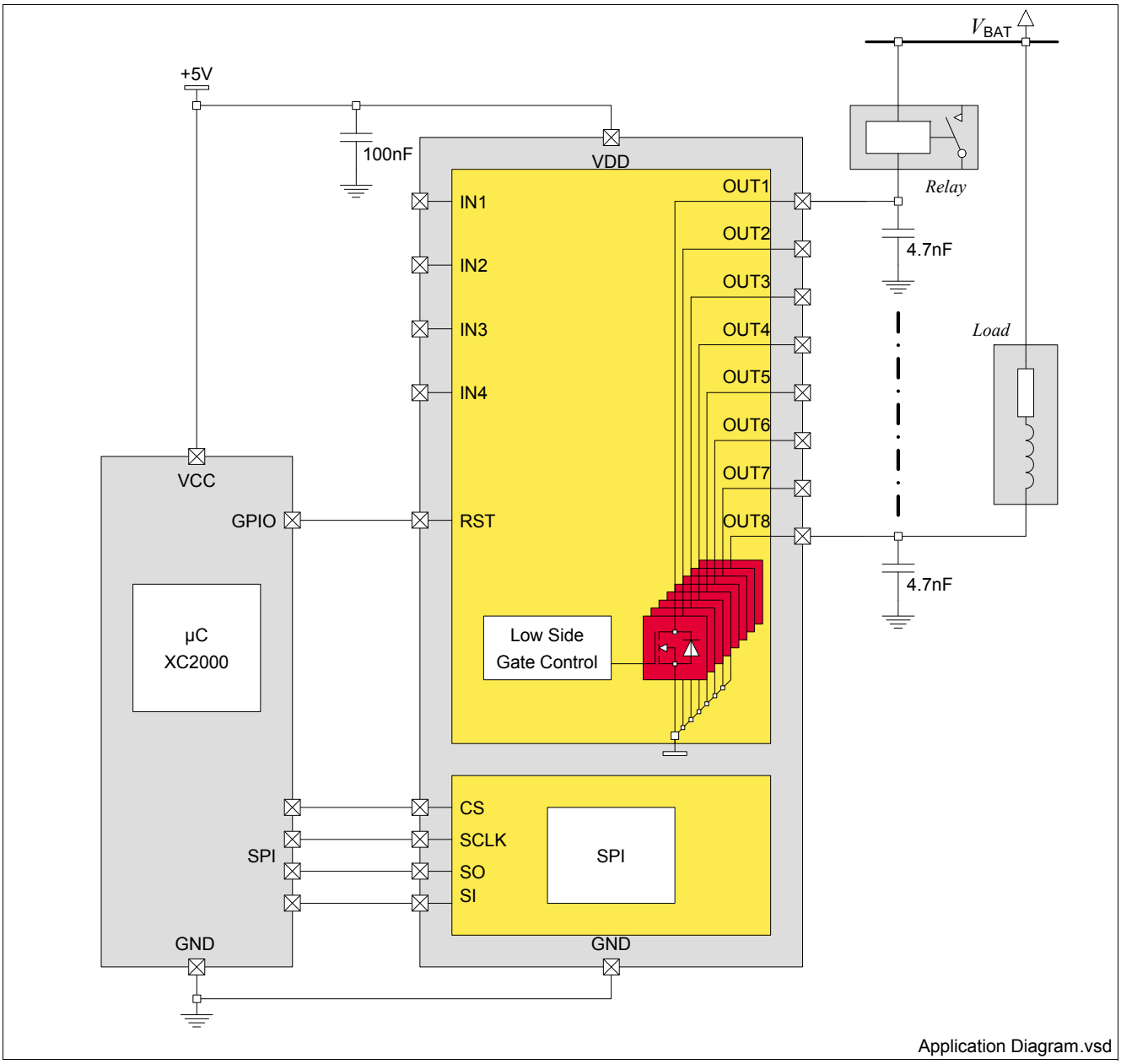


Figure 15 Application Diagram

Note: This is a very simplified example of application circuit. The function must be verified in the real application.

- Application hint: It is suggest to connect a 4.7nF capacitor directly at each output pin for improved EMC performances

For further information you may contact **http://www.infineon.com**

10 Package Outlines

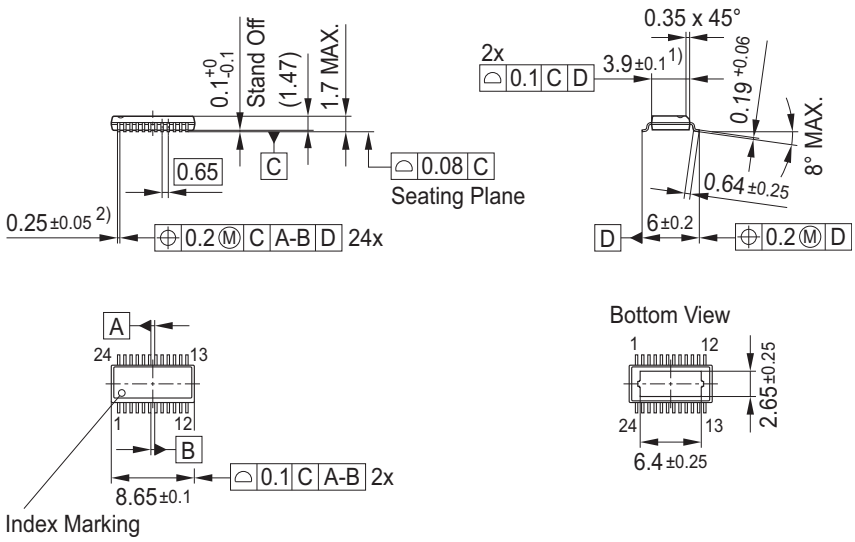


Figure 16 **PG-SSOP-24** (Plastic Dual Small Outline Package)

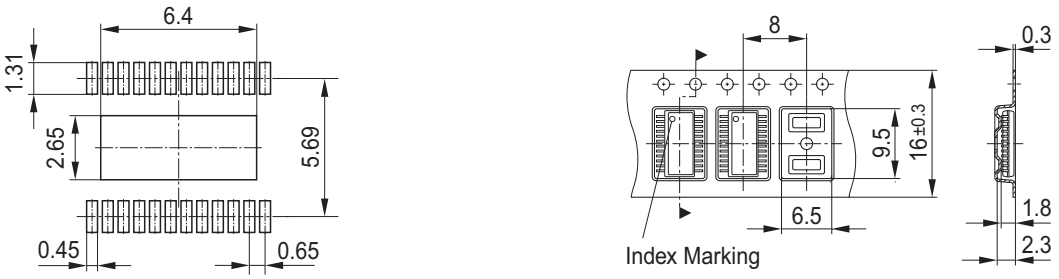


Figure 17 **PG-SSOP-24** Footprint and Packing

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environment friendly products and to be compliant with government regulations, the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Please specify the needed package (e.g. green package) when an order is placed.

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

Dimensions in mm

11 Revision History

Revision	Date	Changes
Rev. 1.0	2011-03-24	Released Data Sheet

Edition 2011-03-23

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

单击下面可查看定价，库存，交付和生命周期等信息

>>Infineon Technologies(英飞凌)

>>点击查看相关商品