1EDI EiceDRIVER™ Compact

Output with Clamp variant for IGBT

Single Channel IGBT Gate Driver IC

1EDI10I12MF
1EDI20I12MF
1EDI30I12MF

Data Sheet

Rev. 2.0, 2014-11-10

Industrial Power Control

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Revision History

Page or Item	**Subjects (major changes since previous revision)**
Rev. 2.0, 2014-11-10	
all pages	Final datasheet, parameter completion and editorial changes
Rev. 1.02, 2014-10-14	
all pages	parameter completion

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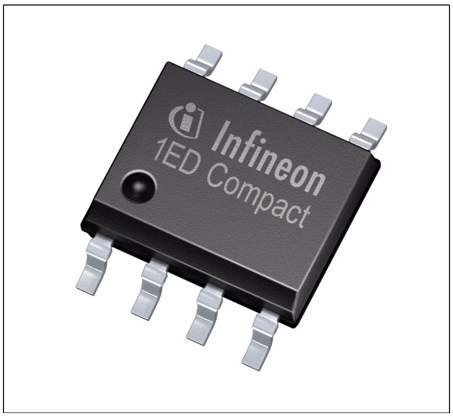

Main Features

- Single channel isolated IGBT Driver
- For 600 V/1200 V IGBTs
- Up to 6 A typical peak current at rail-to-rail outputs
- Active Miller Clamp

Product Highlights

- Galvanically isolated Coreless Transformer Driver
- Wide input voltage operating range
- Suitable for operation at high ambient temperature

Typical Application

- AC and Brushless DC Motor Drives
- High Voltage DC/DC-Converter and DC/AC-Inverter
- Induction Heating Resonant Application
- UPS-Systems
- Welding
- Solar

Description

The 1EDI10I12MF, 1EDI20I12MF and 1EDI30I12MF are galvanically isolated single channel IGBT driver in a PG-DSO-8-51 package that provide minimum peak output currents up to 3 A and an integrated active Miller Clamp circuit with the same current rating to protect against parasitic turn on.

The input logic pins operate on a wide input voltage range from 3 V to 15 V using CMOS threshold levels to support even 3.3 V microcontroller.

Data transfer across the isolation barrier is realized by the Coreless Transformer Technology.

Every driver family member comes with logic input and driver output under voltage lockout (UVLO) and active shutdown.

Product Name	Gate Drive Current (min)	Package
1EDI10I12MF	±1.0 A with 1.0 A Miller Clamp	PG-DSO-8-51
1EDI20I12MF	±2.0 A with 2.0 A Miller Clamp	PG-DSO-8-51
1EDI30I12MF	±3.0 A with 3.0 A Miller Clamp	PG-DSO-8-51

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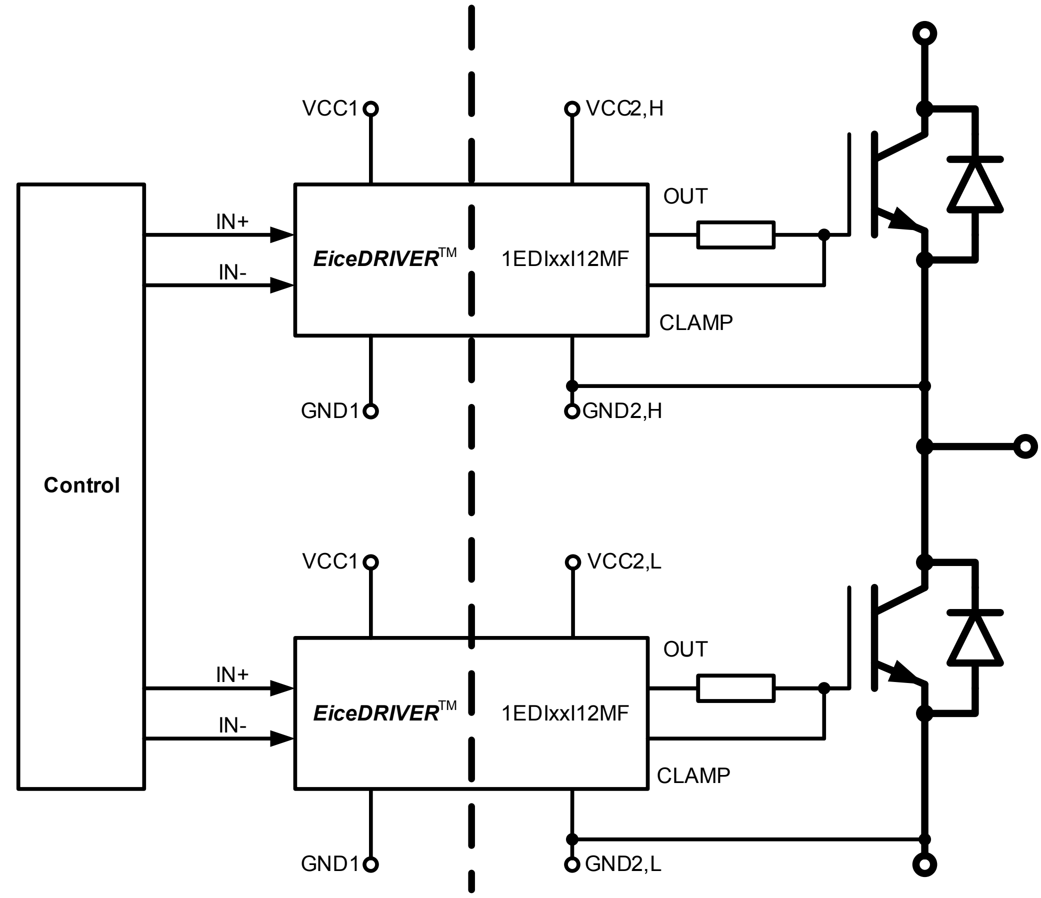

Figure 1 Typical Application

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2 Block Diagram

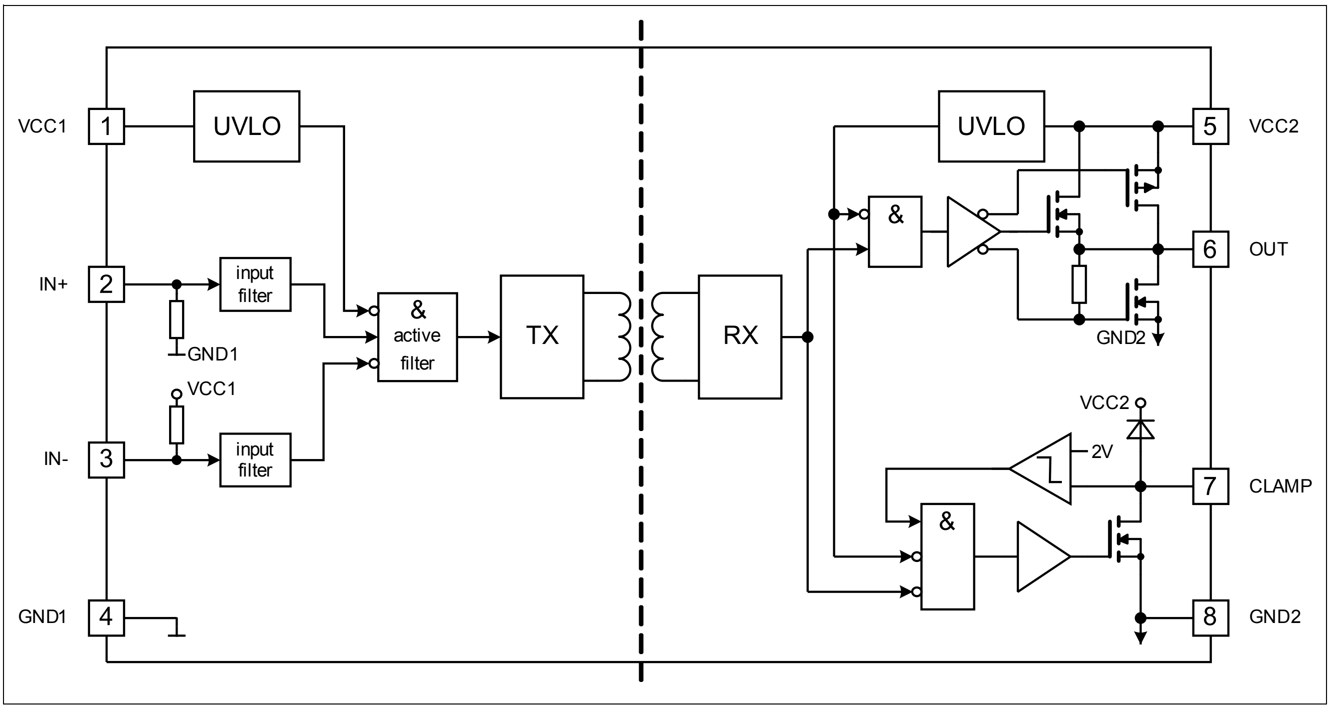

Figure 2 Block Diagram 1EDI10I12MF, 1EDI20I12MF and 1EDI30I12MF

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3 Pin Configuration and Functionality

3.1 Pin Configuration

Table 1 Pin Configuration

Pin No.	Name	Function
1	VCC1	Positive Logic Supply
2	IN+	Non-Inverted Driver Input (active high)
3	IN-	Inverted Driver Input (active low)
4	GND1	Logic Ground
5	VCC2	Positive Power Supply Output Side
6	OUT	Driver Output
7	CLAMP	Active Miller Clamp
8	GND2	Power Ground

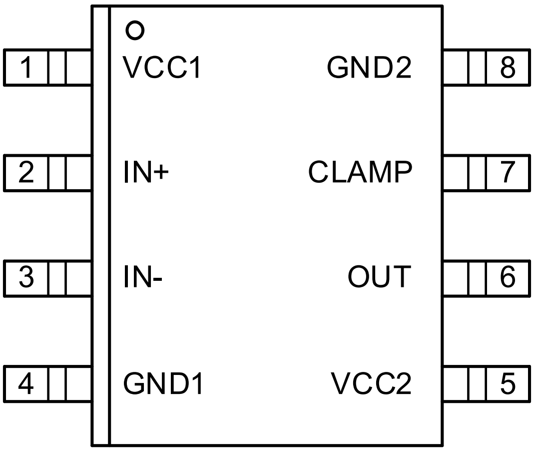

Figure 3 PG-DSO-8-51 (top view)

3.2 Pin Functionality

VCC1

Logic input supply voltage of 3.3 V up to 15 V wide operating range.

IN+ Non Inverting Driver Input

IN+ non-inverted control signal for driver output if IN- is set to low. (Output sourcing active at IN+ = high and IN- = low)

Due to internal filtering a minimum pulse width is defined to ensure robustness against noise at IN+. An internal weak pull-down-resistor favors off-state.

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IN- Inverting Driver Input

IN- inverted control signal for driver output if IN+ is set to high. (Output sourcing active at IN- = low and IN+ = high)

Due to internal filtering a minimum pulse width is defined to ensure robustness against noise at IN-. An internal weak pull-up-resistor favors off-state.

GND1

Ground connection of input circuit.

VCC2

Positive power supply pin of output driving circuit. A proper blocking capacitor has to be placed close to this supply pin.

OUT Driver Output

Combined source and sink output pin to external IGBT. The output voltage will be switched between VCC2 and GND2 and is controlled by IN+ and IN-. In case of an UVLO event this output will be switched off and an active shut down keeps the output voltage at a low level.

CLAMP Active Miller Clamp

Connect gate of external IGBT directly to this pin. As soon as the gate voltage has dropped below 2 V referred to GND2 during turn off state the CLAMP function ties its output to GND2 to avoid parasitic turn on of the connected IGBT.

GND2 Reference Ground

Reference ground of the output driving circuit.

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4 Functional Description

4.1 Introduction

The Output with Clamp variant for IGBT is a general purpose IGBT gate driver. Basic control and protection features support fast and easy design of highly reliable systems.

The integrated galvanic isolation between control input logic and driving output stage grants additional safety. Its wide input voltage supply range support the direct connection of various signal sources like DSPs and microcontrollers.

With the rail-to-rail output and the additional active miller clamp, dynamic turn on due to Miller capacitances are suppressed.

4.2 Supply

The driver can operate over a wide supply voltage range.

The typical positive supply voltage for the configuration in **Figure 4** is 15V at VCC2. Erratical dynamic turn on of the IGBT can be prevented with the active Miller clamp function, in which the CLAMP output is directly connected to the IGBT gate.

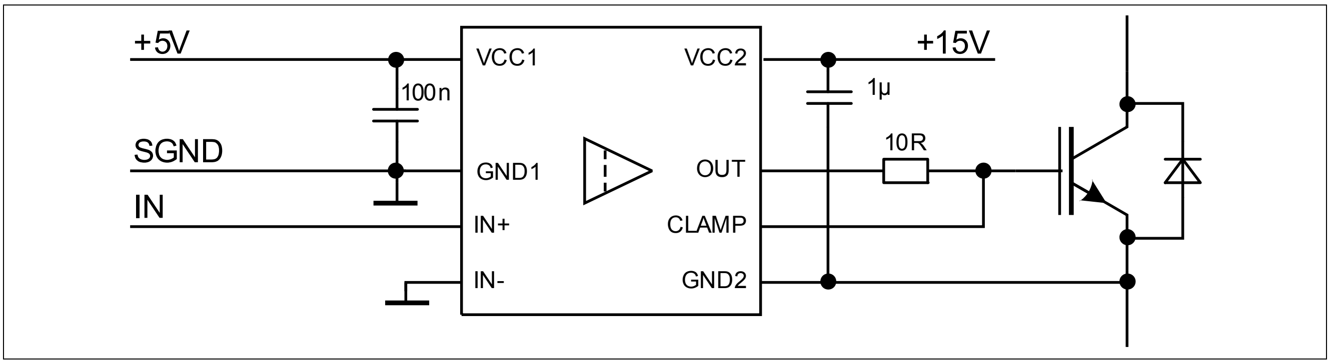

Figure 4 **Application Example**

4.3 Protection Features

4.3.1 Undervoltage Lockout (UVLO)

To ensure correct switching of IGBTs the device is equipped with an undervoltage lockout for input and output independently. Operation starts only after both VCC levels have increased beyond the respective V_{UVLOH} levels (see also **Figure 7**).

If the power supply voltage V_{VCC1} of the input chip drops below V_{UVLOL1} a turn-off signal is sent to the output chip before power-down. The IGBT is switched off and the signals at IN+ and IN- are ignored until V_{VCC1} reaches the power-up voltage V_{UVLOH1} again.

If the power supply voltage V_{VCC2} of the output chip goes down below V_{UVLOL2} the IGBT is switched off and signals from the input chip are ignored until V_{VCC2} reaches the power-up voltage V_{UVLOH2} again.

4.3.2 Active Shut-Down

The active shut-down feature ensures a safe IGBT off-state if the output chip is not connected to the power supply, IGBT gate is clamped at OUT and CLAMP to GND2.

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4.3.3 Short Circuit Clamping

During short circuit the IGBT's gate voltage tends to rise because of the feedback via the Miller capacitance. An additional protection circuit connected to OUT and CLAMP limits this voltage to a value slightly higher than the supply voltage. A maximum current of 500 mA may be fed back to the supply through one of these paths for 10 µs. If higher currents are expected or tighter clamping is desired external Schottky diodes may be added.

4.3.4 Active Miller Clamp

In a half bridge configuration the switched off IGBT tends to dynamically turn on during turn on phase of the opposite IGBT. A Miller clamp allows sinking the Miller current across a low impedance path in this high dV/dt situation. Therefore in many applications, the use of a negative supply voltage can be avoided.

During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage drops below typical 2 V (referred to GND2). The clamp is designed for a Miller current in the same range as the nominal output current.

4.4 Non-Inverting and Inverting Inputs

There are two possible input modes to control the IGBT. At non-inverting mode IN+ controls the driver output while IN- is set to low. At inverting mode IN- controls the driver output while IN+ is set to high, please see **Figure 6**. A minimum input pulse width is defined to filter occasional glitches.

4.5 Driver Output

The output driver section uses MOSFETs to provide a rail-to-rail output. This feature permits that tight control of gate voltage during on-state and short circuit can be maintained as long as the driver's supply is stable. Due to the low internal voltage drop, switching behaviour of the IGBT is predominantly governed by the gate resistor. Furthermore, it reduces the power to be dissipated by the driver.

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5 Electrical Parameters

5.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all parameters refer to GND1.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Power supply output side	V_{VCC2}	-0.3	20	V	1)
Gate driver output	V_{OUT}	V_{GND2}-0.3	V_{VCC2}+0.3	V	–
Pin CLAMP voltage	V_{CLAMP}	-0.3	V_{VCC2} +0.3 1)	V	1)
Maximum short circuit clamping time	t_{CLP}	–	10	µs	$I_{CLAMP/OUT}$ = 500 mA
Positive power supply input side	V_{VCC1}	-0.3	18.0	V	–
Logic input voltages (IN+,IN-)	$V_{LogicIN}$	-0.3	18.0	V	–
Input to output isolation voltage (GND2)	V_{ISO}	-1200	1200	V	
Junction temperature	T_J	-40	150	°C	–
Storage temperature	T_S	-55	150	°C	–
Power dissipation (Input side)	$P_{D, IN}$	–	25	mW	2) @T_A = 25°C
Power dissipation (Output side)	$P_{D, OUT}$	–	400	mW	2) @T_A = 25°C
Thermal resistance (Input side)	$R_{THJA,IN}$	–	145	K/W	2) @T_A = 85°C
Thermal resistance (Output side)	$R_{THJA,OUT}$	–	165	K/W	2) @T_A = 85°C
ESD capability	$V_{ESD,HBM}$	–	2	kV	Human Body Model 3)

1) May be exceeded during short circuit clamping.

2) See **Figure 9** for reference layouts for these thermal data. Thermal performance may change significantly with layout and heat dissipation of components in close proximity.

3) According to EIA/JESD22-A114-C (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).

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5.2 Operating Parameters

Note: Within the operating range the IC operates as described in the functional description. Unless otherwise noted all parameters refer to GND1.

Table 3 Operating Parameters

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Power supply output side	V_{VCC2}	13	18	V	1)
Power supply input side	V_{VCC1}	3.1	17	V	–
Logic input voltages (IN+,IN-)	V_{LogicIN}	-0.3	17	V	–
Pin CLAMP voltage	V_{CLAMP}	V_{GND2}-0.3	V_{VCC2} 2)	V	–
Switching frequency	f_{sw}	–	1.0	MHz	3) 4)
Ambient temperature	T_{A}	-40	125	°C	–
Thermal coefficient, junction-top	$\Psi_{\mathrm{th,jt}}$	–	4.8	K/W	@T_{A} = 85°C
Common mode transient immunity	$\lvert dV_{\mathrm{ISO}}/dt \rvert$	–	100	kV/µs	4) @ 1000 V

1) With respect to GND2.
2) May be exceeded during short circuit clamping.
3) do not exceed max. power dissipation
4) Parameter is not subject to production test - verified by design/characterization

5.3 Electrical Characteristics

Note: The electrical characteristics include the spread of values in supply voltages, load and junction temperatures given below. Typical values represent the median values at T_A = 25°C. Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 1 to 3, GND2 for pins 5 to 7).

5.3.1 Voltage Supply

Table 4 Voltage Supply

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
UVLO threshold input chip	V_{UVLOH1}	–	2.85	3.1	V	–
	V_{UVLOL1}	2.55	2.75	–	V	–
UVLO hysteresis input chip (V_{UVLOH1} - V_{UVLOL1})	V_{HYS1}	90	100	–	mV	–
UVLO threshold output chip (IGBT supply)	V_{UVLOH2}	–	11.9	12.7	V	–
	V_{UVLOL2}	10.5	11.0	–	V	–
UVLO hysteresis output chip (V_{UVLOH1} - V_{UVLOL1})	V_{HYS2}	700	850	–	mV	–

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Table 4 Voltage Supply (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Quiescent current input chip	I_{Q1}	–	0.6	1.0	mA	V_{VCC1} = 5 V IN+ = High, IN- = Low =>OUT = High
Quiescent current output chip	I_{Q2}	–	1.2	2.0	mA	V_{VCC2} = 15 V IN+ = High, IN- = Low =>OUT = High

5.3.2 Logic Input

Note: Unless stated otherwise VCC1 = 5.0V

Table 5 Logic Input

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
IN+,IN- low input voltage	V_{IN+L}, V_{IN-L}	–	–	30	%	of VCC1
IN+,IN- high input voltage	V_{IN+H}, V_{IN-H}	70	–	–	%	of VCC1
IN+,IN- low input voltage	V_{IN+L}, V_{IN-L}	–	–	1.5	V	–
IN+,IN- high input voltage	V_{IN+H}, V_{IN-H}	3.5	–	–	V	–
IN- input current	I_{IN-}	–	70	200	µA	V_{IN-} = GND1
IN+ input current	I_{IN+},	–	70	200	µA	V_{IN+} = VCC1

5.3.3 Gate Driver

Table 6 Gate Driver

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
High level output peak current (source)	$I_{OUT,H,PEAK}$		–	–	A	1) IN+ = High, IN- = Low, V_{VCC2} = 15 V
1EDI10I12MF		1.0	2.2			
1EDI20I12MF		2.0	4.4			
1EDI30I12MF		3.0	5.9			
Low level output peak current (sink)	$I_{OUT,L,PEAK}$		–	–	A	1) IN+ = Low, IN- = Low, VVCC2 = 15 V
1EDI10I12MF		1.0	2.3			
1EDI20I12MF		2.0	4.1			
1EDI30I12MF		3.0	6.2			

1) voltage across the device $V_{(VCC2 - OUT+)}$ or $V_{(OUT- - GND2)}$ < V_{VCC2}.

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5.3.4 Short Circuit Clamping

Table 7 Short Circuit Clamping

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage (OUT) (V_{OUT} - V_{VCC2})	V_{CLPout}	–	0.9	1.3	V	IN+ = High, IN- = Low, I_{OUT} = 500 mA pulse test, t_{CLPmax} = 10 µs)
Clamping voltage (CLAMP) (V_{VCLAMP}-V_{VCC2})	$V_{CLPclamp1}$	–	1.3	–	V	IN+ = High, IN- = Low, I_{CLAMP} = 500 mA (pulse test, t_{CLPmax} = 10 µs)
Clamping voltage (CLAMP)	$V_{CLPclamp2}$	–	0.7	1.1	V	IN+ = High, IN- = Low, I_{CLAMP} = 20 mA

5.3.5 Active Miller Clamp

Table 8 Active Miller Clamp

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Low level clamp current 1EDI10I12MF 1EDI20I12MF 1EDI30I12MF	$I_{CLAMP,PEAK}$	 1.0 2.0 3.0	–	–	A	[1] IN+ = Low, IN- = Low, V_{CLAMP} = 15 V pulsed t_{pulse} = 2 µs
Clamp threshold voltage	V_{CLAMP}	1.6	2.0	2.4	V	Related to GND2

[1] The parameter is not subject to production test - verified by design/characterization

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5.3.6 Dynamic Characteristics

Dynamic characteristics are measured with V_{VCC1} = 5 V and V_{VCC2} = 15 V.

Table 9 Dynamic Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input IN to output propagation delay ON	T_{PDON}	270	300	330	ns	C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50% @ 25°C
Input IN to output propagation delay OFF	T_{PDOFF}	270	300	330	ns	
Input IN to output propagation delay distortion (T_{PDOFF} - T_{PDON})	T_{PDISTO}	-30	5	40	ns	
Input pulse suppression IN+, IN-	T_{MININ+}, T_{MININ-}	230	240	–	ns	–
IN input to output propagation delay ON variation due to temp	T_{PDONt}	–	–	14	ns	1) C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50%
IN input to output propagation delay OFF variation due to temp	T_{PDOFFt}	–	–	14	ns	1) C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50%
IN input to output propagation delay distortion variation due to temp (T_{PDOFF}-T_{PDON})	$T_{PDISTOt}$	–	–	8	ns	1) C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50%
Rise time	T_{RISE}	5	9	19	ns	C_{LOAD} = 1 nF V_L 20%, V_H 80%
Fall time	T_{FALL}	3	6	15	ns	C_{LOAD} = 1 nF V_L 20%, V_H 80%

1) The parameter is not subject to production test - verified by design/characterization

5.3.7 Active Shut Down

Table 10 Active Shut Down

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Active shut down voltage	V_{ACTSD} 1)	–	1.8	2.0	V	$I_{OUT-}/I_{OUT-,PEAK}$=0.1, V_{CC2} open

1) With reference to GND2

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6 Timing Diagramms

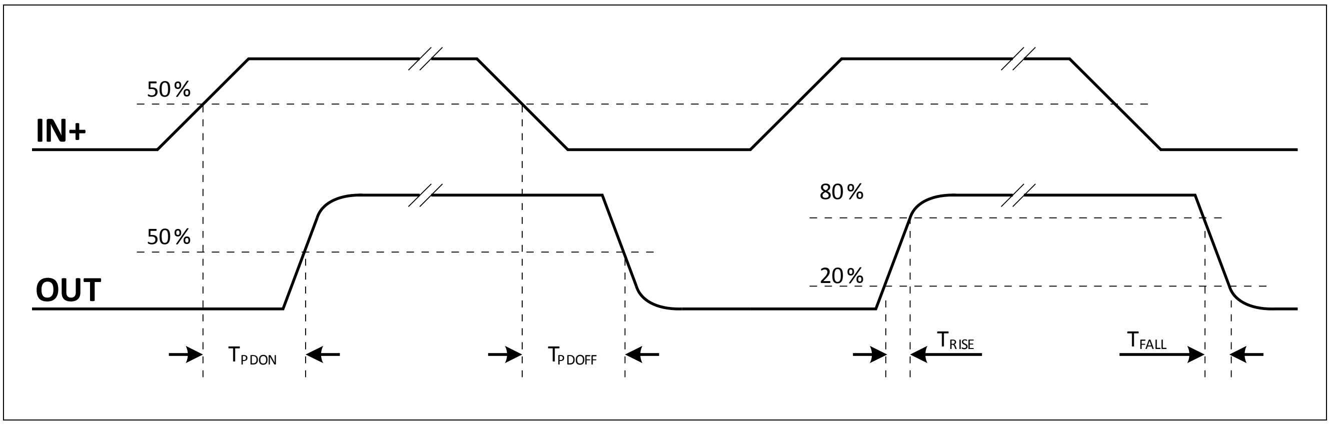

Figure 5 Propagation Delay, Rise and Fall Time

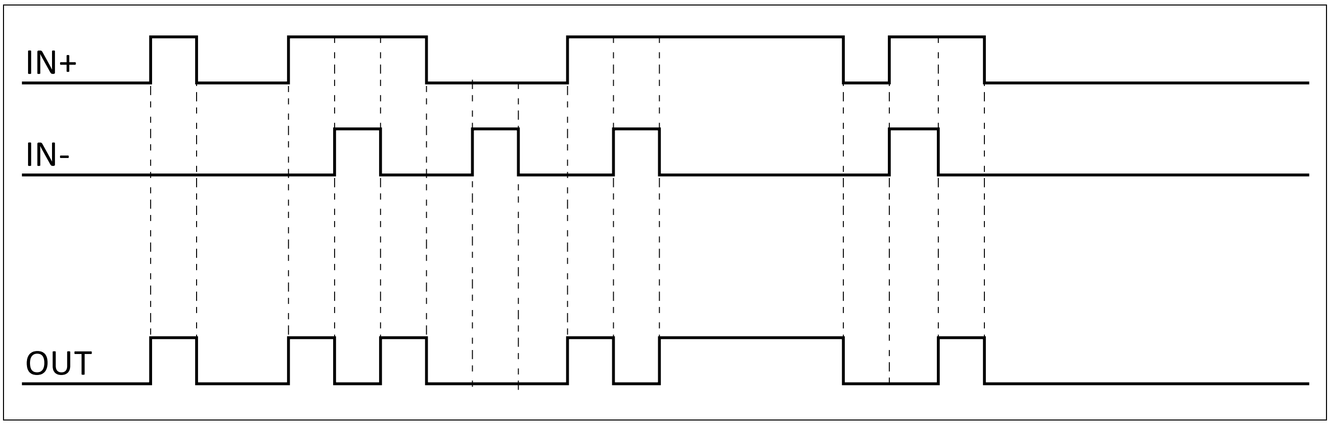

Figure 6 Typical Switching Behavior

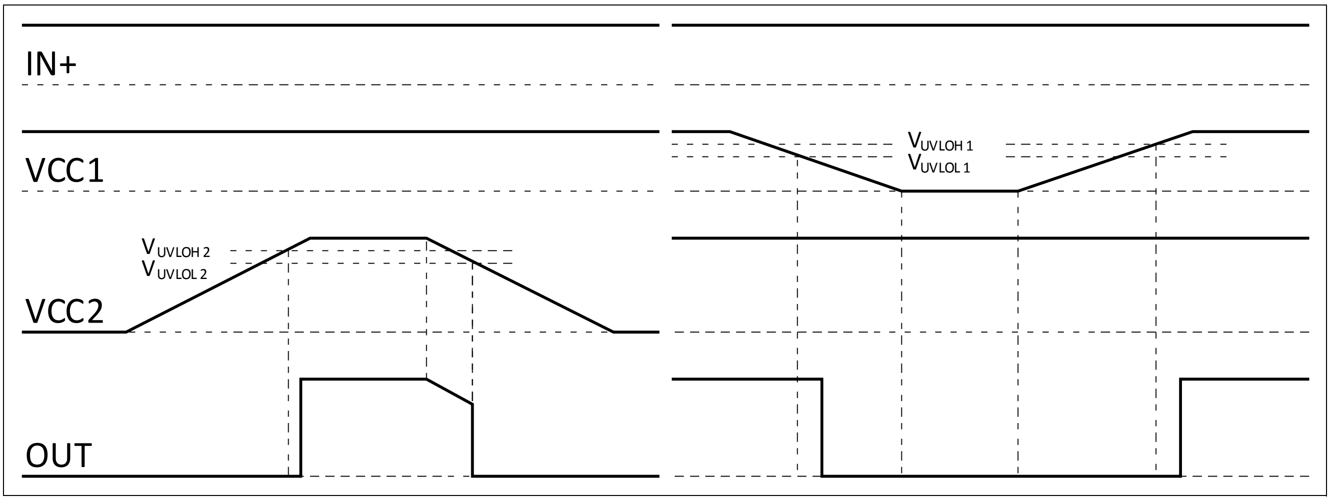

Figure 7 UVLO Behavior

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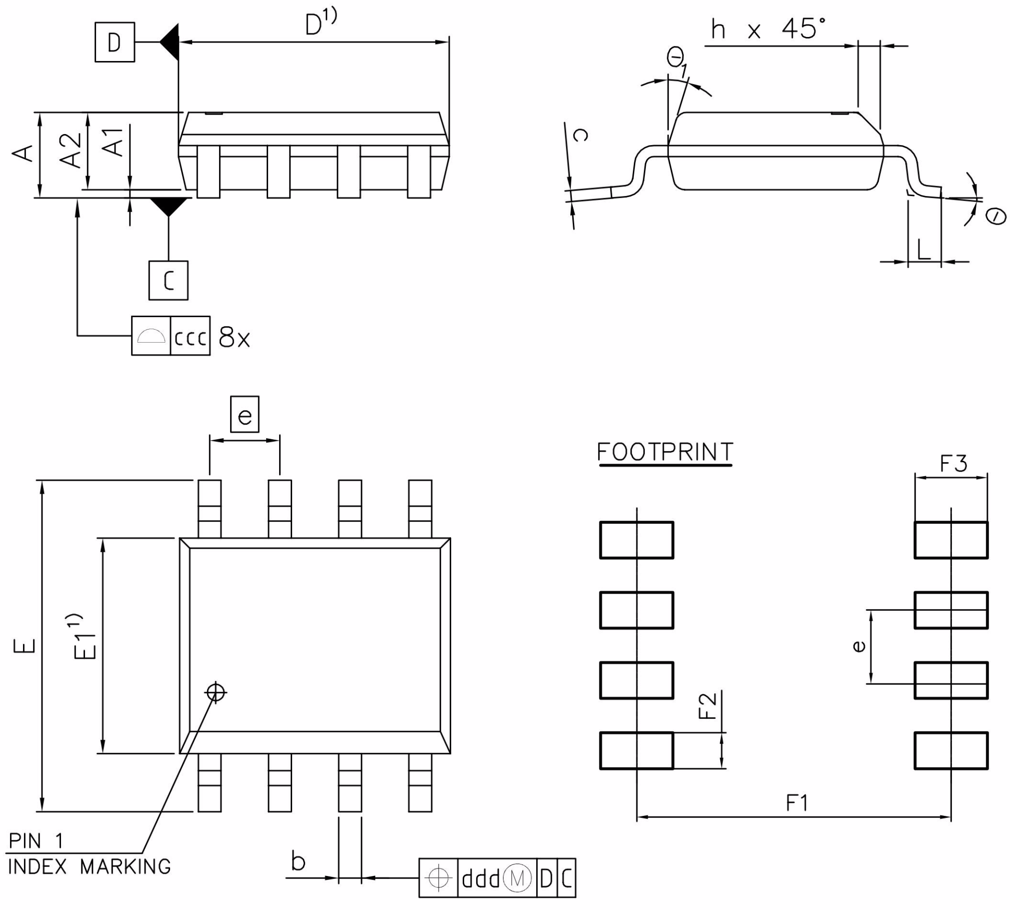
7 Package Outlines



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

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A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	0°	8°	0°	8°
Θ_1	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

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Figure 8 **PG-DSO-8-51** (Plastic (Green) Dual Small Outline Package)

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8 Application Notes

8.1 Reference Layout for Thermal Data

The PCB layout shown in **Figure 9** represents the reference layout used for the thermal characterisation. Pin 4 (GND1) and pin 8 (GND2) require each a ground plane of 100 mm² for achieving maximum power dissipation. The Output with Clamp variant for IGBT is conceived to dissipate most of the heat generated through this pins.

The thermal coefficient junction-top ($\Psi_{th,jt}$) can be used to calculate the junction temperature at a given top case temperature and driver power dissipation:

$$T_j = \Psi_{th,jt} \cdot P_D + T_{top}$$

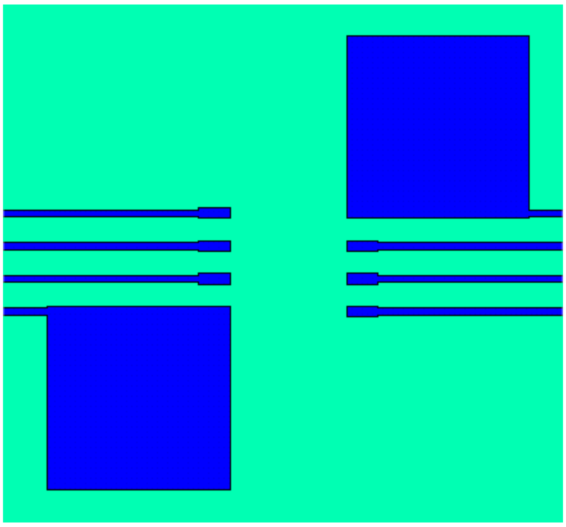

Figure 9 Reference Layout for Thermal Data (Copper thickness 35 µm)

8.2 Printed Circuit Board Guidelines

The following factors should be taken into account for an optimum PCB layout.

- Sufficient spacing should be kept between high voltage isolated side and low voltage side circuits.
- The same minimum distance between two adjacent high-side isolated parts of the PCB should be maintained to increase the effective isolation and to reduce parasitic coupling.
- In order to ensure low supply ripple and clean switching signals, bypass capacitor trace lengths should be kept as short as possible.

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