

# IRFP4710PbF

HEXFET® Power MOSFET

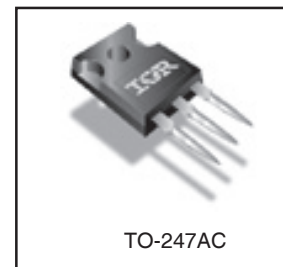
## Applications

- High frequency DC-DC converters
- Motor Control
- Uninterruptible Power Supplies
- Lead-Free

$V_{DSS}$	$R_{DS(on) \max}$	$I_D$
100V	0.014Ω	72A

## Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective  $C_{OSS}$  to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	72	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	51	
$I_{DM}$	Pulsed Drain Current ①	300	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	190	W
	Linear Derating Factor	1.2	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$dv/dt$	Peak Diode Recovery $dv/dt$ ③	8.2	V/ns
$T_J$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
$T_{STG}$			
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.81	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

Notes ① through ③ are on page 8

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1

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## Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	0.011	0.014	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 45A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	3.5	—	5.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	1.0	μA	V <sub>DS</sub> = 95V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V

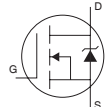
## Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	35	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 45A
Q <sub>g</sub>	Total Gate Charge	—	110	170	nC	I <sub>D</sub> = 45A
Q <sub>gs</sub>	Gate-to-Source Charge	—	43	—		V <sub>DS</sub> = 50V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	40	—		V <sub>GS</sub> = 10V,
t <sub>d(on)</sub>	Turn-On Delay Time	—	35	—	ns	V <sub>DD</sub> = 50V
t <sub>r</sub>	Rise Time	—	130	—		I <sub>D</sub> = 45A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	41	—		R <sub>G</sub> = 4.5Ω
t <sub>f</sub>	Fall Time	—	38	—		V <sub>GS</sub> = 10V ④
C <sub>iss</sub>	Input Capacitance	—	6160	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	440	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	250	—		f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	1580	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V, f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	280	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 80V, f = 1.0MHz
C <sub>oss eff.</sub>	Effective Output Capacitance	—	430	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 80V ⑤

## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy②	—	190	mJ
I <sub>AR</sub>	Avalanche Current①	—	45	A
E <sub>AR</sub>	Repetitive Avalanche Energy①	—	20	mJ

## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	72	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	300		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 45A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	74	110	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 45A
Q <sub>rr</sub>	Reverse Recovery Charge	—	180	260	nC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

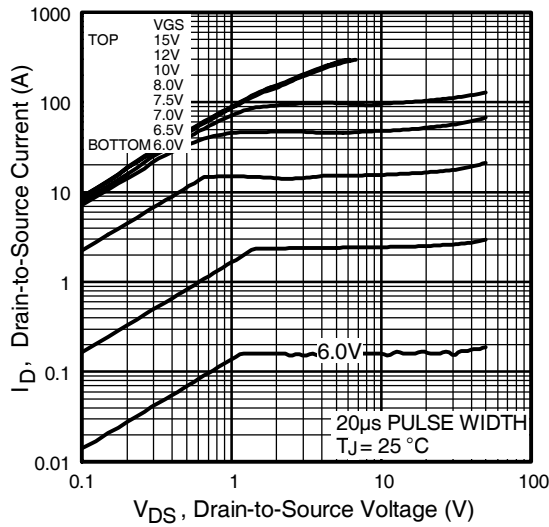


Fig 1. Typical Output Characteristics

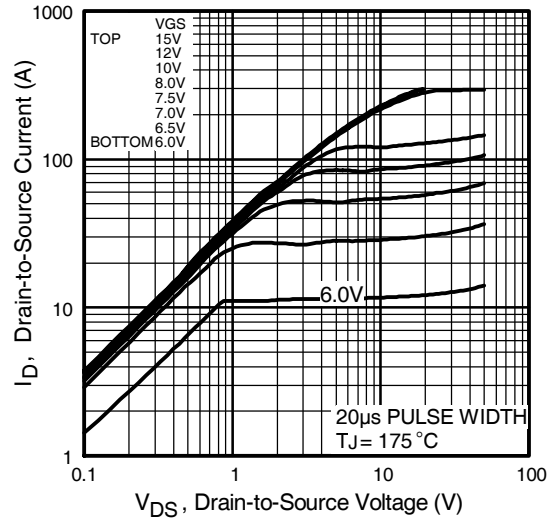


Fig 2. Typical Output Characteristics

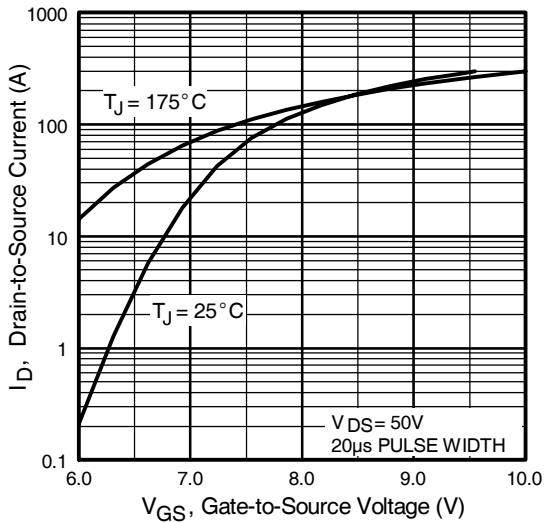


Fig 3. Typical Transfer Characteristics

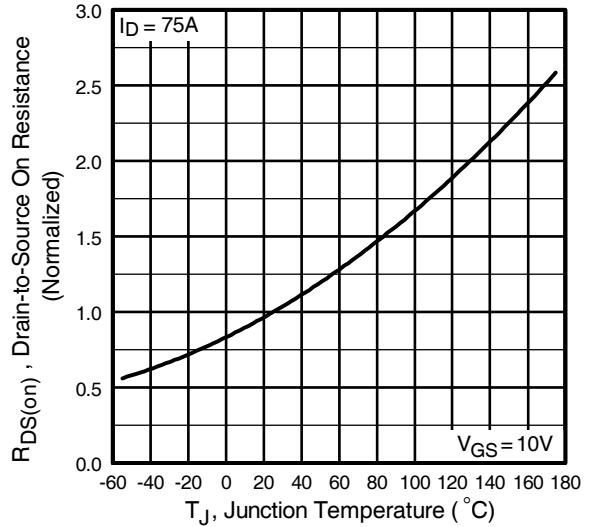
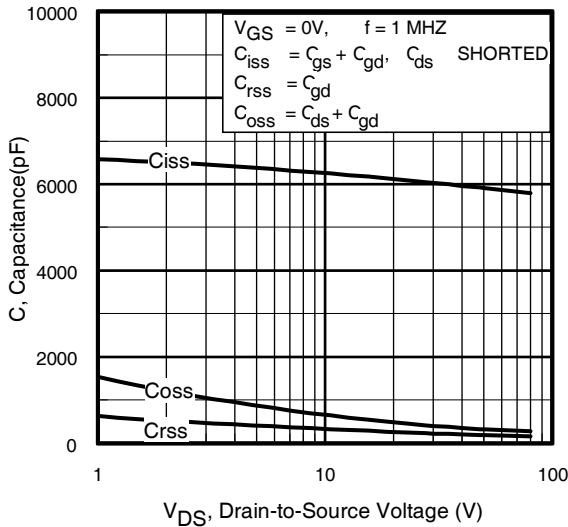


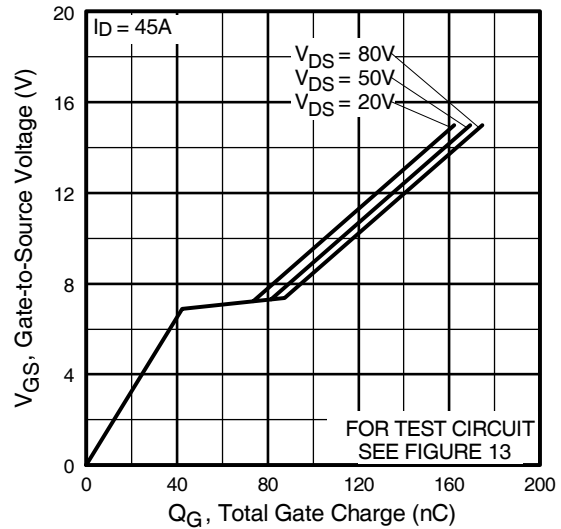
Fig 4. Normalized On-Resistance Vs. Temperature

# IRFP4710PbF

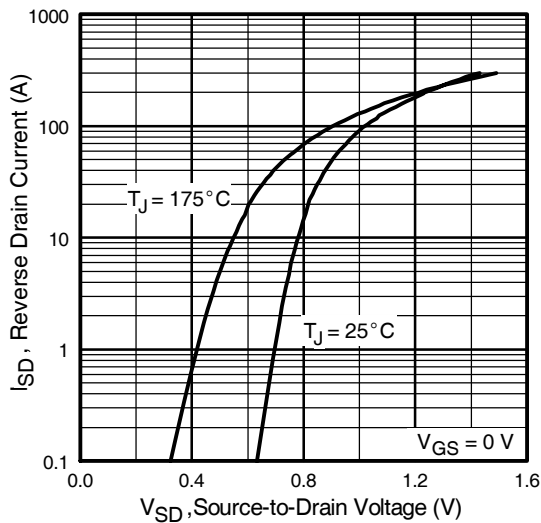
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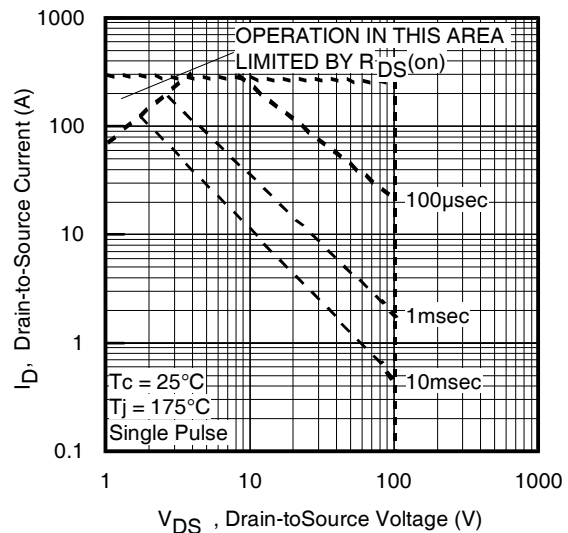
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



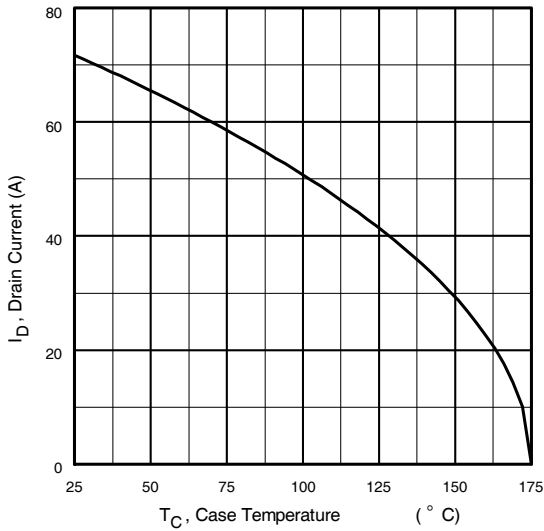
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



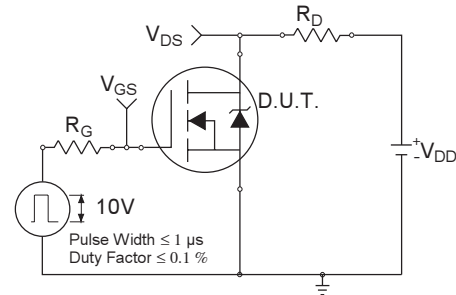
**Fig 7.** Typical Source-Drain Diode Forward Voltage



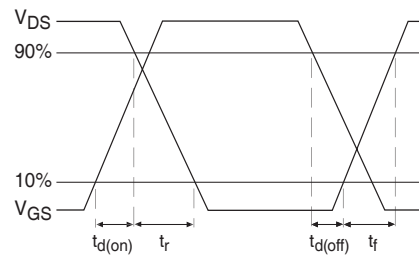
**Fig 8.** Maximum Safe Operating Area



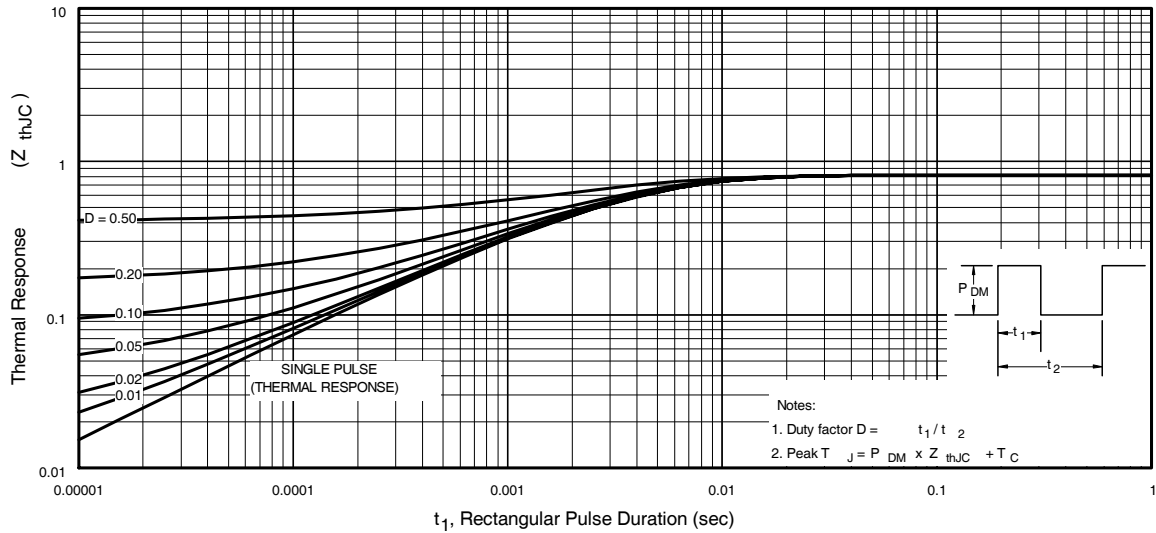
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



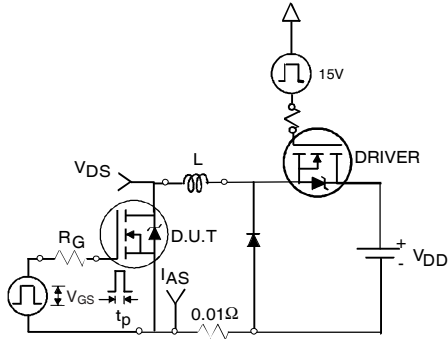
**Fig 10b.** Switching Time Waveforms



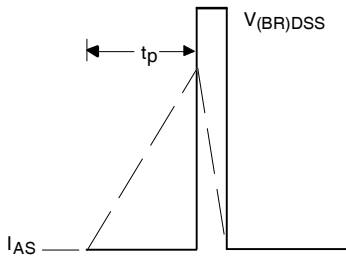
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

# IRFP4710PbF

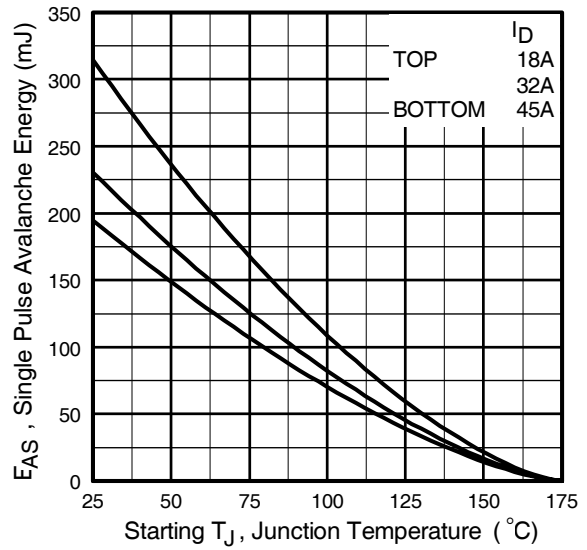
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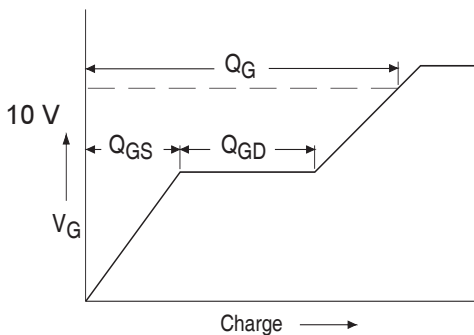
**Fig 12a.** Unclamped Inductive Test Circuit



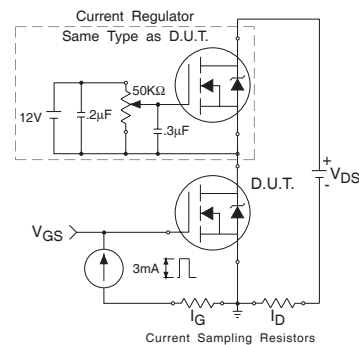
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

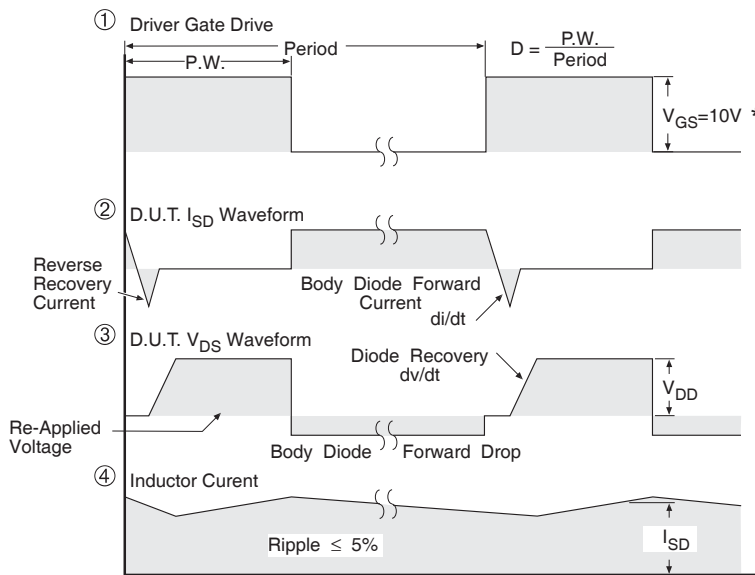
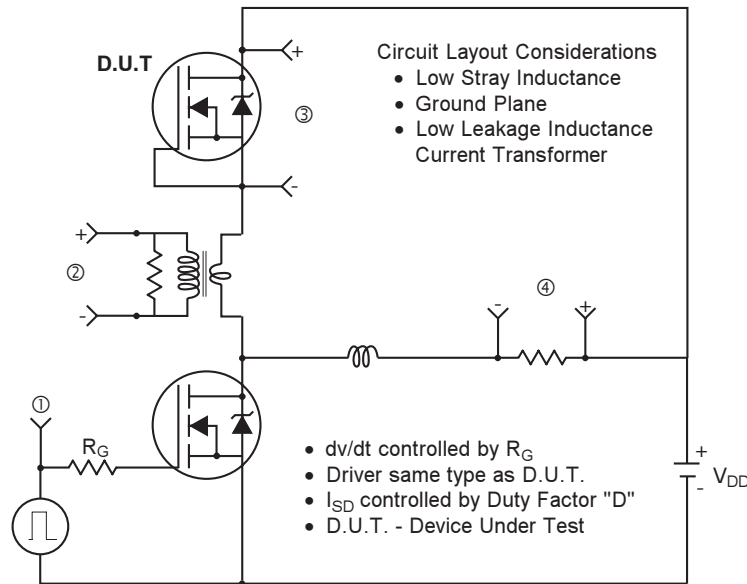


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

**Peak Diode Recovery dv/dt Test Circuit**

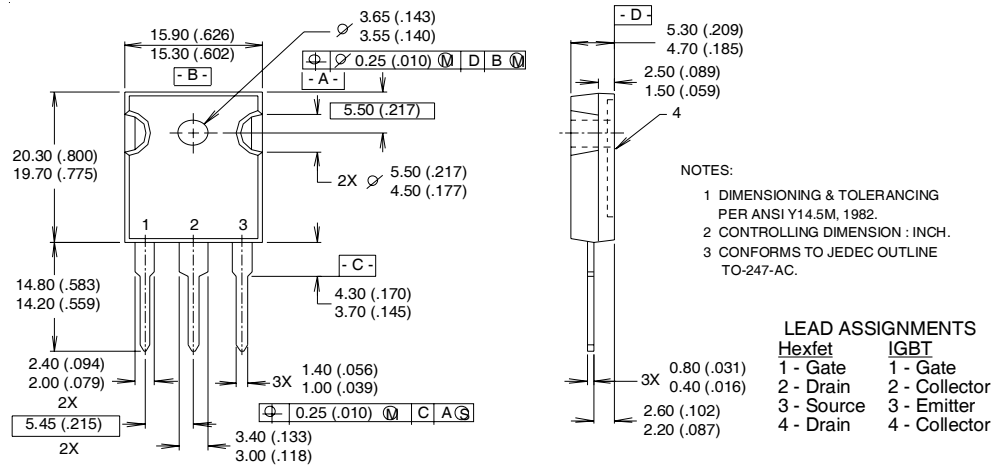


\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFET® Power MOSFETs

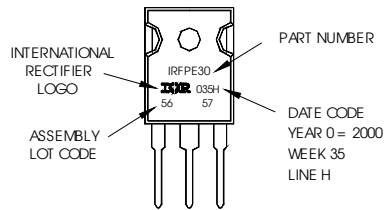
## TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



## TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30  
WITH ASSEMBLY  
LOT CODE 5667  
ASSEMBLED ON WW 35, 2000  
IN THE ASSEMBLY LINE "H"  
**Note:** "P" in assembly line  
position indicates "Lead-Free"



### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 190\mu\text{H}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 45\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ③  $I_{SD} \leq 45\text{A}$ ,  $di/dt \leq 420\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

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Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>

单击下面可查看定价，库存，交付和生命周期等信息

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