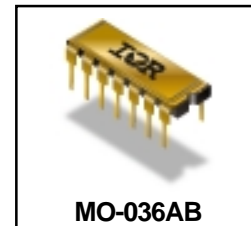


**POWER MOSFET  
 THRU-HOLE (MO-036AB)**

**IRFG5210**  
**200V, Combination 2N-2P-CHANNEL**  
**HEXFET® MOSFET TECHNOLOGY**

**Product Summary**

Part Number	RDS(on)	ID	CHANNEL
IRFG5210	1.6Ω	0.68A	N
IRFG5210	1.6Ω	-0.68A	P



**MO-036AB**

HEXFET® MOSFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance. HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and virtually any application where high reliability is required. The HEXFET transistor's totally isolated package eliminates the need for additional isolating material between the device and the heatsink. This improves thermal efficiency and reduces drain capacitance.

**Features:**

- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Dynamic dv/dt Rating
- Light-weight

**Absolute Maximum Ratings (Per Die)**

**Pre-Irradiation**

	Parameter	N-Channel	P-Channel	Units
ID @ VGS = ±10V, TC = 25°C	Continuous Drain Current	0.68	-0.68	A
ID @ VGS = ±10V, TC = 100°C	Continuous Drain Current	0.4	-0.4	
IDM	Pulsed Drain Current ①	2.72①	-2.72⑤	
PD @ TC = 25°C	Max. Power Dissipation	14	14	W
	Linear Derating Factor	0.011	0.011	W/°C
VGS	Gate-to-Source Voltage	±20	±20	V
EAS	Single Pulse Avalanche Energy	64②	110⑥	mJ
IAR	Avalanche Current ①	—	—	A
EAR	Repetitive Avalanche Energy ①	—	—	mJ
dv/dt	Peak Diode Recovery dv/dt	20③	27⑦	V/ns
TJ	Operating Junction	-55 to 150		°C
TSTG	Storage Temperature Range			
	Lead Temperature	300 (0.63 in./1.6 mm from case for 10s)		
	Weight	1.3 (Typical)		g

For footnotes refer to the last page

**Electrical Characteristics For Each N-Channel Device @ T<sub>J</sub> = 25°C (Unless Otherwise Specified)**

	Parameter	Min	Typ	Max	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	200	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Temperature Coefficient of Breakdown Voltage	—	0.27	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA
R <sub>DSON</sub>	Static Drain-to-Source On-State Resistance	—	—	1.6 1.83	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 0.4A ④ V <sub>GS</sub> = 10V, I <sub>D</sub> = 0.68A
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 0.25mA
g <sub>fs</sub>	Forward Transconductance	0.54	—	—	S (r <sub>θ</sub> )	V <sub>DS</sub> > 15V, I <sub>DS</sub> = 0.4A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	25 250	μA	V <sub>DS</sub> = 160V, V <sub>GS</sub> = 0V V <sub>DS</sub> = 160V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	100	nA	V <sub>GS</sub> = 20V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	—	-100	nA	V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	—	—	9.5	nC	V <sub>GS</sub> = 10V, I <sub>D</sub> = 0.68A, V <sub>DS</sub> = 100V
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	1.4		
Q <sub>gd</sub>	Gate-to-Drain ('Miller') Charge	—	—	4.3		
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	8.7	ns	V <sub>DD</sub> = 100V, I <sub>D</sub> = 0.68A, V <sub>GS</sub> = 10V, R <sub>G</sub> = 7.5Ω
t <sub>r</sub>	Rise Time	—	—	2.4		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	19		
t <sub>f</sub>	Fall Time	—	—	24		
L <sub>S</sub> + L <sub>D</sub>	Total Inductance	—	10	—	nH	Measured from drain lead (6mm/ 0.25in. from package) to source lead (6mm/0.25in. from package)
C <sub>iss</sub>	Input Capacitance	—	140	—	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	56	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	14	—		

**Source-Drain Diode Ratings and Characteristics (Per Die)**

	Parameter	Min	Typ	Max	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	0.63	A	T <sub>J</sub> = 25°C, I <sub>S</sub> = 0.68A, V <sub>GS</sub> = 0V ④
I <sub>SM</sub>	Pulse Source Current (Body Diode) ①	—	—	2.5		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.5	V	T <sub>J</sub> = 25°C, I <sub>F</sub> = 0.68A, di/dt ≤ 100A/μs
t <sub>rr</sub>	Reverse Recovery Time	—	—	110	nS	V <sub>DD</sub> ≤ 50V ④
Q <sub>RR</sub>	Reverse Recovery Charge	—	—	310	nC	
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L <sub>S</sub> + L <sub>D</sub> .				

**Thermal Resistance (Per Die)**

	Parameter	Min	Typ	Max	Units	Test Conditions
R <sub>thJC</sub>	Junction-to-Case	—	—	17	°C/W	Typical socket mount
R <sub>thJA</sub>	Junction-to-Ambient	—	—	90		

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page

**Electrical Characteristics For Each P-Channel Device @ T<sub>j</sub> = 25°C (Unless Otherwise Specified)**

	Parameter	Min	Typ	Max	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	-200	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -1.0mA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Temperature Coefficient of Breakdown Voltage	—	-0.22	—	V/°C	Reference to 25°C, I <sub>D</sub> = -1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance	—	—	1.6 1.83	Ω	V <sub>GS</sub> = -10V, I <sub>D</sub> = -0.4A V <sub>GS</sub> = -10V, I <sub>D</sub> = -0.68A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	-2.0	—	-4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -0.25mA
g <sub>fs</sub>	Forward Transconductance	0.64	—	—	S (τ)	V <sub>DS</sub> > -15V, I <sub>DS</sub> = -0.4A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	-25 -250	μA	V <sub>DS</sub> = -160V, V <sub>GS</sub> = 0V V <sub>DS</sub> = -160V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	-100	nA	V <sub>GS</sub> = -20V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	—	100	nA	V <sub>GS</sub> = 20V
Q <sub>g</sub>	Total Gate Charge	—	—	18	nC	V <sub>GS</sub> = -10V, I <sub>D</sub> = -0.68A, V <sub>DS</sub> = -100V
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	2.8	nC	
Q <sub>gd</sub>	Gate-to-Drain ('Miller') Charge	—	—	8.4	nC	
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	15	ns	V <sub>DD</sub> = -100V, I <sub>D</sub> = -0.68A, V <sub>GS</sub> = -10V, R <sub>G</sub> = 7.5Ω
t <sub>r</sub>	Rise Time	—	—	11		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	36		
t <sub>f</sub>	Fall Time	—	—	43		
L <sub>S</sub> + L <sub>D</sub>	Total Inductance	—	10	—	nH	Measured from drain lead (6mm/ 0.25in. from package) to source lead (6mm/0.25in. from package)
C <sub>iss</sub>	Input Capacitance	—	320	—	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -25V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	110	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	20	—		

**Source-Drain Diode Ratings and Characteristics (Per Die)**

	Parameter	Min	Typ	Max	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	-0.61	A	
I <sub>SM</sub>	Pulse Source Current (Body Diode) ①	—	—	-2.4		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-4.8	V	T <sub>j</sub> = 25°C, I <sub>S</sub> = -0.68A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	—	120	nS	T <sub>j</sub> = 25°C, I <sub>F</sub> = -0.68A, di/dt ≤ -100A/μs
Q <sub>RR</sub>	Reverse Recovery Charge	—	—	420	nC	V <sub>DD</sub> ≤ -50V ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L <sub>S</sub> + L <sub>D</sub> .				

**Thermal Resistance (Per Die)**

	Parameter	Min	Typ	Max	Units	Test Conditions
R <sub>thJC</sub>	Junction-to-Case	—	—	17	°C/W	Typical socket mount
R <sub>thJA</sub>	Junction-to-Ambient	—	—	90		

For footnotes refer to the last page

N-Channel  
Q1,Q3

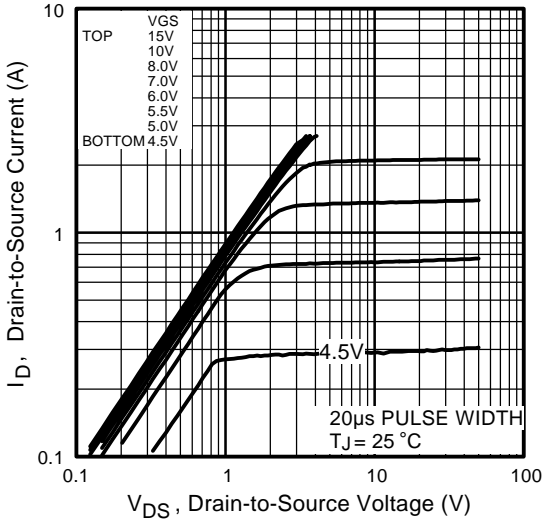


Fig 1. Typical Output Characteristics

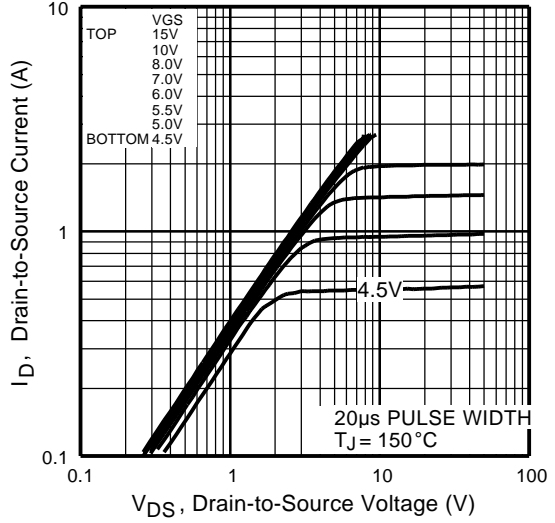


Fig 2. Typical Output Characteristics

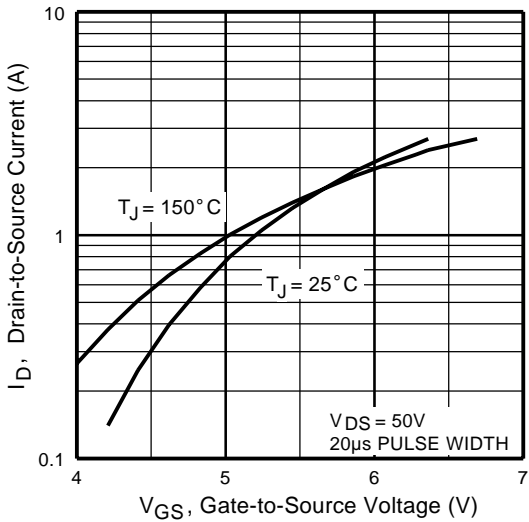


Fig 3. Typical Transfer Characteristics

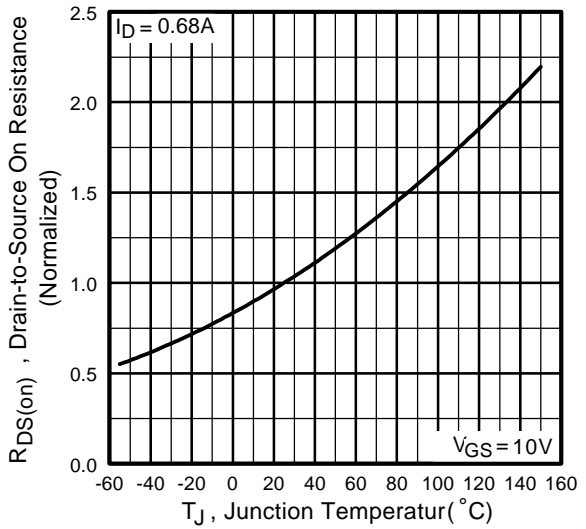


Fig 4. Normalized On-Resistance Vs. Temperature

N-Channel  
Q1,Q3

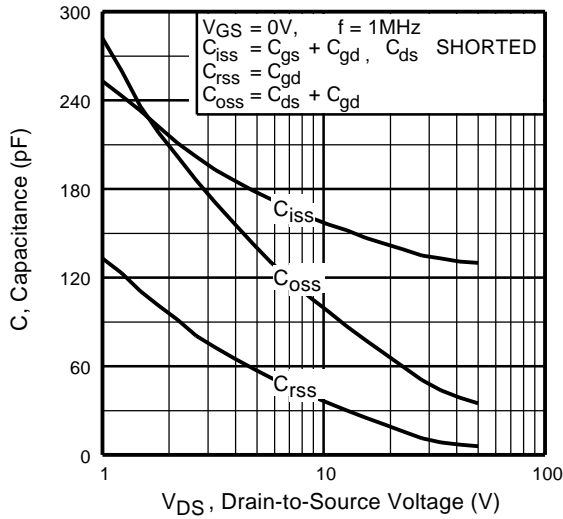


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

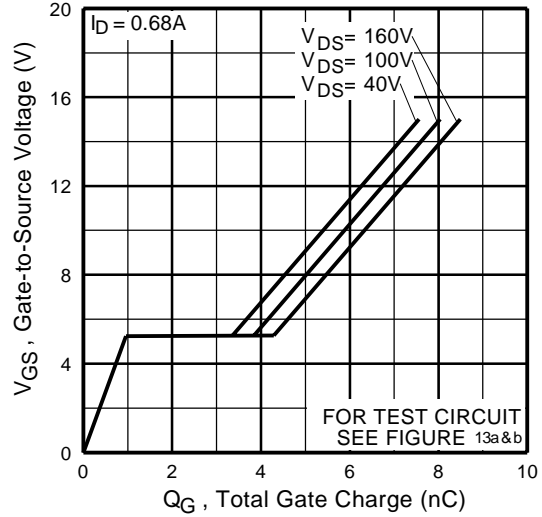


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

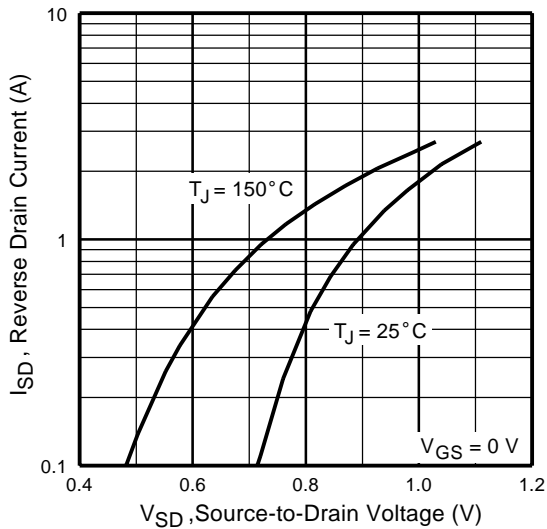


Fig 7. Typical Source-Drain Diode Forward Voltage

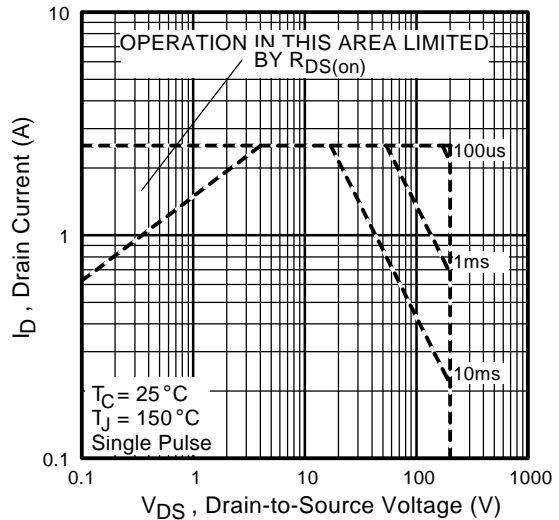


Fig 8. Maximum Safe Operating Area

N-Channel  
Q1,Q3

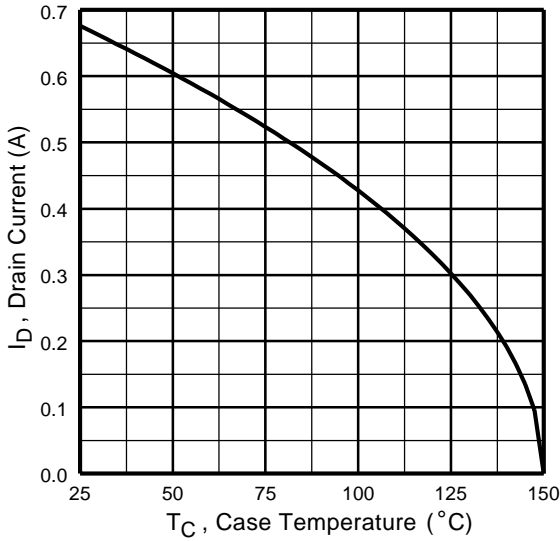


Fig 9. Maximum Drain Current Vs. Case Temperature

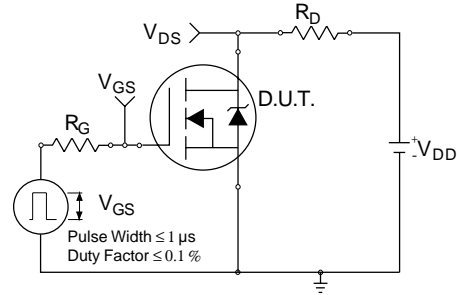


Fig 10a. Switching Time Test Circuit

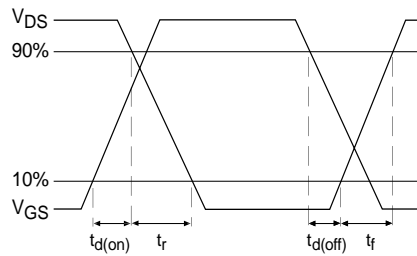


Fig 10b. Switching Time Waveforms

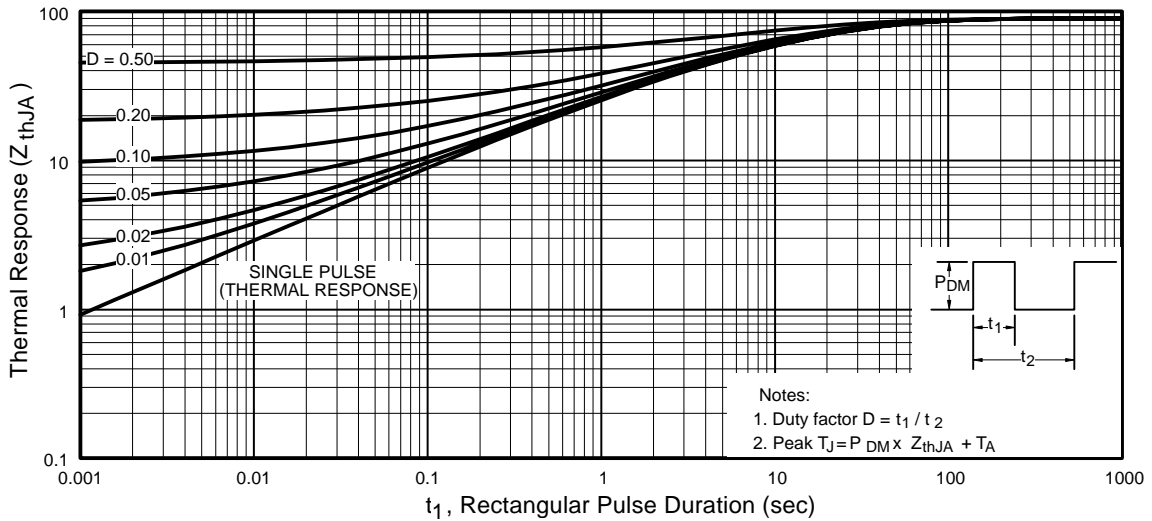
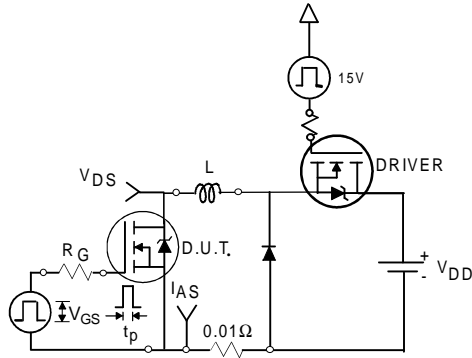
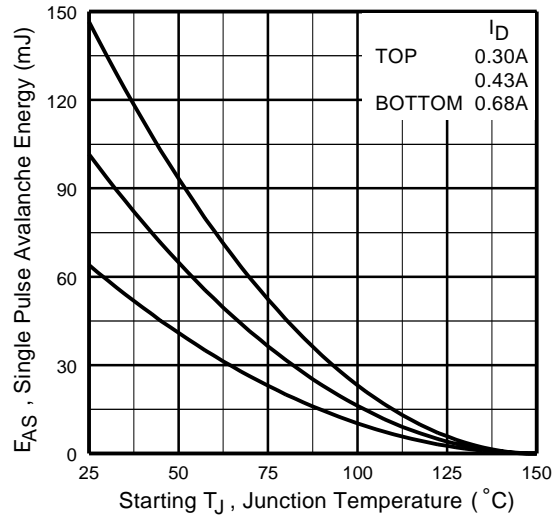


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

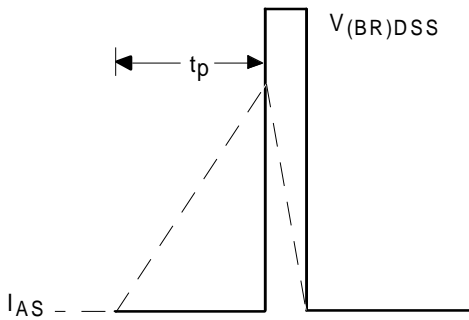
**N-Channel  
Q1,Q3**



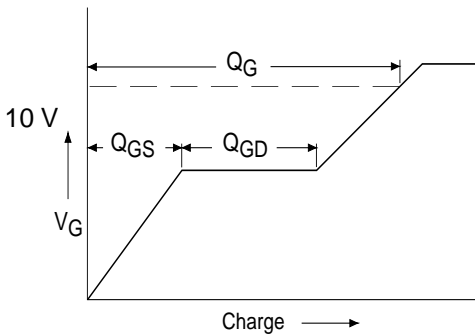
**Fig 12a.** Unclamped Inductive Test Circuit



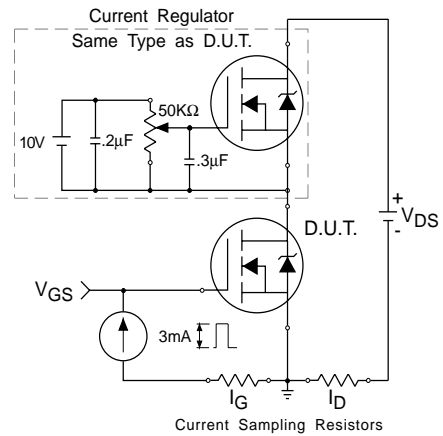
**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 12b.** Unclamped Inductive Waveforms

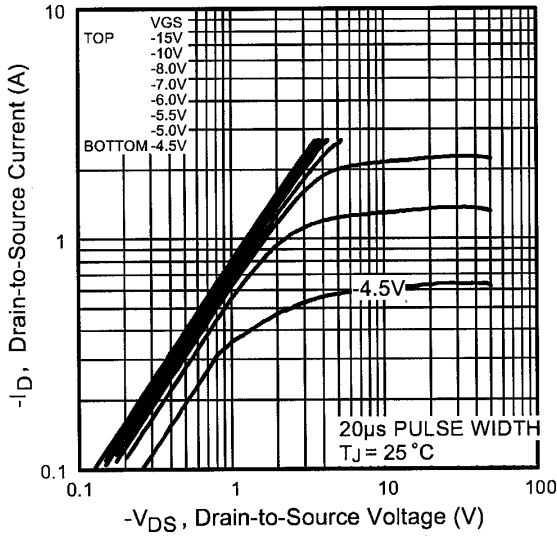


**Fig 13a.** Basic Gate Charge Waveform

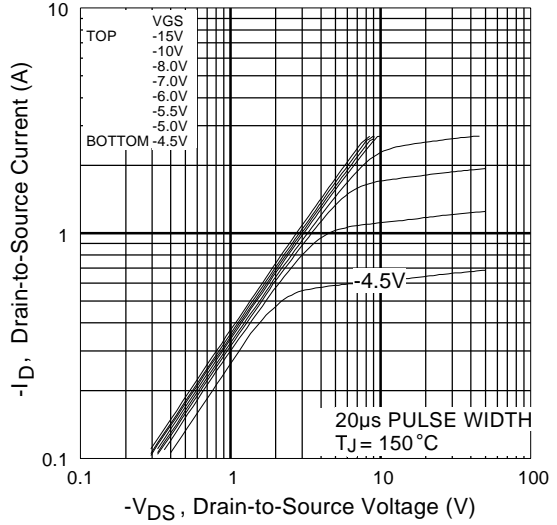


**Fig 13b.** Gate Charge Test Circuit

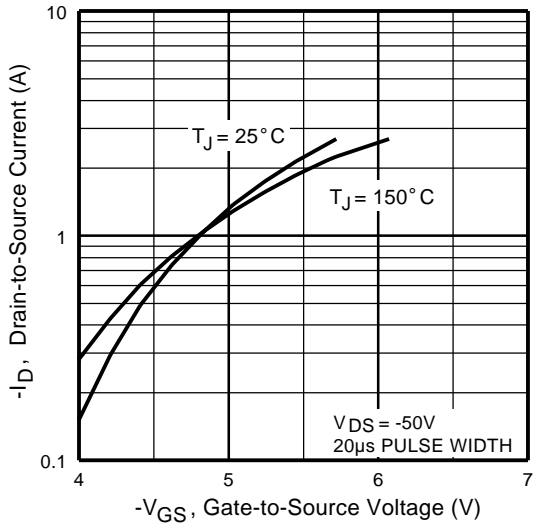
**P-Channel  
Q2,Q4**



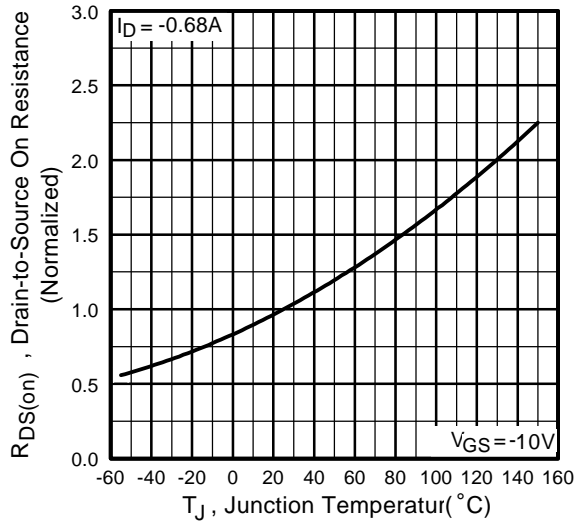
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics



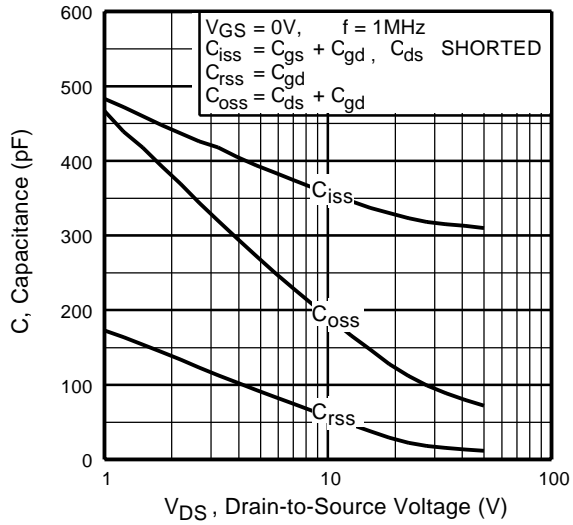
**Fig 3.** Typical Transfer Characteristics



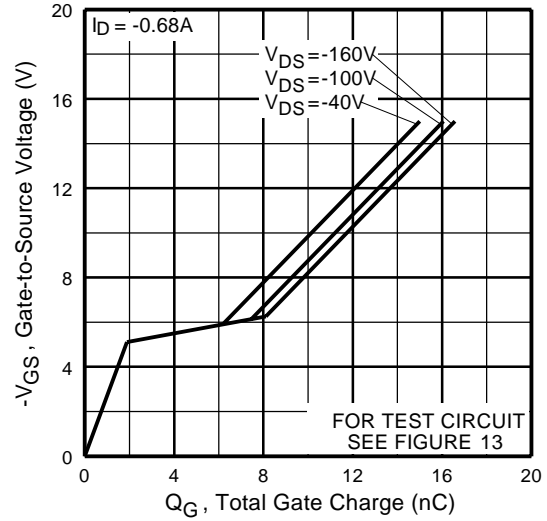
**Fig 4.** Normalized On-Resistance Vs. Temperature



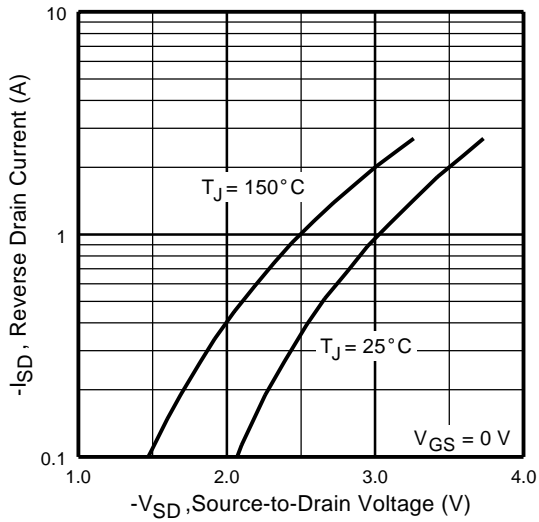
**P-Channel  
Q2,Q4**



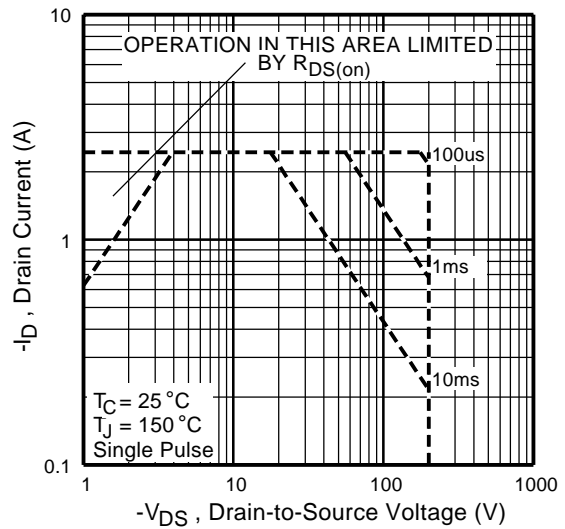
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

P-Channel  
Q2,Q4

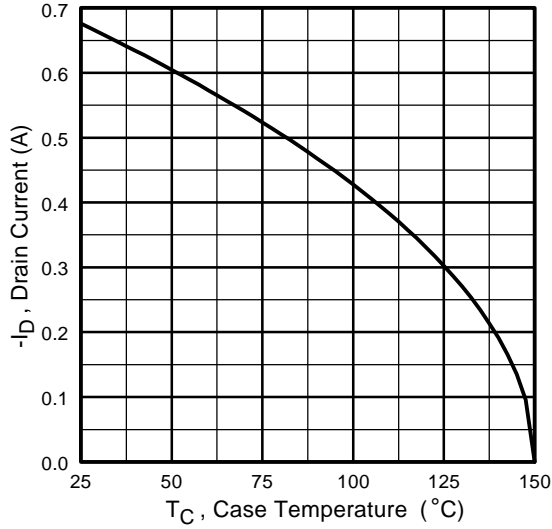


Fig 9. Maximum Drain Current Vs. Case Temperature

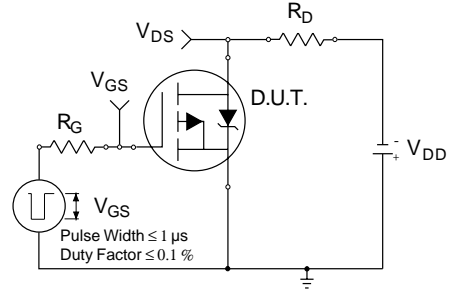


Fig 10a. Switching Time Test Circuit

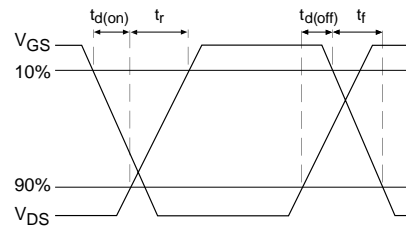


Fig 10b. Switching Time Waveforms

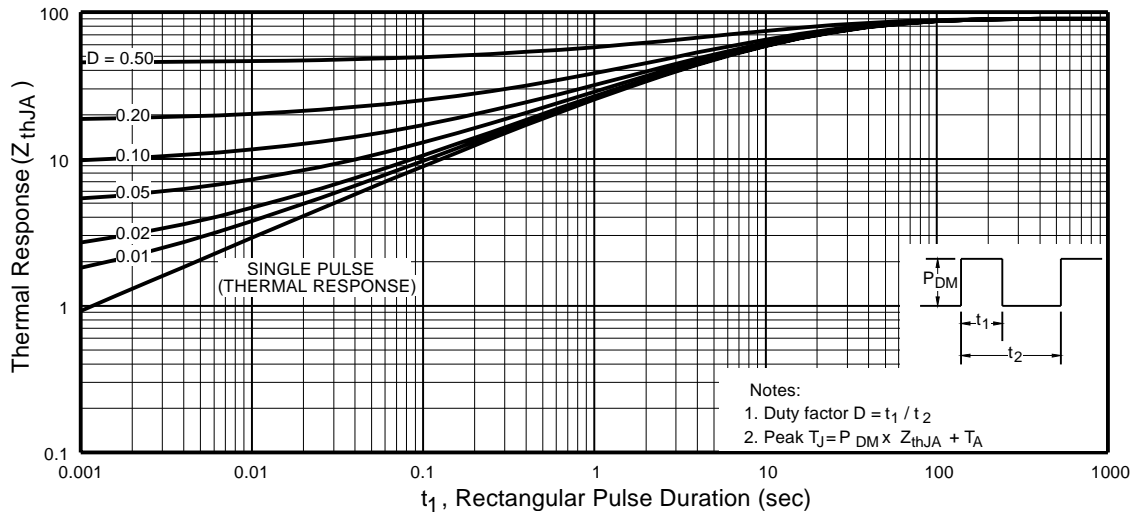
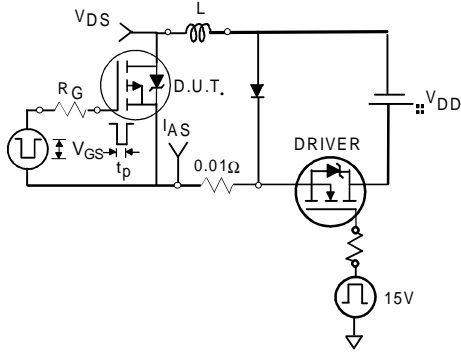
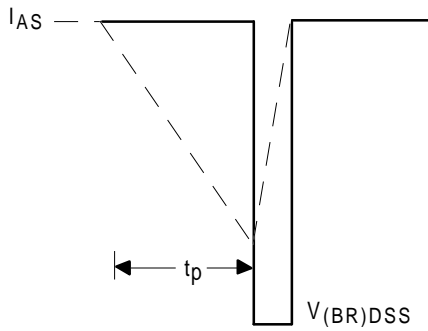


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

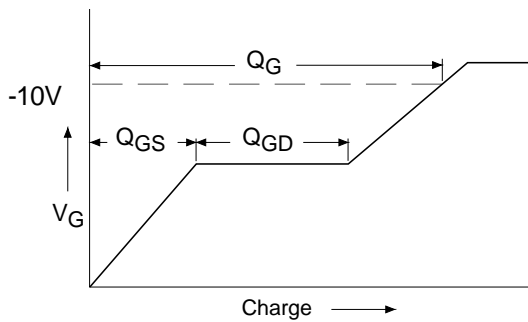
**P-Channel  
Q2,Q4**



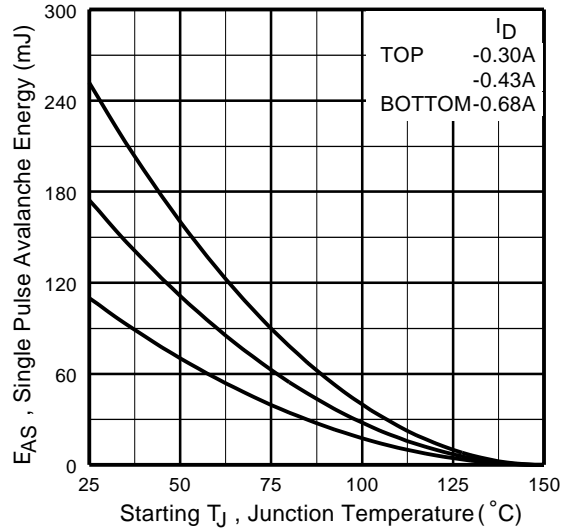
**Fig 12a.** Unclamped Inductive Test Circuit



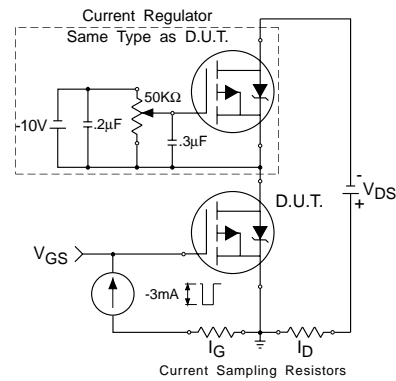
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

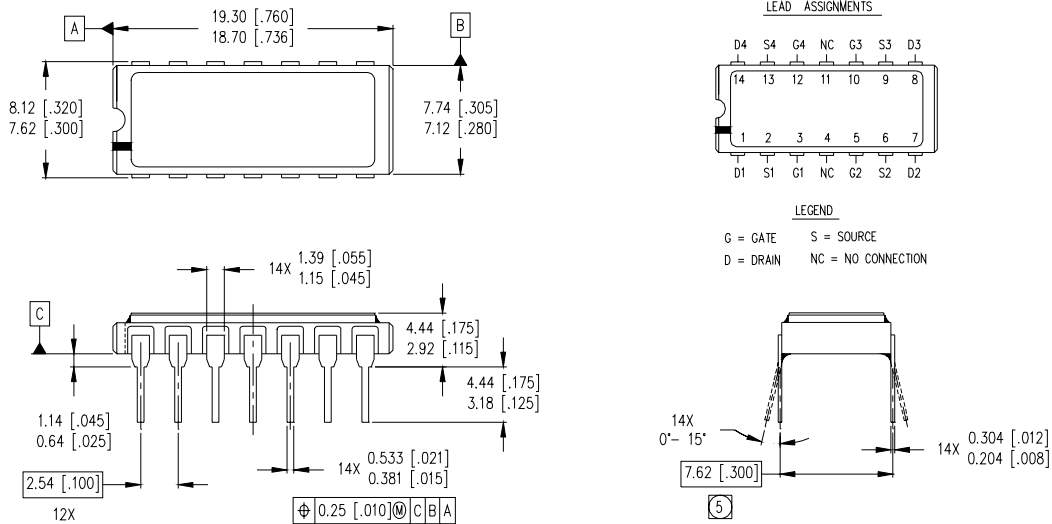
# IRFG5210

International  
**IR** Rectifier

## Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ②  $V_{DD} = 50V$ , starting  $T_J = 25^\circ C$ ,  $L = 276mH$ , Peak  $I_L = 0.68A$ ,  $V_{GS} = 10V$
- ③  $I_{SD} \leq 0.68A$ ,  $di/dt \leq 290A/\mu s$ ,  $V_{DD} \leq 200V$ ,  $T_J \leq 150^\circ C$
- ④ Pulse width  $\leq 300 \mu s$ ; Duty Cycle  $\leq 2\%$
- ⑤ Repetitive Rating; Pulse width limited by maximum junction temperature.
- ⑥  $V_{DD} = -50V$ , starting  $T_J = 25^\circ C$ ,  $L = 475mH$ , Peak  $I_L = -0.68A$ ,  $V_{GS} = -10V$
- ⑦  $I_{SD} \leq -0.68A$ ,  $di/dt \leq -290A/\mu s$ ,  $V_{DD} \leq -200V$ ,  $T_J \leq 150^\circ C$

## Case Outline and Dimensions — MO-036AB



### NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MO-036AB.
- ⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

International  
**IR** Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903

Visit us at [www.irf.com](http://www.irf.com) for sales contact information.  
Data and specifications subject to change without notice. 04/02

单击下面可查看定价，库存，交付和生命周期等信息

[>>Infineon Technologies\(英飞凌\)](#)