

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ C6

650V CoolMOS™ C6 Power Transistor
IPx65R380C6

Data Sheet

Rev. 2.1
Final

Power Management & Multimarket

650V CoolMOS™ C6 Power Transistor

IPD65R380C6, IPI65R380C6
IPB65R380C6, IPP65R380C6
IPA65R380C6

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ C6 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter, and cooler.

Features

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- JEDEC¹⁾ qualified, Pb-free plating, Halogen free²⁾

Applications

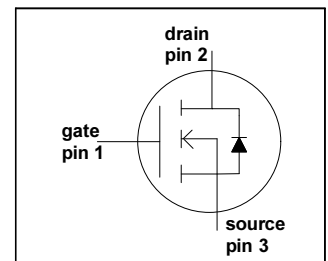
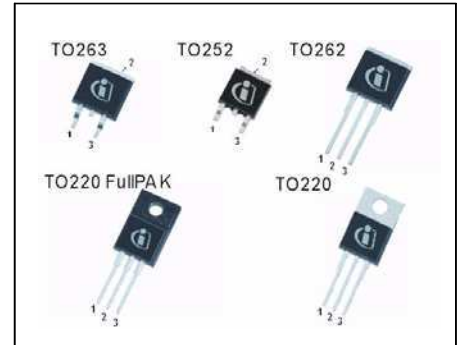
PFC stages, hard switching PWM stages and resonant switching PWM stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	0.38	Ω
$Q_{g,typ}$	39	nC
$I_{D,pulse}$	29	A
$E_{oss} @ 400V$	2.8	μJ
Body diode di/dt	500	$A/\mu s$

Type / Ordering Code	Package	Marking	Related Links
IPD65R380C6	PG-TO252	65C6380	IFX CoolMOS Webpage IFX Design tools
IPI65R380C6	PG-TO262		
IPB65R380C6	PG-TO263		
IPP65R380C6	PG-TO220		
IPA65R380C6	PG-TO220 FullPAK		



1) J-STD20 and JESD22
2) no PG-To252

Table of Contents

1	Description	2
	Table of Contents	3
2	Maximum ratings	4
3	Thermal characteristics	5
4	Electrical characteristics	6
5	Electrical characteristics diagrams	8
6	Test circuits	13
7	Package outlines	14
8	Revision History	19

2 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	10.6	A	$T_C = 25\text{ °C}$
				6.7		$T_C = 100\text{ °C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	29	A	$T_C = 25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	215	mJ	$I_D = 1.8\text{ A}, V_{DD} = 50\text{ V}$ (see table 21)
Avalanche energy, repetitive	E_{AR}	-	-	0.32		$I_D = 1.8\text{ A}, V_{DD} = 50\text{ V}$
Avalanche current, repetitive	I_{AR}	-	-	1.8	A	
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS} = 0 \dots 480\text{ V}$
Gate source voltage	V_{GS}	-20	-	20	V	static
		-30		30		AC ($f > 1\text{ Hz}$)
Power dissipation for TO-220, TO-252, TO-262, TO-263	P_{tot}	-	-	83	W	$T_C = 25\text{ °C}$
Power dissipation for TO-220 FullPAK	P_{tot}	-	-	31	W	$T_C = 25\text{ °C}$
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	
Mounting torque TO-220		-	-	60	Ncm	M3 and M3.5 screws
Mounting torque TO-220 FullPAK				50		M2.5 screws
Continuous diode forward current	I_S	-	-	9.2	A	$T_C = 25\text{ °C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	29	A	$T_C = 25\text{ °C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS} = 0 \dots 480\text{ V}, I_{SD} \leq I_D,$ $T_j = 125\text{ °C}$
Maximum diode commutation speed ³⁾	di/dt			500	A/μs	

1) Limited by $T_{j,max}$. Maximum duty cycle $D = 0.75$

2) Pulse width t_p limited by $T_{j,max}$

3) Identical low side and high side switch with identical R_G

3 Thermal characteristics

Table 3 Thermal characteristics TO-220 & TO-262

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.5	°C/W	leaded
Thermal resistance, junction - ambient	R_{thJA}	-	-	62		
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6 mm (0.063 in.) from case for 10 s

Table 4 Thermal characteristics TO-220FullPAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.0	°C/W	leaded
Thermal resistance, junction - ambient	R_{thJA}	-	-	80		
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6 mm (0.063 in.) from case for 10 s

Table 5 Thermal characteristics TO-263 & TO-252

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.5	°C/W	SMD version, device on PCB, minimal footprint
Thermal resistance, junction - ambient	R_{thJA}	-	-	62		
				35		
Soldering temperature, wave- & reflowsoldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

1) Device on 40mm*40mm*1.5 epoxy PCB FR4 with 6cm² (one layer, 70µm thick) copper area for drain connection. PCB is vertical without air stream cooling.

4 Electrical characteristics

Electrical characteristics, at $T_J=25\text{ °C}$, unless otherwise specified

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0\text{ V}, I_D=1.0\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5		$V_{DS}=V_{GS}, I_D=0.32\text{ mA}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=600\text{ V}, V_{GS}=0\text{ V}, T_J=25\text{ °C}$
		-	10	-		$V_{DS}=600\text{ V}, V_{GS}=0\text{ V}, T_J=150\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.34	0.38	Ω	$V_{GS}=10\text{ V}, I_D=3.2\text{ A}, T_J=25\text{ °C}$
		-	0.89	-		$V_{GS}=10\text{ V}, I_D=3.2\text{ A}, T_J=150\text{ °C}$
Gate resistance	R_G	-	17	-	Ω	$f=1\text{ MHz}, \text{open drain}$

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	
		Min.	Typ.	Max.			
Input capacitance	C_{iss}	-	710	-	pF	$V_{GS}=0\text{ V}, V_{DS}=100\text{ V}, f=1\text{ MHz}$	
Output capacitance	C_{oss}	-	41	-			
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	32	-			$V_{GS}=0\text{ V}, V_{DS}=0\dots480\text{ V}$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	140	-			$I_D=\text{constant}, V_{GS}=0\text{ V}, V_{DS}=0\dots480\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	12	-	ns	$V_{DD}=400\text{ V}, V_{GS}=13\text{ V}, I_D=4.9\text{ A}, R_G=3.4\text{ }\Omega$ (see table 20)	
Rise time	t_r	-	12	-			
Turn-off delay time	$t_{d(off)}$	-	110	-			
Fall time	t_f	-	11	-			

1) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

2) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	4	-	nC	$V_{DD}=480\text{ V}$, $I_D=4.9\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	20	-		
Gate charge total	Q_g	-	39	-		
Gate plateau voltage	$V_{plateau}$	-	5.5	-	V	

Table 9 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0\text{ V}$, $I_F=4.9\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	280	-	ns	$V_R=400\text{ V}$, $I_F=4.9\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$ (see table 22)
Reverse recovery charge	Q_{rr}	-	2.8	-	μC	
Peak reverse recovery current	I_{rrm}	-	17	-	A	

5 Electrical characteristics diagrams

Table 10

Power dissipation Non FullPAK	Power dissipation FullPAK
$P_{tot} = f(T_C)$	$P_{tot} = f(T_C)$

Table 11

Max. transient thermal impedance Non FullPAK	Max. transient thermal impedance FullPAK
$Z_{(thJC)} = f(t_p)$; parameter: $D = t_p / T$	$Z_{(thJC)} = f(t_p)$; parameter: $D = t_p / T$

Table 12

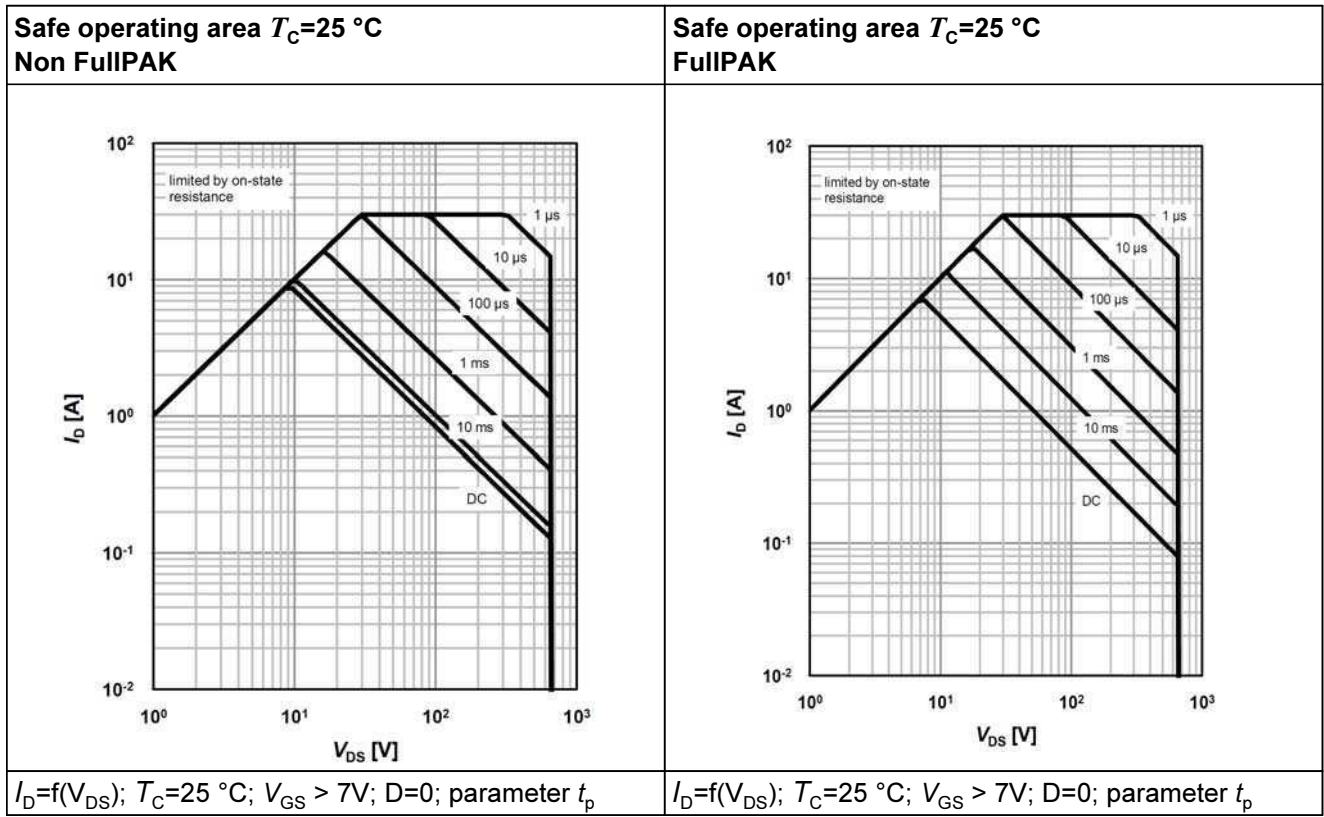


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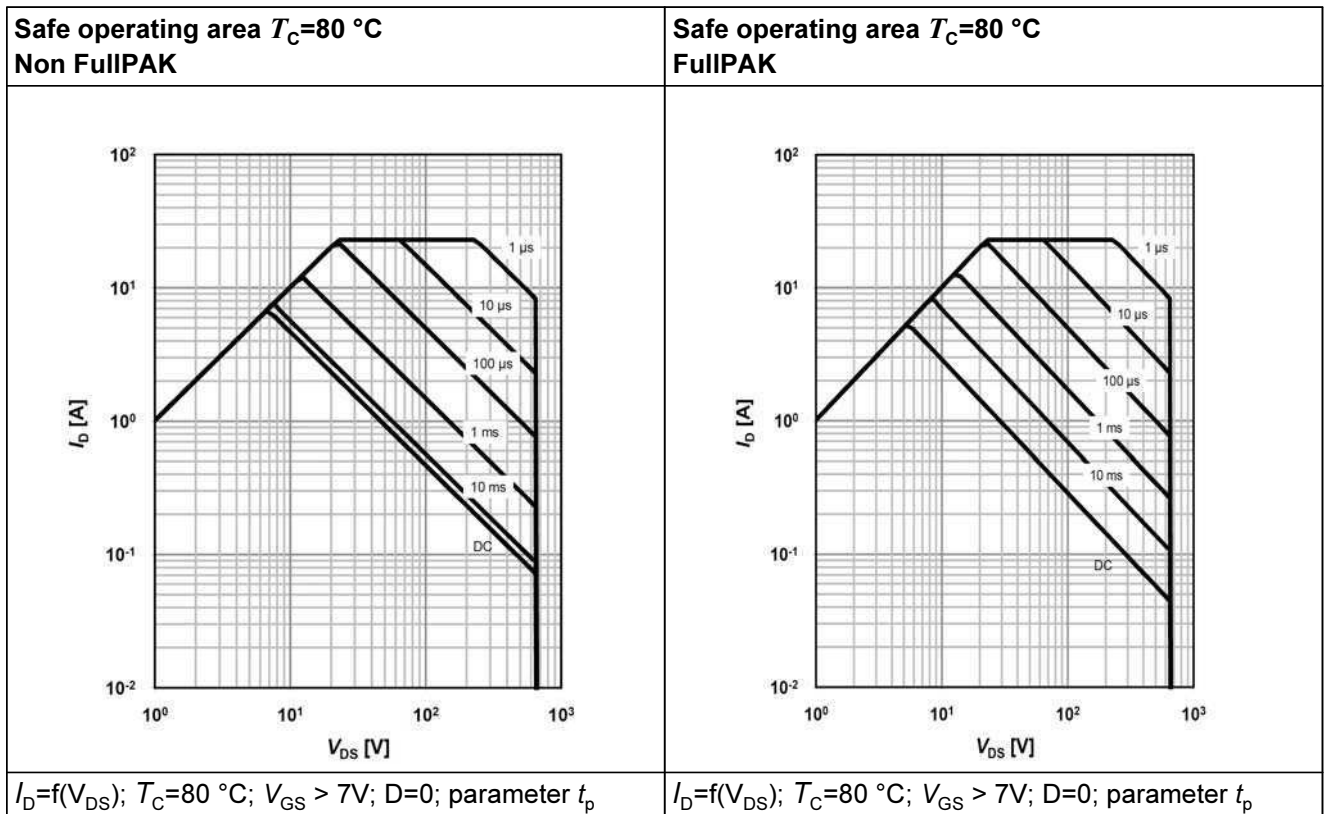


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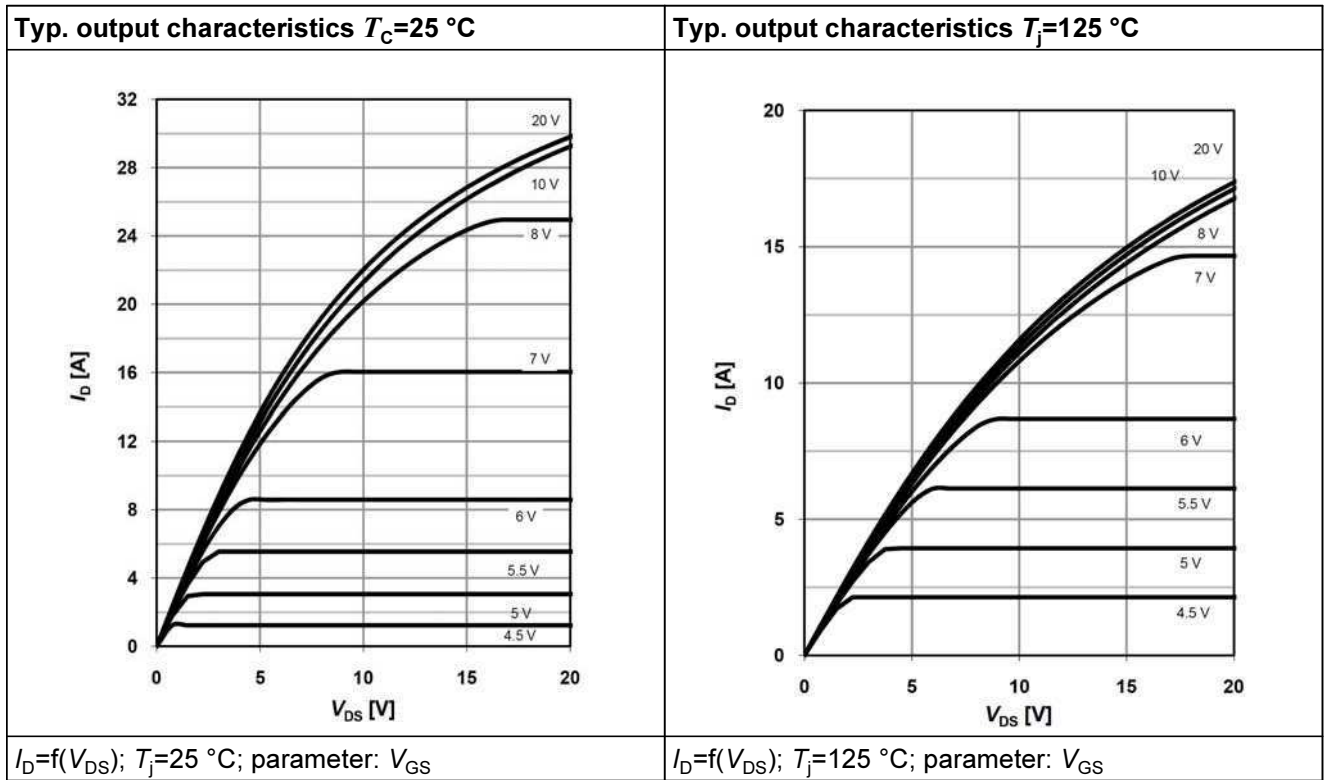


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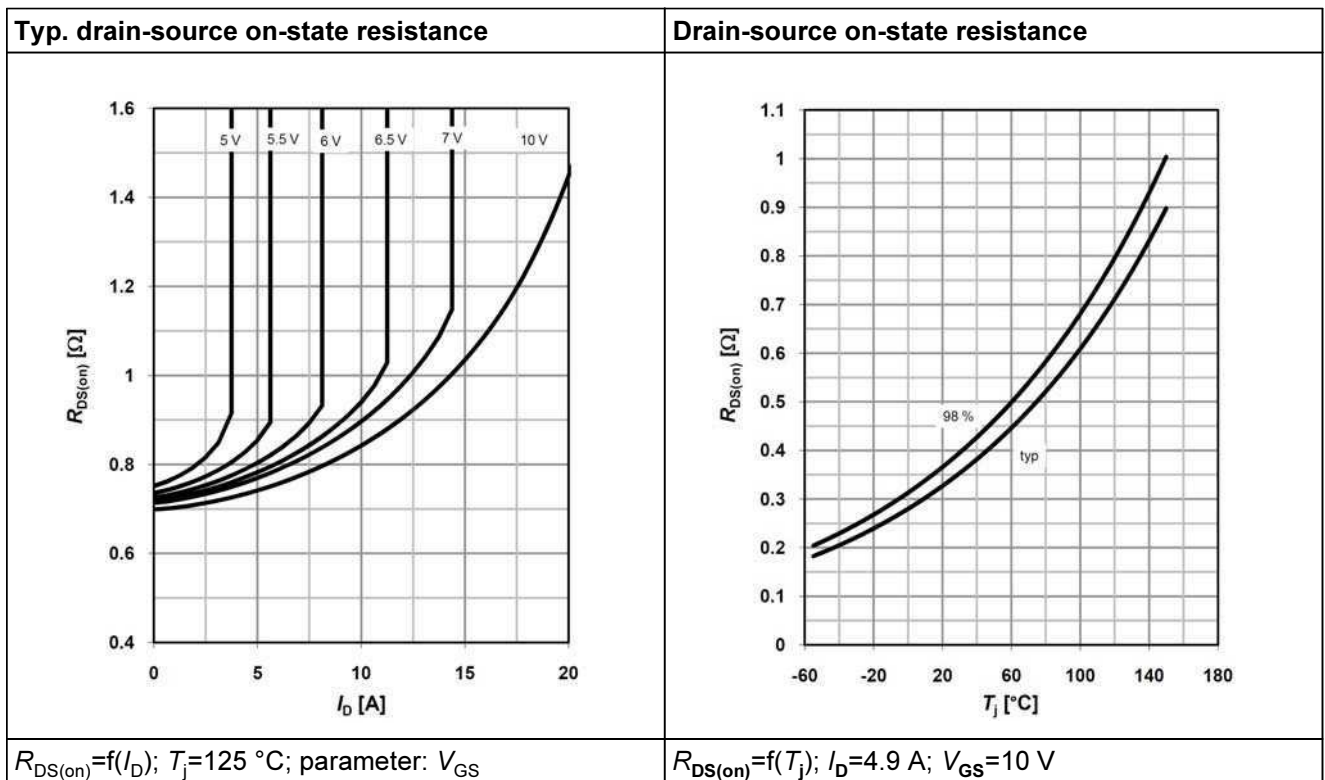


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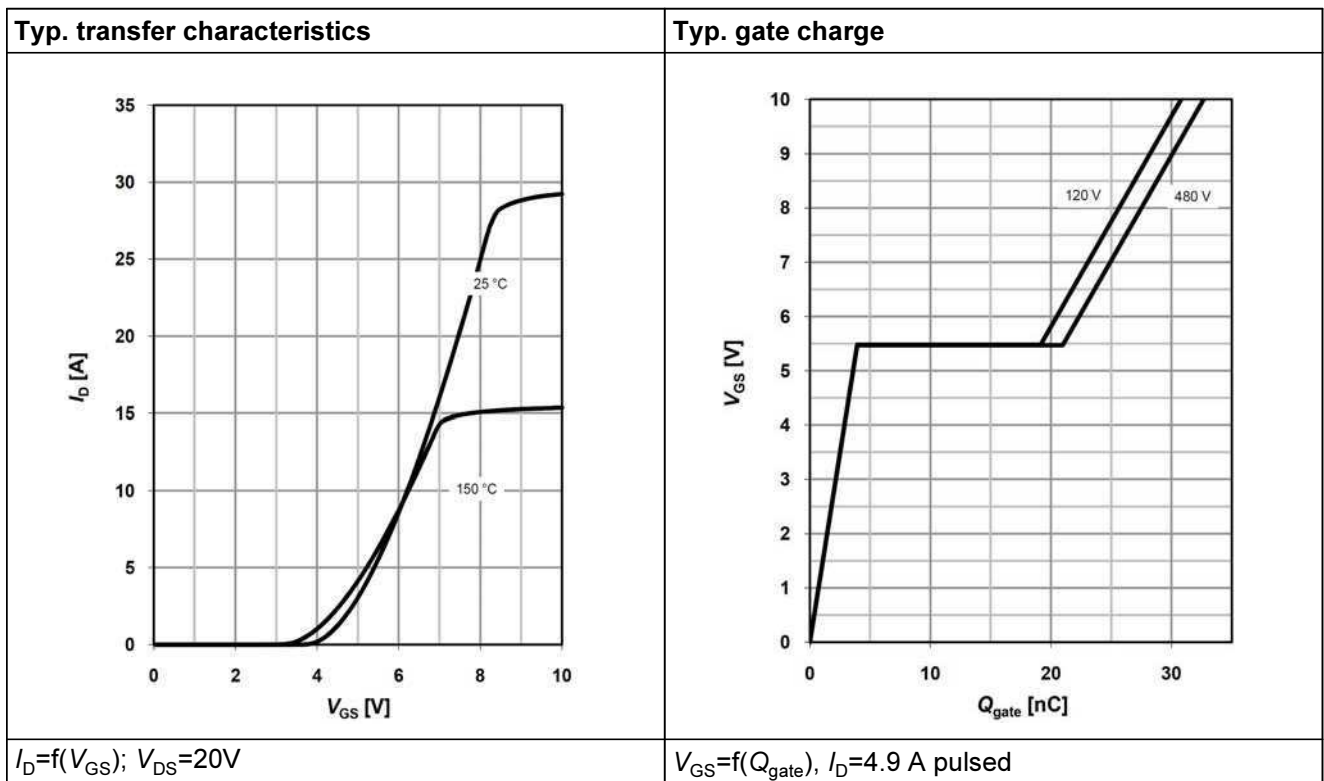


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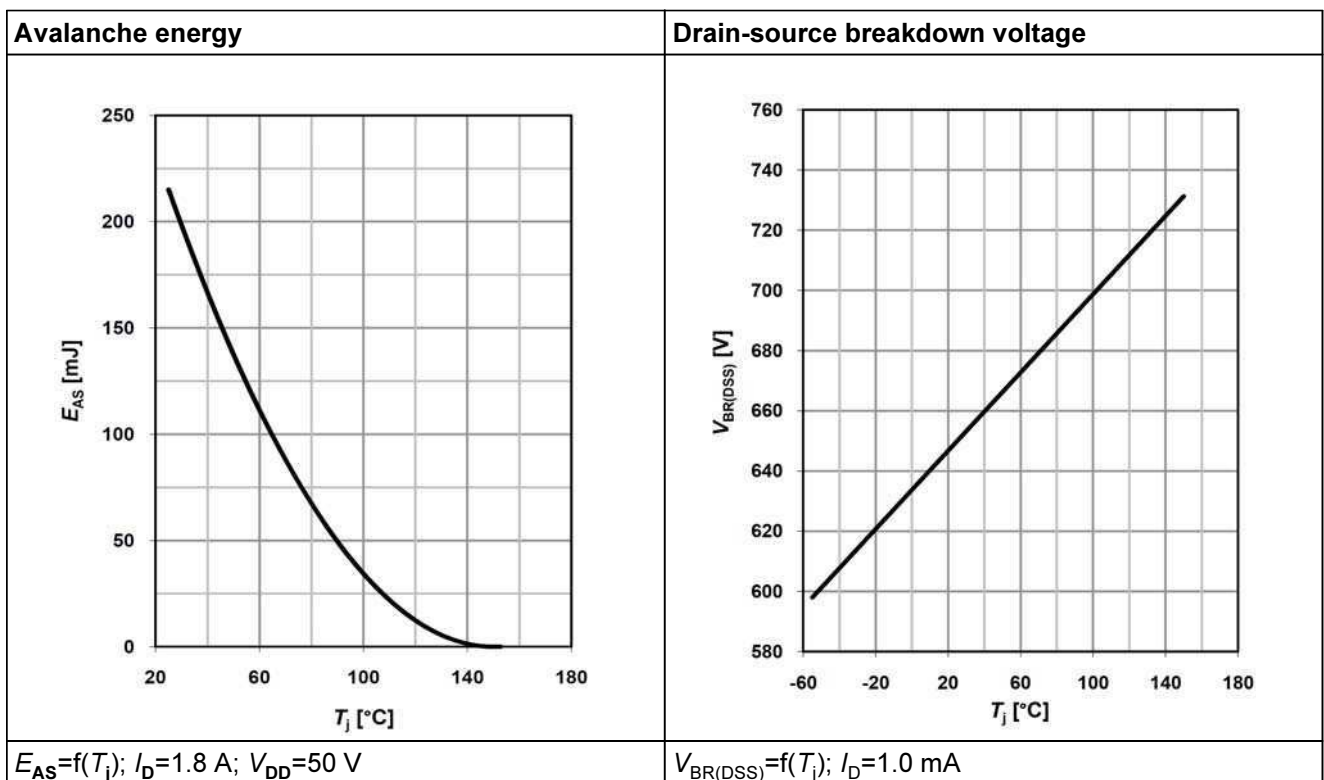


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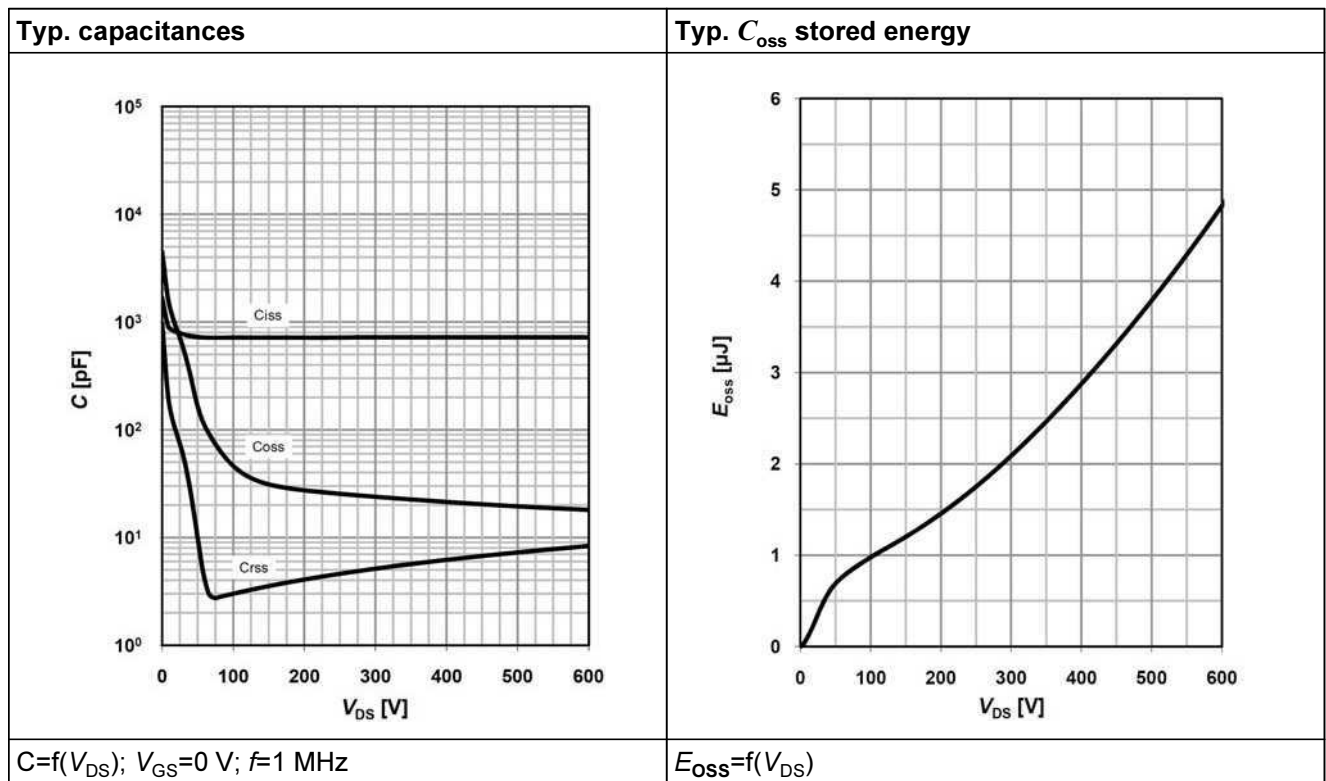
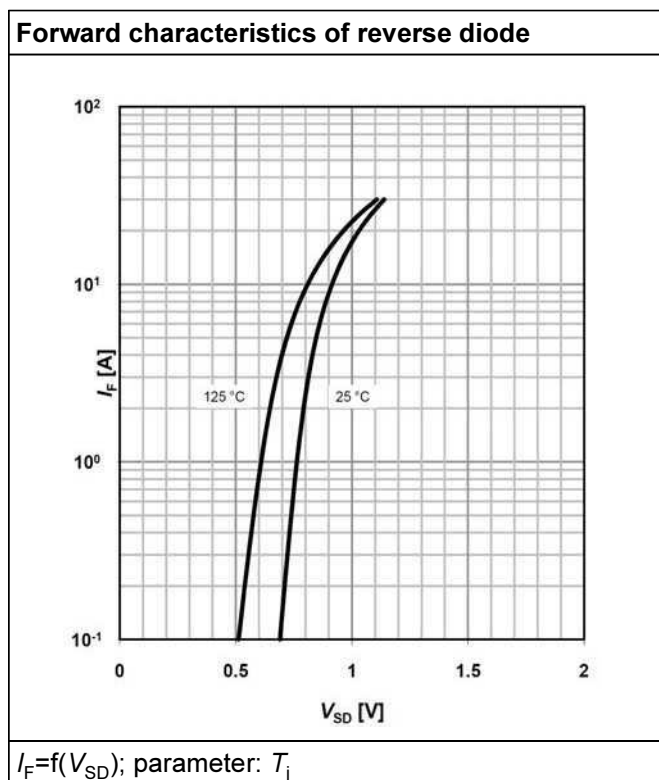


Table 19



6 Test circuits

Table 20 Switching times test circuit and waveform for inductive load

Switching times test circuit for inductive load	Switching time waveform

Table 21 Unclamped inductive load test circuit and waveform

Unclamped inductive load test circuit	Unclamped inductive waveform

Table 22 Test circuit and waveform for diode characteristics

Test circuit for diode characteristics	Diode recovery waveform

7 Package outlines

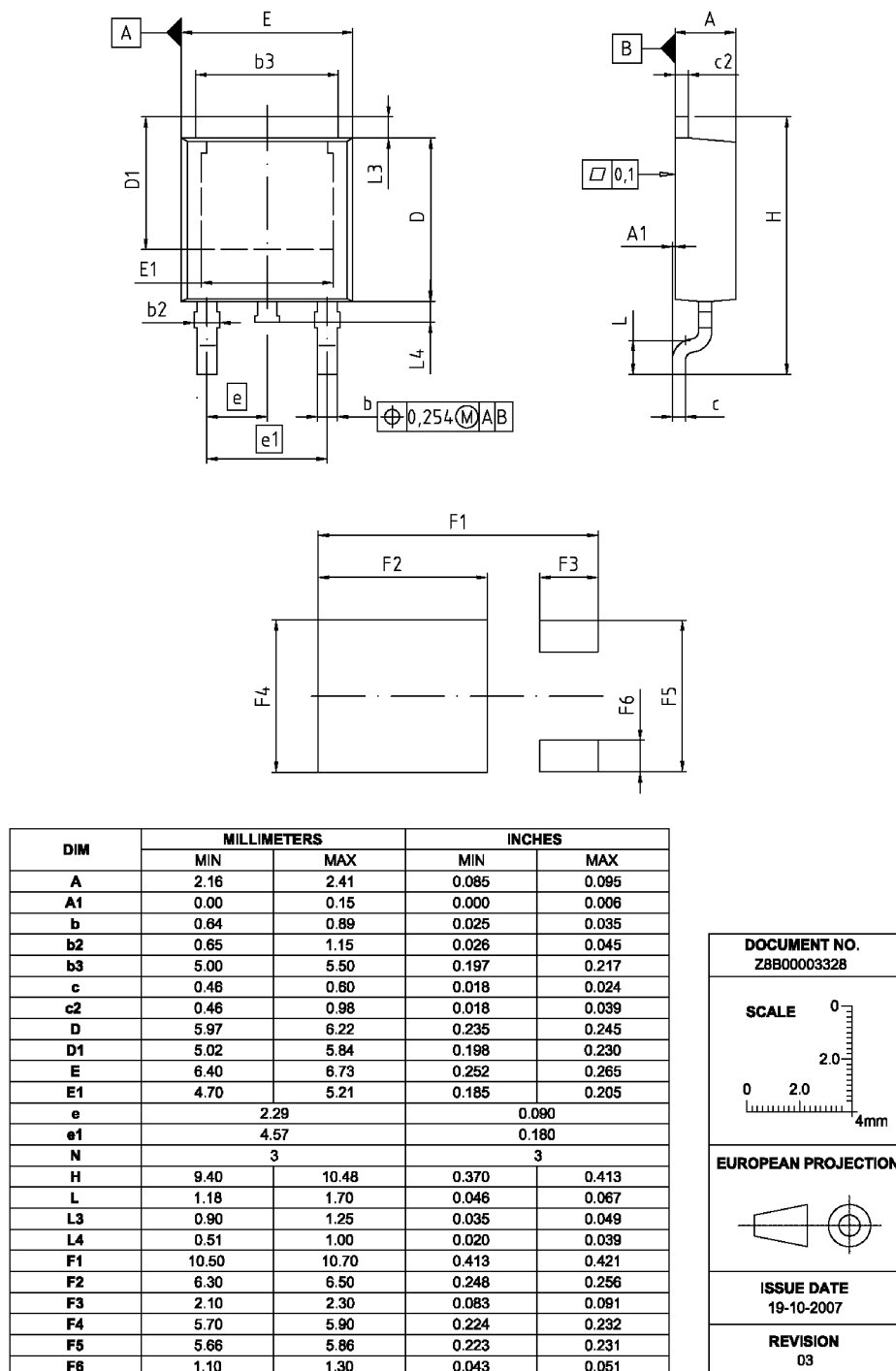
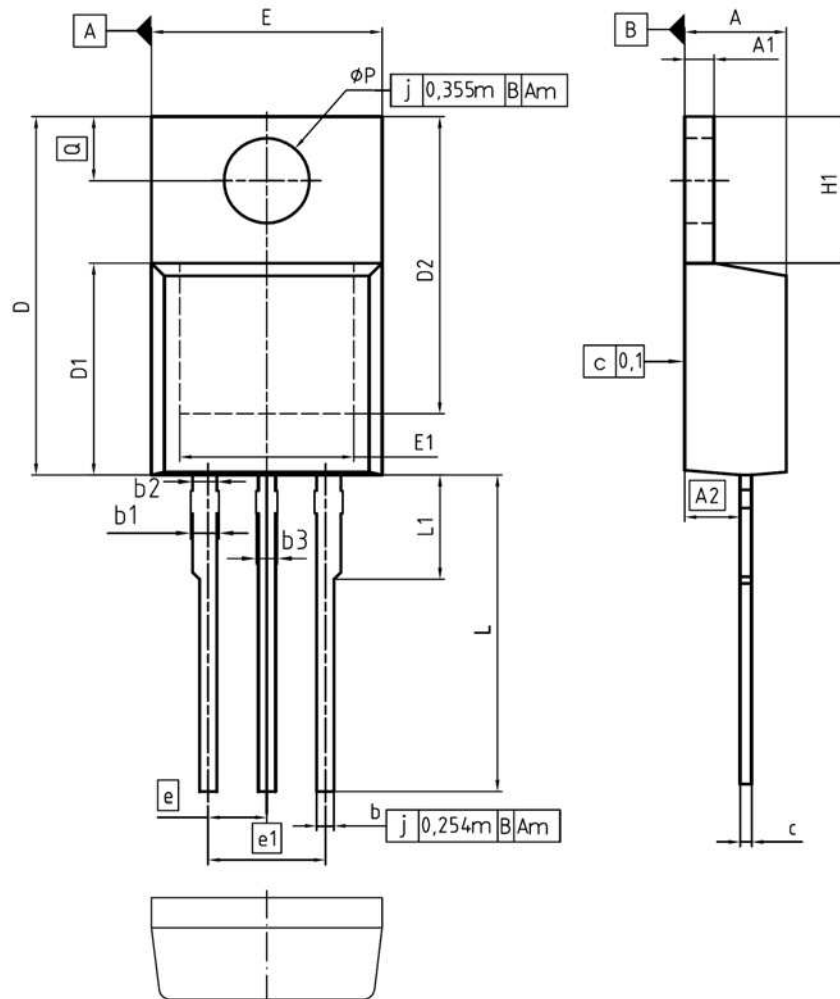


Figure 1 Outlines TO-252, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

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05

Figure 2 Outlines TO-220, dimensions in mm/inches

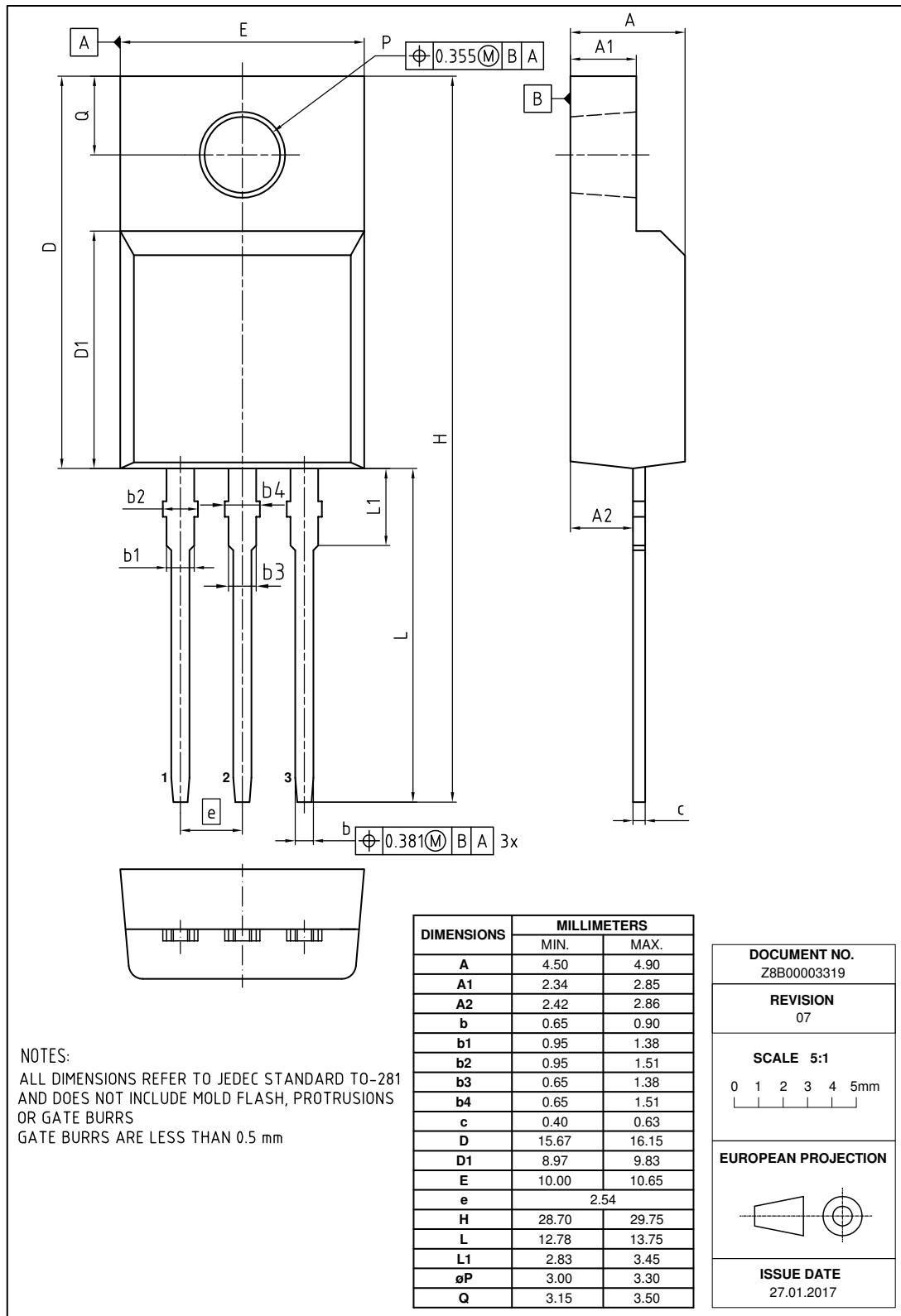
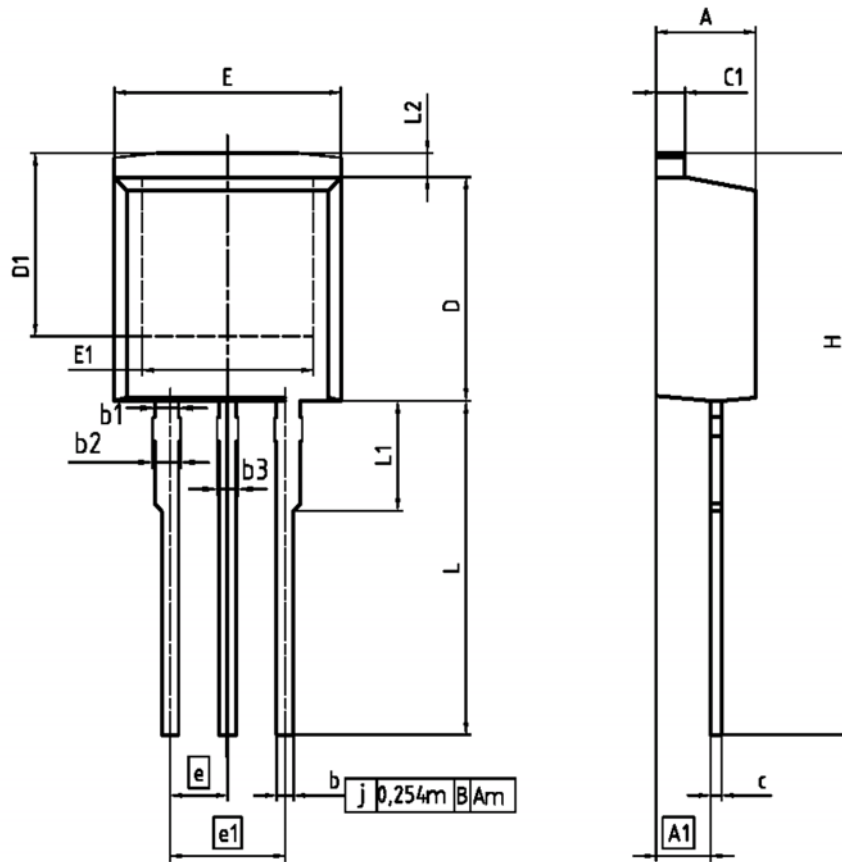


Figure 3 Outline PG-TO-220 FullPAK dimensions in mm



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.300	4.572	0.169	0.180
A1	2.150	2.718	0.085	0.107
b	0.650	0.864	0.026	0.034
b1	0.950	1.093	0.037	0.043
b2	0.950	1.400	0.037	0.055
b3	0.650	1.118	0.026	0.044
c	0.330	0.600	0.013	0.024
c1	1.170	1.400	0.046	0.055
D	8.509	8.450	0.335	0.372
D1	6.900	-	0.272	-
E	9.700	10.363	0.382	0.408
E1	6.500	8.600	0.256	0.339
e	2.540		0.100	
e1	5.080		0.200	
N	3		3	
L	13.000	14.000	0.512	0.551
L1	-	4.800	-	0.189
L2	-	1.727	-	0.068

REFERENCE
JEDEC TO262

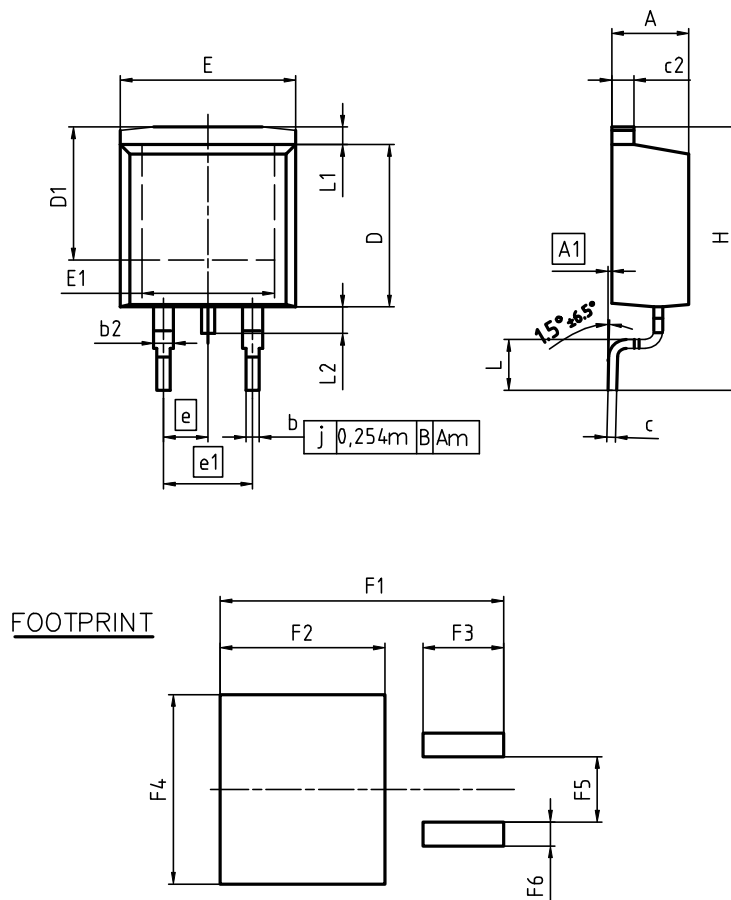
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Figure 4 Outlines TO-262, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	0.00	0.25	0.000	0.010
b	0.65	0.85	0.026	0.033
b2	0.95	1.15	0.037	0.045
c	0.33	0.65	0.013	0.026
c2	1.17	1.40	0.046	0.055
D	8.51	9.45	0.335	0.372
D1	7.10	7.90	0.280	0.311
E	9.80	10.31	0.386	0.406
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	2		2	
H	14.61	15.88	0.575	0.625
L	2.29	3.00	0.090	0.118
L1	0.70	1.60	0.028	0.063
L2	1.00	1.78	0.039	0.070
F1	16.05	16.25	0.632	0.640
F2	9.30	9.50	0.366	0.374
F3	4.50	4.70	0.177	0.185
F4	10.70	10.90	0.421	0.429
F5	3.65	3.85	0.144	0.152
F6	1.25	1.45	0.049	0.057

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Figure 5 Outlines TO-263, dimensions in mm/inches

650V CoolMOS™ C6 Power Transistor

IPx65R380C6

Revision History

IPx65R380C6

Revision: 2018-03-05, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.1	2018-03-05	Outline PG-TO220 FullPAK update

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