BGT24AT2

Silicon Germanium 24 GHz Transmitter MMIC

Data Sheet

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Final

RF & Protection Devices

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BGT24AT2 Silicon Germanium 24 GHz Transmitter MMIC

Revision History: 2016-01-20, Revision 3.2

Previous Revision: 2015-04-27 Revision 3.1	
Page	**Subjects (major changes since last revision)**

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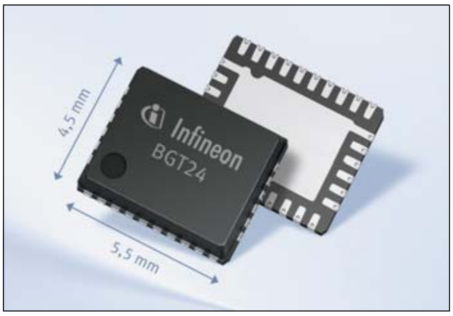
1 Features



- 24 GHz signal source with 2 transmitter outputs and 1 local oscillator output
- External / internal phase inversion and RF pulsing capability
- Programmable gain amplifiers (PGA) with 6 bit resolution
- Fully integrated low phase noise VCO
- Frequency divider with 23.5 MHz output
- On chip RF output level and temperature sensors
- Multiplexed output of analog sensor signals
- Single ended RF terminals
- Single supply voltage 3.3 V
- Low power consumption 775 mW typ.
- 200 GHz bipolar SiGe:C technology b7hf200
- Fully ESD protected device
- VQFN-32-9 leadless plastic package including lead-tip-inspection (LTI) feature
- Pb-free (RoHS compliant) package
- AEC Q100 qualified

RoHS

Description

The BGT24AT2 is a low phase noise 24 GHz ISM band multifunction signal source, manufactured in a monolithic Silicon Germanium semiconductor process technology.

It accommodates a 24 GHz fundamental voltage controlled oscillator and a frequency divider with a division ratio of 1024. The frequency divider output is differential.

The three individual RF outputs generate a typical output power of +10 dBm, adjustable via SPI-programmable 6 bit DAC's. Fast pulsing and phase inversion of the transmit signal is provided either using dedicated control inputs or the 64 bit SPI. Automatic configuration of the LO-output is possible using a dedicated logic.

RF output level sensors as well as a temperature sensor are implemented for monitoring purposes. The analog sensor signals along with an additional optional analog input are multiplexed to one common output.

The MMIC is manufactured in a 200 GHz, 0.18μm SiGe:C technology and is packaged in a 32 pin leadless RoHS compliant VQFN package with LTI feature.

Product Name	Package	Chip	Marking
BGT24AT2	VQFN32-9	T1824	BGT24AT2

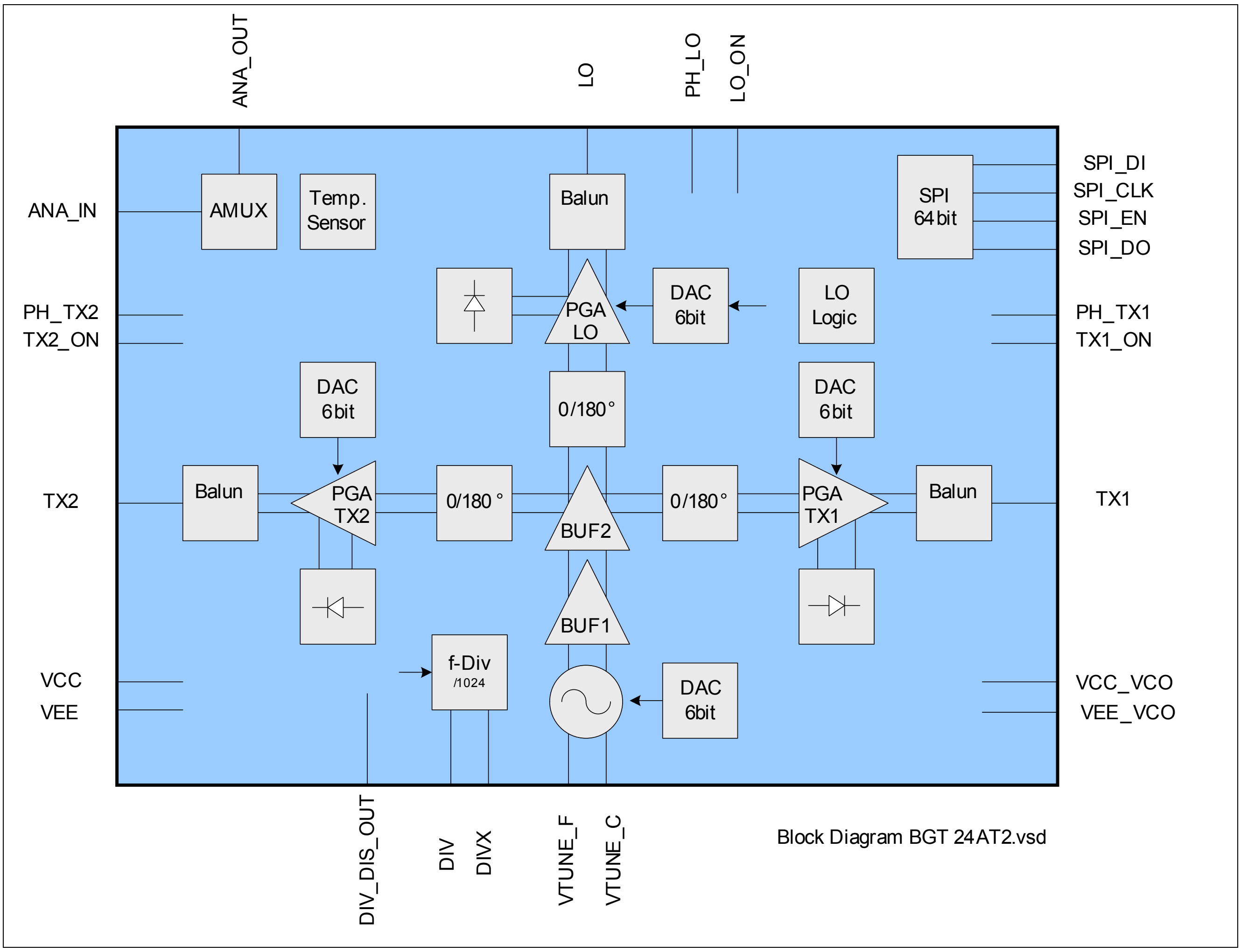


Figure 1 BGT24AT2 Block Diagram

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings, T_A = -40 °C to 125 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
Supply voltage	V_{CC}	-0.3	–	V_{cc} +0.3	V	■	–
Voltage applied to none-RF pins[1)]	V_{IO}	-0.3	–	V_{cc} +0.3	V	■	–
DC voltage at RF pins	VDC_{RF}	–	–	0	V	■	MMIC provides short circuit to GND for TX1, TX2 and LO pins
DC voltage at pins VTUNE_F, VTUNE_C	V_{TUNE}	-0.3	–	V_{cc} +0.3	V	■	–
DC voltage at pins DIV, DIVX	$V_{DIVIDER}$	2	–	V_{cc} +0.3	V	■	–
Total power dissipation	P_{DISS}	–	–	1000	mW	■	–
Junction temperature	T_J	-40	–	170	°C	■	–
Ambient temperature range	T_A	-40	–	125	°C	■	T_A = temperature at package soldering point
Storage temperature range	T_{STG}	-50	–	125	°C	■	–

1) For SPI_EN, SPI_DI, SPI_CLK the applied voltage may exceed given ratings als long as current into these pins is limited to I_{SPI} = 1 mA

***Attention:** Stresses exceeding the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.*

***Attention:** Integrated protection functions are designed to prevent IC destruction under fault conditions as described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

***Attention:** Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.*

Note: ***No permanent damage of the device is possible due to an undefined SPI state***

2.2 ESD Integrity

Table 2 ESD Integrity

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
ESD robustness HBM[1)]	$V_{\text{ESD-HBM}}$	-1	–	1	kV	■	All pins
ESD robustness, CDM[2)]	$V_{\text{ESD-CDM}}$	-500	–	500	V	■	All pins
		-750	–	750		■	Package corner pins

1) According to ANSI/ESDA/JEDEC JS-001 (R = 1.5kOhm, C = 100pF) for Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM)-Component Level

2) According to JEDEC JESD22-C101 Field-Induced Charged Device Model (CDM), Test Method for Electrostatic-Discharge Withstand Thresholds of Microelectronic Components
Please note that this result is subject to:
- lot variations within the manufacturing process as specified by Infineon
- changes in the specific test setup

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

2.3 Power Supply

Table 3 Electrical Characteristics, T_A = -40 °C ... 125 °C, positve current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
Supply voltage	V_{CC}	3.135	3.3	3.465	V		–
Supply current nominal operation mode	$I_{CC,ON}$	–	235	280	mA		nom. operation mode, SPI-state: 9F7F 2903 9F7C 10FF Hex
Supply current standby mode	$I_{CC,STDBY}$	–	65	85	mA		all functional blocks disabled, SPI-state: 0000 0000 0000 0000 Hex

2.4 VCO

Table 4 Electrical Characteristics, , V_{CC} = 3.135 V to 3.465 V, T_A = -40 °C to 125 °C, PGA output power = P_{max}, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24 GHz to 24.25 GHz including matching structures and a package footprint provided by Infineon using the high frequency laminate Rogers 4350B (see Application Note AN359)

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
VCO frequency range	f_{VCO}	24.0	24.125	24.25	GHz		–[1)2)]
VCO tuning voltage for VCO frequency range	V_{TUNE_F}	0.1	–	0.9	V		–
Number of usable VCO coarse tune DAC states	n	2	–	–	–		VTUNE_F applied via series resistor ≥ 1 kΩ
VCO phase noise @ 1 kHz	$P_{N,P\ 1kHz}$	–	-30	-18	dBc/Hz	■	–
VCO phase noise @ 10 kHz	$P_{N,P\ 10kHz}$	–	-59	-50	dBc/Hz	■	–
VCO phase noise @ 100 kHz	$P_{N,P\ 100kHz}$	–	-82	-76.4	dBc/Hz		–
VCO phase noise @ 1 MHz	$P_{N,P\ 1MHz}$	–	-103	-97.4	dBc/Hz	■	–
VCO phase noise @ 10 MHz	$P_{N,P\ 10MHz}$	–	-123	-117.4	dBc/Hz	■	–
VCO amplitude noise @ 10 kHz	$P_{N,A\ 10kHz}$	–	–	-125	dBc/Hz	■	measured at +4 dBm output power
VCO amplitude noise @ 100 kHz	$P_{N,A\ 100kHz}$	–	–	-135	dBc/Hz	■	measured at +4 dBm output power

Table 4 Electrical Characteristics, (cont'd), V_{CC} = 3.135 V to 3.465 V, T_A = -40 °C to 125 °C, PGA output power = P_{max}, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24 GHz to 24.25 GHz including matching structures and a package footprint provided by Infineon using the high frequency laminate Rogers 4350B (see Application Note AN359)

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
VCO amplitude noise @ 1 MHz	$P_{N,A\ 1MHz}$	–	-150	-145	dBc/Hz	■	measured at +4 dBm output power
VTUNE_F input resistance	R_{VTUNE_F}	100	–	–	kΩ	■	nonlinear, see leakage current specification
Leakage current at pin VTUNE_F	I_{VTUNE_F}	-40	–	–	µA		at min. tuning voltage
VTUNE_F input capacitance	C_{VTUNE_F}	–	–	10	pF	■	–
VTUNE_C input resistance	R_{VTUNE_C}	1440	1800	2160	Ω	■	–
VTUNE_C DAC current for PGA state 63	$I_{VTUNE\_C,\ DAC}$	1.2	–	–	mA	■	–
Static pulling f_{VCO} change vs. load	Δf_{sp}	-1	–	+1	MHz	■	at all TX ports, 10 dB mismatch, all phases
Dynamic pulling phase and TX switch change	Δf_{dp1}	-1	–	+1	MHz	■	at all TX ports, 10 dB mismatch, all phases
Dynamic pulling TX1 to TX2 switch change	Δf_{dp2}	-1	–	+1	MHz	■	at all TX ports, 10 dB mismatch, all phases
VCO pushing	$\Delta f / \Delta V_{CC}$	-20 -60	– –	+20 +60	MHz/V	■	$V_{CC} \geq 3.2$ V, $T_A \geq -20$ °C 3) 3)
Spurious level harmonics	a_{harm}	–	–	-32	dBc	■	at max. output power; H2 measured at SWM connector 3)
Spurious level non harmonics	a_{nharm}	–	–	-48	dBm	■	–
VCO tuning speed	$\Delta f / \Delta t$	70	–	–	MHz/µs	■	–
VCO tuning sensitivity	$\Delta f / \Delta V_{TUNE\_F}$	–	–	2800 2200	MHz/V	■	differential sensitivity lin. between f_1 24.05 GHz and f_2 = 24.14 GHz
VCO frequency drift 4)	Δf_{DRIFT}	–	10	–	kHz	■	–

1) Proper adjustment of V_{TUNE_C} required to cover frequency band with specified V_{TUNE_F}
2) Montonic increasing frequency vs. VTUNE_F
3) Dynamic measurement: VTUNE_F = 0.1 V, PGA state = 63, f = 10 kHz, A = 50 mVpp, dynamic V_{CC} must stay within specified limits
4) Within 50ms and under following conditions:
- Ambient temperature - stable
- Supply voltage - stable
- RF ports at least 50 µs after ON/OFF or OFF/ON and phase transitions
- Divider in ON/OFF at least 50 µs after OFF/ON transitions

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

2.5 Frequency Divider

The block diagram of the frequency divider is shown in **Figure 2**, a compatible truth table is given in **Table 5**

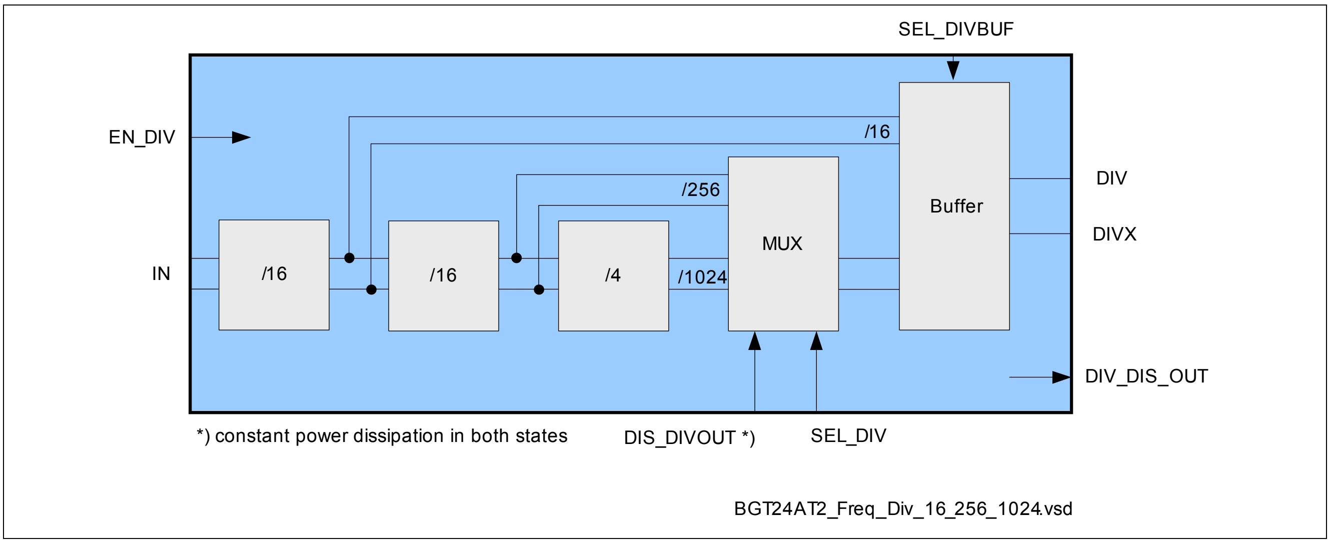


Figure 2 Block Diagram Frequency Divider

Table 5 Frequency Divider Truth Table[1)2)]

EN_DIV	SEL_DIV	SEL_DIVBUF	DIS_DIVOUT	MODE
1	X	1	X	/16
1	1	0	0	/256
1	0	0	0	/1024
1	X	0	1	output disabled
0	X	X	X	shutdown

1) deviating states not allowed, undefined divider output
2) modes /16 and /256 for information only!

Table 6 Electrical Characteristics, V_{CC} = 3.135 V to 3.465 V, T_A = -40 °C to 125 °C, VCO frequency = 24.0 to 24.25 GHz, divider division ratio = 1024, all voltages with respect to ground (unless otherwise specified).

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
Dividing factor	D_{DIV}	–	256 1024	–	–		–
Divider output impedance	Z_{OUT}	240	300	360	Ω	■	Into MMIC[1)]
Output voltage	$V_{DIV,1024}$	900	1150	1400	mVpp		Into 300 Ω load[2)]

Table 6 **Electrical Characteristics,** (cont'd)V_{CC} = 3.135 V to 3.465 V, T_A = -40 °C to 125 °C, VCO frequency = 24.0 to 24.25 GHz, divider division ratio = 1024, all voltages with respect to ground (unless otherwise specified).

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
Common mode output voltage	$V_{DIV,CM,EN}$	2.35	2.75	3.15	V		Output enabled[2)]
	$V_{DIVX,CM,EN}$	2.35	2.75	3.15			Output enabled[2)]
	$V_{DIV,CM,DIS}$	–	V_{cc}	–			Output enabled[2)]
	$V_{DIVX,CM,DIS}$	1.6	2.15	2.60			Output enabled[2)]
	$V_{DIV,CM,OFF}$	–	V_{cc}	–		■	Shutdown[2)]
	$V_{DIVX,CM,OFF}$	–	V_{cc}	–		■	Shutdown[2)]
Duty cycle	DC	–	0.5	–	–	■	–

1) Divider output stable for VSWR < 20:1
2) Measured using T-pad-attenuator on reference PCB as provided by Infineon (see Application Note AN359)

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

2.6 TX and LO PGA

Table 7 **Electrical Characteristics,** V_{CC} = 3 .135 V to 3.465 V, T_A = -40 °C to 125 °C, PGA output power = P_{max} , positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24 GHz to 24.25 GHz include matching structures and a package footprint provided by Infineon using the high frequency laminate Rogers 4350B (see Application Note AN359). Reference board losses and 2.92 mm connector loss deembedded to outer trafo edge (reference plane).

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
Output power PGA_{min}	P_{min}	–	–	-26	dBm		–
Output power PGA_{max}	P_{max}	7	10	13	dBm		–
PGA coarse resolution interval	R_C	–	–	8	dB/bit		P_{out} ≥ -26 dBm
PGA mid resolution interval	R_M	–	–	3	dB/bit		P_{out} ≥ -13 dBm
PGA fine resolution interval	R_F	–	–	0.6	dB/bit		P_{out} ≥ +1 dBm
Output power variation in temp. range	ΔP_{TXtemp}	-1.25	–	0.75	dB	■	–
Output match	S_{22}				dB		V_{CC} =3.3 V, T_A = 25 °C[1)]
		–	–	-8		■	PGA state ≥ 47
		–	–	-5.5		■	PGA state ≥ 23
		–	–	0		■	PGA state ≥ 0
Output impedance	Z_{TX}	–	50	–	Ω	■	Single ended
TX on/off isolation	$I_{TXon/off}$	30	–	–	dB	■	P_{out} ≥ -1 dBm
TX1/TX2 isolation	$I_{TX1/TX2}$	30	–	–	dB	■	P_{out} ≥ -1 dBm
TX on/off switching time	$t_{ON/OFF}$	–	–	2	ns	■	–

Table 7 **Electrical Characteristics,** (cont'd)V_{CC} = 3 .135 V to 3.465 V, T_A = -40 °C to 125 °C, PGA output power = P_{max} , positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24 GHz to 24.25 GHz include matching structures and a package footprint provided by Infineon using the high frequency laminate Rogers 4350B (see Application Note AN359). Reference board losses and 2.92 mm connector loss deembedded to outer trafo edge (reference plane).

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
Phase shifter phase imbalance	ε_p	175	180	185	deg	■	–
Phase shifter amplitude imbalance	ε_A	-0.5	0	0.5	dB		–
Phase shifter switching time	t_{PHASE}	–	–	100	ns	■	–
Following parameter for pins: PH_TX1, PH_LO, PH_TX2, TX1_ON, LO_ON, TX2_ON							
High-level input voltage	V_{I_high}	2.0	–	–	V	■	–
Low-level input voltage	V_{I_low}	–	–	0.8	V	■	–
Input capacitance	C_{in}	–	–	2	pF	■	–
Pull Up resitor	RPL	27.2	34	40.8	kΩ	■	T_A = 25 °C
Leakage current into pins	$I_{Leakage}$	-100	–	75	µA		–

1) SOLT calibration, reference plane at SWM connector

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

2.7 Temperature Sensor

Table 8 **Electrical Characteristics,** V_{CC} = 3.3 V, T_A = -40 °C to 125 °, application and MMIC external circuit acc. to Application Note AN359, all voltages with respect to ground (unless otherwise specified).

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
Temperature sensor operating range	T_{TSENS}	-40	–	125	°C	■	–
Output voltage	$V_{TSENSE25}$	1.4	1.5	1.6	V		at T_{Si} = 25°C
Sensitivity	S_{TSENS}	4.3	4.7	5.1	mV/K	■	–
Setup time	t_{TSENS}	–	–	20	µs	■	$C_{LOAD} \leq$ 2.2 nF and $R_{LOAD} \geq$ 10 kΩ at ANA_OUT
Power supply rejection ratio	$PSRR$	16	24	–	dB		measured at T_{Si} = 25°C and $V_{CC,MIN}/V_{CC,MAX}$

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

2.8 Output Level Detector

Table 9 Electrical Characteristics, V_{CC} = 3.135 V to 3.465 V, T_A = -40 °C to 125 °C, application and MMIC external circuit acc. to Application Note AN359, all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
Output voltage	V_{OUT}	1.17	–	1.29	V	■	PGA state = 0, all channels RF off
Detector TX1 and TX2 absolute error	$E_{TX1, TX2}$	-2	–	+2	dB	■	at P_{OUT} > -1 dBm, calculation based on equation in App. Note AN359
Detector LO absolute error	E_{LO}	-2	–	+2	dB	■	at P_{OUT} > -1 dBm, calculation based on equation in App. Note AN359
Setup time	t_{LSENS}	–	–	20	µs	■	C_{LOAD} ≤ 2.2 nF and R_{LOAD} ≥ 10 kΩ at ANA_OUT

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

2.9 Sensor Multiplexer

Table 10 Electrical Characteristics, V_{CC} = 3.135 V to 3.465 V, T_A = -40 °C to 125 °C, application and MMIC external circuit acc. to Application Note AN359, all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
Input voltage range	V_{IN}	1	–	2	V	■	–
Input current	I_{IN}	–	–	1	µA	■	–
Output impedance	R_{OUT}	–	20	40	Ω	■	–
Offset voltage	V_{OFFSET}	-10	–	10	mV	■	At 10 kΩ load resistance

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

3 Pin Description

Table 11 Pin Definition and Function

Pin No.	Name	Function
1	PH_TX1	TX1 phase
2	TX1_ON	TX1 enable
3	LO_ON	LO enable
4	VEE	Ground
5	LO	LO RF output signal
6	VEE	Ground
7	VEE	Ground
8	PH_LO	LO phase
9	TX2_ON	TX2 enable
10	PH_TX2	TX2 phase
11	VEE	Ground
12	TX2	TX2 RF output signal
13	VEE	Ground
14	VCC	Supply voltage
15	DIV_DIS_OUT	Divider disable output
16	SPI_DO	SPI data output
17	DIVX	Divider output negative port
18	DIV	Divider output positive port
19	ANA_IN	Analog signal input
20	VCC_VCO	Supply voltage VCO
21	VEE	Ground
22	VTUNE_F	VCO tuning voltage (fine)
23	VTUNE_C	VCO tuning voltage (coarse)
24	VEE_VCO	Ground VCO
25	VCC	Supply voltage
26	SPI_EN	SPI enable
27	SPI_CLK	SPI clock
28	SPI_DI	SPI data input
29	ANA_OUT	Analog output signal
30	VEE	Ground
31	TX1	TX1 RF output signal
32	VEE	Ground

Table 12 I/O internal circuits

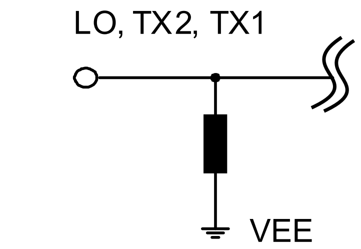
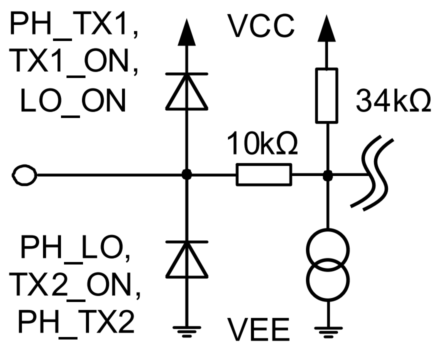
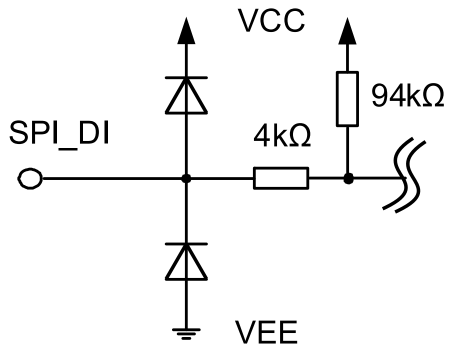
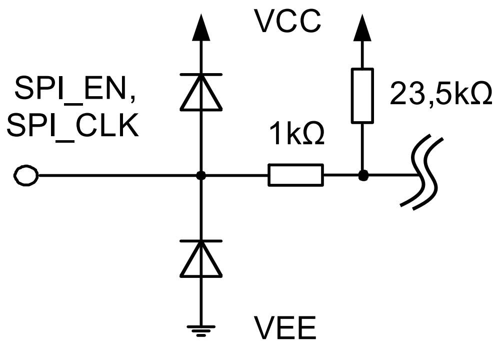
Pin No.	Name	I/O internal circuits
5, 12, 31	LO, TX2, TX1	
1, 2, 3, 8, 9, 10	PH_TX1, TX1_ON, LO_ON, PH_LO, TX2_ON, PH_TX2	
28	SPI_DI	
26, 27	SPI_EN, SPI_CLK	

Table 12 I/O internal circuits

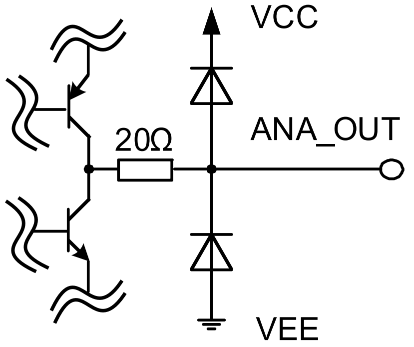
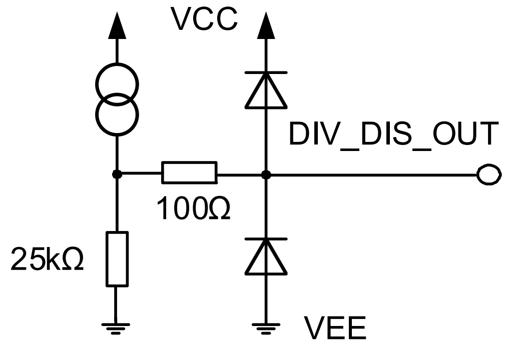
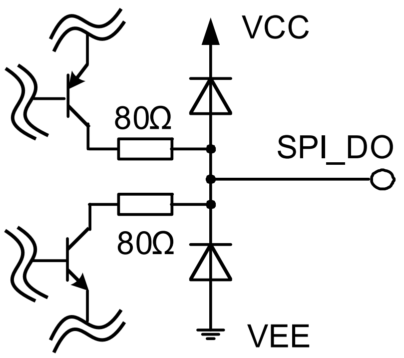
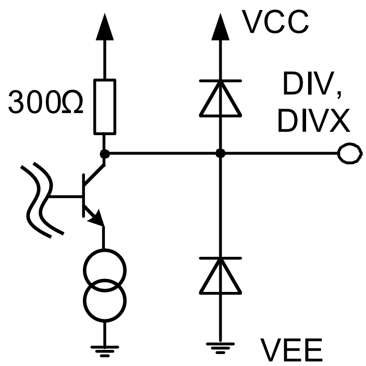
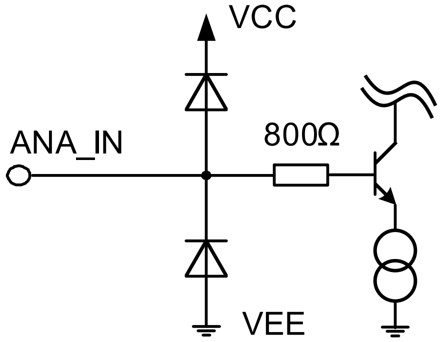
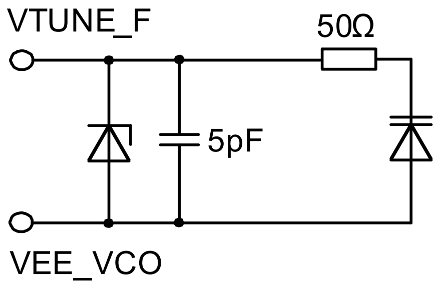
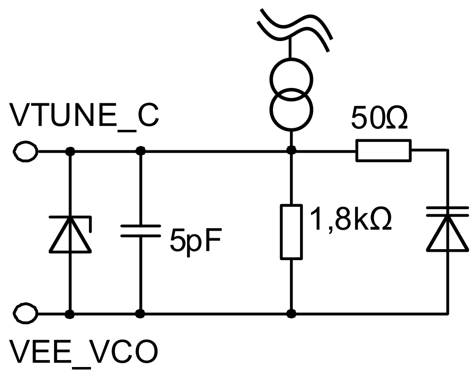
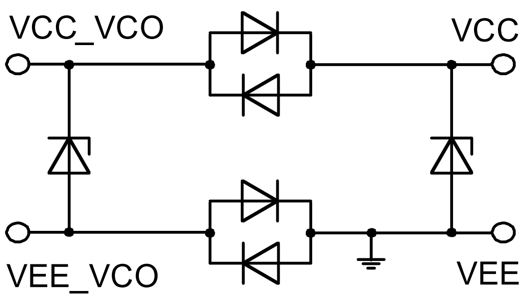
Pin No.	Name	I/O internal circuits
29	ANA_OUT	
15	DIV_DIS_OUT	
16	SPI_DO	
17, 18	DIVX, DIV	

Table 12 I/O internal circuits

Pin No.	Name	I/O internal circuits
19	ANA_IN	
22, 24	VTUNE_F,VEE_VCO	
23, 24	VTUNE_C, VEE_VCO	
4, 6, 7, 11, 13, 14, 20, 21, 24, 25, 30, 32	VEE, VCC, VCC_VCO, VEE_VCO,	

4 SPI

Communication to the transceiver is done via a Serial-Peripheral-Interface (SPI). The 64 bit SPI has a hardwired Power-On reset, which sets the output bits to a defined state after turning on the supply voltage. Data transmission is started by a negative edge on SPI_EN. Data at SPI_DI is then read at the falling edge of SPI_CLK. The most significant bit (MSB) is read first.

Table 13 SPI Data Bit Description

Data Bit	Name	Description (Logic High)	Power ON Reset State
0 (LSB)	TX1_A5	MSB of TX1 PGA DAC output power control	0
1	TX1_A4	TX1 PGA DAC output power control	0
2	TX1_A3	TX1 PGA DAC output power control	0
3	TX1_A2	TX1 PGA DAC output power control	0
4	TX1_A1	TX1 PGA DAC output power control	0
5	TX1_A0	LSB of TX1 PGA DAC output power control	0
6	TX1_EN_DAC	TX1 PGA DAC enable	0
7	LO_EN_DAC	LO PGA DAC enable	0
8	n.c.		0
9	n.c.		0
10	n.c.		0
11	n.c.		0
12	EN_BUF1	buffer amplifier BUF1 enable	0
13	n.c.		0
14	n.c.		0
15	n.c.		0
16	VCO_A5	MSB of coarse tune DAC	0
17	VCO_A4	VCO coarse tune DAC	0
18	VCO_A3	VCO coarse tune DAC	0
19	VCO_A2	VCO coarse tune DAC	0
20	VCO_A1	VCO coarse tune DAC	0
21	VCO_A0	LSB of VCO coarse tune DAC	0
22	EN_DAC_VCO	VCO coarse tune DAC enable	0
23	PH1_SPI_ON	Phase control TX1 via SPI	0
24	TX1_SEL1	TX1 control bit (“0”=via ext. pulse pin, “1”= via SPI)	0
25	TX1_SPI_ON	TX1 enable via SPI	0
26	LO_SPI_ON	LO enable via SPI	0
27	AMUX2_SEL0	AMUX2 control bit	0
28	AMUX2_SEL1	AMUX2 control bit	0
29	AMUX2_SEL2	AMUX2 control bit	0
30	LO_SEL1	LO logic control bit	0

Table 13 SPI Data Bit Description (cont'd)

Data Bit	Name	Description (Logic High)	Power ON Reset State
31	EN_BUF2	Buffer amplifier BUF2 enable	0
32	EN_DIV	Frequency divider enable	0
33	EN_VCO	VCO enable	0
34	AMUX1_SEL0	AMUX1 control bit	0
35	AMUX1_SEL1	AMUX1 control bit	0
36	n.c.		0
37	PHLO_SPI_ON	Phase control LO via SPI	0
38	PH2_SPI_ON	Phase control TX2 via SPI	0
39	PH_SEL1	Phase control bit ("0"=via ext. pulse pin, "1"=via SPI)	0
40	TX2_SEL1	TX2 control bit ("0"=via ext. pulse pin, "1"=via SPI)	0
41	TX2_SPI_ON	TX2 enable via SPI	0
42	AMUX3_SEL1	AMUX3 control bit	0
43	AMUX3_SEL0	AMUX3 control bit	0
44	n.c.		0
45	LO_SEL0	LO control bit	0
46	n.c.		0
47	n.c		0
48	TX2_A5	MSB of TX2 PGA DAC output power control	0
49	TX2_A4	TX2 PGA DAC output power control	0
50	TX2_A3	TX2 PGA DAC output power control	0
51	TX2_A2	TX2 PGA DAC output power control	0
52	TX2_A1	TX2 PGA DAC output power control	0
53	TX2_A0	LSB of TX2 PGA DAC output power control	0
54	TX2_EN_DAC	TX2 PGA DAC enable	0
55	LO_A5	MSB of LO PGA DAC output power control	0
56	LO_A4	LO PGA DAC output power control	0
57	LO_A3	LO PGA DAC output power control	0
58	LO_A2	LO PGA DAC output power control	0
59	LO_A1	LO PGA DAC output power control	0
60	LO_A0	LSB of LO PGA DAC output power control	0
61	SEL_DIVBUF	Frequency divider control bit	0
62	SEL_DIV	Frequency divider control bit	0
63 (MSB)	DIS_DIVOUT	Frequency divider output disable	0

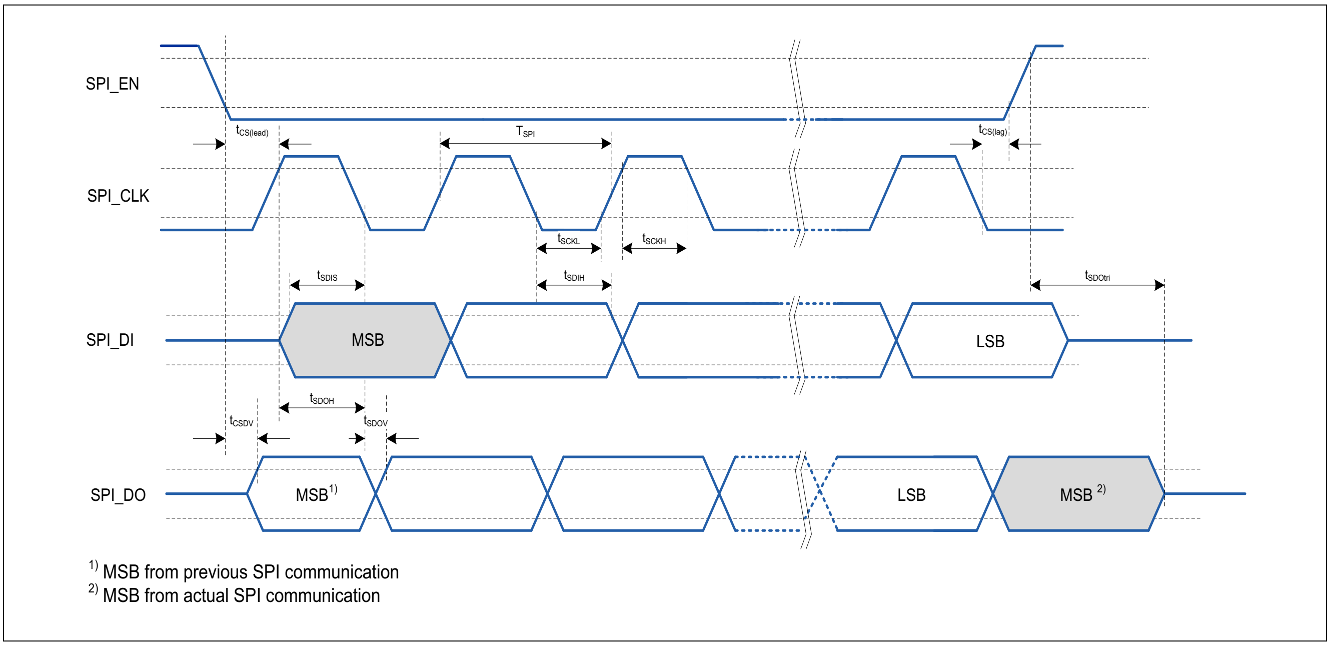


Figure 3 Timing Diagram of the SPI

Table 14 SPI Interface

Parameter	Symbol	Values			Unit	Test
		Min.	Typ.	Max.		
SPI_CLK period	t_{SPI}	50	–	–	ns	
SPI_CLK low time	t_{SCKL}	0.45 t_{SPI}	0.5 t_{SPI}	0.55 t_{SPI}	ns	■
SPI_CLK high time	t_{SCKH}	0.45 t_{SPI}	0.5 t_{SPI}	0.55 t_{SPI}	ns	■
Chip select lead time	$t_{CS(lead)}$	20	–	–	ns	■
Time between falling edge of SPI_CLK and SPI_DO valid	t_{SDOV}	–	–	10	ns	■
Setup time of SPI_DI before falling edge of SPI_CLK	$t_{SDIS} = t_{SI(su)}$	10	–	–	ns	■
Hold time of SPI_DI after falling edge of SPI_CLK	$t_{SI(h)}$	10	–	–	ns	■
Hold time of SPI_DO after rising edge of SPI_CLK	t_{SDOH}	t_{SCKH} - 10ns	–	–	ns	■
Hold time of SPI_EN after last falling edge of SPI_CLK	$t_{CS(lag)}$	30	–	–	ns	■
Delay between rising edge of SPI_EN and SPI_DO tristate (leakage current < 12µA)	t_{SDOtri}	–	–	100	ns	■
Delay between falling edge of SPI_EN and MSB at SPI_DO tristate valid	t_{CSDV}	–	–	125	ns	■
Minimum time between two SPI commands	$t_{min2SPI}$	5	–	–	µs	■

Table 15 Specification for SPI pins

Parameter	Symbol	Values			Unit	Test
		Min.	Typ.	Max.		
High-level input voltage	V_{I_high}	2.0	–	–	V	■
Low-level input voltage	V_{I_low}	–	–	0.8	V	■
Input voltage hysteresis	V_{hys}	50	–	–	mV	■
Input current	I_{IN}	-190	–	150	µA	
Input capacitance (EN, CLK, DI)	CS_{IN}	–	–	2	pF	■
SPI_DO output high voltage (VCC=3.3V,I_{SDO} =1mA)	V_{O_high}	2.4	–	–	V	
SPI_DO output low voltage (VCC=3.3V,I_{SDO} =1mA)	V_{O_low}	–	–	0.8	V	
SPI_DO load capacitance	*CSL DO*	–	–	30	pF	■
SPI_DO load resistance	*RSL DO*	10	–	–	kΩ	■
Pull Up resistor (SPI_DI) T_A = 25 °C	RPL_SPI_DI	78	98	118	kΩ	■
Pull Up resistor (SPI_CLK, SPI_EN) T_A = 25 °C	RPL_SPI_CLK, RPL_SPI_EN	19.6	24.5	29.4	kΩ	■
Leakage current @ SPI_DO in high Z state (test voltage 2.4 V)	*IL DO*	–	–	12	µA	

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

5 Sensor Multiplexer

Output signals of the temperature and output level sensors at TX1, TX2 and LO output are provided multiplexed at the output pin ANA_OUT using an analog multiplexer (AMUX) circuit.

Additionally, a MMIC internal reference voltage (VBG1) can be read out and an analog input signal within 1 V and 2 V can be directed from ANA_IN to ANA_OUT. Tristate capability is implemented in order to combine several analog outputs in the application. In this case it has to be ensured that only one multiplexer output is activated at any time.

Table 16 Truth Table AMUX[1)]

Output at ANA_OUT	AMUX1_ SEL1	AMUX1_ SEL0	AMUX2_ SEL2	AMUX2_ SEL1	AMUX2_ SEL0
Tristate	X	X	0	0	0
ANA_IN	X	X	0	0	1
VTEMP	X	X	0	1	1
PSENSE_TX2	0	0	1	0	0
PSENSE_TX1	0	1	1	0	0
PSENSE_LO	1	X	1	0	0
VBG1 (Bandgap output voltage)	X	X	1	0	1

1) deviating states not allowed, undefined AMUX output

6 LO Logic

The BGT24AT2 accommodates a logic circuit which can be used to either activate the LO-output manually or automatically depending on the TX1/TX2 configuration.

Three operation modes are selectable:

1. manual activation / deactivation of the LO output via external pulse pin LO_ON
2. manual activation / deactivation of the LO output via SPI bit LO_SPI_ON
3. automatic activation / deactivation depending on the TX1 / TX2 configuration.

The configuration of the LO logic operation mode is shown in **Table 17**.

Table 17 Truth Table LO Logic

LO_SEL1	LO_SEL0	Function
0	0	LO activation via external pulse pin LO_ON
0	1	LO activation via SPI bit LO_SPI_ON
1	X	Automatic LO activation via external pulse pins TX1_ON or TX2_ON

7 Package Dimensions

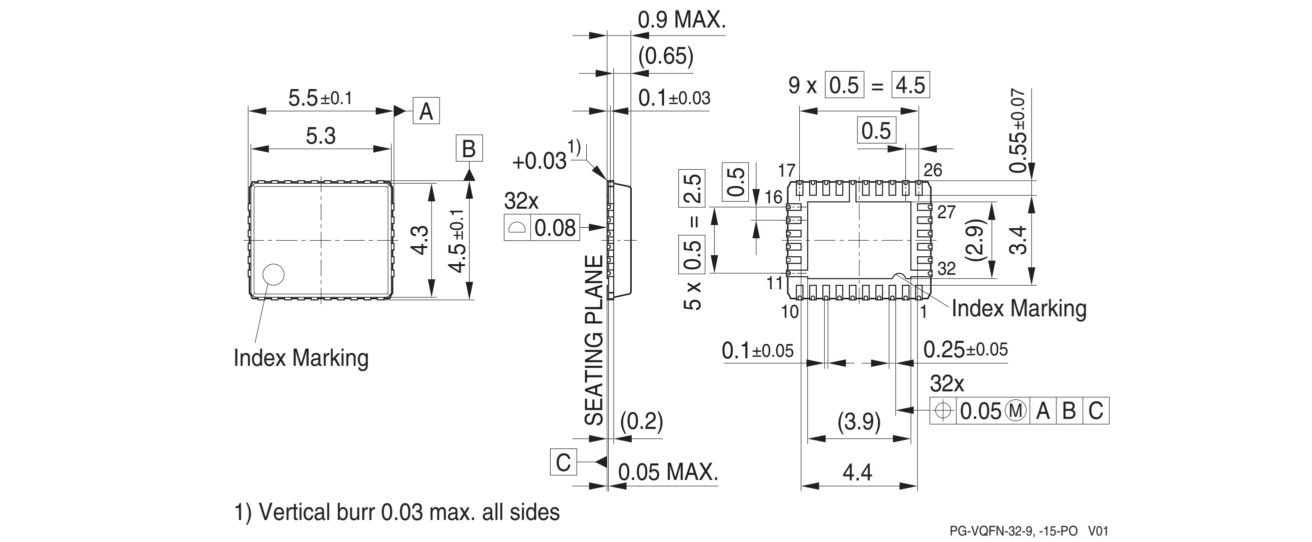


Figure 4 **Package Outline (Top, Side and Bottom View) of VQFN32-9**

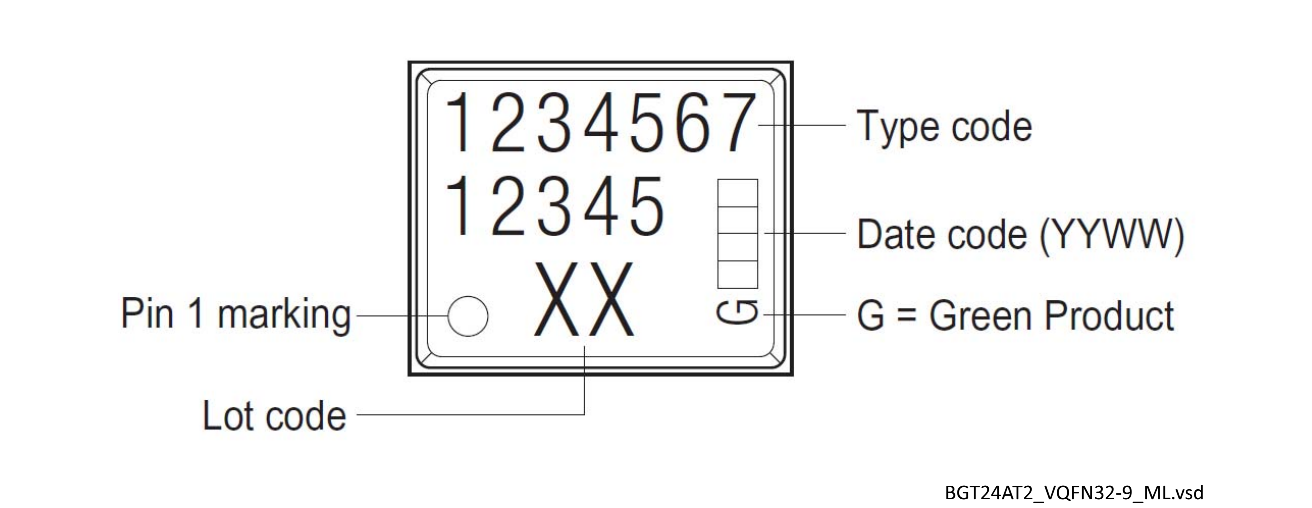


Figure 5 **Marking Layout VQFN32-9**

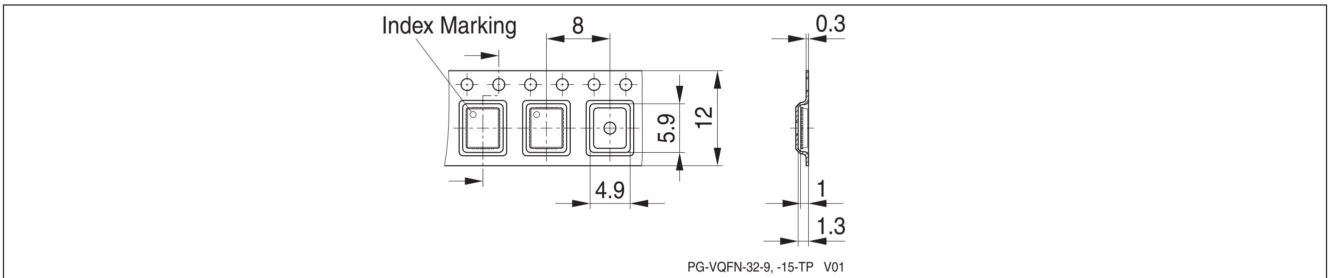


Figure 6 **Tape of VQFN32-9**

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